The raw microprocessor:
a computational fabric for software circuits and general-purpose programs

by Yunqi Zhang
04/09/2013

1. Motivation
    a. wire delay, scalability
2. Basic info
    a. 16 identical programmable tiles
    b. 1 static router, 2 dynamic routers / tile
    c. 8-stage in-order, single-issue MIPS-style processor
3. Network integration
    a. Not only register mapped, but also directly into the bypass paths of pipeline
    b. read/write the FIFO buffer to perform communication as if it is bypass paths
    c. pull the **oldest** value out of the pipeline as soon as it is ready, rather than just at the write-back stage
4. Static network
    a. provide low-latency communication required for software circuits with compile-time predictable communication
    b. software circuits and parallel scalar codes
    c. ordered (in order), flow-controlled (in face of unpredictable events) and reliable transfer
    d. static router: 5-stage pipeline controls 2 routing crossbars
    e. each crossbar routes between: static router pipeline, north, east, south, west neighbors, compute processor and the other crossbar
    f. large cached router program memory -> no limitation on simultaneous communication patterns
    g. knows the route long before the word arrives -> route preparation be pipelined
5. Dynamic network
    a. transport unpredictable operations like interrupts, cache misses and compile-time unpredictable communication between tiles
    b. memory network: restricted usage model, deadlock avoidance -> trusted clients
    c. general network: unrestricted usage model, deadlock recovery -> untrusted clients