SMiTe: Precise QoS Prediction on Real-System SMT Processors to Improve Utilization in Warehouse Scale Computers

Yunqi Zhang, Michael A. Laurenzano, Jason Mars, Lingjia Tang



Clarity-Lab Electrical Engineering and Computer Science University of Michigan

Data centers are expensive





30%

Low utilization leads to inefficiency





Memory Bandwidth
Shared Cache

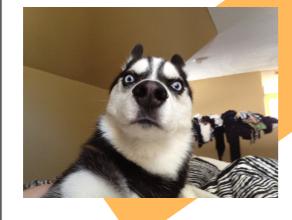
Private Cache

Functional Units

Memory Ports

Branch Predictor

TLB



No co-location

CMP co-location

SMT co-location

Resource Sharing



< 2%
Prediction Error

42%
Utilization Improvement

Session 5A Wednesday at 9:50 A.M.