USB2.0 H.264 Video Encoding Camera Controller

SN9C292B

Datasheet

Document No.-

Version 1.61

Revision	Date	Description
1.3	15-04-16	first release of SN9C292B
1.4	15-04-28	Change QFN88 package type to 292B
1.5	15-07-07	Correct 2.5v LDO to 1.8v for LGA65
1.61	15-09-14	Correct DDR voltage in system / pin description Modify Junction temperature of operation to 100℃

Table of Contents

1 General Description

SN9C292B is a USB 2.0 High-Speed (HS) compatible PC Camera controller. The superior image signal processing engine brings sight video experience. The high performance Motion-JPEG / h.264 compression engine makes variant compression ratio to satisfy bandwidth requirement.

SN9C292B is compliant with USB Video Class and Audio Class. With the integrated sensor interface and color processing engine, it can support most available CMOS sensors that range from VGA to 3MP.

SN9C292B is controlled by the embedded micro-controller, and the statistics for 3A (AE / AWB / AF) are built-in. The flexible architecture is consisted of mask ROM, internal RAM and external serial-flash which can store the customized codes and parameters. With the highly-integrated firmware architecture and the developing kit provided by SONiX, it's easy for 3rd party to fulfill customized features.

2 Features

2.1 System

- 3.3V(analog, I/O), 1.8V(DDR) & 1.2V(core) external power supply are necessary
- Low power consumption of suspend, standby & preview mode
- Input oscillator frequency is 12MHz
- Built-in PLL for internal clock generation
- Using external serial flash to store customized code and data(default 128KBytes)
- Wide serial flash controller speed up to 60 MHz with phase detection
- External RAM is not needed
- 65-pin(use 1.8v LDO) LGA 7.0mmx5.0mm / 88-pin QFN(use 1.8v LDO) 10.0mmx10.0mm package
- Total 9 GPIOs (3 GPIOs are predefined for LED control, serial flash write protect, and sensor reset)

2.2 USB Controller

- USB 2.0 high-speed and full-speed compatible
- USB Video Class 1.1 / 1.5 compliant
- USB Audio Class 1.0 compliant
- USB2.0 HS/FS auto sense and switch
- USB FS mode and USB disconnection are programmable
- 6 endpoints: 1 CONTROL pipe, 2 Interrupt IN, 3 Isochronous-IN(MJPEG/YUY2, H.264 stream, Audio stream)
- 6 alternate settings for Video Streaming Interface

2.3 Sensor Interface

- Support QXGA(3MP, 2048x1536), FHD(1920x1080), UXGA(2MP,1600x1200), SXGA(1.3MP, 1280x1024), HD(1280x720), VGA (0.3MP, 640x480) CMOS ISP/Bayer RAW sensor
- Support YUY2 image data format from sensor (max 96M pixel / sec include dummy)
- Support RAW (Bayer-Pattern) image data format from sensor (max 96M pixel / sec include dummy)
-
- Support industrial standard 2-wire serial interface for sensor control

2.4 Color Processing

- AE histogram statistics
- AWB window statistics
- AF edge window statistics
- On-the fly defect-pixel cancellation
- Mesh lens shading compensation for R/G/B channel separately.
- Color interpolation with low pass filter (less false color)
- Individual digital color gain control for R/Gr/Gb/B channels
- Individual digital color gain control for Y/Cb/Cr channels
- Pixel offset (optical black) compensation for R/Gr/Gb/B channels
- Programmable gamma table for RGB channels
- Programmable color conversion matrix for R/G/B input
- Configurable noise reduction
- De-color aliasing in edge
- Configurable edge enhancement
- Programmable gamma table for Y channel
- Configurable windowing function after processed image
- Programmable hue and saturation

2.5 Scaling Engine

- Fine scalar for maximum 1/256 down-scaling and x4 up-scaling
- For QXGA / UXGA / 1080P / 720P sensors, combined scaling and windowing function provides similar view angle for 1080P / SXGA / 720P / SVGA / VGA / QVGA / QQVGA output format
- The scaling & frame rate adjusting engine are separately controlled for YUV/MJPG and H.264 video streams

2.6 JPEG Encoder

- Built-in JPEG encoder to support USB Video Class MJPEG payload
- JPEG format is YUV420 / YUV422 baseline
- Programmable 128 bytes quantization table for Y and C to adjust compression ratio

2.7 H.264 Encoder

- Profile: Main profile, Level: 4.1
- Built-in H.264 encoder support USB Video Class MPEG2-TS
- Built-in H.264 encoder support USB Video Class Skype-TS
- Built-in H.264 encoder support USB Video Class Microsoft UVC V1.5 driver
- Support UVC 1.1
- Adjustable QP for Y and C to provide programmable compression ratio
- Support multiple stream (with SONiX proprietary driver)
- I & P picture types
- CAVLC/CABAC entropy
- Fully support 4x4 (9 modes) and 16x16 (4 modes) Intra prediction modes
- Fully support 16x16, 16x8, 8x16, 8x8, 8x4, 4x8 and 4x4 Inter prediction modes
- Hadamard SAD (SATD) for Quarter-Pixel Motion Estimation

2.8 Video / Still Image

- Output video / still image format:
  - USB Video Class Uncompressed YUY2 payload (16bits/pixel)
  - USB Video Class MJPEG payload
  - USB Video Class H.264 payload
  - USB Video Class MPEG2-TS payload
  - Skype-TS payload
- Still Image capture up to UXGA and is able to support UVC still image capture method 1/2

2.9 Frame rate

single stream	3M	1080p	2M	1.3M	720p	VGA
H.264	n/a	30	30	30	30	30
MJPG	30	30	30	30	30	60
YUY2	n/a	5	5	5	10	30

multi-stream		1080p	720p	VGA	QVGA
config. 1 (2 streams)	stream1 H.264	30			
	stream2 MJPG	30			
config. 2 (6 streams)	stream1 H.264		30		
	stream2 MJPG		30		
	stream3 H.264			30	
	stream4 MJPG			30	
	stream5 H.264				30
	stream6 MJPG				30

2.10Audio

- Support D-Mic(stereo) input interface & I2S digital audio input with UAC 1.0

- Programmable audio sampling frequency(8, 11.025, 12, 16, 22.05, 24, 44.1, 48 kHz) and resolution (8/16 bits with mono/stereo)

2.11 OSD

- Displays Up to 2 Rows x 24 Characters
- Character Size 16(horizontal) x 16(vertical)
- Line zoom (x1, x2, x3, x4 to x8 for both X and Y coordinates)
- Character with transparency and other 3 color choices.
- 32 different user definable characters can be stored in RAM.
- Start address is 16-pixel alignment to output image window
- OSD reflash time by Sensor Frame Sync

2.12 Motion Detection

- Separate the screen into 16x12 blocks
- One programmable threshold applied to all blocks
- Individual report to indictate motion is detected or not for specific block
- Individual report for specific block can be masked
- Programmable interface via UVC extension unit control

2.13 Micro Controller and USB Device Features

- Built-in 8032 micro controller with 4K bytes data memory
- Maximum CPU clock rate is 60MHz
- Auto load extended F/W from external serial flash (typical 128KB)
- Auto load VID/PID, manufacturer, product and serial number string from external serial flash
- Auto load UVC parameter definition from external serial flash
- Firmware is upgradeable from PC & Linux
- Able to force USB at FS mode & USB disconnect
- Watch dog to auto recovery
- With interrupt when sensor image transferring is finished of each frame

2.14 Pre-Defined for USB Video Class

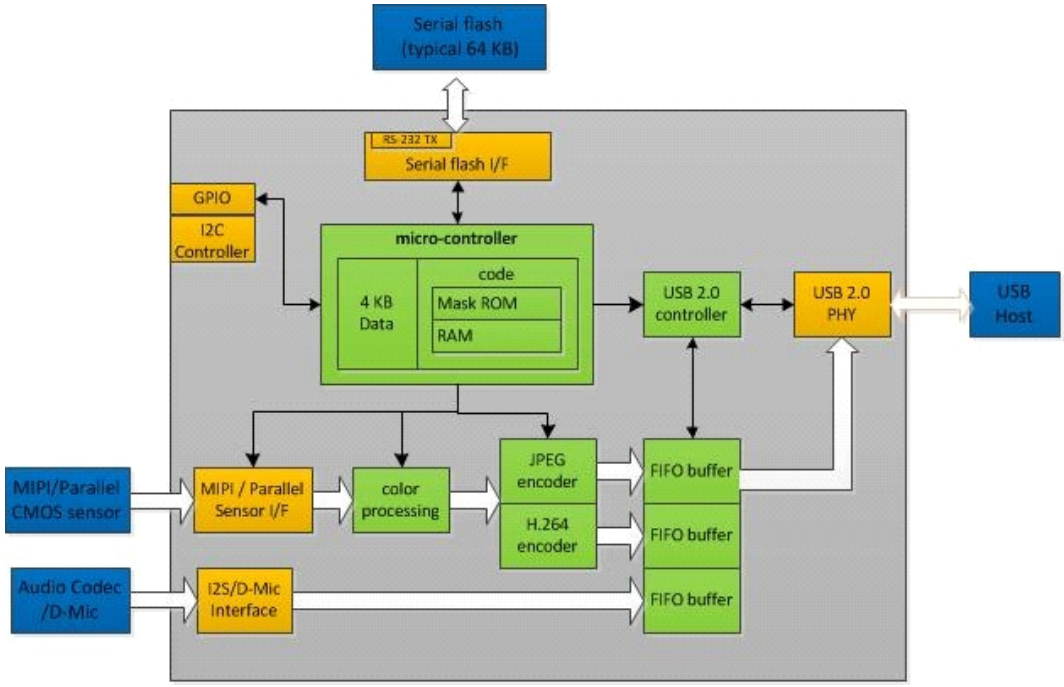
- Brightness control (UVC defined)
- Contrast control (UVC defined)
- Hue control (UVC defined)
- Saturation control (UVC defined)
- Sharpness control (UVC defined)
- Gamma control (UVC defined)
- Privacy control (UVC defined)

- Image auto-flip control triggered by GPIO
- LED indicator on video streaming
- UVC Extension unit support

2.15Platform Support

- Windows OS (Win 7 & Win8)
- Linux OS (kernel 2.6.27 or later)
- Android OS

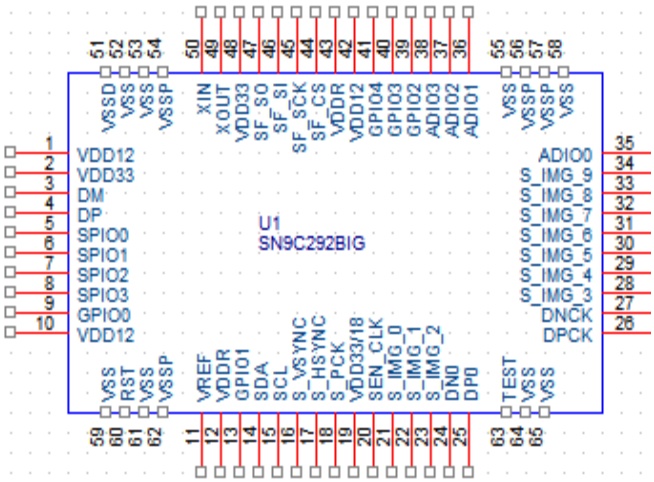
3 Function Block Diagram



4 Pin Assignment

4.1 package type I: LGA65 - SN9C292BIG

4.1.1 Pin-Out Diagram



4.1.2 Pin-Out Description

Pin No.	Pin Name	Mode			Description
		Power Up	Normal	Suspend	
1	VDD12	P	P	P	DSP core power.
2	VDD33	P	P	P	DSP system power.
3	DM	A	A	A	USB D-.
4	DP	A	A	A	USB D+.
5	SPIO0	I			General purpose I/O or SPIO SCK
6	SPIO1	I			General purpose I/O or SPIO SO
7	SPIO2	I			General purpose I/O or SPIO SI
8	SPIO3	I			General purpose I/O or SPIO CS
9	GPIO0	I			General purpose I/O.
10	VDD12	P	P	P	DSP core power.
11	VREF	I	I	I	Via a capacitor 0.1uF to ground.
12	VDDR	P	P	P	Power for DDR.
13	GPIO1	I			General purpose I/O.
14	SDA	I	B	F	I2C data for sensor.
15	SCL	OU	B	F	I2C clock for sensor.
16	S_VSYNC	I	I	I	Parallel sensor vsync.
17	S_HSYNC	I	I	I	Parallel sensor hsync.
18	S_PCK	I	I	I	Parallel sensor pixel clock.
19	VDD33/18	P	P	P	I/O voltage level setting for sensor.
20	SEN_CLK	O	O	O	Sensor clock.

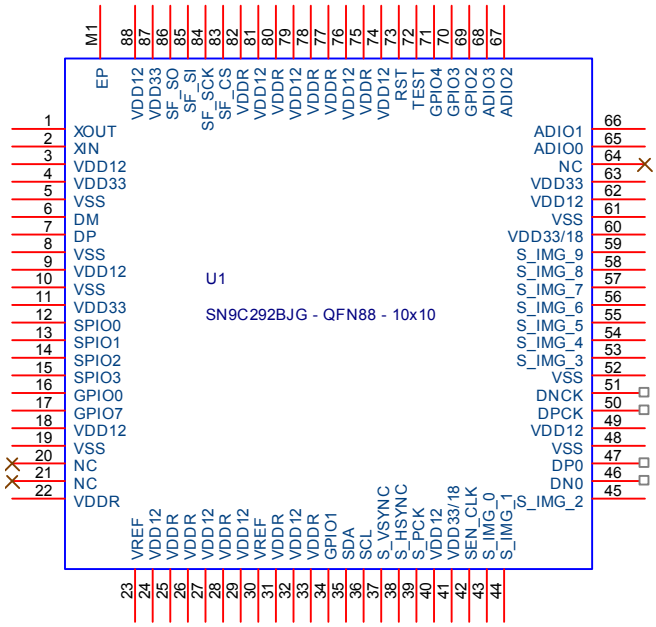
Pin No.	Pin Name	Mode			Description
		Power Up	Normal	Suspend	
21	S_IMG_0	I	I	I	Parallel sensor image data.
22	S_IMG_1	I	I	I	Parallel sensor image data.
23	S_IMG_2	I	I	I	Parallel sensor image data.
24	DN0	A	A	A	MIPI sensor data lane 0 negative signal.
25	DP0	A	A	A	MIPI sensor data lane 0 positive signal.
26	DPCK	A	A	A	MIPI sensor clock lane positive signal.
27	DNCK	A	A	A	MIPI sensor clock lane negative signal.
28	S_IMG_3	I	I	I	Parallel sensor image data.
29	S_IMG_4	I	I	I	Parallel sensor image data.
30	S_IMG_5	I	I	I	Parallel sensor image data.
31	S_IMG_6	I	I	I	Parallel sensor image data.
32	S_IMG_7	I	I	I	Parallel sensor image data.
33	S_IMG_8	I	I	I	Parallel sensor image data.
34	S_IMG_9	I	I	I	Parallel sensor image data.
35	ADIO0	I			I2S DI or DMIC LIN/RIN
36	ADIO1	I			I2S BCLK
37	ADIO2	I			I2S MCLK or DMIC MCLK
38	ADIO3	I			I2S LRCK
39	GPIO2	I			I2S_SDA
40	GPIO3	I			I2S_SCL
41	GPIO4	I			General purpose I/O.
42	VDD12	P	P	P	DSP core power.
43	VDDR	P	P	P	Power for DDR.
44	SF_CS	OH	O	F	SPI chip select to serial flash.
45	SF_SCK	OL	O	OL	SPI clock to serial flash.
46	SF_SI	I	I	I	SPI data in from serial flash.
47	SF_SO	OL	O	OL	SPI data out to serial flash.
48	VDD33	P	P	P	DSP system power.
49	XOUT	O	O	OH	OSC output (Rf=1M).
50	XIN	I	I	I	OSC input (Rf=1M) (12MHz).
51	VSSD	P	P	P	Ground.
52	VSS	P	P	P	Ground.
53	VSS	P	P	P	Ground.
54	VSSP	P	P	P	Ground.
55	VSS	P	P	P	Ground.
56	VSSP	P	P	P	Ground.
57	VSSP	P	P	P	Ground.
58	VSS	P	P	P	Ground.
59	VSS	P	P	P	Ground.
60	RST	I	I	I	Chip reset. Active high.
61	VSS	P	P	P	Ground.
62	VSSP	P	P	P	Ground.
63	TEST	I	I	I	Test pin. Normal low.
64	VSS	P	P	P	Ground.
65	VSS	P	P	P	Ground.

O: output
OU : output unknown
OH : output high
OL L output low

I : input
O : output
B : Bidirection
F: Firmware control
A: Analog

4.2 package type II: QFN88 - SN9C292BJG

4.2.1 Pin-Out Diagram



4.2.2 Pin-Out Description

Pin No.	Pin Name	Mode			Description
		Power Up	Normal	Suspend	
1	XOUT	O	O	OH	OSC output (Rf=1M)
2	XIN	I	I	I	OSC input (Rf=1m) (12MHz)
3	VDD12	P	P	P	DSP core power 1.2V
4	VDD33	P	P	P	DSP system power 3.3V
5	VSS	P	P	P	Ground
6	DM	A	A	A	USB D-
7	DP	A	A	A	USB D+
8	VSS	P	P	P	Ground
9	VDD12	P	P	P	DSP core power 1.2V
10	VSS	P	P	P	Ground
11	VDD33	P	P	P	DSP system power 3.3V
12	SPIO0	I	O	O	General purpose I/O or SPIO SCK
13	SPIO1	I	O	O	General purpose I/O or SPIO SO
14	SPIO2	I	O	O	General purpose I/O or SPIO SI
15	SPIO3	I	O	O	General purpose I/O or SPIO CS
16	GPIO0	I	O	O	General purpose I/O
17	GPIO7	I			General purpose I/O
18	VDD12	P	P	P	DSP core power 1.2V
19	VSS	P	P	P	Ground
20	NC				Not connect

Pin No.	Pin Name	Mode			Description
		Power Up	Normal	Suspend	
21	NC				Not connect
22	VDDR	P	P	P	DDR power 1.8V
23	VREF	I	I	I	DDR VREF via a capacitor 0.1uF to ground
24	VDD12	P	P	P	DSP core power 1.2V
25	VDDR	P	P	P	DDR power 1.8V
26	VDDR	P	P	P	DDR power 1.8V
27	VDD12	P	P	P	DSP core power 1.2V
28	VDDR	P	P	P	DDR power 1.8V
29	VDD12	P	P	P	DSP core power 1.2V
30	VREF	I	I	I	DDR VREF
31	VDDR	P	P	P	DDR power 1.8V
32	VDD12	P	P	P	DSP core power 1.2V
33	VDDR	P	P	P	DDR power 1.8V
34	GPIO1	I			General purpose I/O
35	SDA	I	B	F	I2C data for sensor
36	SCL	OU	B	F	I2C clock for sensor
37	S_VSYNC	I	I	I	Parallel sensor vsync
38	S_HSYNC	I	I	I	Parallel sensor hsync
39	S_PCK	I	I	I	Parallel sensor pixel clock
40	VDD12	P	P	P	DSP core power 1.2V
41	VDD33/18	P	P	P	I/O voltage level setting for sensor
42	SEN_CLK	O	O	O	Sensor clock
43	S_IMG_0	I	I	I	Parallel sensor image data
44	S_IMG_1	I	I	I	Parallel sensor image data
45	S_IMG_2	I	I	I	Parallel sensor image data
46	DN0	A	A	A	MIPI sensor data lane 0 negative signal
47	DP0	A	A	A	MIPI sensor data lane 0 positive signal
48	VSS	P	P	P	Ground
49	VDD12	P	P	P	DSP core power 1.2V
50	DPCK	A	A	A	MIPI sensor clock lane positive signal
51	DNCK	A	A	A	MIPI sensor clock lane negative signal
52	VSS	P	P	P	Ground
53	S_IMG_3	I	I	I	Parallel sensor image data
54	S_IMG_4	I	I	I	Parallel sensor image data
55	S_IMG_5	I	I	I	Parallel sensor image data
56	S_IMG_6	I	I	I	Parallel sensor image data
57	S_IMG_7	I	I	I	Parallel sensor image data
58	S_IMG_8	I	I	I	Parallel sensor image data
59	S_IMG_9	I	I	I	Parallel sensor image data
60	VDD33/18	P	P	P	I/O voltage level setting for sensor
61	VSS	P	P	P	Ground
62	VDD12	P	P	P	DSP core power 1.2V
63	VDD33	P	P	P	DSP system power 3.3V
64	NC				Not connect
65	ADIO0	I			I2S DI or DMIC LIN/RIN

Pin No.	Pin Name	Mode			Description
		Power Up	Normal	Suspend	
66	ADIO1	I			I2S BCLK
67	ADIO2	I			I2S MCLK or DMIC CLK
68	ADIO3	I			I2S LRCK
69	GPIO2	I			I2S SDA
70	GPIO3	I	O	O	I2S SCL
71	GPIO4	I	O	O	General purpose I/O
72	TEST	I	I	I	TEST pin normal low
73	RST	I	I	I	Chip reset active high
74	VDD12	P	P	P	DSP core power 1.2V
75	VDDR	P	P	P	DDR power 1.8V
76	VDD12	P	P	P	DSP core power 1.2V
77	VDDR	P	P	P	DDR power 1.8V
78	VDDR	P	P	P	DDR power 1.8V
79	VDD12	P	P	P	DSP core power 1.2V
80	VDDR	P	P	P	DDR power 1.8V
81	VDD12	P	P	P	DSP core power 1.2V
82	VDDR	P	P	P	DDR power 1.8V
83	SF_CS	OH	O	F	Serial flash chip select
84	SF_SCK	OL	O	OL	Serial flash clock
85	SF_SI	I	I	I	Serial flash data input
86	SF_SO	OL	O	OL	Serial flash data output
87	VDD33	P	P	P	DSP system power 3.3V
88	VDD12	P	P	P	DSP core power 1.2V

O: output
OU : output unknown
OH : output high
OL L output low

I : input
O : output
B : Bidirection
F: Firmware control
A: Analog

5 Electrical Characteristics

5.1 DC Operating Condition

5.1.1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
VDD33	Power Supply	-0.3 ~ 3.6	V
VDD33_18	Power Supply	-0.3 ~ 3.6	V
DVDD	Power Supply	-0.12 ~ 1.32	V
Vin	Input Voltage	-0.3 ~ VDD33 + 0.3	V
Vout	Output Voltage	-0.3 ~ VDD33 + 0.3	V

5.1.2 Recommened Operating Conditions

Symbol	Parameter	Typ	Units
VDD33	Power Supply	3.3	V
VDD33_18	Power Supply	3.3/1.8	V
DVDD	Power Supply	1.2	V
Vin	Input voltage	3.3	V

5.1.3 DC Electrical Characteristics

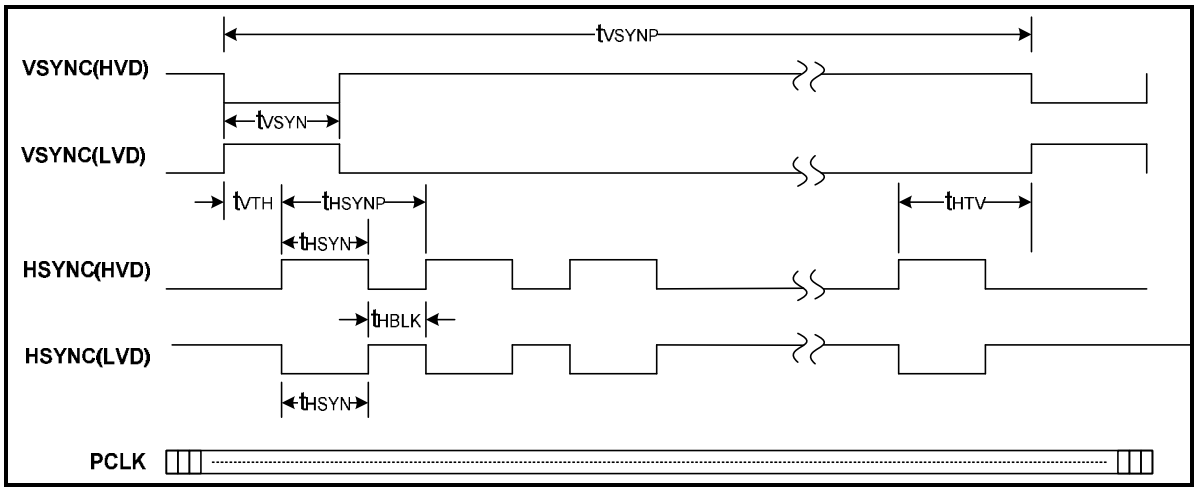
(Under Recommended Operating Conditions and
VDD33=3.0 ~ 3.6V, VDD33_18=1.62 ~ 3.6V, Ta=0 to +70 °C)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Vil (VDD33)	Input low voltage	CMOS	-0.3		0.2*VDD33	V
Vih(VDD33)	Input high voltage	CMOS	0.8*VDD33		VDD33+0.3	V
Vil (VDD33_18)	Input low voltage	CMOS	-0.3		0.2*VDD33_18	V
Vih(VDD33_18)	Input high voltage	CMOS	0.8*VDD33_18		VDD33_18+0.3	V
Iil	Input low current	no pull-up or pull-down	-1		1	µA
Iih	Input high current	no pull-up or pull-down	-1		1	µA
Ioz	Tri-state leakage current		-1		1	µA
Vol	Output Low voltage	Iol=4mA / 8mA			0.4	V
Voh	Output high voltage	Ioh=4mA / 8mA	2.4			V
Cin	Input capacitance			10		pF

Cout	Output capacitance			10		pF
Cbid	Bi-directional buffer Capacitance			10		pF
Rpu	Pull-up resistor			70K		Ω
Rpd	Pull-down resistor			70K		Ω

5.2 AC Operating Condition

5.2.1 Parallel Sensor Interface

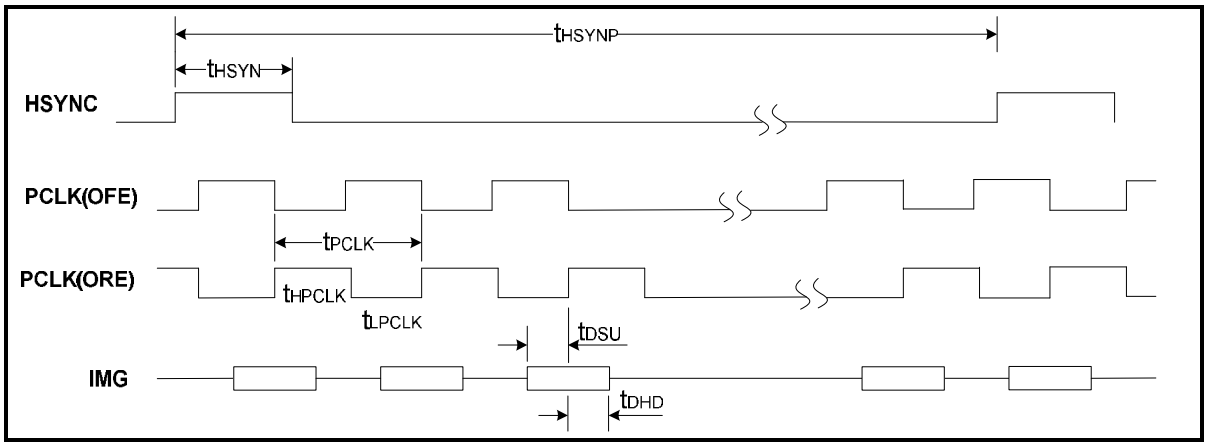


Parameter	Symbol	Min.	Typ.	Max.	Unit
VSYNC pulse width	tVSYNC	tPCLK	-	-	ns
VSYNC to HSYNC	tVTH	tPCLK	-	-	ns
HSYNC pulse width	tHSYN	tPCLK	-	-	ns
Blank time between two HSYNC	tHBLK	tPCLK	-	-	ns
HSYNC to VSYNC	tHTV	tHSYNP			ns

Note:

1. t_{SENCK} is period of internal clock for sensor post processing.
2. t_{HSYNP} is period of Hsync, t_{VSYNP} is period of Vsync.
3. HVD (High Valid), LVD (Low Valid).

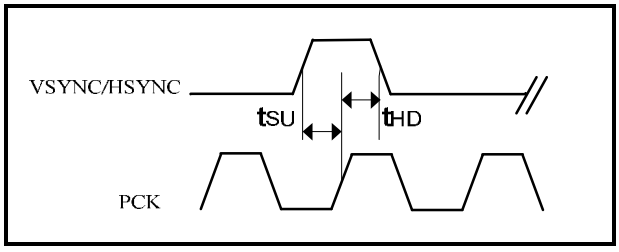
SYNC_MODE = 1 : (PCLK is free run)



Parameter	Symbol	Min.	Typ.	Max.	Unit
HSYNC pulse width	t_{HSYN}	t_{PCLK}	-	-	ns
PCLK Low Pulse Width	t_{LPCLK}	2.0	-	-	ns
PCLK High Pulse Width	t_{HPCLK}	2.0	-	-	ns
Frequency of pixel clock	f_{PCLK}	-	-	96	MHz
Image data setup time	t_{DSU}	2.0	-	-	ns
Image data hold time	t_{DHD}	2.0	-	-	ns

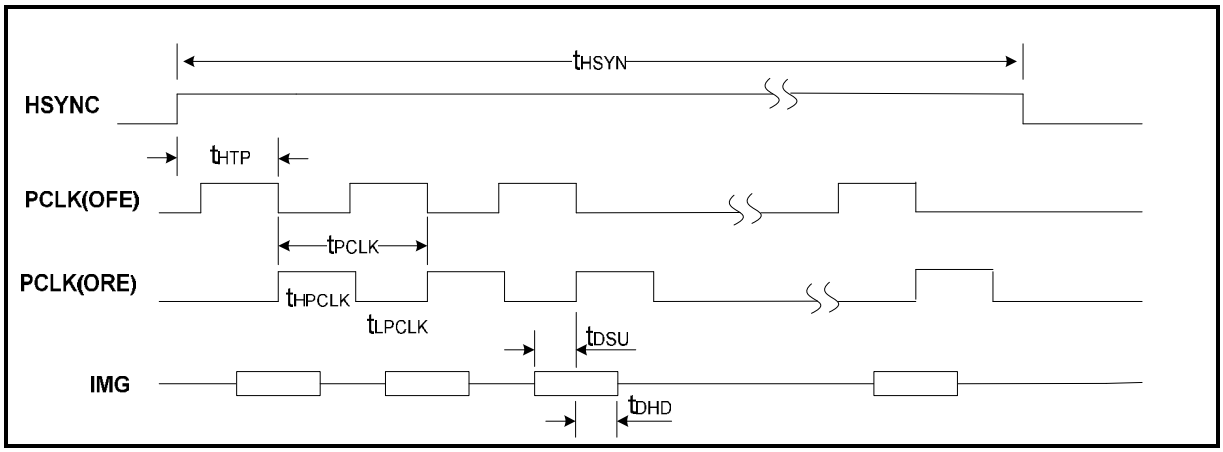
Note:

1. t_{SENCK} is period of internal clock for sensor post processing
2. ORE (On Rising Edge) means the timing act on rising edge
3. OFE (On Falling Edge) means the timing act on falling edge



Parameter	Symbol	Min.	Typ.	Max.	Unit
VSYNC / HSYNC setup time	tSU	2	-	-	ns
VSYNC / HSYNC hold time	tHD	2	-	-	ns

SYNC_MODE = 0 : **(PCLK is output only when hsync active)**



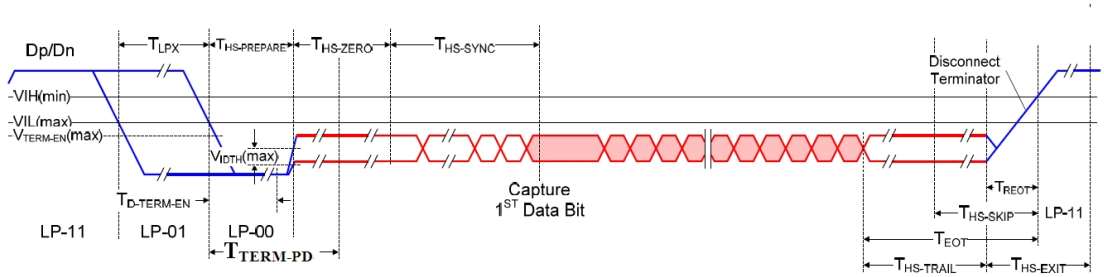
Parameter	Symbol	Min.	Typ.	Max.	Unit
HSYNC pulse width	t_{HSYN}	HSIZE * tPCLK	-	-	ns
HSYNC to PCLK	t_{HTP}	t_{SENCK}	-	-	
PCLK Low Pulse Width	t_{LPCLK}	2.0	-	-	ns
PCLK High Pulse Width	t_{HPCLK}	2.0	-	-	ns
Frequency of pixel clock	f_{PCLK}	-	-	96	MHz
Image data setup time	t_{DSU}	2.0	-	-	ns
Image data hold time	t_{DHD}	2.0	-	-	ns

Note:

1. t_{SENCK} is period of internal clock for sensor post processing
2. ORE (On Rising Edge) means the timing act on rising edge
3. OFE (On Falling Edge) means the timing act on falling edge
4. HSIZE represents total valid PCLK number per horizontal line

5.2.2 MIPI Sensor Interface

■ High-speed Data Transmission



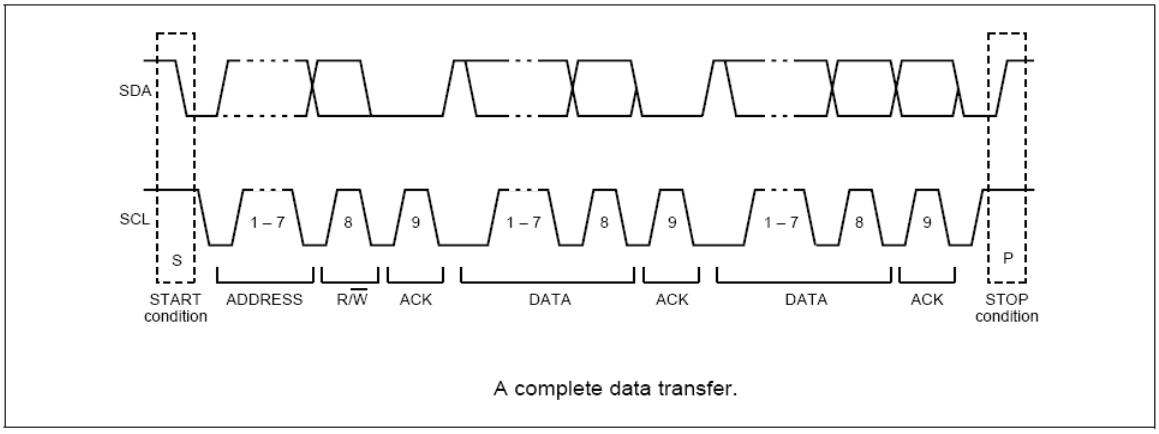
- MIPI Operation Timing Parameters

Parameter	Min	Max	Unit
$T_{LPX(1)}$	66		ns
$T_{HS-PREPARE(2)}$	66	85ns + 6*$UI_{(3)}$	ns
$T_{HS-ZERO(4)}$	120	2*[$T_{HS-EXIT}$ – (110ns+10*UI)]	ns
$T_{HS-TRAIL(5)}$	16*UI		ns
$T_{HS-EXIT(6)}$	240ns + 110*UI		ns
$T_{EOT(7)}$	16*UI	105ns + 12*UI	ns

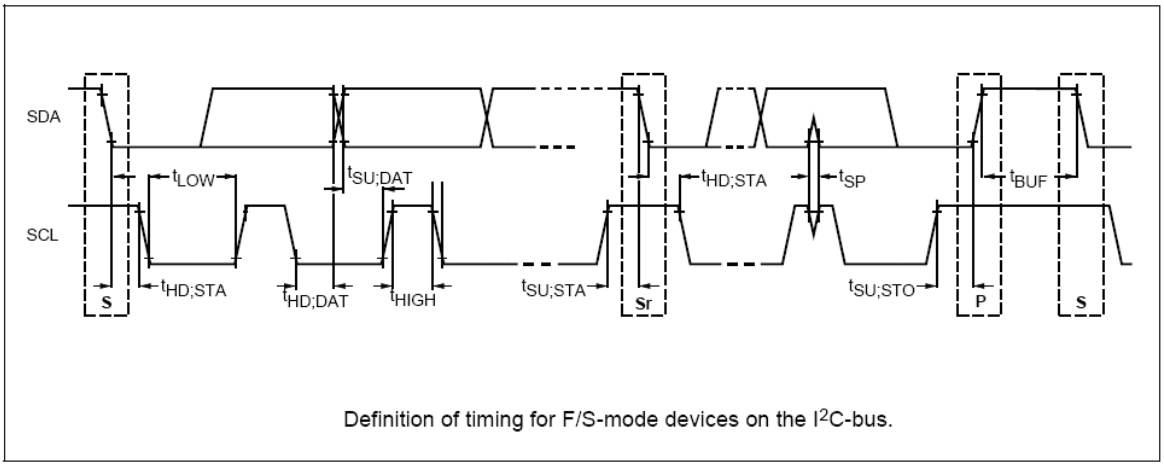
1. T_{LPX} is the time from the end of LP-11state to the start of LP-00 state.
2. $T_{HS-PREPARE}$ is the time from the start of LP-00 to the start of the HS-0 state.
3. UI is the one data bit time.
4. $T_{HS-ZERO}$ is the time during HS-0 state.
5. $T_{HS-TRAIL}$ is the time that the transmitter drives the differential state after last data bit of HS burst.
6. $T_{HS-EXIT}$ is the time from the end of $T_{HS-TRAIL}$ to the start of the LP-01 of the next packet.
7. T_{EOT} is the time from the end of $T_{HS-TRAIL}$ to Low-Power state that mean DP = 1 and DN = 1.

- Note1: The ranges of the red marked parameters for the above table must be satisfied. The other parameters can reference the document of MIPI Alliance Specification for DPHY.
- Note2: $T_{TERM-PD}$ is the time from termination enable to the release of power down. The range of $T_{TERM-PD}$ is from ($T_{HS-PREPARE}$ + 33 ns) to ($T_{HS-ZERO}$ + $T_{HS-PREPARE}$ – 33ns) and the suggestion value is the min($T_{HS-PREPARE}$ + 0.5*$T_{HS-ZERO}$, 495ns).

5.2.3 I2C Control Interface



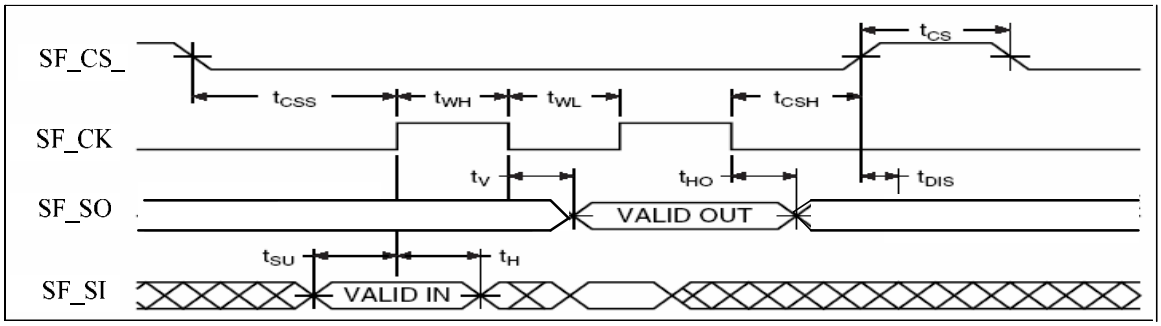
A complete data transfer.



Definition of timing for F/S-mode devices on the I²C-bus.

Parameter	Symbol	Standard mode			Fast mode			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	-	98.7	-	-	394.7	-	kHz
Hold time START condition	$t_{HD;STA}$	-	5067	-	-	1267	-	ns
LOW period of the SCL clock	t_{LOW}	-	5067	-	-	1267	-	ns
HIGH period of the SCL clock	$t_{HD;STA}$	-	5067	-	-	1267	-	ns
Setup time for a repeated START condition	$t_{SU;STA}$	-	5067	-	-	1267	-	ns
Data hold time: Write	$t_{HD:DAT}$	-	2533	-	-	633	-	ns
Data hold time: Read	$t_{HD:DAT}$	10	-	-	10	-	-	ns
Data setup time: Write	$t_{SU:DAT}$	-	2533	-	-	633	-	ns
Data setup time: Read	$t_{SU:DAT}$	10	-	-	10	-	-	ns
Setup time for STOP condition	$t_{SU:STO}$	-	5066	-	-	1267	-	ns
Bus free time between a STOP and START condition	t_{BUF}	4.8	-	-	1.4	-	-	us

5.2.4 Serial Flash Interface



When f_{SCK} = 60 Mhz (SPEED=1 , SFCK_SEL=1)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCK clock frequency	f_{SCK}	-	60	-	MHz
Chip Select low to SF_CK Edge	t_{CSS}	136	-	-	ns
SF_CK Edge to Chip Select High	t_{CSH}	32	-	-	ns
Chip High period	t_{CS}	120	-	-	ns
Clock high period	t_{WH}	8	-	-	ns
Clock low period	t_{WL}	8	-	-	ns
Input Data setup time	t_{SU}	6	-	-	ns
Input Data hold time	t_{H}	6	-	-	ns
Output Data Valid time @ CL=20pF	t_{V}	-	-	5	ns
Output Data Hold time @ CL=20pF	t_{HO}	0	-	-	ns

When f_{SCK} = 40 Mhz (SPEED=2 , SFCK_SEL=1)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCK clock frequency	f_{SCK}	-	40	-	MHz
Chip Select low to SF_CK Edge	t_{CSS}	144	-	-	ns
SF_CK Edge to Chip Select High	t_{CSH}	32	-	-	ns
Chip High period	t_{CS}	120	-	-	ns
Clock high period	t_{WH}	8	-	-	ns
Clock low period	t_{WL}	16	-	-	ns
Input Data setup time	t_{SU}	10	-	-	ns
Input Data hold time	t_{H}	10	-	-	ns
Output Data Valid time @ CL=20pF	t_{V}	-	-	5	ns
Output Data Hold time @ CL=20pF	t_{HO}	0	-	-	ns

When f_{SCK} = 24 Mhz (SPEED=1 , SFCK_SEL=0)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCK clock frequency	f_{SCK}	-	24	-	MHz
Chip Select low to SF_CK Edge	t_{CSS}	340	-	-	ns
SF_CK Edge to Chip Select High	t_{CSH}	80	-	-	ns
Chip High period	t_{CS}	300	-	-	ns
Clock high period	t_{WH}	20	-	-	ns
Clock low period	t_{WL}	20	-	-	ns
Input Data setup time	t_{SU}	10	-	-	ns
Input Data hold time	t_{H}	10	-	-	ns

Output Data Valid time @ CL=20pF	t_V	-	-	5	ns
Output Data Hold time @ CL=20pF	t_{HO}	0	-	-	ns

When f_{SCK} = 12 Mhz (SPEED=2 , SFCK_SEL=0)

Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**
SCK clock frequency	f_{SCK}	-	12	-	MHz
Chip Select low to SF_CK Edge	t_{CSS}	360	-	-	ns
SF_CK Edge to Chip Select High	t_{CSH}	80	-	-	ns
Chip High period	t_{CS}	300	-	-	ns
Clock high period	t_{WH}	20	-	-	ns
Clock low period	t_{WL}	40	-	-	ns
Input Data setup time	t_{SU}	10	-	-	ns
Input Data hold time	t_H	10	-	-	ns
Output Data Valid time @ CL=20pF	t_V	-	-	5	ns
Output Data Hold time @ CL=20pF	t_{HO}	0	-	-	ns

5.3 Temperature

5.3.1 Storage Temperature

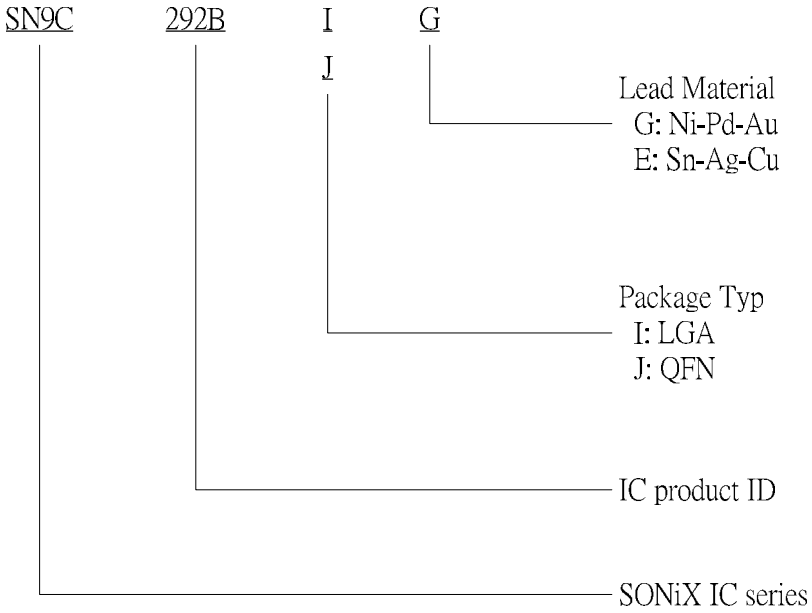
From -40’C to +150’C

5.3.2 Operation Temperature

Max. Junction Temp. (℃)	Max. Lead Temp.	Ta (℃)	θja (℃/W)
100	+390℃±10℃, 5sec	0 ~ 70	

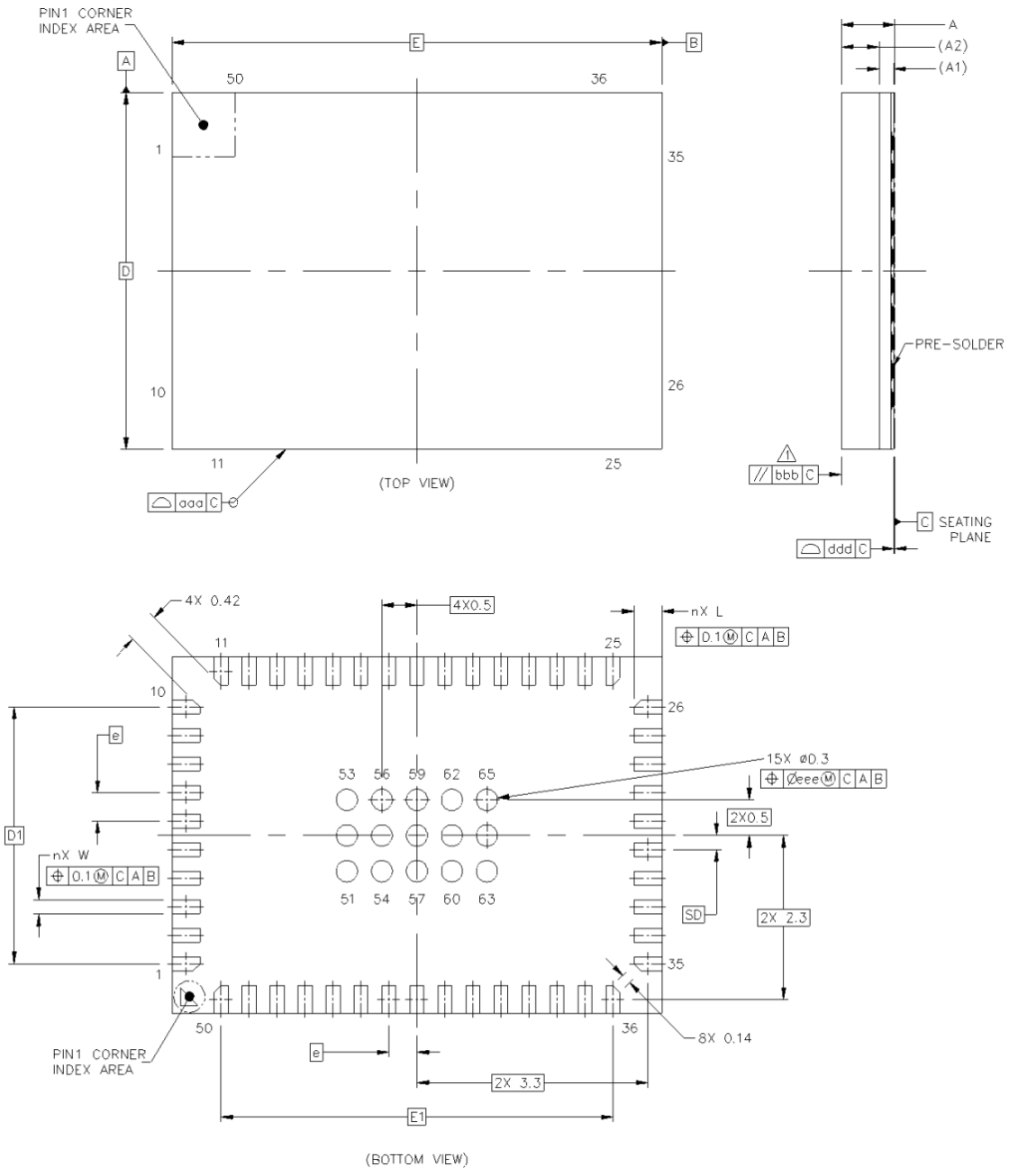
6 Package

6.1 Nomenclature



6.2 package type I: LGA65 - SN9C292BIG

6.2.1 Drawing

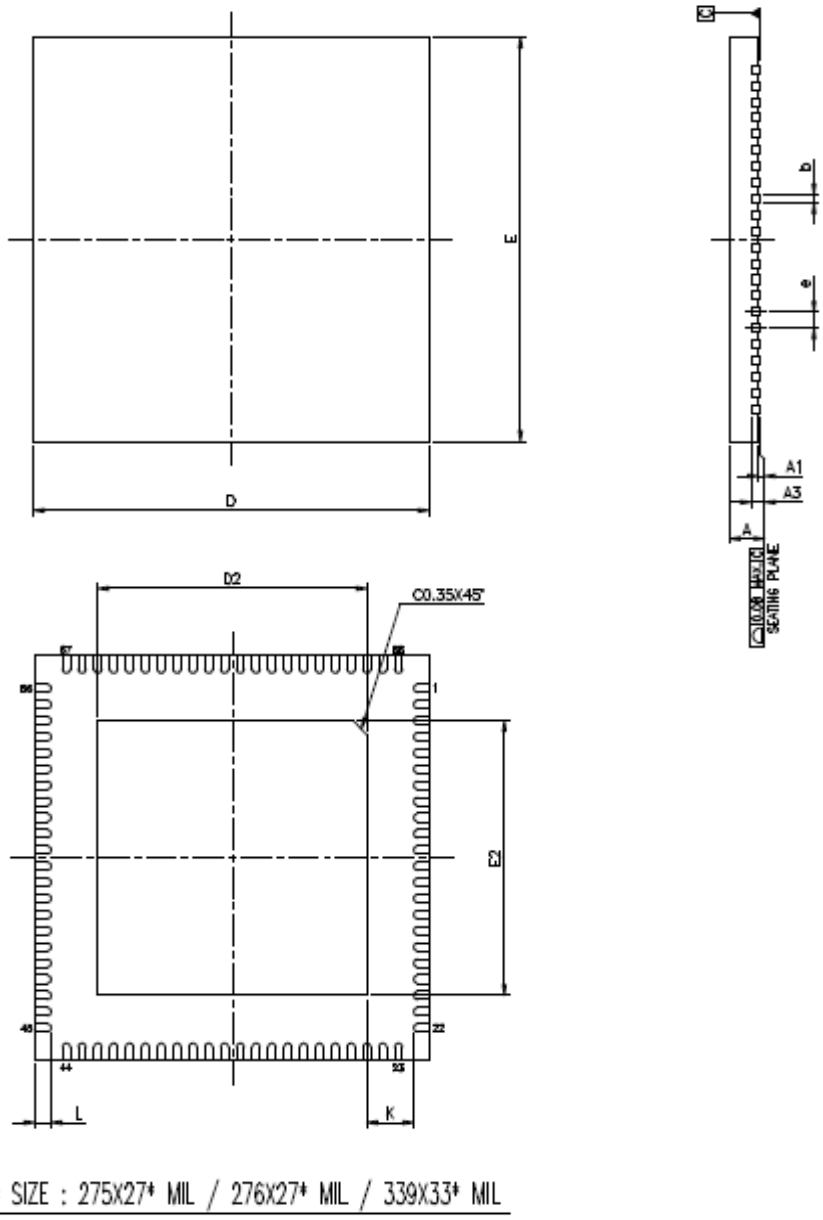


6.2.2 Dimension

	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	0.9
SUBSTRATE THICKNESS	A1		0.21	REF
MOLD THICKNESS	A2		0.54	REF
BODY SIZE	D		5	BSC
	E		7	BSC
LEAD WIDTH	W	0.15	0.2	0.25
LEAD LENGTH	L	0.3	0.4	0.5
LEAD PITCH	e		0.4	BSC
LEAD COUNT	n		50	
EDGE BALL CENTER TO CENTER	D1		3.6	BSC
	E1		5.6	BSC
BODY CENTER TO CONTACT BALL	SD		0.2	BSC
	SE		---	BSC
BALL WIDTH	b	---	---	---
BALL DIAMETER			---	
BALL OPENING			0.3	
BALL PITCH	e1		---	
BALL COUNT	n1		---	
PRE-SOLDER		0.01	---	0.07
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COMPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET(BALL)	fff		---	

6.3 package type II: QFN88 - SN9C292BJG

6.3.1 Drawing



PAD SIZE : 275X27* MIL / 276X27* MIL / 339X33* MIL

6.3.2 Dimension

SYMBOL	COMMON DIMENSIONS		
	MIN.	NOR.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.203		REF.
D	10.00		BSC
E	10.00		BSC
e	0.40		BSC
L	0.30	0.40	0.50
K	0.20	---	---
D2	6.75	6.80	6.85
E2	6.75	6.80	6.85
b	0.15	0.20	0.25

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