**數位電路設計**

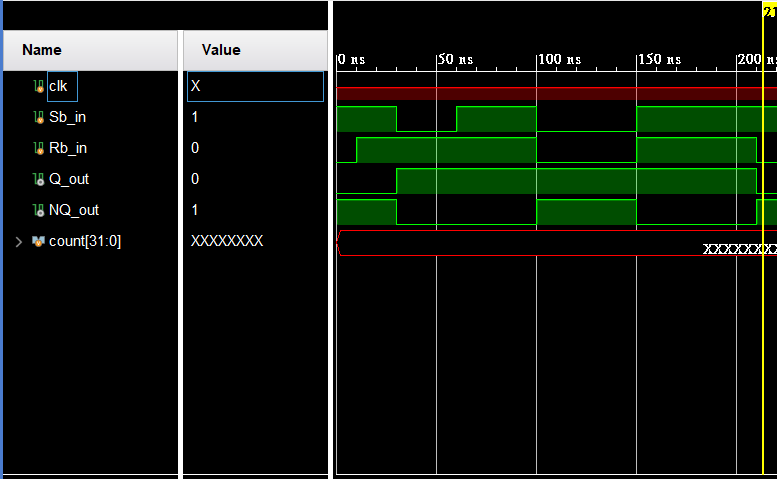
**Lab3 – 同步循序電路之 HDL 模組撰寫與測試**

0613144 葉之晴

(1)2.A

Using two nand gates represents SR-Latch.

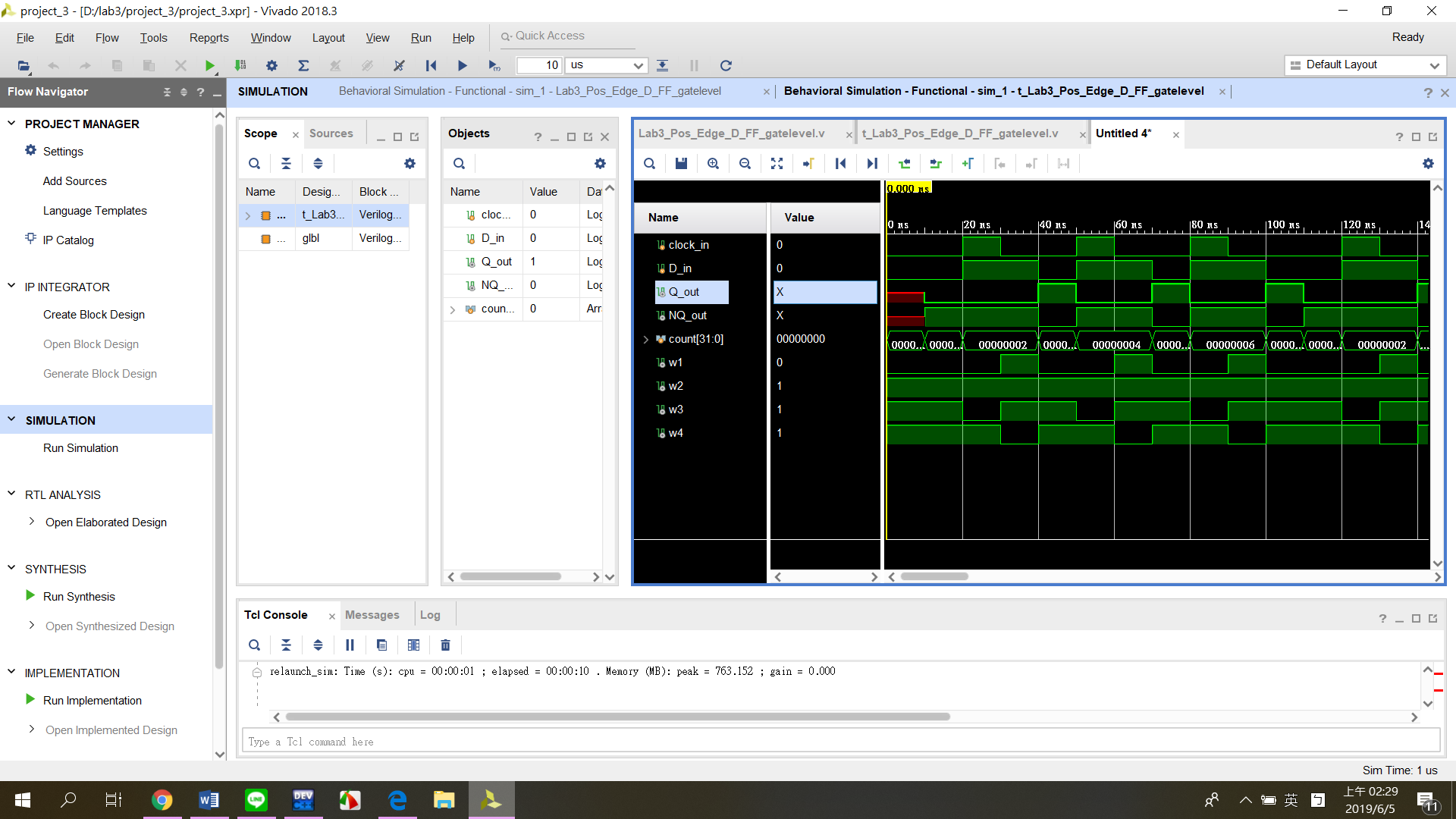
The circuit diagram is correct because the data of diagram is the same as the data of table from the teacher.



(2)2.B

Use four nand gates, SR-Latch from 2.A and D flip flop.

The circuit diagram is correct because the data of diagram is the same as the data of table from the teacher.

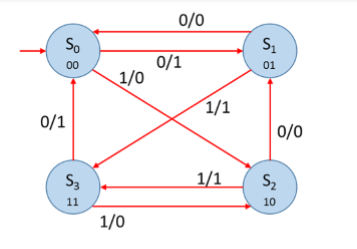


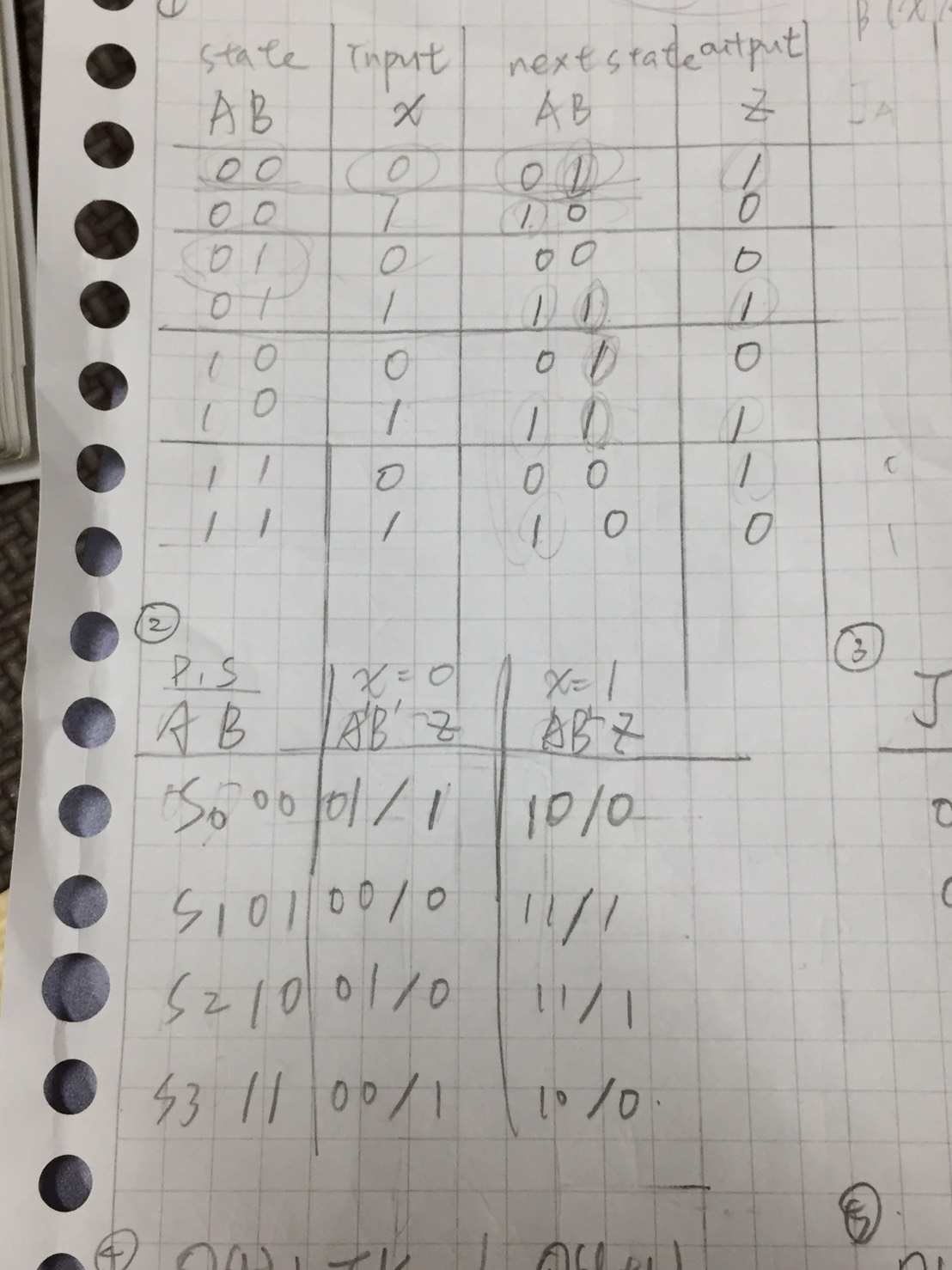
(3)2.C

(a)explain how to do it

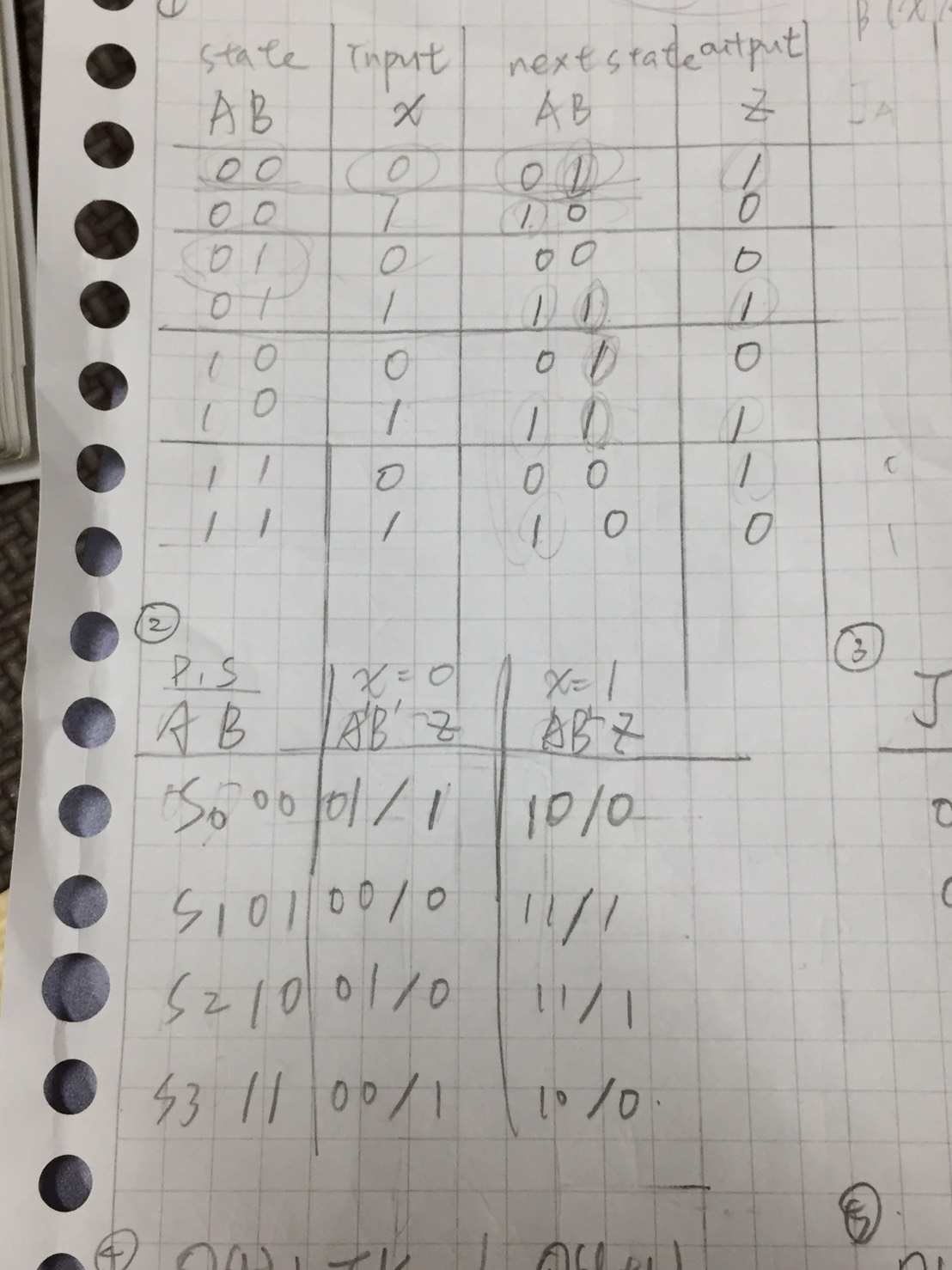
**Step1**

Make the table from the state diagram.



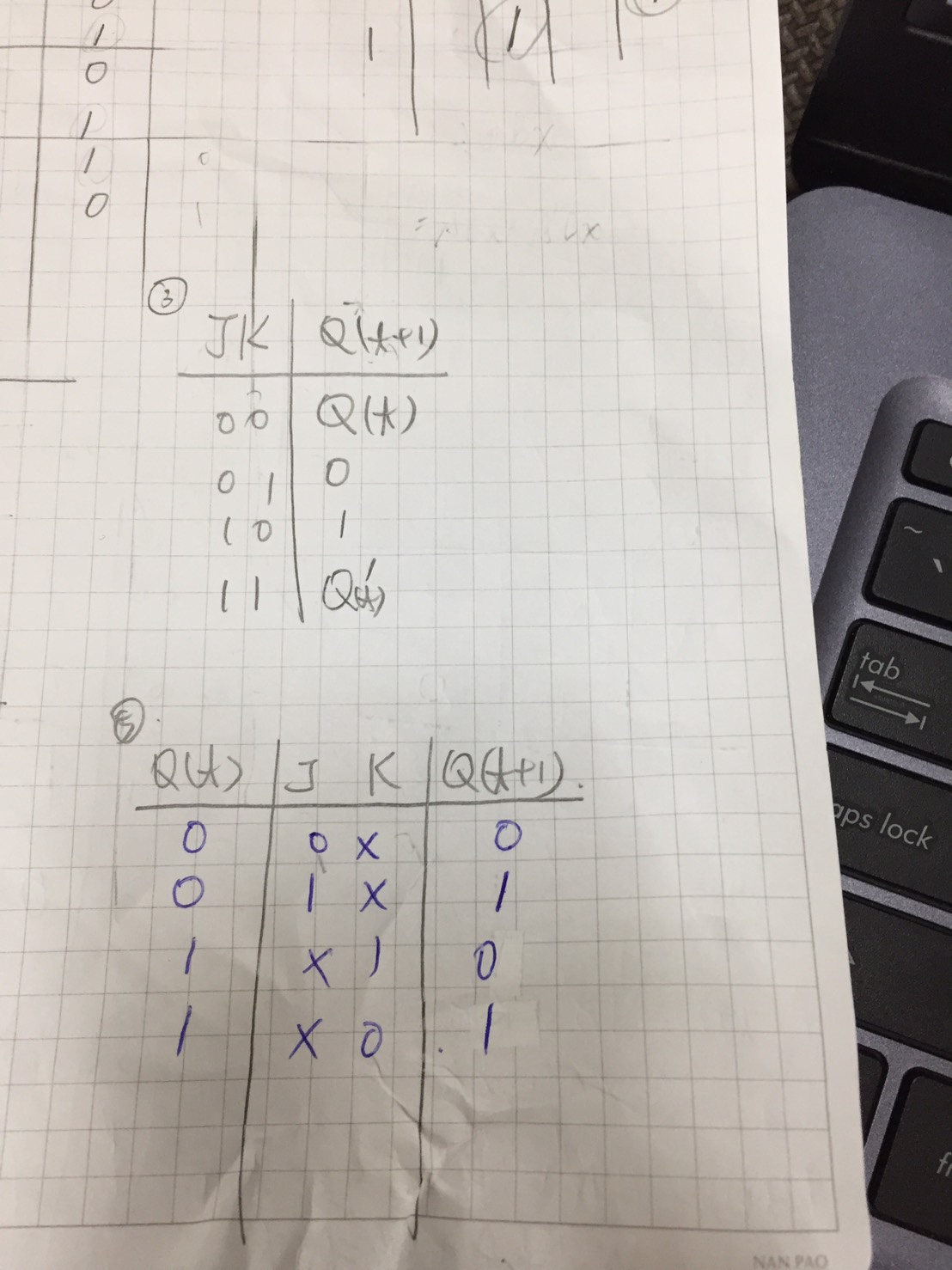


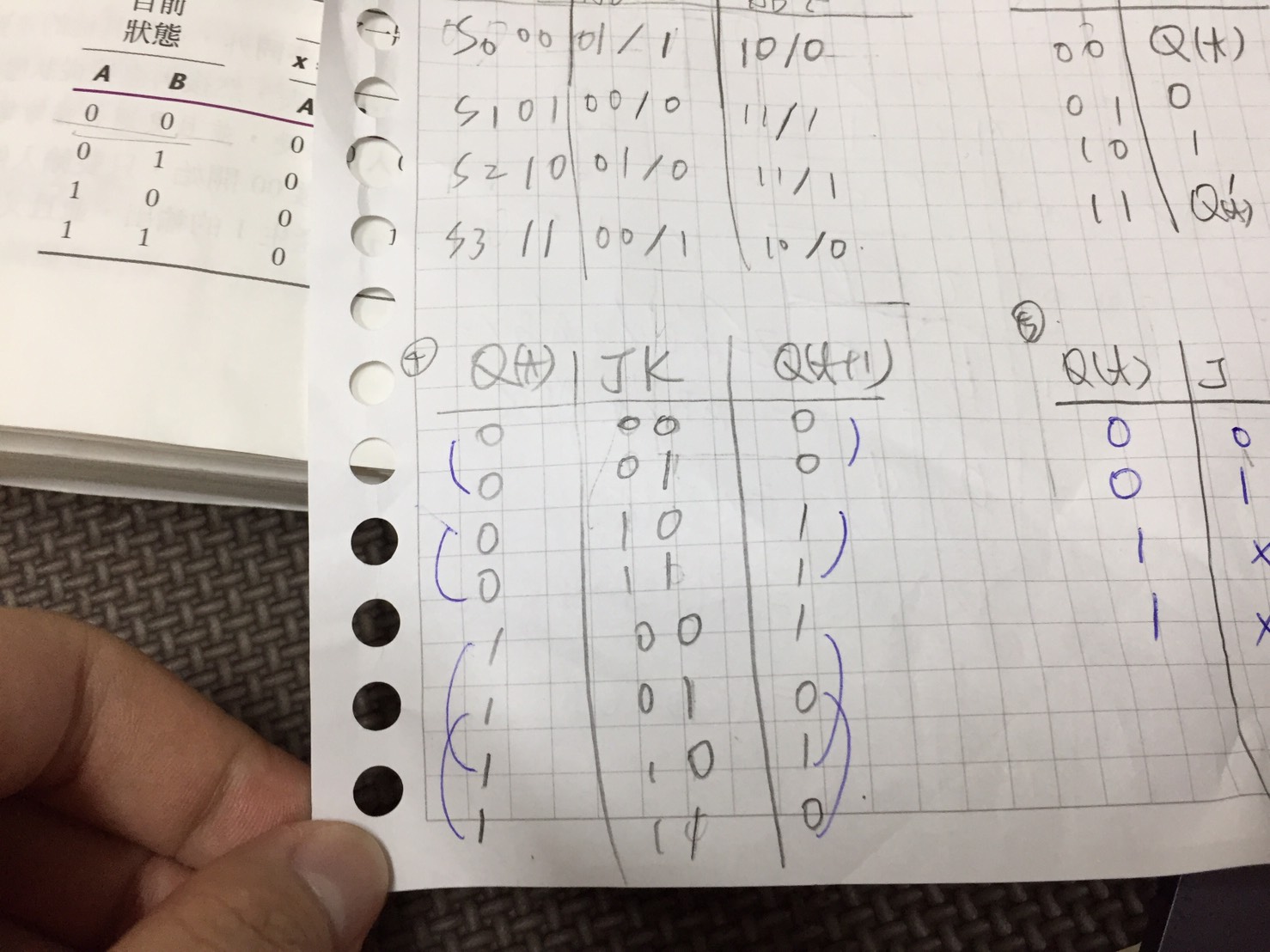
Then, arrange the table.

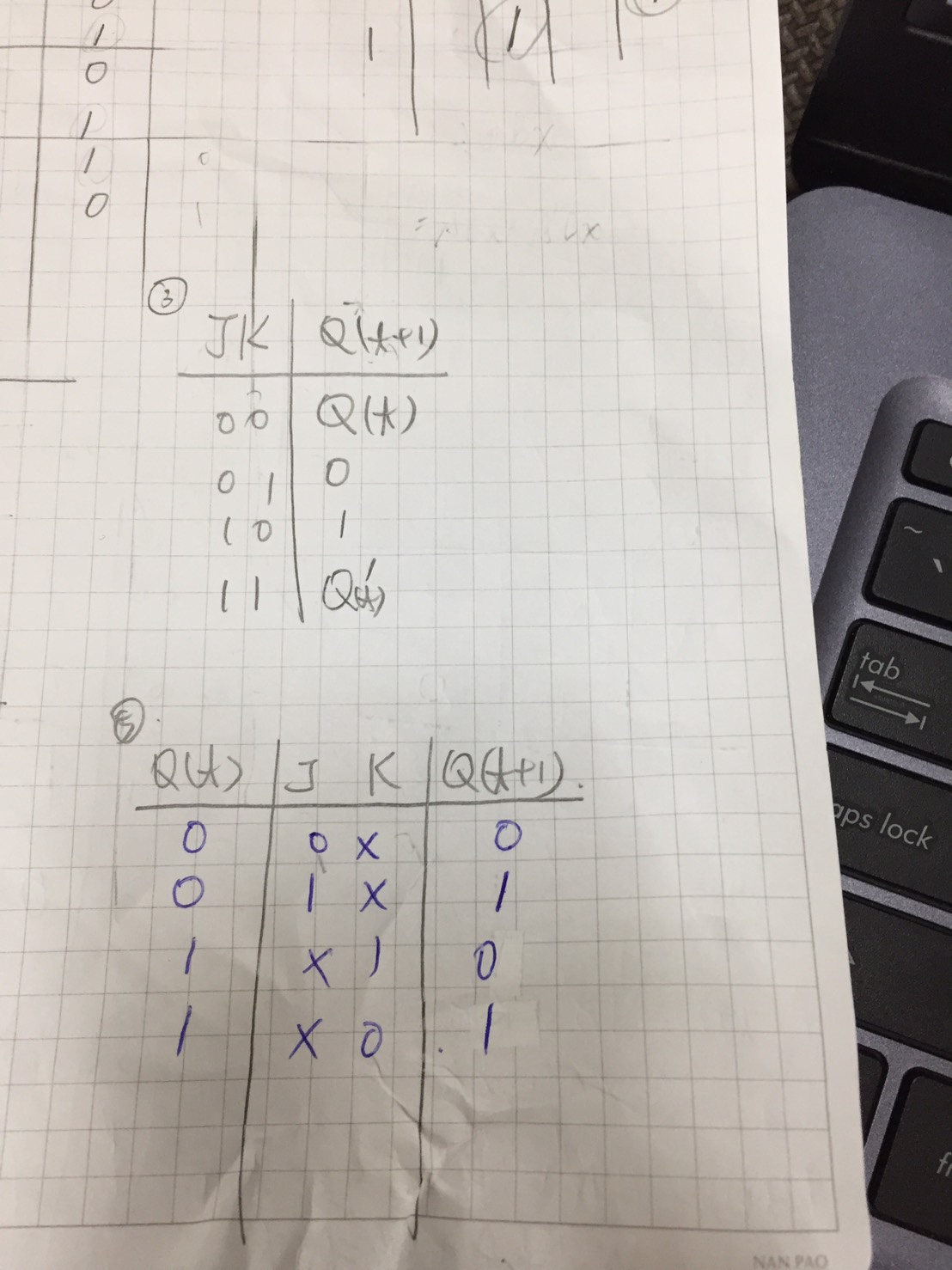


**Step2**

Explain JK flip flop by using following tables.

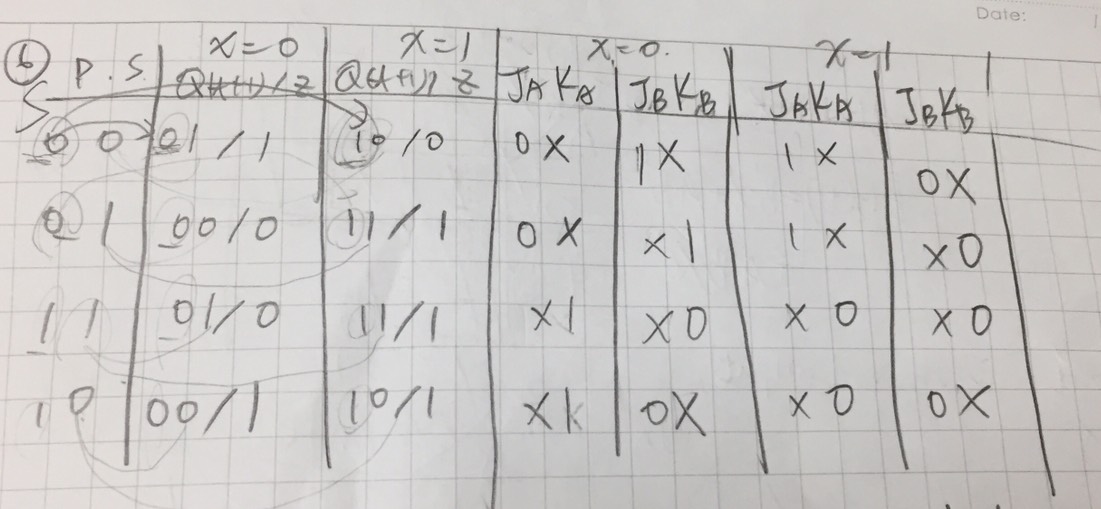






**Step3**

Using the result from step2, we can rearrange the table.



**Step4**

Use k map to sort out the result.

We will know the final result as following equations.

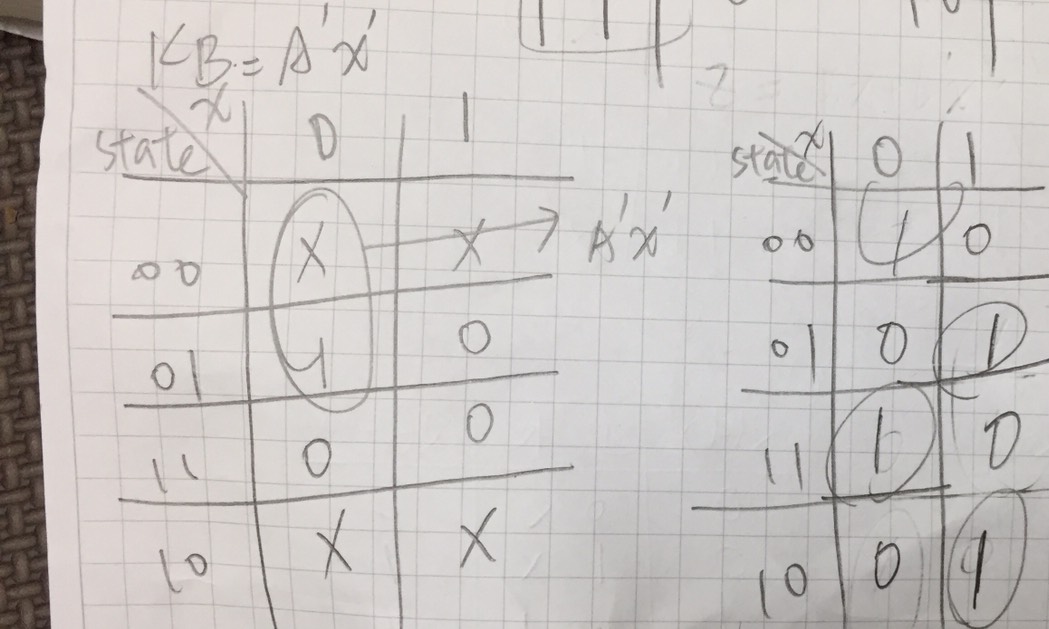
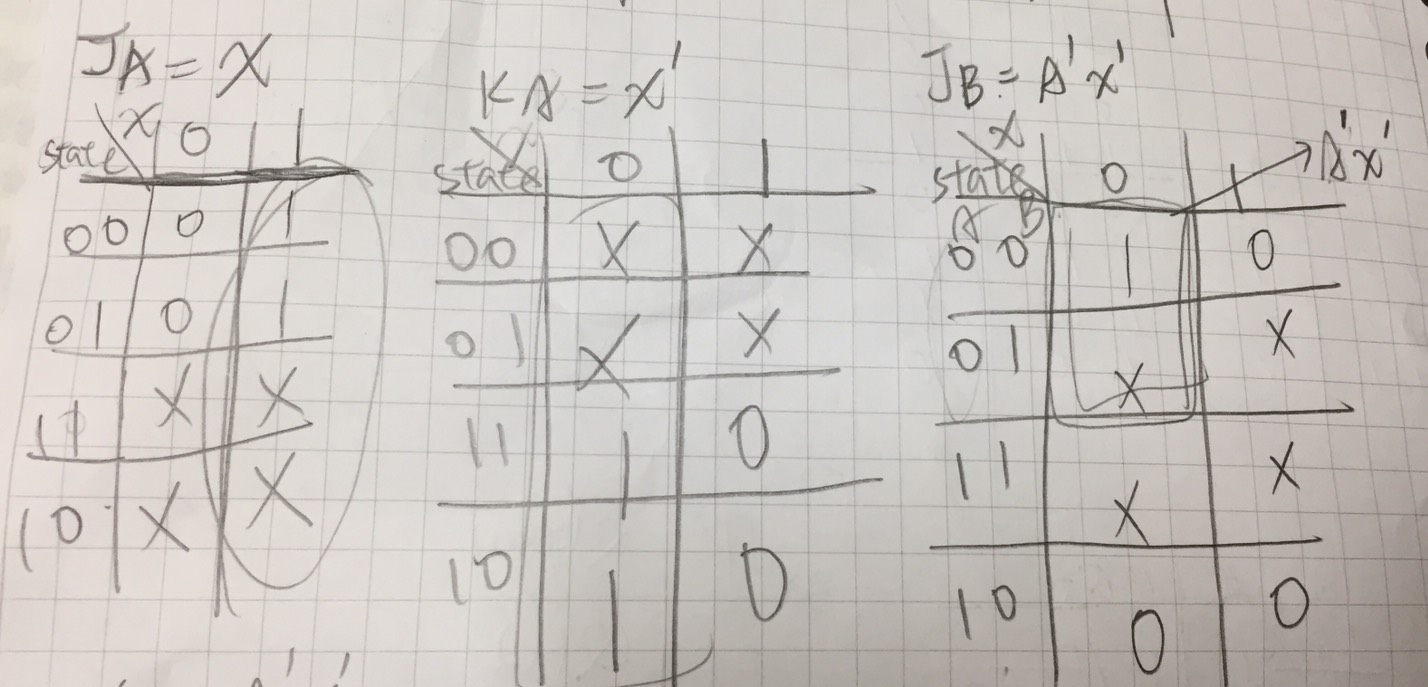
JA=x

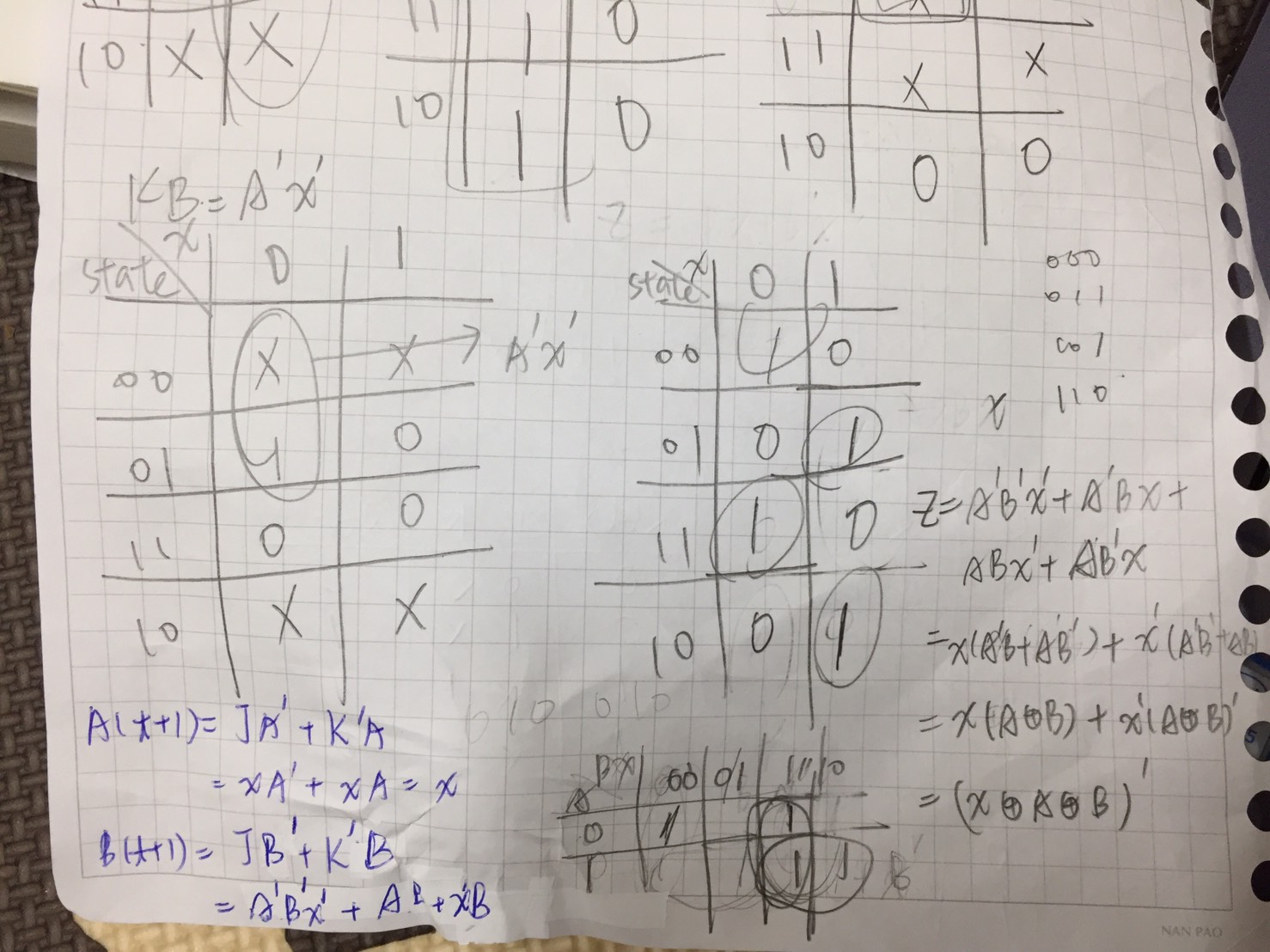
KA=x’

JB=A’x’

KB=A’x’

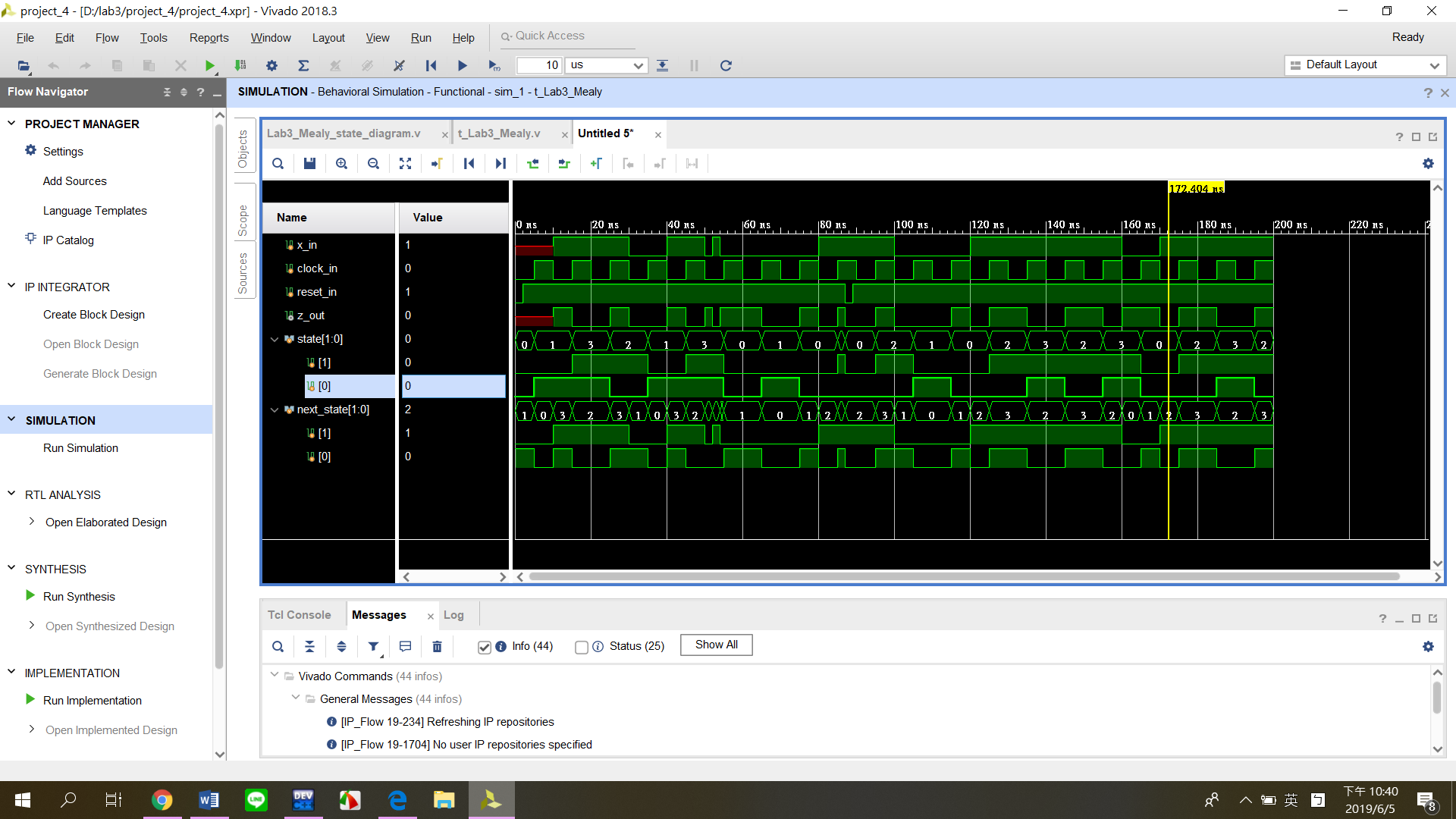
Z=(A ⊕ B ⊕ x)’



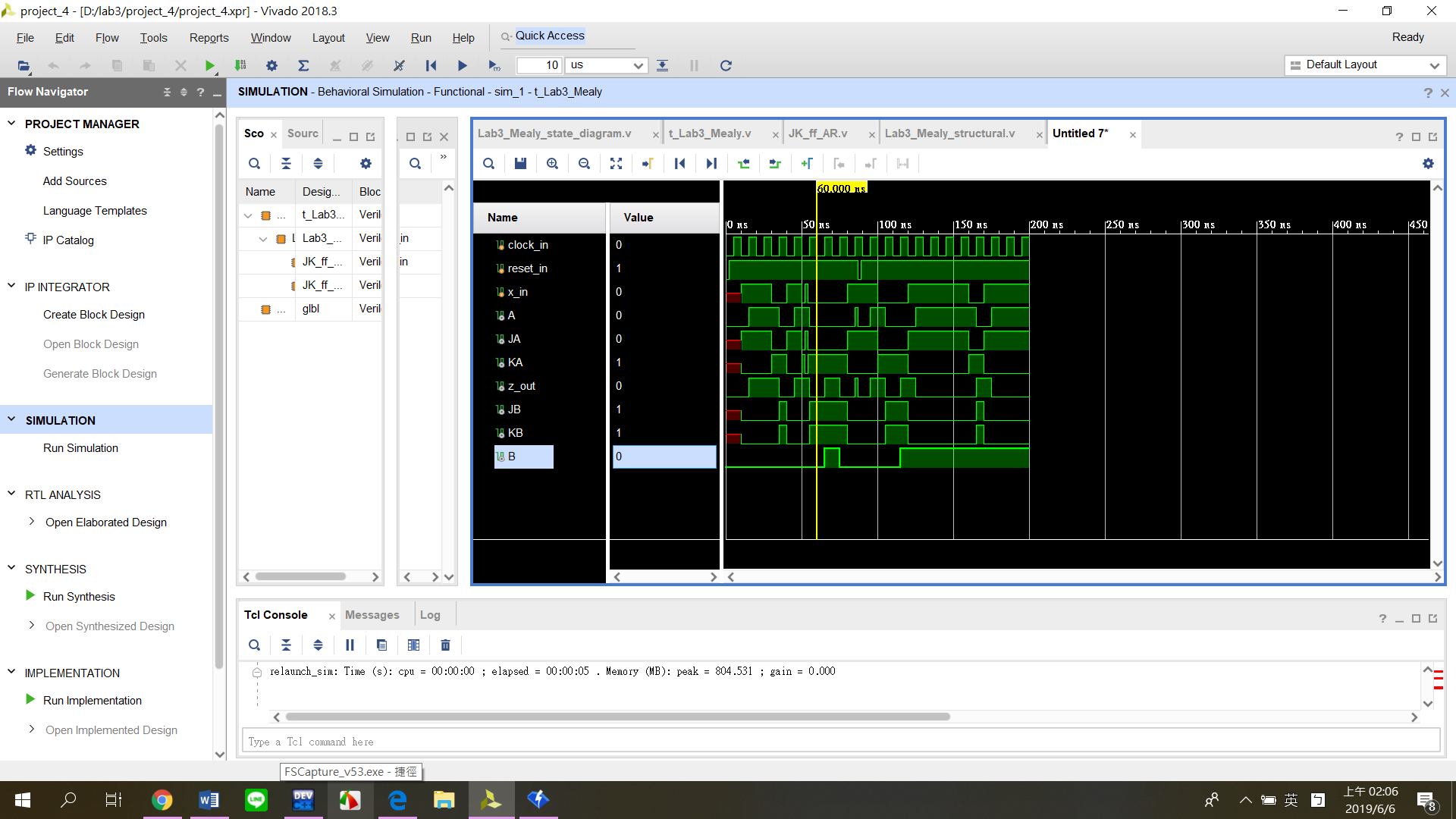


(b)show the circuit diagram

(i)circuit diagram



(ii)circuit diagram



(c)explain the testbench

**Testbench** follows the opinion of the textbook. When time goes to 87, the reset will influence the circuit. As result, it will make diagram have the fail signal.

(4)

There are still some problems in this lab. In 2.C, the data which Verilog shows to me is not the same as the data I wrote down on the paper. However I repeatedly check, I still couldn’t find where the wrong is.

By this lab, I can learn more about the flip flop, and also try many ways to represent the circuit. Although there are some mistakes which I can’t solve it, I still think this lab make me know more about the circuit.