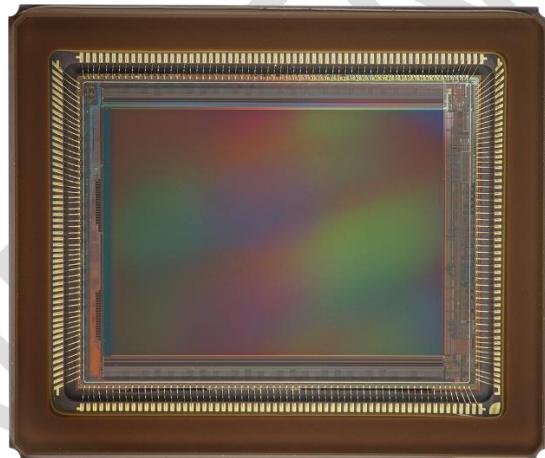


# Gpixel

## GMAX3412

12MP Global Shutter CMOS Image Sensor



Pre Datasheet V0.3.0

## Features

- Resolution: 4096(H) x 3072(V)
- 3.4µm square pixels
- Optical Format: 1.1"
- Electronic global shutter
- High speed and good PLS
- Internal/External triggering
- Functions:
  - Vertical sub-sampling
  - Vertical/Horizontal image flipping
  - Vertical ROI with speed boosting
- PGA Gain: 0dB – 24.91dB
- Digital Gain: x1 - x15.5
- 10/12 bit ADC depth
- Optional output channel:
  - Sub-LVDS
  - MIPI(CSI-2, D-PHY)
- On chip sequencer
- SPI and I<sup>2</sup>C control
- One Time Programmable(OTP) Memory

## Applications

- Machine Vision
- Logistics Bar Code Readers
- Intelligent Traffic System (ITS)

## Description

GMAX3412 is a 1.1" optical format CMOS image sensor with 4096 x 3072 effective pixels with frame rates up to 128/60 fps in 10/12-bit mode with sub LVDS interface and 30 fps over the alternative 4 MIPI D-PHY channels.

Based on a high-performance 3.4 µm charge domain global shutter pixel, GMAX3412 achieves a max full well capacity of 9.0 ke- and min dark noise of 1.9 e-, delivering max 67.9 dB linear dynamic range. Red Fox technology delivers QE of 75% @ 540 nm, and a NIR QE of 33% @850 nm. GMAX3412 is housed in 176 pin ceramic LGA package, 22.93 mm x 19.39 mm outer dimensions, and pin-compatible to GMAX3405.

GMAX3412 is configurable through I<sup>2</sup>C or SPI, and supports features such as multi-slope HDR and short

exposure time modes making it an ideal solution for an easy integration into cost-sensitive applications in machine vision, industrial bar code reading, logistics, and traffic.

## Specifications

Parameter	Value
Photosensitive area	14.0mm x 10.5mm
Pixel size	3.4µm x 3.4µm
Number of active pixels	4096 (H) x 3072 (V) Effective 4240 (H) x 3090 (V) Readable
Full well capacity(FWC)	9.0 ke- @12-bit, PGA gain x1.0
Temporal noise	3.7 e- @ 12-bit, PGA gain x1.0
Dynamic range	67.9 dB @ 12-bit, PGA gain x1.0
Peak QE	75% @540 nm; 33% @850 nm
Parasitic light sensitivity	- 88 dB (angular dependence)
Angular Response	> 15 ° (80% response)
Dark Current (35 °C die temperature)	6.5 e-/s/pixel
Input clock rate	20 – 62.5MHz (Recommended value: 40MHz)
Max. Frame rate	128 fps @Sub-LVDS 10bit 60 fps @Sub-LVDS 12bit 30 fps @MIPI 12bit
Data rate	Max. 1.2Gbps per channel @Sub-LVDS Max. 1.2Gbps per lane @MIPI
Supply voltage	3.6V for pixel 3.3V for analog 1.8V – 3.3V for IO 1.2V for digital
Output format	16 pairs of Sub-LVDS data output 2 pair of Sub-LVDS clock output or 4 lanes of MIPI data output 1 lane of MIPI clock output
Channel Multiplexing	16/14/12/10/8/6/4/2/1 @ Sub-LVDS; 4 @ MIPI
Power consumption	< 1.5 W
Chroma	Bayer RGB or Mono
Package	LGA 176 pins

## Revision History

Version	Date(dd/mm/yyyy)	Comment
V0.1.0	27/07/2023	First release
V0.1.1	22/08/2023	<ul style="list-style-type: none"> <li>1. Update readable regions in 'Specifications'.</li> <li>2. Update readable regions and user defined region in Figure 3.</li> <li>3. Update vertical window start address range : 0~4239 in Table 24.</li> <li>4. Update 'Channel Multiplexing' and Figure 48, Figure 41, Figure 51, update LVDS channel output columns.</li> <li>5. Update 'MIPI Serial Output ' and Figure 50, Figure 54, update MIPI channel output columns.</li> <li>6. Add note: total columns is multiple of 16 in LVDS output mode in 'Image Data Output Format'.</li> <li>7. Update total columns is multiple of 16 in MIPI mode in 'Image Data Output Format'.</li> <li>8. Update 'Multiple Region HDR' register setting and region N in Table 38.</li> </ul>
V0.2.0	18/10/2023	<ul style="list-style-type: none"> <li>1. Update PGA gain value in 'Features'.</li> <li>2. Add description information in 'Description'.</li> <li>3. Update PLS, QE, frame time and FWC in 'Specifications'.</li> <li>4. Update Figure 1 in 'Package Outline'.</li> <li>5. Add MIPI identification in Figure 5 in 'Internal Block Diagram'.</li> <li>6. Update power supplies in 'DC Characteristics' and 'Pin Description'.</li> <li>7. Update power consumption in 'Power Consumption'.</li> <li>8. Update register value in 'Register Map'.</li> <li>9. Update analog power, digital power, array supply, charge pump and bias pin connections in 'Periphery Connections'.</li> <li>10. Update clock frequency in 'SPI Communication Operation' and 'I2C Communication Operation'.</li> <li>11. Update TBD value in 'Exposure End Delay', 'Exposure Time Calculation', 'Power On/Off Sequence', 'Reset Sequence' and 'Minimum Exposure'.</li> <li>12. Update SI_CNT and FOT_CNT value in 'Windowing', 'SYNC Code', 'Exposure Start Delay' and 'Frame Rate Calculation'.</li> <li>13. Update information in Table 20, Table 21, Table 29, Figure 3 and Figure 29.</li> <li>14. Update Figure 30 in 'Clock System'.</li> <li>15. Remove figure information and add Table 47 for PGA gain in 'PGA Gain'.</li> <li>16. Update 'Multiple Region HDR' register setting and region 47 in Table 51.</li> <li>17. Update pixel data output in Figure 54.</li> <li>18. Update DNmax value in 'Test Image'.</li> <li>19. Complete the preliminary version of Blemish Specification</li> <li>20. Update the Product Ordering Information chapter.</li> </ul>
V0.3.0	17/11/2023	<ul style="list-style-type: none"> <li>1. Update PGA gain value in 'Features'.</li> <li>2. Update EO specs in Description and Specifications according to validation results.</li> <li>3. Update "Operation Temperature" Rating for Absolute Maximum Ratings.</li> <li>4. Add the min. and max. value of VIH in 'DC Characteristics'.</li> </ul>

	<ul style="list-style-type: none"><li>5. Update Image Sensor Characteristics chapter.</li><li>6. Refresh the registers in Table 15, Table 16 and Table 17.</li><li>7. Update min. value in 'Power On/Off Sequence' and 'Reset Sequence'.</li><li>8. Update information in Table 26 and Figure 30.</li><li>9. Update text information in 'SPI Communication Operation', 'Sub-LVDS Output', 'Channel Multiplexing', 'Multiple Slope HDR' and 'Test Image'.</li><li>10. Update information in Table 29, Figure 53 and Figure 54.</li><li>11. Add 10bit minimum line time value in Table 41.</li><li>12. Remove 1-lane and 2-lane information in MIPI mode in 'Image Data Output Format'.</li><li>13. Update information in Table 47 and note for PGA gain in 'PGA Gain'.</li><li>14. Add Figure 59 and update text information in Temperature Readout.</li><li>15. Update information in Figure 60 and Figure 61.</li><li>16. Add internal exposure description in Multiple Region HDR and Multiple Slope HDR.</li><li>17. Update Figure 58 in Test Image.</li><li>18. Update Defect limits of the demo grade.</li></ul>
--	---

CONFIDENTIAL

## Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Remarks
Supply Voltage (Analog 3.3V)	VDDA	-0.3 to 4.0	V	
Supply Voltage (Interface 1.8V to 3.3V)	VDDIO	-0.3 to 4.0	V	
Supply Voltage (Digital 1.2V)	VDDD	-0.3 to 1.7	V	
Supply Voltage (Pixel Voltage)	VDDPIX	-0.3 to 4.0	V	
Input Voltage	VI	-0.3 to VDDIO+0.3	V	Not exceed 4.0V
Output Voltage	VO	-0.3 to VDDIO+0.3	V	Not exceed 4.0V
Operation Temperature	Topr	-40 to +85	°C	Junction temperature
Storage Temperature	Tstg	T.B.D.	°C	Environment temperature

## Content

Features .....	1
Applications .....	1
Description.....	1
Specifications .....	1
Revision History .....	2
Absolute Maximum Ratings.....	4
Content .....	5
Package Outline .....	8
Optical Center & Temperature Sensor.....	9
Pixel Arrangement .....	10
Bayer pattern arrangement on pixel array.....	11
Internal Block Diagram and Pin Configuration.....	12
Internal Block Diagram.....	12
Pin Description.....	13
Electrical Characteristics .....	18
DC Characteristics .....	18
AC Characteristics .....	19
Power Consumption .....	21
Image Sensor Characteristics .....	22
Key Specification .....	22
Temporal Dark Noise Distribution.....	23
Spectral Sensitivity Characteristics .....	24
Dark Current with Different Die Temperature .....	26
Angular Response .....	27
Register Map.....	28
Driving the Sensor.....	42
Sensor Setting Flow .....	42
Periphery Connections.....	43
Analog Power Connections.....	43
Digital Power Connections .....	44
Array Supply Connections .....	45
Charge Pump Connection .....	46
Bias Pin Connections.....	46
Digital I/O and Clock inputs .....	47
Data Outputs.....	48
Power On/Off Sequence .....	49
Sensor Configuration .....	51
Line Time.....	51
Sub-Sampling .....	51
Windowing.....	52
Frame Number and Exposure Setting.....	56

Clock System .....	57
Reset Sequence.....	59
Register Communication Timing.....	60
SPI Communication Operation.....	60
I <sup>2</sup> C Communication Operation .....	63
Synchronization of Registers.....	65
Requesting Frames.....	67
Internal Exposure Control .....	67
External Exposure Control .....	69
Exposure Delay .....	70
Exposure Start Delay.....	70
Exposure End Delay.....	70
Exposure Time Calculation.....	71
Frame Rate Calculation.....	72
Reading Out The Sensor .....	73
Sub-LVDS Output.....	73
Data Interface Training.....	73
SYNC Code.....	74
Image Data Output Format.....	76
Channel Multiplexing.....	76
MIPI Serial Output .....	79
Image Data Output Format.....	79
Description of Various Functions .....	80
Minimum Exposure.....	80
Pins for Status Monitoring .....	80
Gain Adjustment .....	81
Digital Gain.....	81
PGA Gain .....	82
Image Flipping.....	83
Horizontal.....	83
Vertical .....	84
Black Level.....	85
Multiple Region HDR.....	85
Multiple Slope HDR.....	86
Test Image .....	88
Temperature Readout.....	89
OTP Memory Readout .....	90
SPI Interface .....	90
I <sup>2</sup> C Interface .....	91
OTP Data Description .....	92
Blemish Specification .....	93
Test images .....	93
Defect definitions.....	94

Defect limits .....	94
Storage Condition, Handling and Soldering .....	95
Product Ordering Information .....	96
Packing and Tray Specification .....	97
Rights .....	98
For More Information .....	99

CONFIDENTIAL

## Package Outline

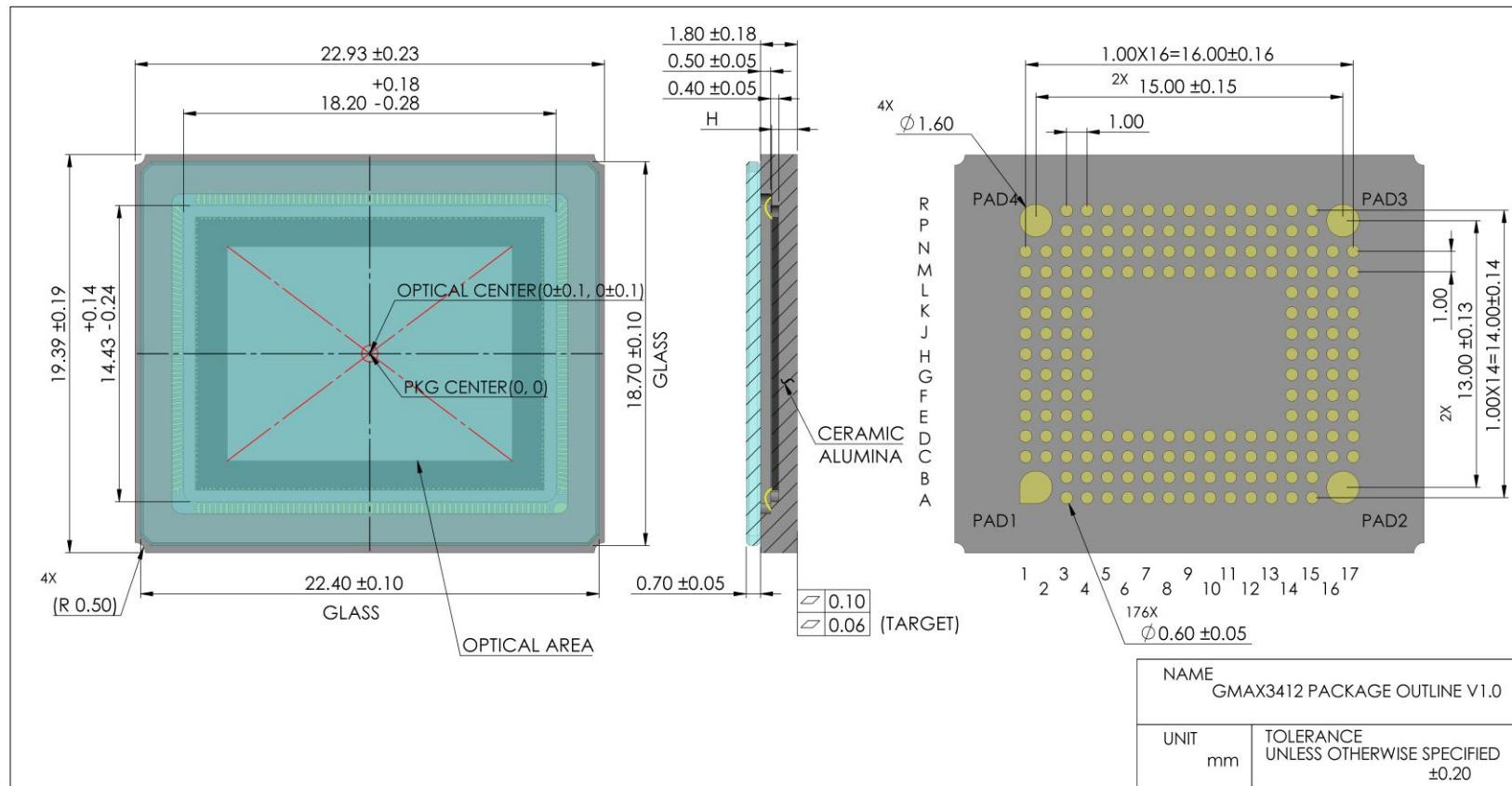


Figure 1 Package outline

Note:

1. The center of the optical sensitive area is at  $(0 \pm 0.10\text{mm}, 0 \pm 0.10\text{mm})$  relative to the center of the ceramic package.
2. The deviation of the die center relative to the cavity edge of the ceramic package is  $\pm 0.10\text{mm}$ . The rotation angle of the die relative to the cavity edge of the ceramic package is  $\pm 0.3^\circ$ . The tilt of the die relative to the die attach surface of the ceramic package is less than  $0.06\text{mm}$ .
3. The distance from the die surface to the bottom of the ceramic package (exclude the pin height) is  $1.25 \pm 0.15\text{mm}$  (H).
4. The thermal conductivity of the ceramic package is  $14 \text{ W}/(\text{mK})$ .
5. The thermal expansion coefficient of the ceramic package is  $7.1 \times 10^{-6}/\text{K}$  from room temperature ( $25 \pm 5^\circ\text{C}$ ) to  $400^\circ\text{C}$ .

## Optical Center & Temperature Sensor

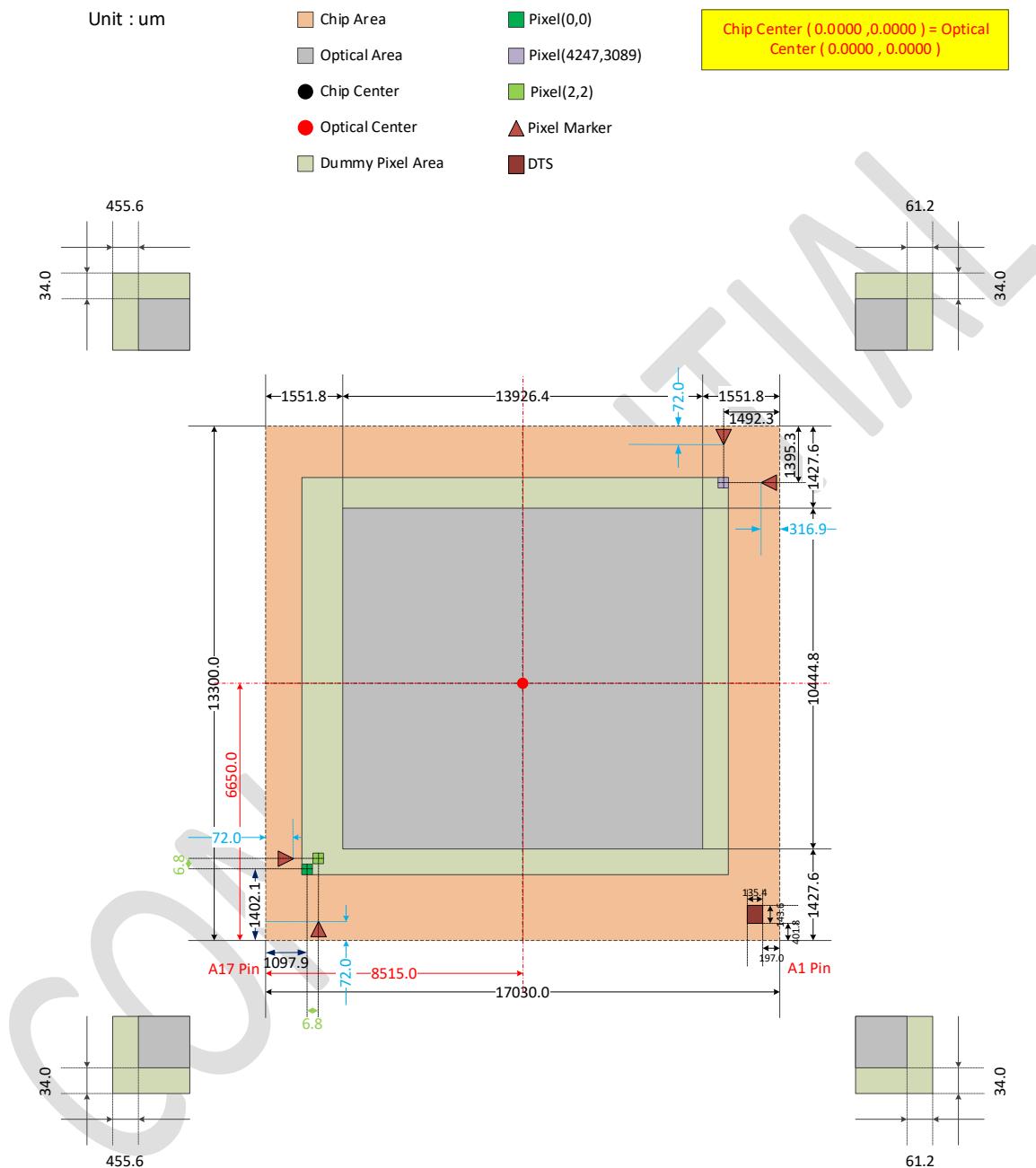


Figure 2 Optical center (top view)

Note: Figure 2 Optical center is with reference to the Chip (silicon die) center, for camera mechanic design, please refer to Figure 1 for optical center with reference to sensor package.

## Pixel Arrangement

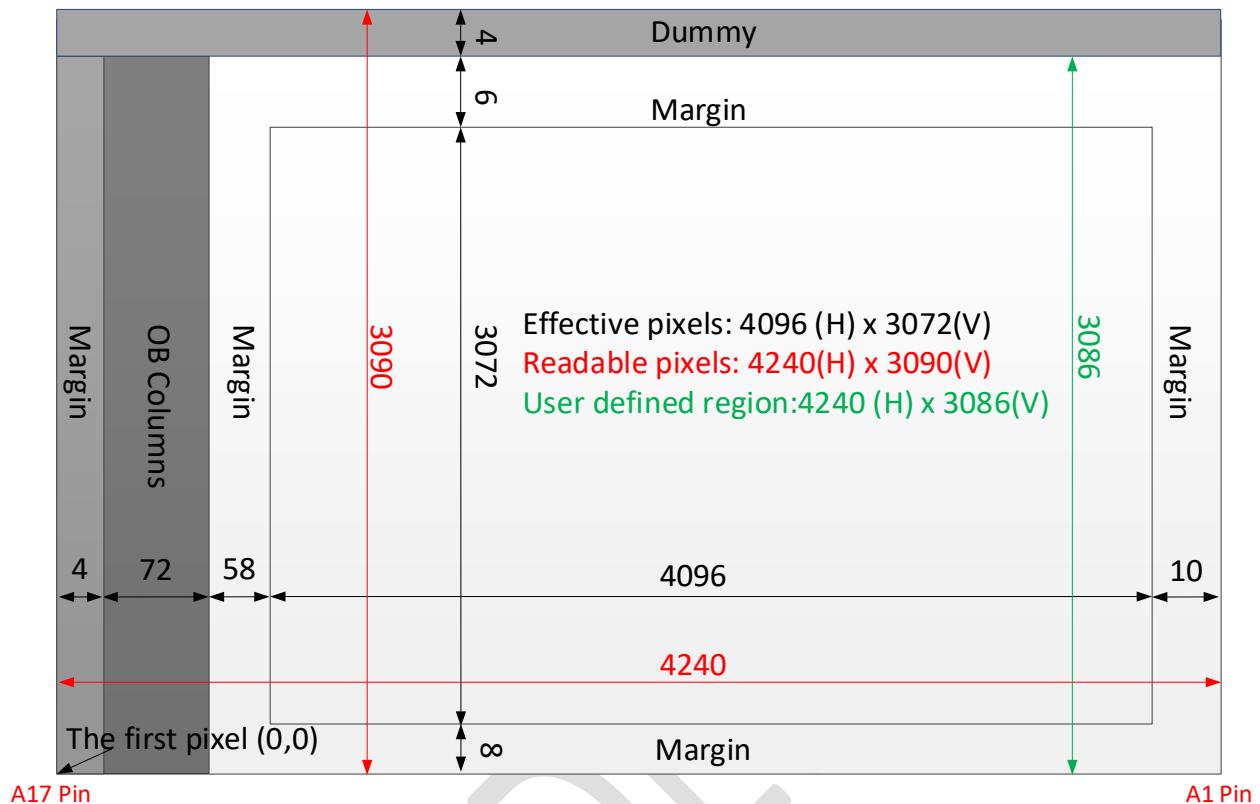


Figure 3 Pixel arrangement in physical(top view)

## Bayer pattern arrangement on pixel array

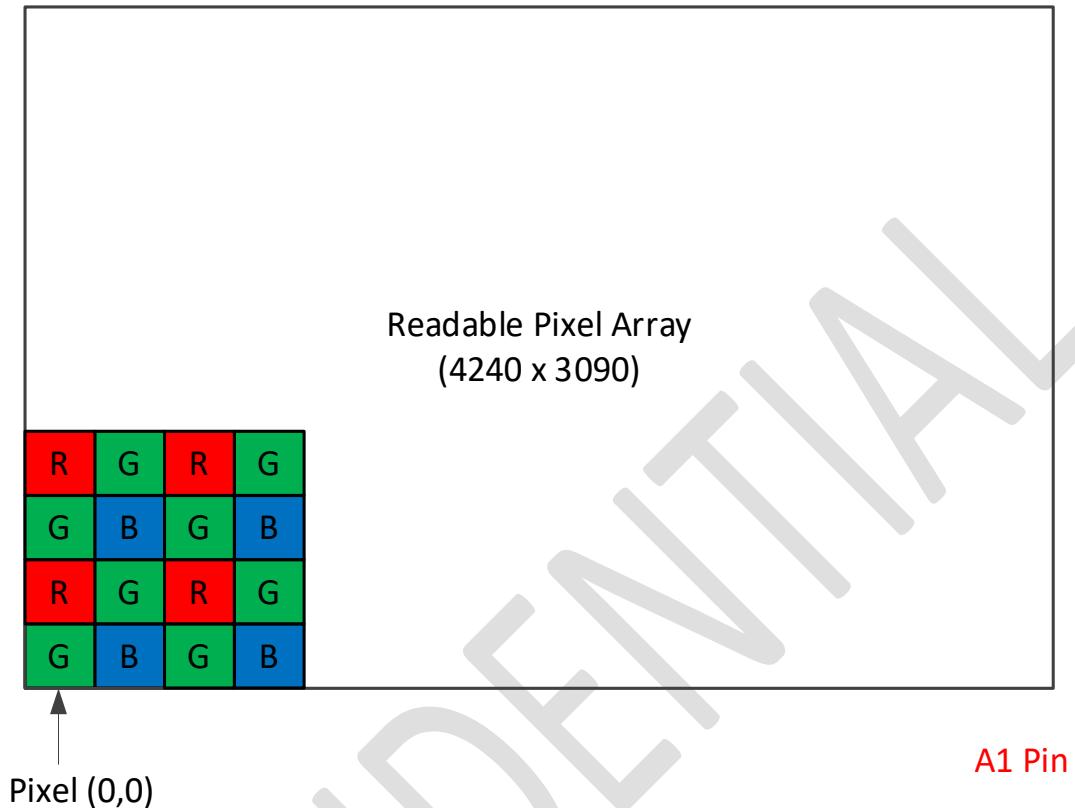


Figure 4 Bayer pattern on top of pixel array(top view)

## Internal Block Diagram and Pin Configuration

### Internal Block Diagram

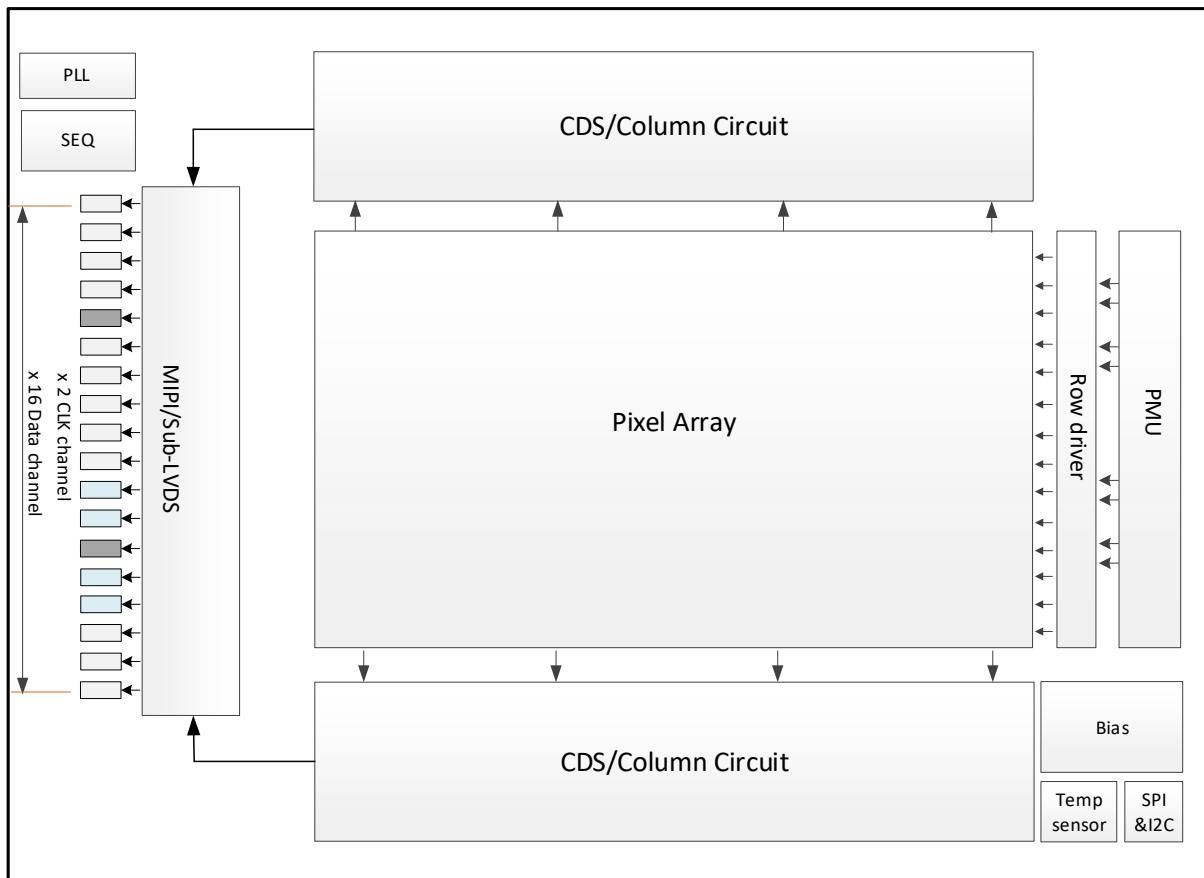


Figure 5 Block diagram

## Pin Description

Table 1 Pin description

No.	Pin No.	I/O	Symbol	Description	Type
1	A3	Power	VDDA	Analog supply	Supply
2	A4	Power	VDDD	Digital supply	Supply
3	A5	I/O	VBIASP	Internally generated bias voltage	Bias
4	A6	I/O	VREF	Internally generated reference voltage	Bias
5	A7	Power	VDDD	Digital supply	Supply
6	A8	Power	VDDA	Analog supply	Supply
7	A9	Power	VDDD	Digital supply	Supply
8	A10	Power	VDDD	Digital supply	Supply
9	A11	Power	VDDA	Analog supply	Supply
10	A12	Power	VDDD	Digital supply	Supply
11	A13	Power	VDDPIX	Pixel supply	Supply
12	A14	Power	VDDA	Analog supply	Supply
13	A15	--	NC	N/A	Leave floating
14	B3	GND	GNDA	Analog ground	Ground
15	B4	GND	GNDD	Digital ground	Ground
16	B5	--	NC	N/A	Leave floating
17	B6	--	NC	N/A	Leave floating
18	B7	GND	GNDD	Digital ground	Ground
19	B8	GND	GNDA	Analog ground	Ground
20	B9	Power	VDDD	Digital supply	Supply
21	B10	GND	GNDD	Digital ground	Ground
22	B11	GND	GNDA	Analog ground	Ground
23	B12	Power	VDDD	Digital supply	Supply
24	B13	GND	GNDPIX	Pixel ground	Ground
25	B14	O	OUTP<15>	Data positive channel 15	Data output
26	B15	O	OUTN<15>	Data negative channel 15	Data output
27	C1	GND	GNDA	Analog ground	Ground
28	C2	I/O	RES_EXT_NODE_P	Connected to Analog ground through a 12.4KΩ resistor	Analog input/output
29	C3	I/O	VBGR	Internal generated reference voltage	Bias
30	C4	--	NC	N/A	Leave floating
31	C5	--	NC	N/A	Leave floating
32	C6	--	NC	N/A	Leave floating
33	C7	Power	VDDD	Digital supply	Supply
34	C8	--	NC	N/A	Leave floating
35	C9	GND	GNDD	Digital ground	Ground
36	C10	Power	VDDD	Digital supply	Supply

37	C11	--	NC	N/A	Leave floating
38	C12	GND	GNDD	Digital ground	Ground
39	C13	--	NC	N/A	Leave floating
40	C14	O	OUTP<9>	Data positive channel 9	Data output
41	C15	O	OUTN<9>	Data negative channel 9	Data output
42	C16	O	OUTP<13>	Data positive channel 13	Data output
43	C17	O	OUTN<13>	Data negative channel 13	Data output
44	D1	Power	VDDA	Analog supply	Supply
45	D2	GND	GNDA	Analog ground	Ground
46	D3	O	TANA	Analog test signal output	Analog output
47	D4	--	NC	N/A	Leave floating
48	D5	--	NC	N/A	Leave floating
49	D6	--	NC	N/A	Leave floating
50	D7	GND	GNDD	Digital ground	Ground
51	D8	--	NC	N/A	Leave floating
52	D9	GND	GNDD	Digital ground	Ground
53	D10	GND	GNDD	Digital ground	Ground
54	D11	--	NC	N/A	Leave floating
55	D12	GND	GNDD	Digital ground	Ground
56	D13	--	NC	N/A	Leave floating
57	D14	O	OUTP<7>	Data positive channel 7	Data output
58	D15	O	OUTN<7>	Data negative channel 7	Data output
59	D16	O	OUTP<11>	Data positive channel 11	Data output
60	D17	O	OUTN<11>	Data negative channel 11	Data output
61	E1	I/O	VCPNO	Internal generated pixel supply	Bias
62	E2	GND	GNDA	Analog ground	Ground
63	E3	Power	VDDA	Analog supply	Supply
64	E4	GND	GNDA	Analog ground	Ground
65	E14	O	CLKP_OUT1	Clock 1 positive output	Data output
66	E15	O	CLKN_OUT1	Clock 1 negative output	Data output
67	E16	GND	GNDD	Digital ground	Ground
68	E17	Power	VDDD	Digital supply	Supply
69	F1	I/O	VCPNI	Internal generated pixel supply	Bias
70	F2	I/O	VTX2H	Internal generated pixel supply	Bias
71	F3	I/O	VTX1H	Internal generated pixel supply	Bias
72	F4	I/O	VGRSTH	Internal generated pixel supply	Bias
73	F14	O	OUTP<5>	Data positive channel 5	Data output
74	F15	O	OUTN<5>	Data negative channel 5	Data output
75	F16	GND	GNDD	Digital ground	Ground
76	F17	Power	VDDD	Digital supply	Supply
77	G1	Power	VDDA	Analog supply	Supply
78	G2	I/O	VTX1L	Internal generated pixel supply	Bias

79	G3	I/O	VTX2L	Internal generated pixel supply	Bias
80	G4	I/O	VGRSTL	Internal generated pixel supply	Bias
81	G14	O	OUTP<3>	Data positive channel 3	Data output
82	G15	O	OUTN<3>	Data negative channel 3	Data output
83	G16	O	OUTP<1>	Data positive channel 1	Data output
84	G17	O	OUTN<1>	Data negative channel 1	Data output
85	H1	I/O	VCPP1	Internal generated pixel supply	Bias
86	H2	--	NC	N/A	Leave floating
87	H3	--	NC	N/A	Leave floating
88	H4	I/O	VGRSTL2	Internal generated pixel supply	Bias
89	H14	O	OUTP<0>	Data positive channel 0	Data output
90	H15	O	OUTN<0>	Data negative channel 0	Data output
91	H16	GND	GNDD	Digital ground	Ground
92	H17	Power	VDDD	Digital supply	Supply
93	J1	I/O	VCPO	Internal generated pixel supply	Bias
94	J2	GND	GNDA	Analog ground	Ground
95	J3	Power	VDDA	Analog supply	Supply
96	J4	GND	GNDA	Analog ground	Ground
97	J14	O	OUTP<2>	Data positive channel 2	Data output
98	J15	O	OUTN<2>	Data negative channel 2	Data output
99	J16	GND	GNDD	Digital ground	Ground
100	J17	Power	VDDD	Digital supply	Supply
101	K1	GND	GNDA	Analog ground	Ground
102	K2	--	NC	N/A	Leave floating
103	K3	Power	VDDA	Analog supply	Supply
104	K4	GND	GNDA	Analog ground	Ground
105	K14	O	OUTP<4>	Data positive channel 4	Data output
106	K15	O	OUTN<4>	Data negative channel 4	Data output
107	K16	O	OUTP<6>	Data positive channel 6	Data output
108	K17	O	OUTN<6>	Data negative channel 6	Data output
109	L1	I	SYS_RST_N	System reset signal	Digital input
110	L2	I	TEXP2	External trigger 2	Digital input
111	L3	I	TEXP1	External trigger 1	Digital input
112	L4	--	NC	N/A	Leave floating
113	L14	O	OUTP<8>	Data positive channel 8	Data output
114	L15	O	OUTN<8>	Data negative channel 8	Data output
115	L16	O	CLKP_OUT0	Clock 0 positive output	Data output
116	L17	O	CLKN_OUT0	Clock 0 negative output	Data output
117	M1	Power	VDDIO	IO ring supply	Supply
118	M2	I	XCE_SLAMODE	XCE: SPI input SLAMODE:I <sup>2</sup> C slave address select	Digital input

119	M3	O	SDO_TDIG	SDO :SPI output TDIG: Digital test signal output	Digital output
120	M4	I	SCK	SPI clock	Digital input
121	M5	--	NC	N/A	Leave floating
122	M6	--	NC	N/A	Leave floating
123	M7	GND	GNDD	Digital ground	Ground
124	M8	--	NC	N/A	Leave floating
125	M9	GND	GNDD	Digital ground	Ground
126	M10	GND	GNDD	Digital ground	Ground
127	M11	--	NC	N/A	Leave floating
128	M12	GND	GNDD	Digital ground	Ground
129	M13	--	NC	N/A	Leave floating
130	M14	O	OUTP<10>	Data positive channel 10	Data output
131	M15	O	OUTN<10>	Data negative channel 10	Data output
132	M16	O	OUTP<12>	Data positive channel 12	Data output
133	M17	O	OUTN<12>	Data negative channel 12	Data output
134	N1	I	CLK_REF	PLL reference clock	Digital input
135	N2	I	SDI	SPI input	Digital input
136	N3	I	SCL	I <sup>2</sup> C serial clock line	Digital input
137	N4	I/O	SDA	I <sup>2</sup> C serial data line	Digital input/output
138	N5	GND	GNDD	Digital ground	Ground
139	N6	--	NC	N/A	Leave floating
140	N7	Power	VDDD	Digital supply	Supply
141	N8	--	NC	N/A	Leave floating
142	N9	GND	GNDD	Digital ground	Ground
143	N10	Power	VDDD	Digital supply	Supply
144	N11	--	NC	N/A	Leave floating
145	N12	GND	GNDD	Digital ground	Ground
146	N13	--	NC	N/A	Leave floating
147	N14	GND	GNDA	Analog ground	Ground
148	N15	O	OUTP<14>	Data positive channel 14	Data output
149	N16	O	OUTN<14>	Data negative channel 14	Data output
150	N17	--	NC	N/A	Leave floating
151	P3	I	CCI_EN	SPI and I <sup>2</sup> C optional input control (0:SPI, 1:I <sup>2</sup> C)	Digital input
152	P4	GND	GNDA	Analog ground	Ground
153	P5	Power	VDDD	Digital supply	Supply
154	P6	I/O	VRS	Internal generated reference voltage	Bias
155	P7	GND	GNDD	Digital ground	Ground
156	P8	GND	GNDA	Analog ground	Ground
157	P9	Power	VDDD	Digital supply	Supply
158	P10	GND	GNDD	Digital ground	Ground
159	P11	GND	GNDA	Analog ground	Ground

160	P12	Power	VDDD	Digital supply	Supply
161	P13	GND	GNDPIX	Pixel ground	Ground
162	P14	GND	GNDA	Analog ground	Ground
163	P15	GND	GNDD	Digital ground	Ground
164	R3	GND	GNDD	Digital ground	Supply
165	R4	Power	VDDA	Analog supply	Supply
166	R5	Power	VDDA	Analog supply	Supply
167	R6	I/O	VRF	Internal generated reference voltage	Bias
168	R7	Power	VDDD	Digital supply	Supply
169	R8	Power	VDDA	Analog supply	Supply
170	R9	Power	VDDD	Digital supply	Supply
171	R10	Power	VDDD	Digital supply	Supply
172	R11	Power	VDDA	Analog supply	Supply
173	R12	Power	VDDD	Digital supply	Supply
174	R13	Power	VDDPIX	Pixel supply	Supply
175	R14	Power	VDDA	Analog supply	Supply
176	R15	Power	VDDD	Digital supply	Supply

## Electrical Characteristics

### DC Characteristics

Table 2 DC characteristics

Item		Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Analog	VDDA		3.25	3.3	3.35	V
	Digital	VDDIO		1.7	1.8	3.3	V
		VDDD		1.15	1.2	1.25	V
	Pixel	VDDPIX		3.55	3.6	3.65	V
Digital Input		XCE_SLAMODE					
		SCK					
		SDI	VIH	0.8xVDDIO	VDDIO	VDDIO+0.3V	V
		CCI_EN					
		SCL					
		SDA					
		CLK_REF					
		SYS_RST_N	VIL	0	0	0.3	V
		TEXP1					
		TEXP2					
Digital Output		SDO_TDIG	VOH		VDDIO		V
			VOL	0	0	0	V
Sub-LVDS Output		CLKN_OUT0	VCM		0.9		V
		CLKP_OUT0					
		CLKN_OUT1					
		CLKP_OUT1					
		OUTN<0:15>	VOD	0.1	0.15	0.2	V
		OUTP<0:15>					

**Note:**

- 1) The characterization results are measured with typical values of all supplies in the above table.

## AC Characteristics

### 1. Digital input reference clock (CLK\_REF) waveform diagram

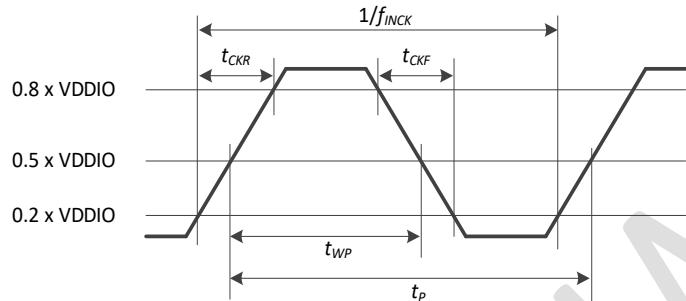


Figure 6 AC input reference clock

Table 3 AC characteristics for CLK\_REF

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
CLK_REF frequency	$f_{INCK}$	20	40	62.5	MHz	
CLK_REF rising edge	$t_{CKR}$			5	ns	Define with $0.2 \times VDDIO$ and $0.8 \times VDDIO$
CLK_REF falling edge	$t_{CKF}$			5	ns	Define with $0.2 \times VDDIO$ and $0.8 \times VDDIO$
CLK_REF duty ratio		45	50	55	%	Define with $0.5 \times VDDIO$

### 2. Digital input control signal waveform diagram

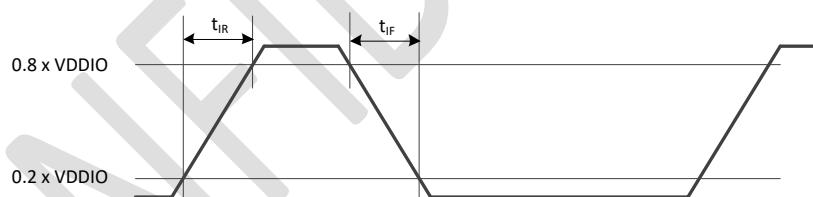


Figure 7 AC digital input control signal

Table 4 AC characteristics for digital input control signals

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Control signal rising edge	$t_{IR}$	—	3	5	ns	Define with $0.2 \times VDDIO$ and $0.8 \times VDDIO$
Control signal falling edge	$t_{IF}$	—	3	5	ns	Define with $0.2 \times VDDIO$ and $0.8 \times VDDIO$

### 3. Digital Output Signal waveform diagram

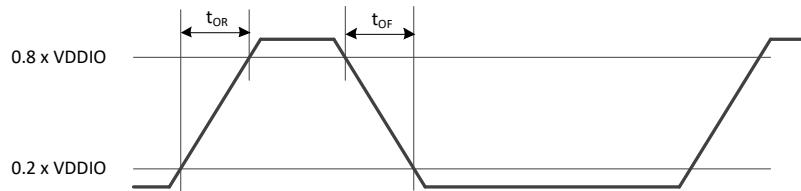


Figure 8 AC digital output control signal

Table 5 AC characteristics for digital input control signal

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Digital output signal rising edge	$t_{OR}$		0.9		ns	Define with 0.2 x VDDIO and 0.8 x VDDIO Simulated with 15pF capacitance load
Digital output signal falling edge	$t_{OF}$		0.9		ns	Define with 0.2 x VDDIO and 0.8 x VDDIO Simulated with 15pF capacitance load

**Note:**

- 1) Output load capacitance < 18pF.

## 4. Sub-LVDS Driver Output

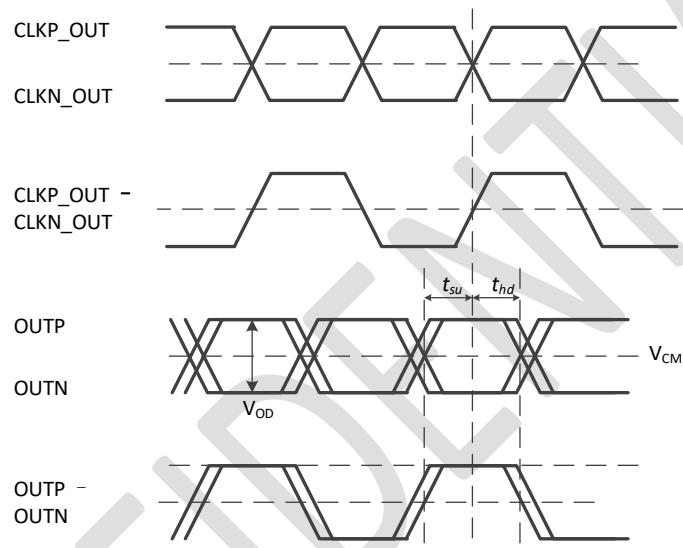


Figure 9 Sub-LVDS driver output

Table 6 Sub-LVDS driver output

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Clock Duty Cycle		40	50	60	%	DDR clock 600MHz
Data setup time	$t_{su}$	T.B.D.			ps	Data rate 1200Mbps
Data hold time	$t_{hd}$	T.B.D.			ps	Data rate 1200Mbps
Differential voltage swing	$V_{OD}$	100	150	200	mV	
Common mode voltage	$V_{CM}$	0.8	0.9	1.0	V	

**Note:**

- 1) The same AC characteristics applies for clock channel.  
 2) Output load capacitance < 8pF.

## Power Consumption

The typical current for each supply based is listed in Table 7, Table 8 and Table 9.

Table 7 Power Consumption for 12bit @1.2GHz sub-LVDS

Supply source	Typical voltage (V)	Average current (mA)	Peak current (mA)	Average power consumption (mW)
VDDA	3.3	150	175	495
VDDD	1.2	360	420	432
VDDIO	1.8	<1	1	1.8
VDDPIX	3.6	80	123	288
Total Power consumption (mW)				1216.8

Table 8 Power Consumption for 12bit @1.2GHz MIPI

Supply source	Typical voltage (V)	Average current (mA)	Peak current (mA)	Average power consumption (mW)
VDDA	3.3	145	162	478.5
VDDD	1.2	260	335	312
VDDIO	1.8	<1	<1	1.8
VDDPIX	3.6	85	115	306
Total Power consumption (mW)				1098.3

Table 9 Power Consumption for 10bit @1.2GHz sub-LVDS

Supply source	Typical voltage (V)	Average current (mA)	Peak current (mA)	Average power consumption (mW)
VDDA	3.3	195	210	643.5
VDDD	1.2	365	380	438
VDDIO	1.8	11	25	19.8
VDDPIX	3.6	105	122	378
Total Power consumption (mW)				1479.3

## Image Sensor Characteristics

### Key Specification

Table 10 Key performance for Sub-LVDS 12bit mode

Item	PGA Gain x1			Typ.	Unit	Note
	Min.	Typ.	Max.			
Conversion factor		0.43		6.31	DN/e-	
Full well capacity	T.B.D	9.0		0.6	ke-	1
Non-linearity error		0.3	T.B.D	0.6	%	2
Max. SNR		39.5		27.7	dB	3
Temporal dark noise		3.6	T.B.D	1.9	e-	
Dynamic range		67.9		49.9	dB	4
Peak QE @ 540nm		75			%	5
Sensitivity @ 540nm		2.36 x10 <sup>7</sup>			e- / (W/m <sup>2</sup> )·s)	
Dark current		81.6			e-/s	6
DSUN		2.2	T.B.D	2.4	e-	7
PRNU		0.6	T.B.D	0.9	%	7

Table 11 Key performance for MIPI 12bit mode

Item	PGA Gain x1			Typ.	Unit	Note
	Min.	Typ.	Max.			
Conversion factor		0.43		7.23	DN/e-	
Full well capacity	T.B.D	9.0		0.5	ke-	1
Non-linearity error		0.2	T.B.D	0.5	%	2
Max. SNR		39.5		26.9	dB	3
Temporal dark noise		4.1	T.B.D	1.8	e-	
Dynamic range		66.8		48.8	dB	4
DSUN		2.5	T.B.D	2.2	e-	7
PRNU		0.6	T.B.D	1.0	%	7

Table 12 Key performance for Sub-LVDS 10bit mode

Item	PGA Gain x1			Typ.	Unit	Note
	Min.	Typ.	Max.			
Conversion factor		0.12		0.23	DN/e-	
Full well capacity	T.B.D	8.0		4.0	ke-	1
Non-linearity error		0.3	T.B.D	0.3	%	2
Max. SNR		39.0		36.0	dB	3
Temporal dark noise		6.4	T.B.D	3.3	e-	
Dynamic range		61.9		61.6	dB	4
DSNU		3.9	T.B.D	4.9	e-	7
PRNU		0.6	T.B.D	0.6	%	7

**Notes for key specification:**

1. Full well capacity (FWC) is calculated by dividing the saturation level (DN) by the conversion factor (DN/e<sup>-</sup>).
2. Non-linearity error is calculated in range between 5-95% of the saturation level.
3. Maximum SNR is calculated by square root of the FWC (e<sup>-</sup>), the unit of dB is 20 x log (SNR).
4. Dynamic range is the ratio of FWC (e<sup>-</sup>) to temporal dark noise (e<sup>-</sup>)
5. The measurement result equals to QE x FF (fill factor).
6. Dark current is measured at 58.6°C die temperature which is obtained by calibration of the die temperature sensor.
7. DSNU and PRNU results are both measured with full scale image without defect rows or columns.
8. All measurement methods are based on the EMVA Standard 1288 (Release 4.0) if no special noted.

## Temporal Dark Noise Distribution

The curves below show the cumulative histogram for temporal dark noise distribution with PGA gain x1.0.

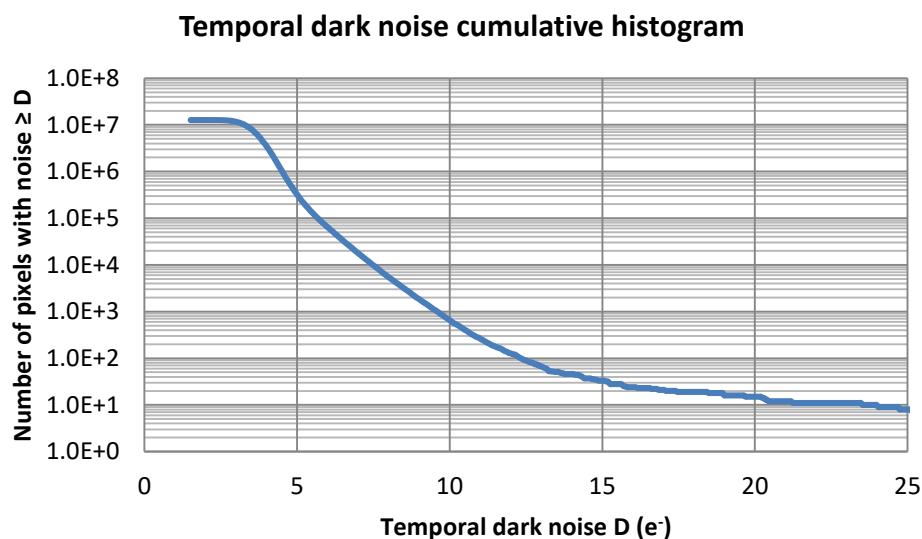


Figure 10 Temporal dark noise distribution for sub-LVDS 12bit

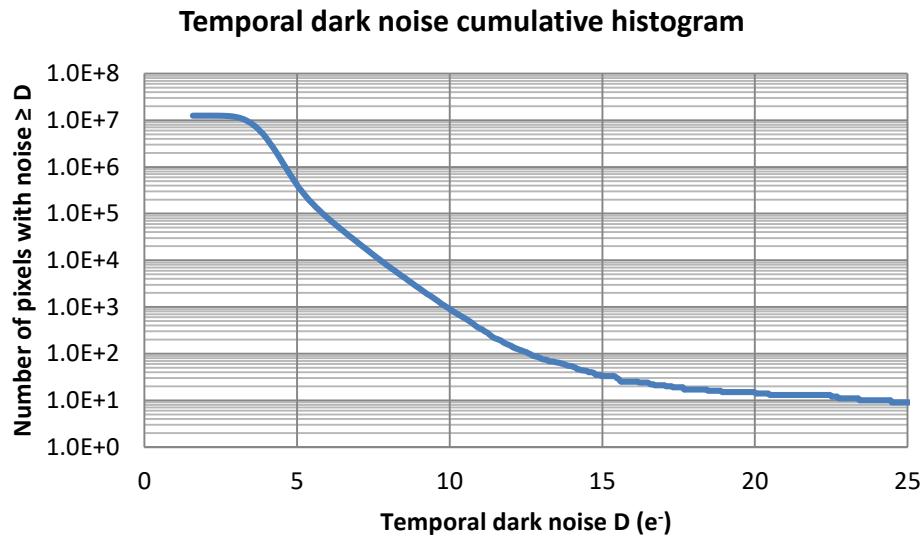


Figure 11 Temporal dark noise distribution for MIPI 12bit

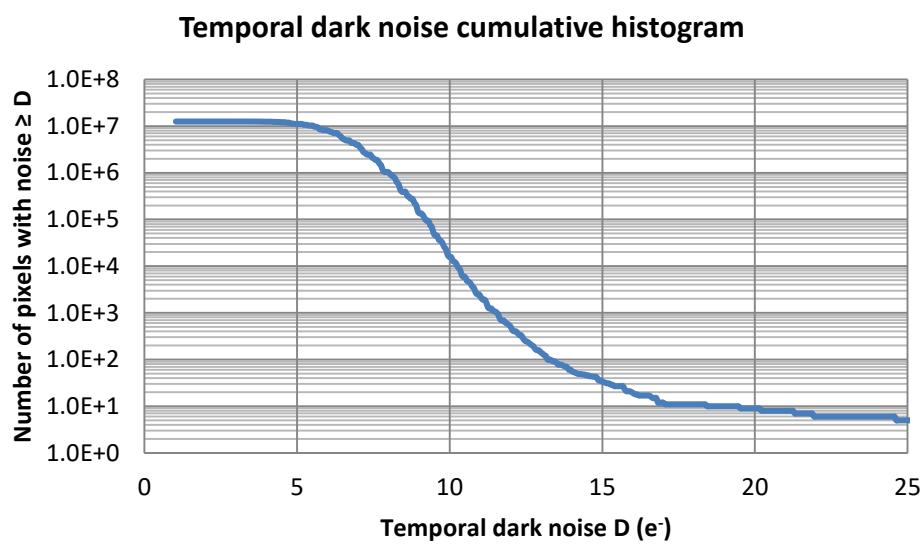


Figure 12 Temporal dark noise distribution for sub-LVDS 10bit

## Spectral Sensitivity Characteristics

The curve below displays the spectral response for spectrum of 350-1100nm.

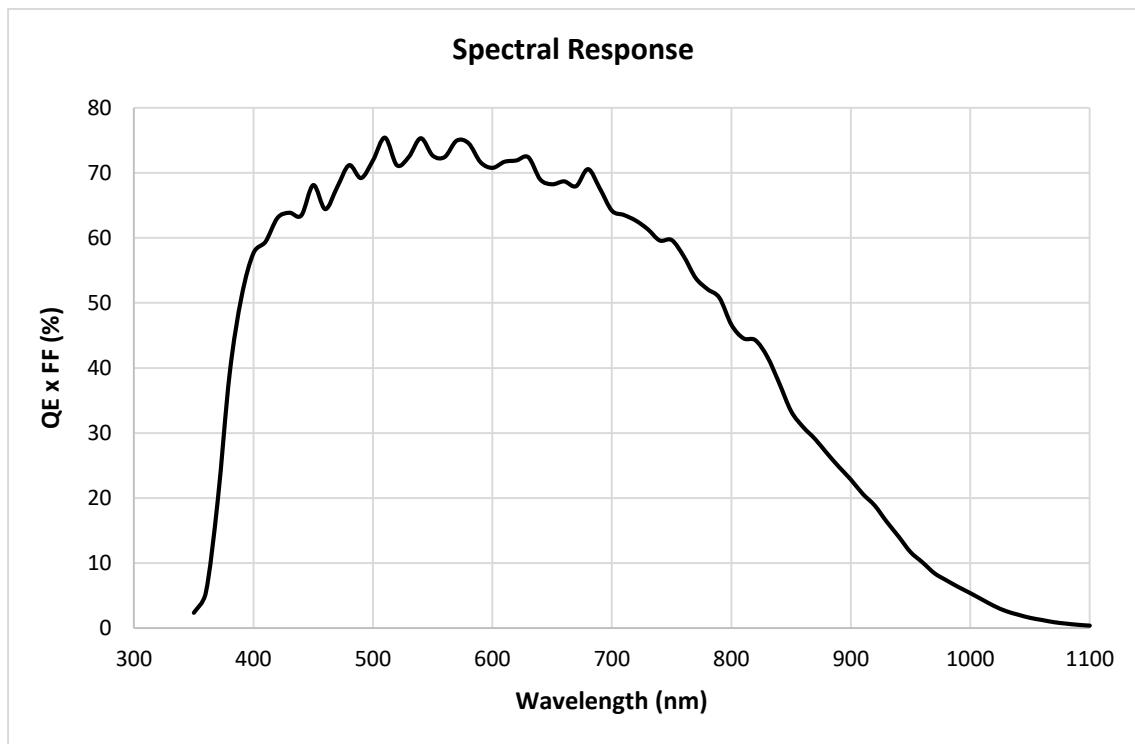


Figure 13 Spectral Sensitivity Characteristics

The table below shows more details about the QE measurement results.

Table 13 Detailed QE measurement results

Wavelength (nm)	QE x FF (%)
350	2.3
400	57.7
450	68.1
500	71.9
540	75.3
550	72.7
600	70.8
650	68.2
700	64.2
750	59.7
800	46.6
850	33.3
900	22.8
950	11.7
1000	5.4
1050	1.6
1100	0.4

## Dark Current with Different Die Temperature

Dark current test results with different temperature are shown below. The die temperature is measured with on-chip temperature sensor.

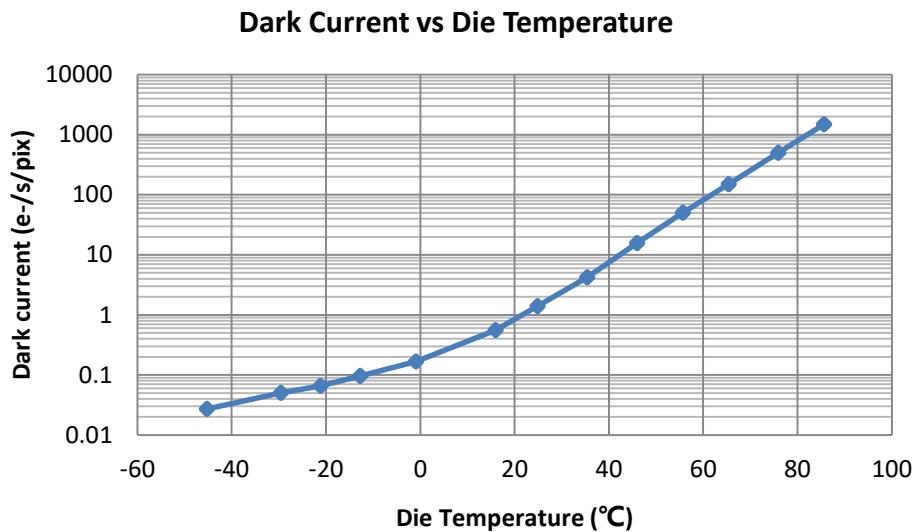


Figure 14 Dark current with different die temperature

The graph below shows the dark current distribution of the sensor tested at 0°C of die temperature. The dark current value with the most pixel counts is around 0.2 e-/s/pix.

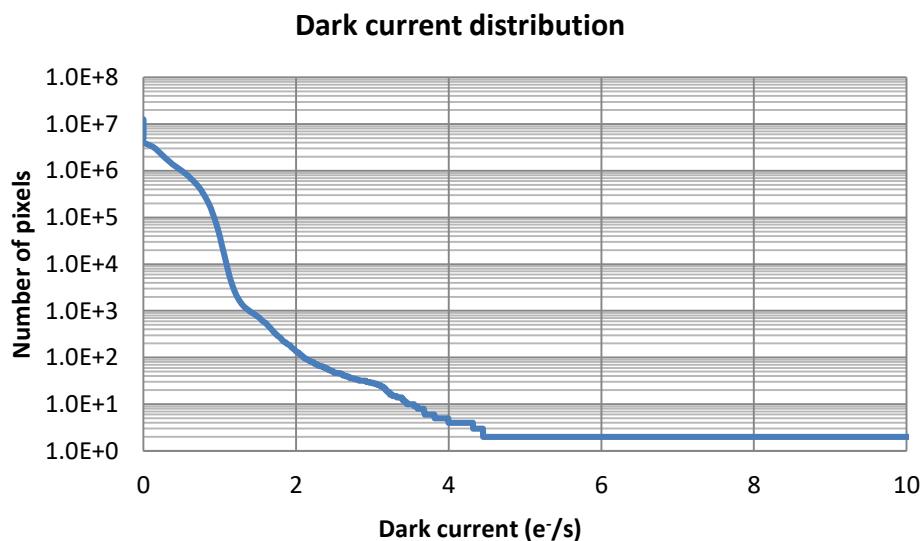


Figure 15 Dark current distribution

## Angular Response

The sensor response depends on CRA of the incident light. To measure the angle response of the pixels, a pixel array consists of 10x1 pixels are selected for this measurement. At each angle of the light ray, 20 grabbed images are averaged in order to reduce temporal noise influence. Then the averaged image is averaged over all its pixels. The typical angle response for the sensor can be seen in the figure below. The data includes the horizontal and vertical angles.

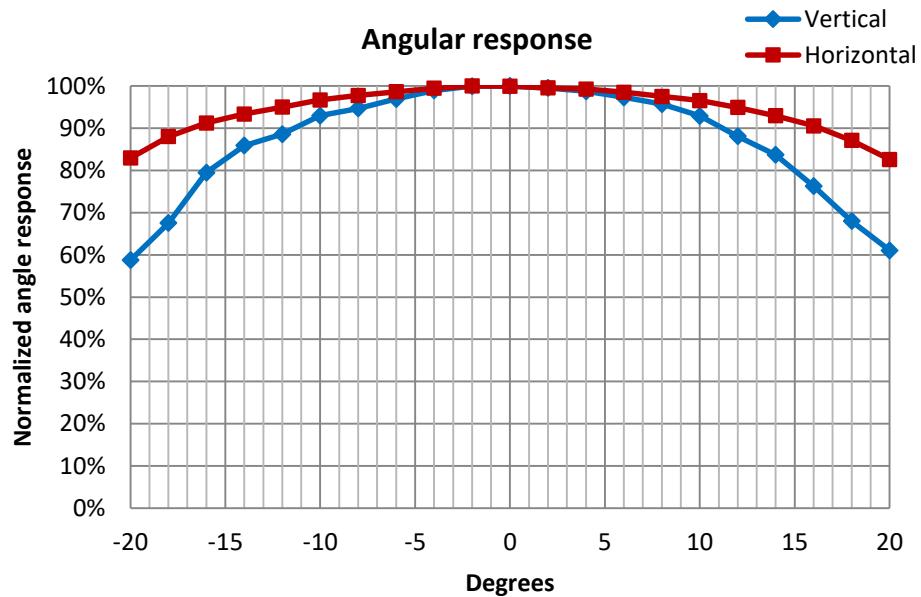


Figure 16 Angular response of the horizontal and vertical directions

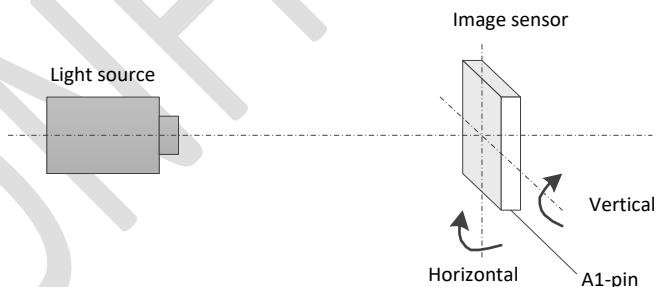


Figure 17 Horizontal and vertical definition

## Register Map

Table 14 gives the default register setting after sensor power-on. The recommend register setting for GMAX3412 working is shown in Table 15, Table 16 and Table 17.

Some of the registers may need to be tuned based on specific applications, i. e. the registers described in section ‘Sensor Configuration’ and ‘Description of Various Functions’. These registers can have digital setting bits separated in two or more neighbor bytes(Address). In this case, the grouping is not always from high to low. For example, register DOFF\_ODD is 12-bit shown in Table 50. Its digital bit from high to low in SPI protocol is from 906-Bit <3:0> to 907-Bit <7:0>.

Table 14 Default register map after sensor power-on

Address (hex)		Hex value									
SPI	I <sup>2</sup> C										
0000	2E00	02	0085	2E85	1E	0415	3215	03	0541	3341	01
0001	2E01	00	0086	2E86	20	0416	3216	28	0542	3342	00
0002	2E02	00	0087	2E87	99	0417	3217	04	0543	3343	01
0003	2E03	00	0088	2E88	9B	0418	3218	00	0544	3344	00
0004	2E04	00	0089	2E89	20	0419	3219	07	0545	3345	00
0005	2E05	0A	008A	2E8A	2A	041A	321A	28	0546	3346	00
0006	2E06	00	008B	2E8B	22	041B	321B	00	0547	3347	00
0007	2E07	00	008C	2E8C	A1	041C	321C	07	0548	3348	00
0008	2E08	01	008D	2E8D	05	041D	321D	04	0549	3349	00
0009	2E09	01	008E	2E8E	2B	041E	321E	28	054A	334A	00
000A	2E0A	00	008F	2E8F	FF	041F	321F	04	054B	334B	00
000B	2E0B	00	0090	2E90	FF	0420	3220	00	054C	334C	00
000C	2E0C	01	0091	2E91	01	0421	3221	07	054D	334D	10
000D	2E0D	01	0092	2E92	02	0422	3222	68	054E	334E	32
000E	2E0E	00	0093	2E93	FF	0423	3223	03	054F	334F	54
000F	2E0F	00	0094	2E94	FF	0424	3224	00	0550	3350	86
0010	2E10	01	0095	2E95	FF	0425	3225	00	0551	3351	A9
0011	2E11	00	0096	2E96	FF	0426	3226	68	0552	3352	CB
0012	2E12	BE	0097	2E97	FF	0427	3227	03	0553	3353	ED
0013	2E13	04	0098	2E98	FF	0428	3228	00	0554	3354	7F
0014	2E14	01	0099	2E99	FF	0429	3229	00	0555	3355	10
0015	2E15	00	009A	2E9A	FF	042A	322A	11	0556	3356	32
0016	2E16	00	009B	2E9B	14	042B	322B	03	0557	3357	54
0017	2E17	00	009C	2E9C	00	042C	322C	1B	0558	3358	87
0018	2E18	00	009D	2E9D	04	042D	322D	00	0559	3359	A9
0019	2E19	BA	009E	2E9E	0C	042E	322E	07	055A	335A	CB
001A	2E1A	04	009F	2E9F	03	042F	322F	0F	055B	335B	ED

001B	2E1B	00	00A0	2EA0	00	0430	3230	0E	055C	335C	5F
001C	2E1C	00	00A1	2EA1	01	0431	3231	00	055D	335D	00
001D	2E1D	00	00A2	2EA2	00	0432	3232	13	055E	335E	00
001E	2E1E	00	00A3	2EA3	01	0433	3233	07	055F	335F	00
001F	2E1F	08	00A4	2EA4	03	0434	3234	07	0560	3360	00
0020	2E20	00	00A5	2EA5	00	0435	3235	07	0561	3361	01
0021	2E21	00	00A6	2EA6	00	0436	3236	07	0562	3362	00
0022	2E22	00	00A7	2EA7	00	0437	3237	07	0563	3363	76
0023	2E23	00	00A8	2EA8	01	0438	3238	0F	0564	3364	E8
0024	2E24	00	00A9	2EA9	28	0439	3239	07	0565	3365	03
0025	2E25	00	00AA	2EAA	0C	043A	323A	13	0566	3366	E8
0026	2E26	00	00AB	2EAB	00	043B	323B	13	0567	3367	03
0027	2E27	00	00AC	2EAC	00	043C	323C	09	0568	3368	88
0028	2E28	00	00AD	2EAD	01	043D	323D	09	0569	3369	13
0029	2E29	00	00AE	2EAE	00	043E	323E	28	056A	336A	88
002A	2E2A	00	00AF	2EAF	00	043F	323F	64	056B	336B	13
002B	2E2B	00	00B0	2EB0	00	0440	3240	00	056C	336C	00
002C	2E2C	00	00B1	2EB1	00	0441	3241	0A	0600	3400	00
002D	2E2D	00	00B2	2EB2	00	0442	3242	29	0601	3401	12
002E	2E2E	00	00B3	2EB3	00	0443	3243	15	0602	3402	00
002F	2E2F	00	00B4	2EB4	00	0444	3244	13	0603	3403	00
0030	2E30	00	00B5	2EB5	00	0445	3245	13	0604	3404	64
0031	2E31	00	00B6	2EB6	00	0446	3246	30	0605	3405	02
0032	2E32	00	00B7	2EB7	00	0447	3247	0E	0700	3500	10
0033	2E33	00	00B8	2EB8	00	0448	3248	01	0701	3501	86
0034	2E34	00	00B9	2EB9	05	0449	3249	20	0702	3502	00
0035	2E35	00	00BA	2EBA	00	044A	324A	01	0703	3503	00
0036	2E36	00	00BB	2EBB	00	044B	324B	13	0704	3504	00
0037	2E37	00	0200	3000	00	044C	324C	95	0705	3505	00
0038	2E38	00	0201	3001	00	044D	324D	08	0706	3506	00
0039	2E39	00	0202	3002	00	044E	324E	08	0707	3507	00
003A	2E3A	00	0203	3003	00	044F	324F	28	0708	3508	00
003B	2E3B	00	0204	3004	01	0450	3250	04	0709	3509	00
003C	2E3C	00	0205	3005	00	0451	3251	00	070A	350A	00
003D	2E3D	01	0206	3006	00	0452	3252	07	070B	350B	00
003E	2E3E	01	0207	3007	00	0453	3253	00	070C	350C	00
003F	2E3F	00	0208	3008	00	0454	3254	00	070D	350D	00
0040	2E40	02	0209	3009	08	0455	3255	00	070E	350E	00
0041	2E41	02	020A	300A	00	0456	3256	00	070F	350F	00
0042	2E42	44	020B	300B	01	0457	3257	00	0710	3510	00
0043	2E43	01	020C	300C	01	0458	3258	00	0711	3511	00
0044	2E44	02	020D	300D	0F	0500	3300	00	0712	3512	10

0045	2E45	02	020E	300E	00	0501	3301	00	0713	3513	00
0046	2E46	02	020F	300F	11	0502	3302	00	0714	3514	00
0047	2E47	28	0210	3010	00	0503	3303	00	0715	3515	00
0048	2E48	28	0211	3011	01	0504	3304	00	0716	3516	00
0049	2E49	06	0212	3012	00	0505	3305	00	0717	3517	00
004A	2E4A	00	0213	3013	00	0506	3306	00	0718	3518	00
004B	2E4B	07	0214	3014	6E	0507	3307	01	0719	3519	00
004C	2E4C	00	0215	3015	08	0508	3308	00	071A	351A	00
004D	2E4D	84	0216	3016	04	0509	3309	01	071B	351B	00
004E	2E4E	84	0217	3017	00	050A	330A	00	071C	351C	00
004F	2E4F	63	0218	3018	08	050B	330B	01	071D	351D	00
0050	2E50	02	0219	3019	07	050C	330C	00	071E	351E	00
0051	2E51	5C	021A	301A	10	050D	330D	01	071F	351F	00
0052	2E52	98	021B	301B	07	050E	330E	00	0720	3520	00
0053	2E53	0C	021C	301C	27	050F	330F	01	0721	3521	00
0054	2E54	48	021D	301D	00	0510	3310	00	0722	3522	10
0055	2E55	52	021E	301E	0B	0511	3311	01	0723	3523	52
0056	2E56	FF	021F	301F	09	0512	3312	00	0724	3524	04
0057	2E57	FF	0220	3020	05	0513	3313	2C	0725	3525	00
0058	2E58	FF	0221	3021	06	0514	3314	01	0726	3526	00
0059	2E59	53	0222	3022	96	0515	3315	01	0727	3527	00
005A	2E5A	99	0223	3023	C8	0516	3316	00	0728	3528	00
005B	2E5B	01	0224	3024	14	0517	3317	E2	0729	3529	00
005C	2E5C	2B	0225	3025	00	0518	3318	04	072A	352A	00
005D	2E5D	FF	0226	3026	00	0519	3319	E2	0900	3700	20
005E	2E5E	FF	0227	3027	00	051A	331A	04	0901	3701	08
005F	2E5F	01	0228	3028	00	051B	331B	E2	0902	3702	6E
0060	2E60	9E	0229	3029	00	051C	331C	04	0903	3703	00
0061	2E61	50	022A	302A	00	051D	331D	E2	0904	3704	00
0062	2E62	9F	022B	302B	00	051E	331E	04	0905	3705	7A
0063	2E63	51	022C	302C	00	051F	331F	E2	0906	3706	00
0064	2E64	9E	022D	302D	00	0520	3320	04	0907	3707	00
0065	2E65	05	022E	302E	00	0521	3321	E2	0908	3708	00
0066	2E66	41	022F	302F	00	0522	3322	04	0909	3709	00
0067	2E67	37	0230	3030	00	0523	3323	EE	090A	370A	32
0068	2E68	A1	0231	3031	00	0524	3324	02	090B	370B	00
0069	2E69	05	0232	3032	06	0525	3325	EE	090C	370C	02
006A	2E6A	50	0233	3033	1F	0526	3326	02	090D	370D	24
006B	2E6B	64	0234	3034	22	0527	3327	01	090E	370E	3F
006C	2E6C	9D	0235	3035	14	0528	3328	00	090F	370F	00
006D	2E6D	03	0236	3036	08	0529	3329	01	0910	3710	00
006E	2E6E	20	0237	3037	00	052A	332A	00	0911	3711	00

006F	2E6F	29	0238	3038	10	052B	332B	01	0912	3712	00
0070	2E70	9B	0400	3200	20	052C	332C	00	0913	3713	3A
0071	2E71	02	0401	3201	07	052D	332D	01	0A00	3800	20
0072	2E72	22	0402	3202	04	052E	332E	00	0A01	3801	08
0073	2E73	24	0403	3203	03	052F	332F	77	0A02	3802	6E
0074	2E74	A1	0404	3204	14	0530	3330	01	0A03	3803	00
0075	2E75	03	0405	3205	03	0531	3331	01	0A04	3804	00
0076	2E76	23	0406	3206	03	0532	3332	00	0A05	3805	7A
0077	2E77	25	0407	3207	03	0533	3333	E2	0A06	3806	00
0078	2E78	A2	0408	3208	14	0534	3334	04	0A07	3807	00
0079	2E79	04	0409	3209	04	0535	3335	E2	0A08	3808	00
007A	2E7A	20	040A	320A	07	0536	3336	04	0A09	3809	00
007B	2E7B	2A	040B	320B	16	0537	3337	E2	0A0A	380A	32
007C	2E7C	9B	040C	320C	04	0538	3338	04	0A0B	380B	00
007D	2E7D	01	040D	320D	16	0539	3339	E2	0A0C	380C	02
007E	2E7E	02	040E	320E	0F	053A	333A	04	0A0D	380D	24
007F	2E7F	23	040F	320F	07	053B	333B	E2	0A0E	380E	3F
0080	2E80	24	0410	3210	11	053C	333C	04	0A0F	380F	00
0081	2E81	04	0411	3211	07	053D	333D	E2	0A10	3810	00
0082	2E82	20	0412	3212	00	053E	333E	04	0A11	3811	00
0083	2E83	2A	0413	3213	0E	053F	333F	01	0A12	3812	00
0084	2E84	9B	0414	3214	1B	0540	3340	00	0A13	3813	3A

Table 15 Recommended register map with x1 PGA gain for 12bit @1.2GHz sub-LVDS

Address (hex)		Hex value									
SPI	I <sup>2</sup> C										
0000	2E00	00	0085	2E85	7E	0415	3215	03	0541	3341	01
0001	2E01	00	0086	2E86	80	0416	3216	21	0542	3342	00
0002	2E02	00	0087	2E87	FA	0417	3217	04	0543	3343	01
0003	2E03	02	0088	2E88	FC	0418	3218	07	0544	3344	00
0004	2E04	00	0089	2E89	80	0419	3219	00	0545	3345	00
0005	2E05	08	008A	2E8A	8A	041A	321A	29	0546	3346	00
0006	2E06	00	008B	2E8B	84	041B	321B	07	0547	3347	00
0007	2E07	01	008C	2E8C	FF	041C	321C	00	0548	3348	00
0008	2E08	00	008D	2E8D	FF	041D	321D	04	0549	3349	00
0009	2E09	00	008E	2E8E	FF	041E	321E	29	054A	334A	00
000A	2E0A	00	008F	2E8F	FF	041F	321F	04	054B	334B	00
000B	2E0B	00	0090	2E90	FF	0420	3220	07	054C	334C	00
000C	2E0C	00	0091	2E91	01	0421	3221	00	054D	334D	10
000D	2E0D	00	0092	2E92	02	0422	3222	0F	054E	334E	32
000E	2E0E	00	0093	2E93	FF	0423	3223	03	054F	334F	54

**12MP Global Shutter CMOS Image Sensor****GMAX3412**

000F	2E0F	00	0094	2E94	FF	0424	3224	00	0550	3350	86
0010	2E10	01	0095	2E95	FF	0425	3225	00	0551	3351	A9
0011	2E11	00	0096	2E96	FF	0426	3226	29	0552	3352	CB
0012	2E12	0C	0097	2E97	FF	0427	3227	03	0553	3353	ED
0013	2E13	0C	0098	2E98	FF	0428	3228	00	0554	3354	7F
0014	2E14	01	0099	2E99	FF	0429	3229	00	0555	3355	10
0015	2E15	00	009A	2E9A	FF	042A	322A	11	0556	3356	32
0016	2E16	00	009B	2E9B	24	042B	322B	03	0557	3357	54
0017	2E17	00	009C	2E9C	1C	042C	322C	1B	0558	3358	87
0018	2E18	00	009D	2E9D	1E	042D	322D	00	0559	3359	A9
0019	2E19	0C	009E	2E9E	0C	042E	322E	07	055A	335A	CB
001A	2E1A	0C	009F	2E9F	03	042F	322F	0F	055B	335B	ED
001B	2E1B	00	00A0	2EA0	00	0430	3230	0E	055C	335C	5F
001C	2E1C	00	00A1	2EA1	01	0431	3231	61	055D	335D	00
001D	2E1D	08	00A2	2EA2	00	0432	3232	53	055E	335E	00
001E	2E1E	00	00A3	2EA3	01	0433	3233	53	055F	335F	00
001F	2E1F	00	00A4	2EA4	03	0434	3234	46	0560	3360	00
0020	2E20	0C	00A5	2EA5	01	0435	3235	49	0561	3361	01
0021	2E21	00	00A6	2EA6	01	0436	3236	49	0562	3362	00
0022	2E22	00	00A7	2EA7	00	0437	3237	47	0563	3363	76
0023	2E23	00	00A8	2EA8	01	0438	3238	4F	0564	3364	E8
0024	2E24	00	00A9	2EA9	1E	0439	3239	47	0565	3365	03
0025	2E25	00	00AA	2EAA	0C	043A	323A	53	0566	3366	E8
0026	2E26	00	00AB	2EAB	00	043B	323B	53	0567	3367	03
0027	2E27	00	00AC	2EAC	00	043C	323C	49	0568	3368	88
0028	2E28	00	00AD	2EAD	01	043D	323D	49	0569	3369	13
0029	2E29	00	00AE	2EAE	12	043E	323E	68	056A	336A	88
002A	2E2A	00	00AF	2EAF	00	043F	323F	64	056B	336B	13
002B	2E2B	00	00B0	2EB0	00	0440	3240	00	056C	336C	00
002C	2E2C	00	00B1	2EB1	00	0441	3241	1A	0600	3400	00
002D	2E2D	00	00B2	2EB2	00	0442	3242	1C	0601	3401	12
002E	2E2E	00	00B3	2EB3	00	0443	3243	04	0602	3402	00
002F	2E2F	00	00B4	2EB4	00	0444	3244	13	0603	3403	01
0030	2E30	00	00B5	2EB5	00	0445	3245	13	0604	3404	64
0031	2E31	00	00B6	2EB6	00	0446	3246	32	0605	3405	02
0032	2E32	00	00B7	2EB7	00	0447	3247	0A	0700	3500	10
0033	2E33	00	00B8	2EB8	00	0448	3248	7D	0701	3501	86
0034	2E34	00	00B9	2EB9	05	0449	3249	20	0702	3502	00
0035	2E35	00	00BA	2EBA	00	044A	324A	0F	0703	3503	00
0036	2E36	00	00BB	2EBB	00	044B	324B	53	0704	3504	00
0037	2E37	00	0200	3000	00	044C	324C	84	0705	3505	00
0038	2E38	00	0201	3001	02	044D	324D	1C	0706	3506	00

0039	2E39	00	0202	3002	02	044E	324E	28	0707	3507	00
003A	2E3A	00	0203	3003	00	044F	324F	07	0708	3508	00
003B	2E3B	00	0204	3004	03	0450	3250	04	0709	3509	00
003C	2E3C	00	0205	3005	00	0451	3251	00	070A	350A	00
003D	2E3D	05	0206	3006	00	0452	3252	0F	070B	350B	00
003E	2E3E	06	0207	3007	00	0453	3253	00	070C	350C	00
003F	2E3F	00	0208	3008	00	0454	3254	00	070D	350D	00
0040	2E40	02	0209	3009	08	0455	3255	00	070E	350E	00
0041	2E41	03	020A	300A	00	0456	3256	00	070F	350F	00
0042	2E42	FE	020B	300B	01	0457	3257	00	0710	3510	00
0043	2E43	01	020C	300C	01	0458	3258	00	0711	3511	00
0044	2E44	02	020D	300D	0F	0500	3300	00	0712	3512	10
0045	2E45	02	020E	300E	00	0501	3301	00	0713	3513	00
0046	2E46	02	020F	300F	11	0502	3302	00	0714	3514	00
0047	2E47	1E	0210	3010	01	0503	3303	00	0715	3515	00
0048	2E48	1E	0211	3011	01	0504	3304	00	0716	3516	00
0049	2E49	06	0212	3012	00	0505	3305	00	0717	3517	00
004A	2E4A	00	0213	3013	00	0506	3306	00	0718	3518	00
004B	2E4B	07	0214	3014	65	0507	3307	01	0719	3519	00
004C	2E4C	00	0215	3015	01	0508	3308	00	071A	351A	00
004D	2E4D	A4	0216	3016	04	0509	3309	01	071B	351B	00
004E	2E4E	84	0217	3017	00	050A	330A	00	071C	351C	00
004F	2E4F	62	0218	3018	08	050B	330B	01	071D	351D	00
0050	2E50	02	0219	3019	07	050C	330C	00	071E	351E	00
0051	2E51	5F	021A	301A	10	050D	330D	01	071F	351F	00
0052	2E52	FA	021B	301B	07	050E	330E	00	0720	3520	00
0053	2E53	0A	021C	301C	27	050F	330F	01	0721	3521	00
0054	2E54	46	021D	301D	00	0510	3310	00	0722	3522	10
0055	2E55	FF	021E	301E	0B	0511	3311	01	0723	3523	52
0056	2E56	FF	021F	301F	09	0512	3312	00	0724	3524	04
0057	2E57	FF	0220	3020	05	0513	3313	2C	0725	3525	00
0058	2E58	FF	0221	3021	06	0514	3314	01	0726	3526	00
0059	2E59	80	0222	3022	01	0515	3315	01	0727	3527	00
005A	2E5A	9E	0223	3023	F8	0516	3316	00	0728	3528	00
005B	2E5B	19	0224	3024	14	0517	3317	E2	0729	3529	00
005C	2E5C	FF	0225	3025	00	0518	3318	04	072A	352A	00
005D	2E5D	FF	0226	3026	00	0519	3319	E2	0900	3700	E0
005E	2E5E	FF	0227	3027	00	051A	331A	04	0901	3701	08
005F	2E5F	01	0228	3028	00	051B	331B	E2	0902	3702	6E
0060	2E60	FD	0229	3029	00	051C	331C	04	0903	3703	0D
0061	2E61	01	022A	302A	04	051D	331D	E2	0904	3704	00
0062	2E62	FE	022B	302B	04	051E	331E	04	0905	3705	00

0063	2E63	FF	022C	302C	04	051F	331F	E2	0906	3706	00
0064	2E64	FF	022D	302D	04	0520	3320	04	0907	3707	64
0065	2E65	05	022E	302E	00	0521	3321	E2	0908	3708	00
0066	2E66	3E	022F	302F	00	0522	3322	04	0909	3709	F9
0067	2E67	FF	0230	3030	00	0523	3323	EE	090A	370A	32
0068	2E68	FF	0231	3031	00	0524	3324	02	090B	370B	00
0069	2E69	05	0232	3032	00	0525	3325	EE	090C	370C	02
006A	2E6A	7E	0233	3033	1F	0526	3326	02	090D	370D	24
006B	2E6B	BE	0234	3034	1F	0527	3327	01	090E	370E	3F
006C	2E6C	FA	0235	3035	08	0528	3328	00	090F	370F	0F
006D	2E6D	63	0236	3036	08	0529	3329	01	0910	3710	64
006E	2E6E	80	0237	3037	00	052A	332A	00	0911	3711	00
006F	2E6F	89	0238	3038	10	052B	332B	01	0912	3712	00
0070	2E70	FC	0400	3200	20	052C	332C	00	0913	3713	3A
0071	2E71	2A	0401	3201	00	052D	332D	01	0A00	3800	E0
0072	2E72	FF	0402	3202	04	052E	332E	00	0A01	3801	08
0073	2E73	FF	0403	3203	03	052F	332F	77	0A02	3802	6E
0074	2E74	FF	0404	3204	20	0530	3330	01	0A03	3803	0D
0075	2E75	2B	0405	3205	03	0531	3331	01	0A04	3804	00
0076	2E76	FF	0406	3206	03	0532	3332	00	0A05	3805	00
0077	2E77	FF	0407	3207	03	0533	3333	E2	0A06	3806	00
0078	2E78	FF	0408	3208	16	0534	3334	04	0A07	3807	64
0079	2E79	64	0409	3209	04	0535	3335	E2	0A08	3808	00
007A	2E7A	80	040A	320A	00	0536	3336	04	0A09	3809	F9
007B	2E7B	8A	040B	320B	16	0537	3337	E2	0A0A	380A	32
007C	2E7C	FC	040C	320C	04	0538	3338	04	0A0B	380B	00
007D	2E7D	61	040D	320D	16	0539	3339	E2	0A0C	380C	02
007E	2E7E	62	040E	320E	0F	053A	333A	04	0A0D	380D	24
007F	2E7F	87	040F	320F	00	053B	333B	E2	0A0E	380E	3F
0080	2E80	88	0410	3210	11	053C	333C	04	0A0F	380F	0F
0081	2E81	64	0411	3211	07	053D	333D	E2	0A10	3810	64
0082	2E82	80	0412	3212	00	053E	333E	04	0A11	3811	00
0083	2E83	8A	0413	3213	0E	053F	333F	01	0A12	3812	00
0084	2E84	FC	0414	3214	1B	0540	3340	00	0A13	3813	3A

Table 16 Recommended register map with x1 PGA gain for 12bit @1.2GHz MIPI

Address (hex)		Hex value	Address (hex)		Hex value	Address (hex)		Hex value	Address (hex)		Hex value
			SPI	I <sup>2</sup> C		SPI	I <sup>2</sup> C		SPI	I <sup>2</sup> C	
0000	2E00	00	0085	2E85	7E	0415	3215	03	0541	3341	01
0001	2E01	00	0086	2E86	80	0416	3216	21	0542	3342	00
0002	2E02	00	0087	2E87	FA	0417	3217	04	0543	3343	01

0003	2E03	02	0088	2E88	FC	0418	3218	07	0544	3344	00
0004	2E04	00	0089	2E89	80	0419	3219	00	0545	3345	00
0005	2E05	08	008A	2E8A	8A	041A	321A	29	0546	3346	00
0006	2E06	00	008B	2E8B	84	041B	321B	07	0547	3347	00
0007	2E07	01	008C	2E8C	FF	041C	321C	00	0548	3348	00
0008	2E08	00	008D	2E8D	FF	041D	321D	04	0549	3349	00
0009	2E09	00	008E	2E8E	FF	041E	321E	29	054A	334A	00
000A	2E0A	00	008F	2E8F	FF	041F	321F	04	054B	334B	00
000B	2E0B	00	0090	2E90	FF	0420	3220	07	054C	334C	00
000C	2E0C	00	0091	2E91	01	0421	3221	00	054D	334D	10
000D	2E0D	00	0092	2E92	02	0422	3222	0F	054E	334E	32
000E	2E0E	00	0093	2E93	FF	0423	3223	03	054F	334F	54
000F	2E0F	00	0094	2E94	FF	0424	3224	00	0550	3350	86
0010	2E10	01	0095	2E95	FF	0425	3225	00	0551	3351	A9
0011	2E11	00	0096	2E96	FF	0426	3226	29	0552	3352	CB
0012	2E12	0C	0097	2E97	FF	0427	3227	03	0553	3353	ED
0013	2E13	0C	0098	2E98	FF	0428	3228	00	0554	3354	7F
0014	2E14	01	0099	2E99	FF	0429	3229	00	0555	3355	10
0015	2E15	00	009A	2E9A	FF	042A	322A	11	0556	3356	32
0016	2E16	00	009B	2E9B	24	042B	322B	03	0557	3357	54
0017	2E17	00	009C	2E9C	1C	042C	322C	1B	0558	3358	87
0018	2E18	00	009D	2E9D	1E	042D	322D	00	0559	3359	A9
0019	2E19	0C	009E	2E9E	0C	042E	322E	07	055A	335A	CB
001A	2E1A	0C	009F	2E9F	03	042F	322F	0F	055B	335B	ED
001B	2E1B	00	00A0	2EA0	00	0430	3230	0E	055C	335C	5F
001C	2E1C	00	00A1	2EA1	01	0431	3231	61	055D	335D	00
001D	2E1D	08	00A2	2EA2	00	0432	3232	53	055E	335E	00
001E	2E1E	00	00A3	2EA3	01	0433	3233	53	055F	335F	00
001F	2E1F	00	00A4	2EA4	03	0434	3234	46	0560	3360	00
0020	2E20	0C	00A5	2EA5	01	0435	3235	49	0561	3361	01
0021	2E21	00	00A6	2EA6	01	0436	3236	49	0562	3362	00
0022	2E22	00	00A7	2EA7	00	0437	3237	47	0563	3363	76
0023	2E23	00	00A8	2EA8	01	0438	3238	4F	0564	3364	E8
0024	2E24	00	00A9	2EA9	1E	0439	3239	47	0565	3365	03
0025	2E25	00	00AA	2EAA	0C	043A	323A	53	0566	3366	E8
0026	2E26	00	00AB	2EAB	00	043B	323B	53	0567	3367	03
0027	2E27	00	00AC	2EAC	00	043C	323C	49	0568	3368	88
0028	2E28	00	00AD	2EAD	01	043D	323D	49	0569	3369	13
0029	2E29	00	00AE	2EAE	12	043E	323E	68	056A	336A	88
002A	2E2A	00	00AF	2EAF	00	043F	323F	64	056B	336B	13
002B	2E2B	00	00B0	2EB0	00	0440	3240	00	056C	336C	00
002C	2E2C	00	00B1	2EB1	00	0441	3241	1A	0600	3400	00

002D	2E2D	00	00B2	2EB2	00	0442	3242	1C	0601	3401	12
002E	2E2E	00	00B3	2EB3	00	0443	3243	04	0602	3402	00
002F	2E2F	00	00B4	2EB4	00	0444	3244	13	0603	3403	01
0030	2E30	00	00B5	2EB5	00	0445	3245	13	0604	3404	64
0031	2E31	00	00B6	2EB6	00	0446	3246	32	0605	3405	02
0032	2E32	00	00B7	2EB7	00	0447	3247	08	0700	3500	10
0033	2E33	00	00B8	2EB8	00	0448	3248	7D	0701	3501	86
0034	2E34	00	00B9	2EB9	05	0449	3249	20	0702	3502	00
0035	2E35	00	00BA	2EBA	00	044A	324A	0F	0703	3503	00
0036	2E36	00	00BB	2EBB	00	044B	324B	53	0704	3504	00
0037	2E37	00	0200	3000	01	044C	324C	84	0705	3505	00
0038	2E38	00	0201	3001	02	044D	324D	1C	0706	3506	00
0039	2E39	00	0202	3002	02	044E	324E	28	0707	3507	00
003A	2E3A	00	0203	3003	00	044F	324F	07	0708	3508	00
003B	2E3B	00	0204	3004	03	0450	3250	04	0709	3509	00
003C	2E3C	00	0205	3005	00	0451	3251	00	070A	350A	00
003D	2E3D	05	0206	3006	00	0452	3252	0F	070B	350B	00
003E	2E3E	06	0207	3007	00	0453	3253	00	070C	350C	00
003F	2E3F	00	0208	3008	00	0454	3254	00	070D	350D	00
0040	2E40	02	0209	3009	08	0455	3255	00	070E	350E	00
0041	2E41	03	020A	300A	00	0456	3256	00	070F	350F	00
0042	2E42	2A	020B	300B	01	0457	3257	00	0710	3510	00
0043	2E43	04	020C	300C	01	0458	3258	00	0711	3511	00
0044	2E44	04	020D	300D	0F	0500	3300	00	0712	3512	10
0045	2E45	04	020E	300E	00	0501	3301	00	0713	3513	00
0046	2E46	04	020F	300F	11	0502	3302	00	0714	3514	00
0047	2E47	1E	0210	3010	01	0503	3303	00	0715	3515	00
0048	2E48	1E	0211	3011	01	0504	3304	00	0716	3516	00
0049	2E49	06	0212	3012	00	0505	3305	00	0717	3517	00
004A	2E4A	00	0213	3013	00	0506	3306	00	0718	3518	00
004B	2E4B	07	0214	3014	65	0507	3307	01	0719	3519	00
004C	2E4C	00	0215	3015	01	0508	3308	00	071A	351A	00
004D	2E4D	A4	0216	3016	04	0509	3309	01	071B	351B	00
004E	2E4E	84	0217	3017	00	050A	330A	00	071C	351C	00
004F	2E4F	62	0218	3018	08	050B	330B	01	071D	351D	00
0050	2E50	02	0219	3019	07	050C	330C	00	071E	351E	00
0051	2E51	50	021A	301A	10	050D	330D	01	071F	351F	00
0052	2E52	9E	021B	301B	07	050E	330E	00	0720	3520	00
0053	2E53	05	021C	301C	27	050F	330F	01	0721	3521	00
0054	2E54	37	021D	301D	00	0510	3310	00	0722	3522	10
0055	2E55	FF	021E	301E	0B	0511	3311	01	0723	3523	52
0056	2E56	FF	021F	301F	09	0512	3312	00	0724	3524	04

0057	2E57	FF	0220	3020	05	0513	3313	2C	0725	3525	00
0058	2E58	FF	0221	3021	06	0514	3314	01	0726	3526	00
0059	2E59	85	0222	3022	96	0515	3315	01	0727	3527	00
005A	2E5A	94	0223	3023	F8	0516	3316	00	0728	3528	00
005B	2E5B	19	0224	3024	14	0517	3317	E2	0729	3529	00
005C	2E5C	FF	0225	3025	00	0518	3318	04	072A	352A	00
005D	2E5D	FF	0226	3026	00	0519	3319	E2	0900	3700	E0
005E	2E5E	FF	0227	3027	00	051A	331A	04	0901	3701	08
005F	2E5F	01	0228	3028	00	051B	331B	E2	0902	3702	6E
0060	2E60	FD	0229	3029	00	051C	331C	04	0903	3703	0D
0061	2E61	01	022A	302A	04	051D	331D	E2	0904	3704	00
0062	2E62	FE	022B	302B	04	051E	331E	04	0905	3705	00
0063	2E63	FF	022C	302C	04	051F	331F	E2	0906	3706	00
0064	2E64	FF	022D	302D	04	0520	3320	04	0907	3707	64
0065	2E65	05	022E	302E	00	0521	3321	E2	0908	3708	00
0066	2E66	3E	022F	302F	00	0522	3322	04	0909	3709	F9
0067	2E67	2A	0230	3030	00	0523	3323	EE	090A	370A	32
0068	2E68	FE	0231	3031	00	0524	3324	02	090B	370B	00
0069	2E69	05	0232	3032	00	0525	3325	EE	090C	370C	02
006A	2E6A	7E	0233	3033	1F	0526	3326	02	090D	370D	24
006B	2E6B	BE	0234	3034	1F	0527	3327	01	090E	370E	3F
006C	2E6C	FA	0235	3035	08	0528	3328	00	090F	370F	0F
006D	2E6D	71	0236	3036	08	0529	3329	01	0910	3710	64
006E	2E6E	80	0237	3037	00	052A	332A	00	0911	3711	00
006F	2E6F	C2	0238	3038	10	052B	332B	01	0912	3712	00
0070	2E70	FC	0400	3200	20	052C	332C	00	0913	3713	3A
0071	2E71	2A	0401	3201	00	052D	332D	01	0A00	3800	E0
0072	2E72	FF	0402	3202	04	052E	332E	00	0A01	3801	08
0073	2E73	FF	0403	3203	03	052F	332F	77	0A02	3802	6E
0074	2E74	FF	0404	3204	20	0530	3330	01	0A03	3803	0D
0075	2E75	2B	0405	3205	03	0531	3331	01	0A04	3804	00
0076	2E76	FF	0406	3206	03	0532	3332	00	0A05	3805	00
0077	2E77	FF	0407	3207	03	0533	3333	E2	0A06	3806	00
0078	2E78	FF	0408	3208	16	0534	3334	04	0A07	3807	64
0079	2E79	72	0409	3209	04	0535	3335	E2	0A08	3808	00
007A	2E7A	80	040A	320A	00	0536	3336	04	0A09	3809	F9
007B	2E7B	C3	040B	320B	16	0537	3337	E2	0A0A	380A	32
007C	2E7C	FC	040C	320C	04	0538	3338	04	0A0B	380B	00
007D	2E7D	6F	040D	320D	16	0539	3339	E2	0A0C	380C	02
007E	2E7E	70	040E	320E	0F	053A	333A	04	0A0D	380D	24
007F	2E7F	C0	040F	320F	00	053B	333B	E2	0A0E	380E	3F
0080	2E80	C1	0410	3210	11	053C	333C	04	0A0F	380F	0F

0081	2E81	72	0411	3211	07	053D	333D	E2	0A10	3810	64
0082	2E82	80	0412	3212	00	053E	333E	04	0A11	3811	00
0083	2E83	C3	0413	3213	0E	053F	333F	01	0A12	3812	00
0084	2E84	FC	0414	3214	1B	0540	3340	00	0A13	3813	3A

Table 17 Recommended register map with x1 PGA gain for 10bit @1.2GHz sub-LVDS

Address (hex)		Hex value									
SPI	I <sup>2</sup> C										
0000	2E00	00	0085	2E85	14	0415	3215	03	0541	3341	01
0001	2E01	00	0086	2E86	15	0416	3216	21	0542	3342	00
0002	2E02	00	0087	2E87	5D	0417	3217	04	0543	3343	01
0003	2E03	02	0088	2E88	5F	0418	3218	07	0544	3344	00
0004	2E04	00	0089	2E89	16	0419	3219	00	0545	3345	00
0005	2E05	08	008A	2E8A	1C	041A	321A	29	0546	3346	00
0006	2E06	00	008B	2E8B	19	041B	321B	07	0547	3347	00
0007	2E07	01	008C	2E8C	FF	041C	321C	00	0548	3348	00
0008	2E08	00	008D	2E8D	FF	041D	321D	04	0549	3349	00
0009	2E09	00	008E	2E8E	FF	041E	321E	29	054A	334A	00
000A	2E0A	00	008F	2E8F	FF	041F	321F	04	054B	334B	00
000B	2E0B	00	0090	2E90	FF	0420	3220	07	054C	334C	00
000C	2E0C	00	0091	2E91	01	0421	3221	00	054D	334D	10
000D	2E0D	00	0092	2E92	02	0422	3222	0F	054E	334E	32
000E	2E0E	00	0093	2E93	FF	0423	3223	03	054F	334F	54
000F	2E0F	00	0094	2E94	FF	0424	3224	00	0550	3350	86
0010	2E10	01	0095	2E95	FF	0425	3225	00	0551	3351	A9
0011	2E11	00	0096	2E96	FF	0426	3226	29	0552	3352	CB
0012	2E12	0C	0097	2E97	FF	0427	3227	03	0553	3353	ED
0013	2E13	0C	0098	2E98	FF	0428	3228	00	0554	3354	7F
0014	2E14	01	0099	2E99	FF	0429	3229	00	0555	3355	10
0015	2E15	00	009A	2E9A	FF	042A	322A	11	0556	3356	32
0016	2E16	00	009B	2E9B	24	042B	322B	03	0557	3357	54
0017	2E17	00	009C	2E9C	1C	042C	322C	1B	0558	3358	87
0018	2E18	00	009D	2E9D	1E	042D	322D	00	0559	3359	A9
0019	2E19	0C	009E	2E9E	0C	042E	322E	07	055A	335A	CB
001A	2E1A	0C	009F	2E9F	03	042F	322F	0F	055B	335B	ED
001B	2E1B	00	00A0	2EA0	00	0430	3230	0E	055C	335C	5F
001C	2E1C	00	00A1	2EA1	01	0431	3231	6E	055D	335D	00
001D	2E1D	08	00A2	2EA2	00	0432	3232	53	055E	335E	00
001E	2E1E	00	00A3	2EA3	01	0433	3233	5B	055F	335F	00
001F	2E1F	00	00A4	2EA4	03	0434	3234	4F	0560	3360	00
0020	2E20	0C	00A5	2EA5	01	0435	3235	49	0561	3361	01

0021	2E21	00	00A6	2EA6	01	0436	3236	49	0562	3362	00
0022	2E22	00	00A7	2EA7	00	0437	3237	47	0563	3363	76
0023	2E23	00	00A8	2EA8	01	0438	3238	4F	0564	3364	E8
0024	2E24	00	00A9	2EA9	1E	0439	3239	47	0565	3365	03
0025	2E25	00	00AA	2EAA	0C	043A	323A	53	0566	3366	E8
0026	2E26	00	00AB	2EAB	00	043B	323B	53	0567	3367	03
0027	2E27	00	00AC	2EAC	00	043C	323C	49	0568	3368	88
0028	2E28	00	00AD	2EAD	01	043D	323D	49	0569	3369	13
0029	2E29	00	00AE	2EAE	12	043E	323E	68	056A	336A	88
002A	2E2A	00	00AF	2EAF	09	043F	323F	64	056B	336B	13
002B	2E2B	00	00B0	2EB0	01	0440	3240	00	056C	336C	00
002C	2E2C	00	00B1	2EB1	00	0441	3241	1A	0600	3400	00
002D	2E2D	00	00B2	2EB2	00	0442	3242	24	0601	3401	12
002E	2E2E	00	00B3	2EB3	00	0443	3243	04	0602	3402	00
002F	2E2F	00	00B4	2EB4	00	0444	3244	13	0603	3403	01
0030	2E30	00	00B5	2EB5	00	0445	3245	13	0604	3404	64
0031	2E31	00	00B6	2EB6	00	0446	3246	32	0605	3405	02
0032	2E32	00	00B7	2EB7	00	0447	3247	0A	0700	3500	10
0033	2E33	00	00B8	2EB8	00	0448	3248	7D	0701	3501	86
0034	2E34	00	00B9	2EB9	00	0449	3249	21	0702	3502	00
0035	2E35	00	00BA	2EBA	00	044A	324A	0E	0703	3503	00
0036	2E36	00	00BB	2EBB	00	044B	324B	53	0704	3504	00
0037	2E37	00	0200	3000	00	044C	324C	84	0705	3505	00
0038	2E38	00	0201	3001	00	044D	324D	1C	0706	3506	00
0039	2E39	00	0202	3002	02	044E	324E	28	0707	3507	00
003A	2E3A	00	0203	3003	00	044F	324F	07	0708	3508	00
003B	2E3B	00	0204	3004	03	0450	3250	04	0709	3509	00
003C	2E3C	00	0205	3005	00	0451	3251	00	070A	350A	00
003D	2E3D	0F	0206	3006	00	0452	3252	0F	070B	350B	00
003E	2E3E	06	0207	3007	00	0453	3253	00	070C	350C	00
003F	2E3F	00	0208	3008	00	0454	3254	00	070D	350D	00
0040	2E40	02	0209	3009	08	0455	3255	00	070E	350E	00
0041	2E41	03	020A	300A	00	0456	3256	00	070F	350F	00
0042	2E42	FA	020B	300B	01	0457	3257	00	0710	3510	00
0043	2E43	00	020C	300C	01	0458	3258	00	0711	3511	00
0044	2E44	02	020D	300D	0F	0500	3300	00	0712	3512	10
0045	2E45	02	020E	300E	00	0501	3301	00	0713	3513	00
0046	2E46	02	020F	300F	11	0502	3302	00	0714	3514	00
0047	2E47	28	0210	3010	01	0503	3303	00	0715	3515	00
0048	2E48	04	0211	3011	01	0504	3304	00	0716	3516	00
0049	2E49	06	0212	3012	00	0505	3305	00	0717	3517	00
004A	2E4A	00	0213	3013	00	0506	3306	00	0718	3518	00

004B	2E4B	07	0214	3014	65	0507	3307	01	0719	3519	00
004C	2E4C	00	0215	3015	01	0508	3308	00	071A	351A	00
004D	2E4D	A4	0216	3016	04	0509	3309	01	071B	351B	00
004E	2E4E	84	0217	3017	00	050A	330A	00	071C	351C	00
004F	2E4F	62	0218	3018	08	050B	330B	01	071D	351D	00
0050	2E50	02	0219	3019	07	050C	330C	00	071E	351E	00
0051	2E51	46	021A	301A	10	050D	330D	01	071F	351F	00
0052	2E52	78	021B	301B	07	050E	330E	00	0720	3520	00
0053	2E53	05	021C	301C	27	050F	330F	01	0721	3521	00
0054	2E54	41	021D	301D	00	0510	3310	00	0722	3522	10
0055	2E55	FF	021E	301E	0B	0511	3311	01	0723	3523	52
0056	2E56	FF	021F	301F	09	0512	3312	00	0724	3524	04
0057	2E57	FF	0220	3020	05	0513	3313	2C	0725	3525	00
0058	2E58	FF	0221	3021	06	0514	3314	01	0726	3526	00
0059	2E59	39	0222	3022	01	0515	3315	01	0727	3527	00
005A	2E5A	57	0223	3023	F8	0516	3316	00	0728	3528	00
005B	2E5B	12	0224	3024	14	0517	3317	E2	0729	3529	00
005C	2E5C	FF	0225	3025	00	0518	3318	04	072A	352A	00
005D	2E5D	FF	0226	3026	00	0519	3319	E2	0900	3700	F0
005E	2E5E	FF	0227	3027	00	051A	331A	04	0901	3701	08
005F	2E5F	01	0228	3028	00	051B	331B	E2	0902	3702	6E
0060	2E60	7C	0229	3029	00	051C	331C	04	0903	3703	10
0061	2E61	01	022A	302A	04	051D	331D	E2	0904	3704	00
0062	2E62	7C	022B	302B	04	051E	331E	04	0905	3705	00
0063	2E63	FF	022C	302C	04	051F	331F	E2	0906	3706	00
0064	2E64	FF	022D	302D	04	0520	3320	04	0907	3707	20
0065	2E65	01	022E	302E	00	0521	3321	E2	0908	3708	00
0066	2E66	1E	022F	302F	00	0522	3322	04	0909	3709	20
0067	2E67	0A	0230	3030	00	0523	3323	EE	090A	370A	32
0068	2E68	7C	0231	3031	00	0524	3324	02	090B	370B	00
0069	2E69	01	0232	3032	00	0525	3325	EE	090C	370C	02
006A	2E6A	38	0233	3033	1F	0526	3326	02	090D	370D	24
006B	2E6B	3A	0234	3034	1F	0527	3327	01	090E	370E	3F
006C	2E6C	7A	0235	3035	08	0528	3328	00	090F	370F	08
006D	2E6D	03	0236	3036	08	0529	3329	01	0910	3710	37
006E	2E6E	16	0237	3037	00	052A	332A	00	0911	3711	00
006F	2E6F	23	0238	3038	10	052B	332B	01	0912	3712	00
0070	2E70	5F	0400	3200	20	052C	332C	00	0913	3713	3A
0071	2E71	01	0401	3201	00	052D	332D	01	0A00	3800	F0
0072	2E72	64	0402	3202	04	052E	332E	00	0A01	3801	08
0073	2E73	FF	0403	3203	03	052F	332F	77	0A02	3802	6E
0074	2E74	FF	0404	3204	20	0530	3330	01	0A03	3803	10

**12MP Global Shutter CMOS Image Sensor****GMAX3412**

0075	2E75	02	0405	3205	03	0531	3331	01	0A04	3804	00
0076	2E76	64	0406	3206	03	0532	3332	00	0A05	3805	00
0077	2E77	FF	0407	3207	03	0533	3333	E2	0A06	3806	00
0078	2E78	FF	0408	3208	16	0534	3334	04	0A07	3807	20
0079	2E79	04	0409	3209	04	0535	3335	E2	0A08	3808	00
007A	2E7A	15	040A	320A	00	0536	3336	04	0A09	3809	20
007B	2E7B	24	040B	320B	16	0537	3337	E2	0A0A	380A	32
007C	2E7C	5F	040C	320C	04	0538	3338	04	0A0B	380B	00
007D	2E7D	01	040D	320D	16	0539	3339	E2	0A0C	380C	02
007E	2E7E	02	040E	320E	0F	053A	333A	04	0A0D	380D	24
007F	2E7F	21	040F	320F	00	053B	333B	E2	0A0E	380E	3F
0080	2E80	22	0410	3210	11	053C	333C	04	0A0F	380F	08
0081	2E81	04	0411	3211	07	053D	333D	E2	0A10	3810	37
0082	2E82	15	0412	3212	00	053E	333E	04	0A11	3811	00
0083	2E83	24	0413	3213	0E	053F	333F	01	0A12	3812	00
0084	2E84	5F	0414	3214	1B	0540	3340	00	0A13	3813	3A

CONFIDENTIAL

## Driving the Sensor

### Sensor Setting Flow

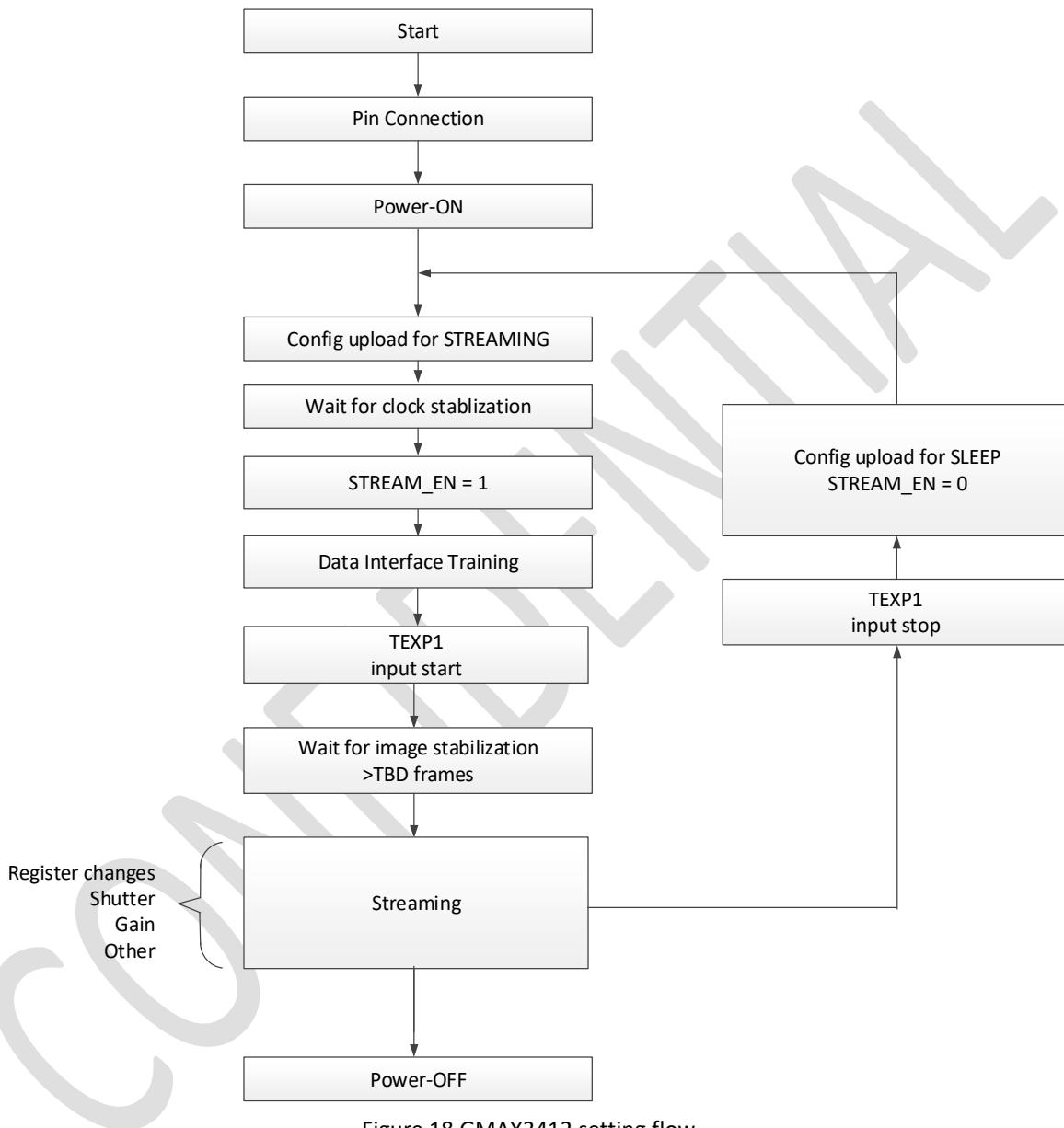


Figure 18 GMAX3412 setting flow

Registers for 'STREAM\_EN' is described as below:

Table 18 Register description for 'STREAM\_EN'

Address (hex)		Bit	Name	Description
SPI	I <sup>2</sup> C			
0	2E00	1	STREAM_EN	0: Disable image capture 1: Enable image capture

## Periphery Connections

This section shows the typical examples for hardware connections of GMAX3412. They are provided for user's reference, Gpixel does not take any responsibility for use of these circuits.

### Analog Power Connections

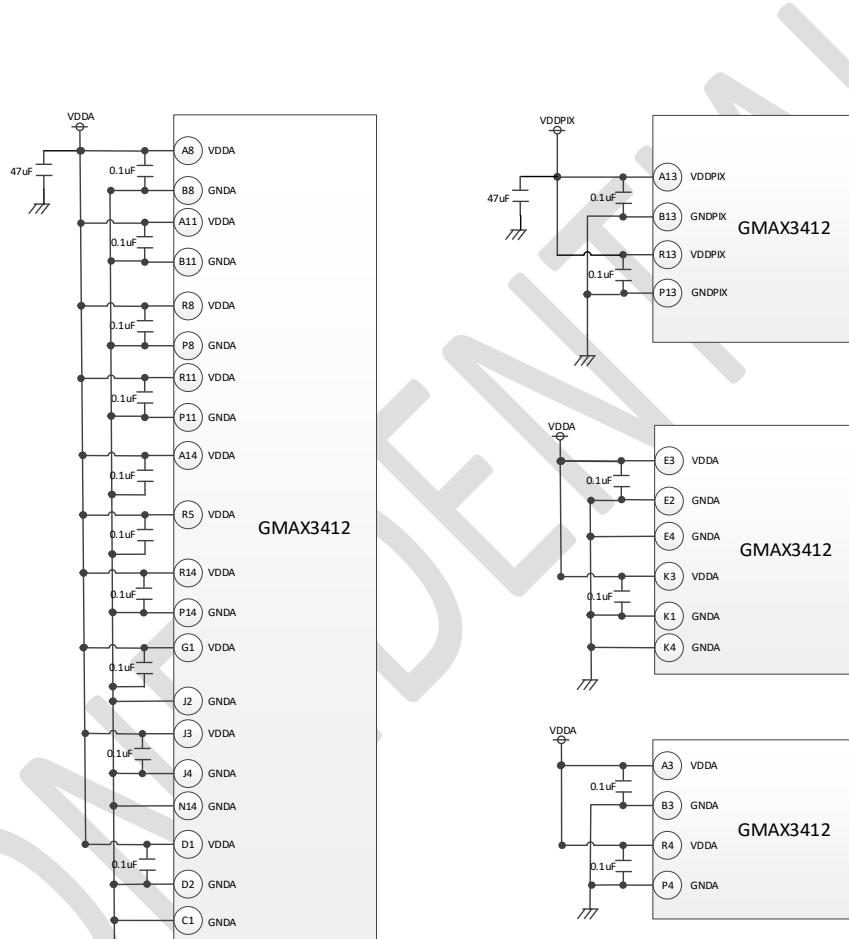


Figure 19 GMAX3412 analog power/ground connections

#### Note:

- 1) Avoid using switching power for analog supplies.

## Digital Power Connections

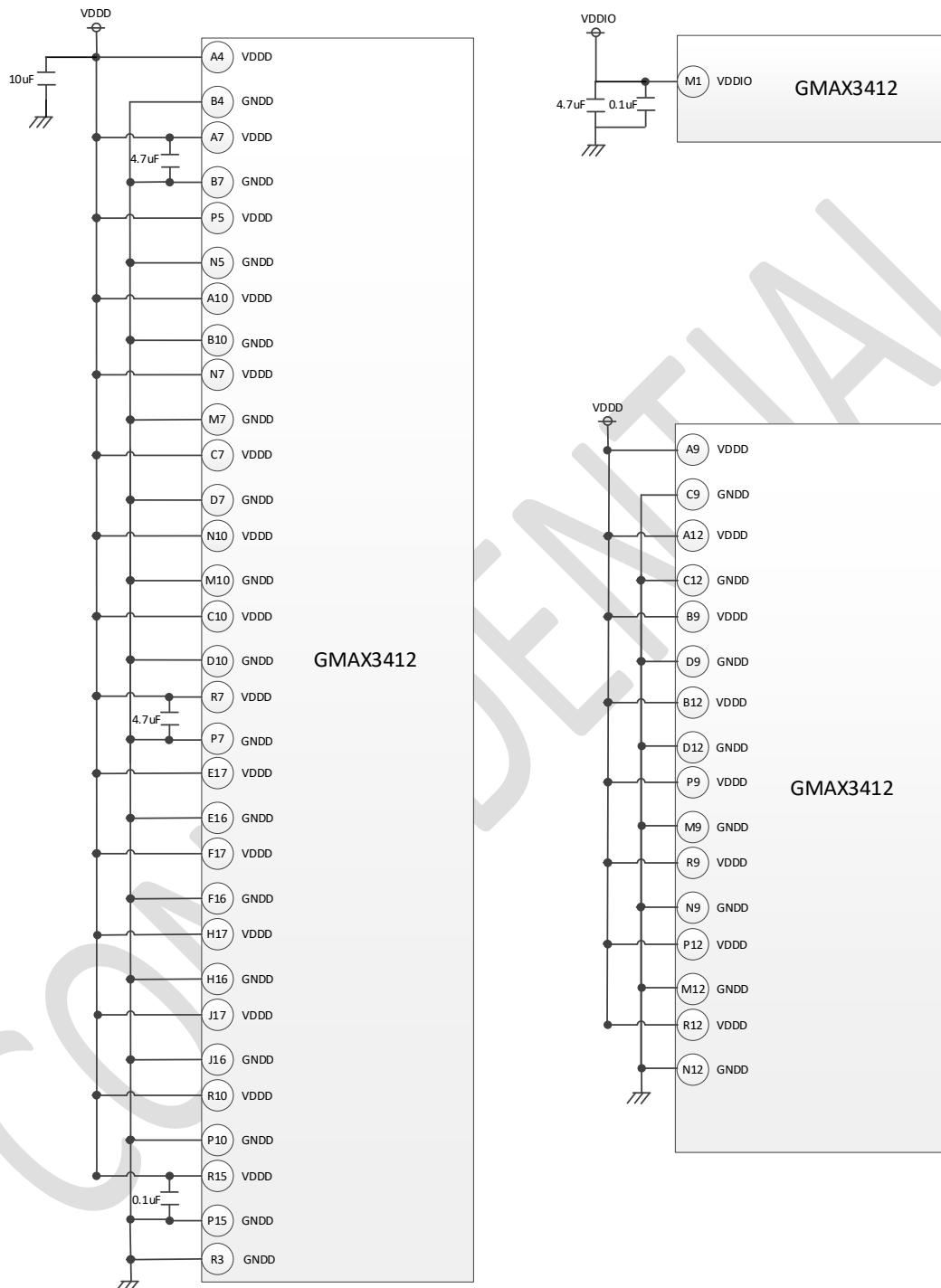


Figure 20 GMAX3412 digital power/ground connections

## Array Supply Connections

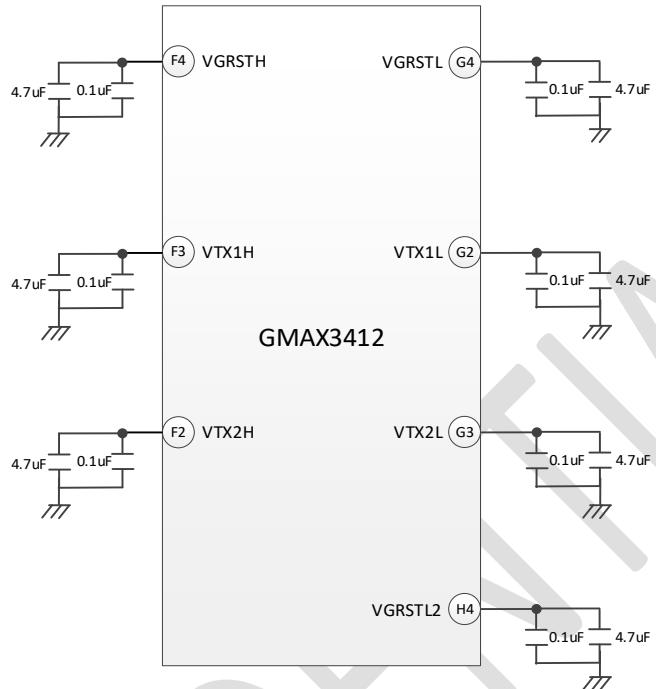


Figure 21 GMAX3412 array supply connections

## Charge Pump Connection

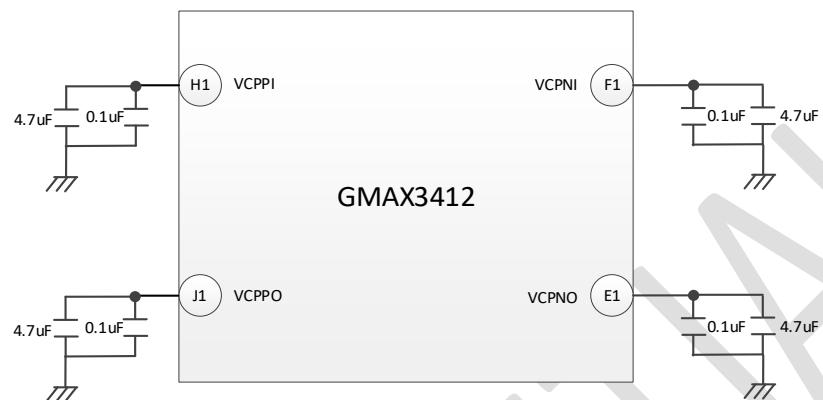


Figure 22 GMAX3412 charge pump connection

## Bias Pin Connections

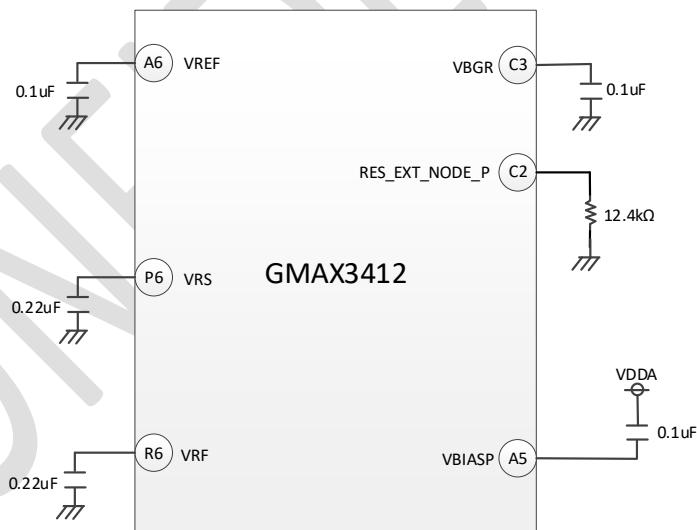


Figure 23 GMAX3412 bias pin connections

### Note:

- 1) The decoupling capacitance values might be updated after characterization phase. Meanwhile, it is advised to foresee an empty footprint for each of those capacitors until the values are finalized.

## Digital I/O and Clock inputs

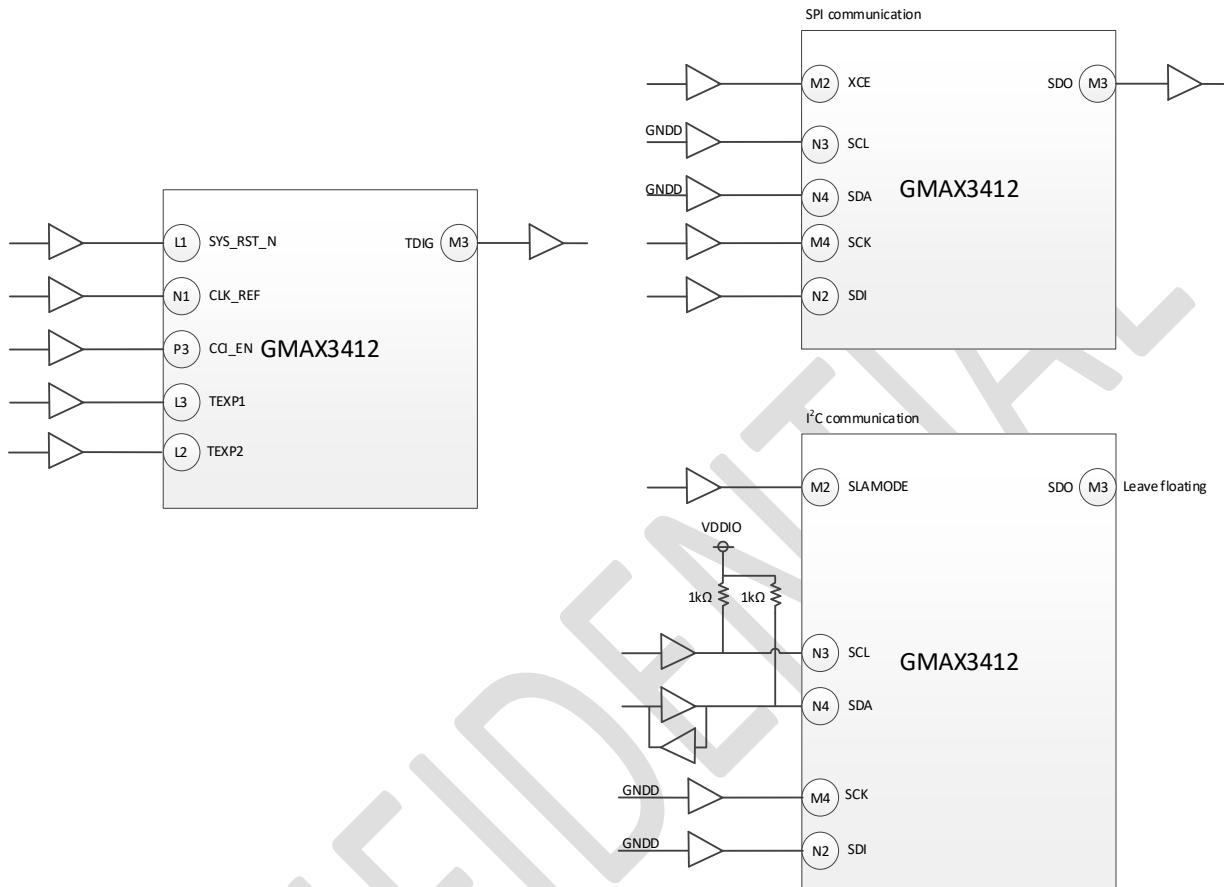


Figure 24 GMAX3412 digital IO and clock input connections

**Note:**

- 1) For the connection of pin-N3 and pin-N4 under I<sup>2</sup>C communication, the recommended range of connected resistance value is from 648Ω to 2951Ω, and the load capacitance is from 10pF to 400pF.
- 2) With register SDO\_TDIG\_SEL described in Table 19, Pin SDO\_TDIG (pin-M3) could be used as SDO which is SPI output or TDIG which is monitor output.

Table 19 register setting for SDO pin

Address (hex)		Bit	Name	Description
SPI	I <sup>2</sup> C			
AF	2EAF	1	SDO_TDIG_SEL	0: SDO, SPI output, refer section SPI Communication Operation 1: TDIG, monitor output, refer section Pins for Status Monitoring

## Data Outputs

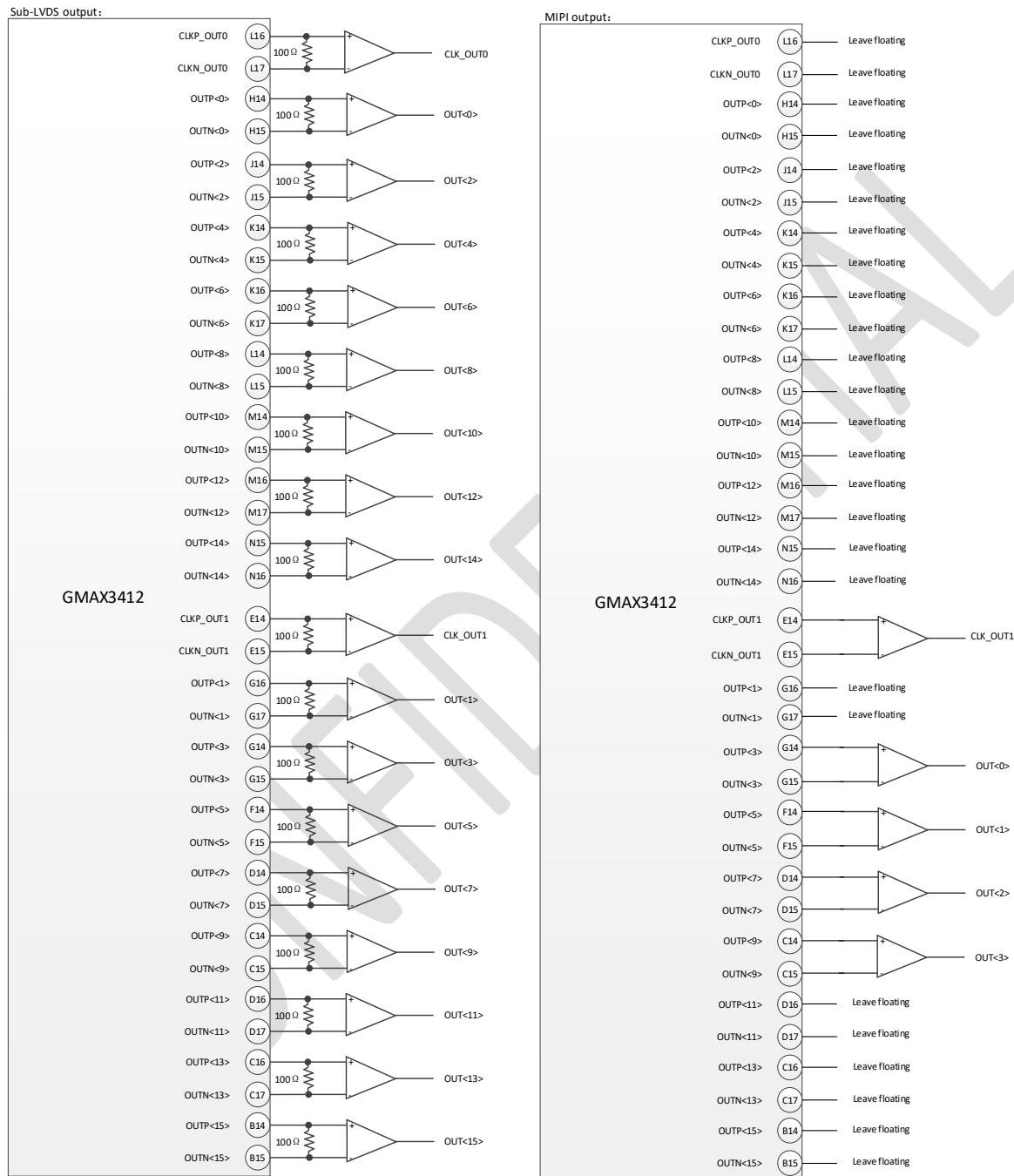


Figure 25 GMAX3412 data output connections

## Power On/Off Sequence

The power supplies should follow the power on/off sequence as illustrated in Figure 26 to avoid current peaks during power on and off. Minimum time delay should be guaranteed. After power on, user should first upload the sensor register setting \* based on section ‘Sensor Configuration’ and ‘Clock System’ then wait for PLL output clock to stabilize. This can take up to 5ms. Then set PWR\_UP\_EN to ‘1’ and waiting for minimum 80ms for internal supplies power-on. Then set CH\_CLK\_EN to ‘1’ and waiting for minimum 1ms . After this ,PHY calibration (PHY cal in Figure 26) needs to be added. Then STREAM\_EN can be set to ‘1’ so the sensor will enter IDLE state. Related registers to control the power-on/off sequence are listed in Table 20.

\*:Please follow the protocol as shown in Figure 41 when changing category A type registers.

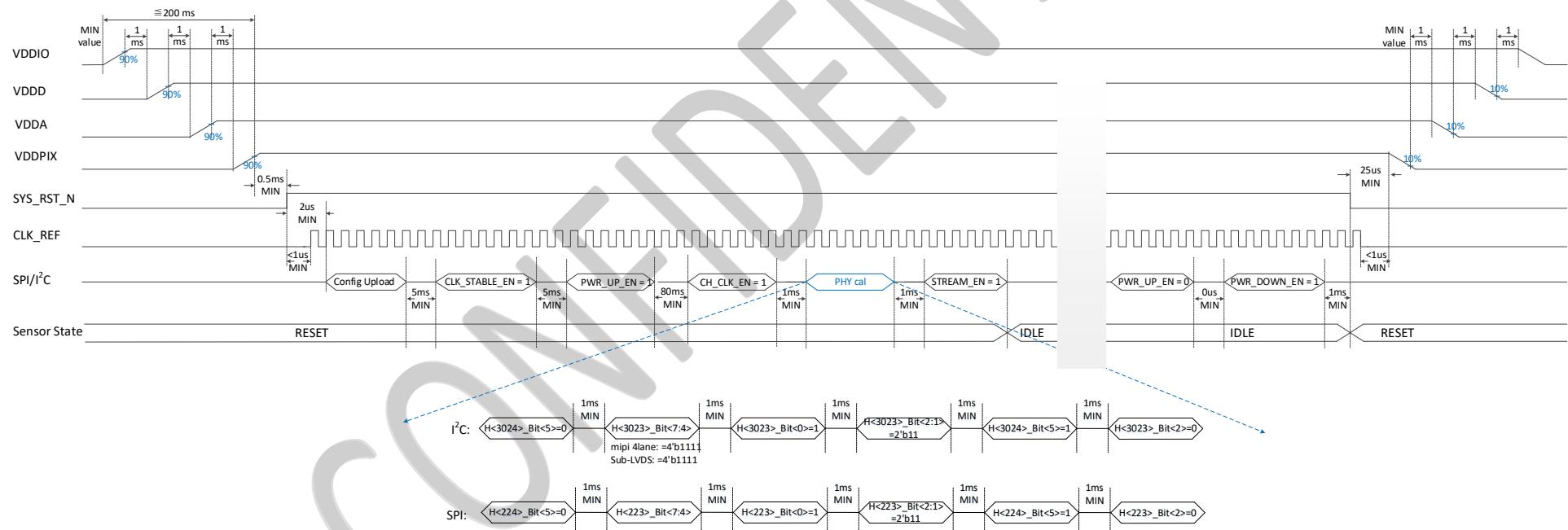


Figure 26 Power-on and power-off sequence

Table 20 Register description for power-on/off sequence

Address (hex)		Bit	Name	Description
SPI	I <sup>2</sup> C			
0	2E00	0	CLK_STABLE_EN	Enable internal clock system
501	3301	0	PWR_UP_EN	Enable internal supplies power on
502	3302	0	PWR_DOWN_EN	Enable internal supplies power down
205	3005	0	CH_CLK_EN	Enable interface(Sub-LVDS or MIPI) clock system

## Sensor Configuration

All on-chip registers should be programmed to the recommended value before image capture. This section lists some basic sensor configuration that user may want to change for specific applications. For more options please refer to section ‘Description of Various Functions’.

### Line Time

GMAX3412 readout is always line time based. In each line time, one row of image data will be output from the output channels. It is always calculated in number of CLK\_PIX cycles.

Table 21 Register setting for line time unit length

Address (hex)		Bit	Name	Description
SPI	I <sup>2</sup> C			
43:42	2E43:2E42	all	LINE_TIME	Value must be an integer. (250≤LINE_TIME≤65535)

The line time can be calculated as:

$$T_{\text{LINE}} = \text{LINE\_TIME} \times T_{\text{CLK\_PIX}}$$

where  $T_{\text{CLK\_PIX}}$  is the period of CLK\_PIX.

**Note:**

- 1) Change of  $T_{\text{LINE}}$  may cause shift of image dark offset.

### Sub-Sampling

To maintain the same optical format but reduce the amount of sensor output data, GMAX3412 supports sub-sampling function. This function can also achieve a higher frame rate without losing the basic information of the captured image.

Sub-sampling in Y-direction is supported. User can set the register SUBSMP\_SPACE to change the space between readout rows. Figure 27 and Figure 28 show the sub-sampling for mono sensor and color sensor respectively. For mono sensor, one row will be selected for readout. For color sensor, two neighbor rows will be selected for readout. This is set through register COLR\_EN. Table 22 gives more detail for this two registers.

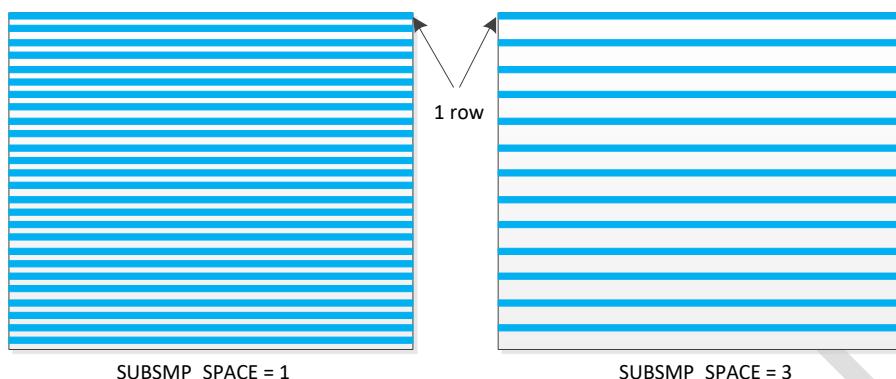


Figure 27 Y-direction sub-sampling for mono sensor

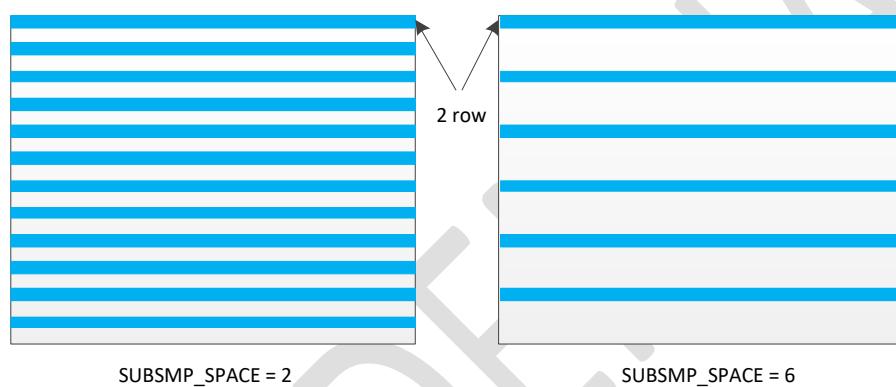


Figure 28 Y-direction sub-sampling for color sensor

Table 22 Register setting for sub-sampling

Address (hex)		Bit	Name	Description
SPI	I <sup>2</sup> C			
2	2E02	0	COLR_EN	0: Mono sensor 1: Color sensor
18	2E18	all	SUBSMP_SPACE	Space between the readout rows

## Windowing

Maximum 8x8 regions of interest can be support in GMAX3412 pixel array (User Defined region, please refer to Figure 3). The start address, length and width can be set by different register settings. For vertical window, all the 8 regions should have the same x-direction address and width which with the unit of 16 columns. For horizontal window, all the 8 regions should have the same y-direction address and length. GMAX3412 can also output electric black rows. The row output sequence of GMAX3412 during image readout is shown in Figure 29. Firstly, EB window will be output and later on user defined(UD) windows. Definition of these windows are shown in Table 23. The description for related registers of windowing is listed in Table 24.

Table 23 Definition of different windows in GMAX3412

Symbol	Description	Size restrictions
EB	Electrical Black(EB) pixel windows, pixel output does not contain any dark current information	Minimum 0 row and maximum 65535 rows.
UD	User defined pixel windows	Limitation for the size is depending on the window start address. In general, it is not allowed to readout rows outside the windowing region shown in Figure 3.

The figure below shows the image output sequence with windowing operation. Note location of pixel(0,0) is different from drawing in Figure 3, the drawing here is based on data output sequence coming out from the output channels.



Figure 29 Image output sequence with windowing operation

Table 24 Register setting for windowing operation

Address (hex)		Bit	Name	Description
SPI	I <sup>2</sup> C			
3C:3B	2E3C:2E3B	all	WIN8_L	Number of readout rows in UD window 8
3A:39	2E3A:2E39	all	WIN8_S	Start row address in UD window 8. Should be set between 0 and 3085
38:37	2E38:2E37	all	WIN7_L	Number of readout rows in UD window 7
36:35	2E36:2E35	all	WIN7_S	Start row address in UD window 7. Should be set between 0 and 3085
34:33	2E34:2E33	all	WIN6_L	Number of readout rows in UD window 6
32:31	2E32:2E31	all	WIN6_S	Start row address in UD window 6. Should be set between 0 and 3085
30:2F	2E30:2E2F	all	WIN5_L	Number of readout rows in UD window 5
2E:2D	2E2E:2E2D	all	WIN5_S	Start row address in UD window 5. Should be set between 0 and 3085
2C:2B	2E2C:2E2B	all	WIN4_L	Number of readout rows in UD window 4
2A:29	2E2A:2E29	all	WIN4_S	Start row address in UD window 4. Should be set between 0 and 3085
28:27	2E28:2E27	all	WIN3_L	Number of readout rows in UD window 3
26:25	2E26:2E25	all	WIN3_S	Start row address in UD window 3. Should be set between 0 and 3085
24:23	2E24:2E23	all	WIN2_L	Number of readout rows in UD window 2
22:21	2E22:2E21	all	WIN2_S	Start row address in UD window 2. Should be set between 0 and 3085
20:1F	2E20:2E1F	all	WIN1_L	Number of readout rows in UD window 1
1E:1D	2E1E:2E1D	all	WIN1_S	Start row address in UD window 1. Should be set between 0 and 3085
17:16	2E17:2E16	all	EB_L	Number of readout rows for EB window
15:14	2E15:2E14	all	NR_MIN	Minimum readout rows for frame readout. This registers can be used to limit the frame rate.
700	3500	7:4	WIN_X_NUM	The front total number of open horizontal windows effective
722:721	3522:3521	12:0	WIN_ALL_LEN	The value =WIN0_X_L+WIN1_X_L+WIN2_X_L+WIN3_X_L+WIN4_X_L+WIN5_X_L+ WIN6_X_L+ WIN7_X_L.
712:711	3512:3511	12:0	WIN0_X_L	Number of readout columns in UD window.Only valid when WIN_X_NUM >0. Should be multiple of 16, minmum WIN0_X_L value is 32.
702:701	3502:3501	12:0	WIN0_X_S	Start column address in UD window. Only valid when WIN_X_NUM >0, WIN0_X_S value must be even number.Should be set between 0 and 4239.
714:713	3514:3513	12:0	WIN1_X_L	Number of readout columns in UD window.Only valid when WIN_X_NUM >1. Should be multiple of 16, minmum WIN1_X_L value is 32.
704:703	3504:3503	12:0	WIN1_X_S	Start column address in UD window. Only valid when WIN_X_NUM >1, WIN1_X_S value must be even number. Should be set between 0 and 4239.
716:715	3516:3515	12:0	WIN2_X_L	Number of readout columns in UD window.Only valid when WIN_X_NUM >2. Should be multiple of 16, minmum WIN2_X_L value is 32.
706:705	3506:3505	12:0	WIN2_X_S	Start column address in UD window. Only valid when WIN_X_NUM >2, WIN2_X_S value must be even number.Should be set between 0 and 4239.

718:717	3518:3517	12:0	WIN3_X_L	Number of readout columns in UD window. Only valid when WIN_X_NUM >3. Should be multiple of 16, minimum WIN3_X_L value is 32.
708:707	3508:3507	12:0	WIN3_X_S	Start column address in UD window. Only valid when WIN_X_NUM >3, WIN3_X_S value must be even number. Should be set between 0 and 4239.
71A:719	351A:3519	12:0	WIN4_X_L	Number of readout columns in UD window. Only valid when WIN_X_NUM >4. Should be multiple of 16, minimum WIN4_X_L value is 32.
70A:709	350A:3509	12:0	WIN4_X_S	Start column address in UD window. Only valid when WIN_X_NUM >4, WIN4_X_S value must be even number. Should be set between 0 and 4239.
71C:71B	351C:351B	12:0	WIN5_X_L	Number of readout columns in UD window. Only valid when WIN_X_NUM >5. Should be multiple of 16, minimum WIN5_X_L value is 32.
70C:70B	350C:350B	12:0	WIN5_X_S	Start column address in UD window. Only valid when WIN_X_NUM >5, WIN5_X_S value must be even number. Should be set between 0 and 4239.
71E:71D	351E:351D	12:0	WIN6_X_L	Number of readout columns in UD window. Only valid when WIN_X_NUM >6. Should be multiple of 16, minimum WIN6_X_L value is 32.
70E:70D	350E:350D	12:0	WIN6_X_S	Start column address in UD window. Only valid when WIN_X_NUM >6, WIN6_X_S value must be even number. Should be set between 0 and 4239.
720:71F	3520:351F	12:0	WIN7_X_L	Number of readout columns in UD window. Only valid when WIN_X_NUM >7. Should be multiple of 16, minimum WIN7_X_L value is 32.
710:70F	3510:350F	12:0	WIN7_X_S	Start column address in UD window. Only valid when WIN_X_NUM >7, WIN7_X_S value must be even number. Should be set between 0 and 4239.

Suppose we define  $N_{W\_SUM}$  the summation of output rows in EB and User defined pixel windows which is:

$$N_{W\_SUM} = WIN1\_L + WIN2\_L + \dots + WIN8\_L + EB\_L$$

The number of row readouts for each frame will be:

$$N_{ROW} = \begin{cases} NR\_MIN + 2, & N_{W\_SUM} + 10 < NR\_MIN \\ N_{W\_SUM} + 12, & N_{W\_SUM} + 10 \geq NR\_MIN \end{cases}$$

$N_{ROW}$  is an important parameter in frame rate calculation.

**Note:**

- 1) The selected readout rows in each window should take sub-sampling related registers into account. For example, Set WIN1\_S = 1000, WIN1\_L = 4, COLR\_EN = 0, SUBSMP\_SPACE= 2 will select Row 1000, 1003, 1006, 1009.
- 2) Vertical window overlap is allowed, however, due to destructive readout, the 2<sup>nd</sup> readout of the overlapped rows will output dark image data.

- 3) Horizontal window overlap is allowed, unlike vertical window overlap, the 2<sup>nd</sup> readout of the overlapped columns will output valid data.
- 4) The windowing function stops as soon as the readout rows in a specific window is set to 0. For instance, if WIN2\_L set to 0, then all selected rows in WIN3\_L, WIN4\_L, etc... will be invalid.
- 5) Vertical windowing helps speed boosting.

## Frame Number and Exposure Setting

For internal exposure, the exposure time and requested frame number are set by uploading the relevant registers. For external exposure, the exposure time is set by pulse width of TEXP1. Only one frame will be output with the trigger signal in external exposure. The registers related are listed below. For info on exposure time please refer to section ‘Exposure Time Calculation’.

Table 25 Register setting for exposure control

Address (hex)		Bit	Name	Description
SPI	I <sup>2</sup> C			
11:10	2E11:2E10	all	FRAME_NUM	65535: Continous image capture Others: Number of frames
3	2E03	0	INT_EXP_EN	0: External exposure 1: Internal exposure
8	2E08	all	EXPO_F	Fine setting for exposure time
B:9	2E0B:2E09	all	EXPO_C	Coarse setting for exposure time

## Clock System

The clock system of GMAX3412 is illustrated in Figure 30. There are three clock inputs: SCK, SCL and CLK\_REF. SCK is needed for SPI programming, SCL is needed for I<sup>2</sup>C programming. CLK\_REF is input to PLL to generate the on-chip high speed clock CLK\_SER. This clock is used to control most of the functional blocks such as Sequencer, ADC, sub-LVDS/MIPI outputs etc.

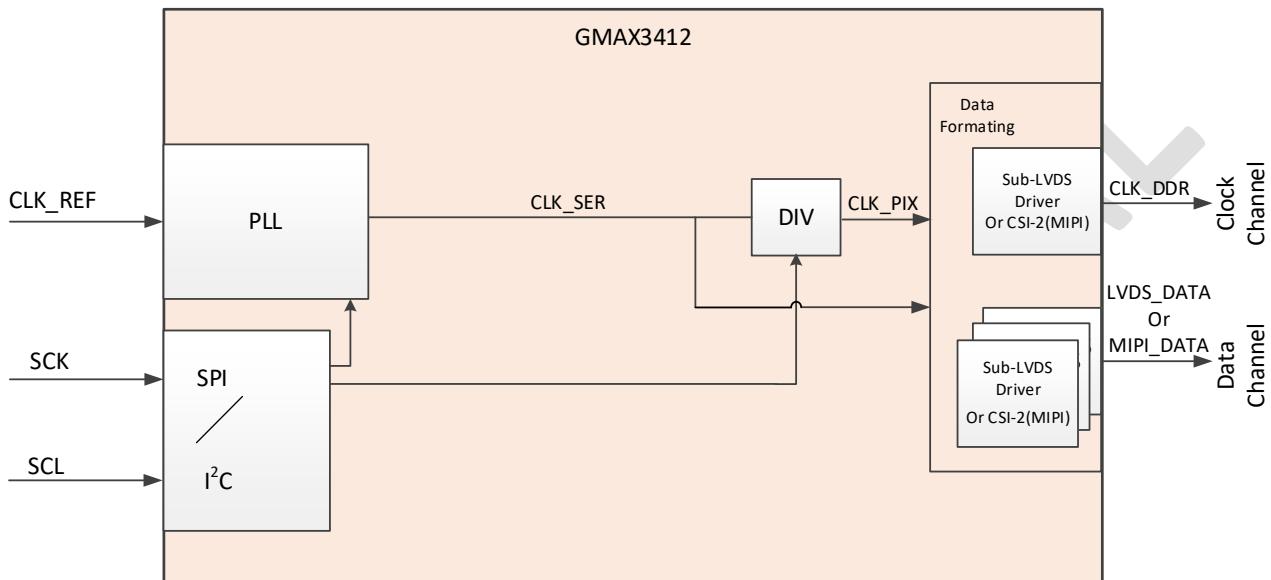


Figure 30 The block diagram of clock management

Table 26 Clock system in GMAX3412

Clock	Symbol	Type	Description
CLK_REF	F <sub>INCLK</sub>	Input	Clock input for on chip PLL
SCK	F <sub>SCK</sub>	Input	SPI clock
SCL	F <sub>SCL</sub>	Input	I <sup>2</sup> C clock
CLK_PIX	F <sub>CLK_PIX</sub>	Internal	F <sub>CLK_PIX</sub> = F <sub>CLK_SER</sub> /12 for 12-bit Sub-LVDS mode F <sub>CLK_PIX</sub> = F <sub>CLK_SER</sub> /12 for 10-bit Sub-LVDS mode F <sub>CLK_PIX</sub> = F <sub>CLK_SER</sub> /12 for 12-bit MIPI mode
CLK_SER	F <sub>CLK_SER</sub>	Internal	On chip high speed clock
CLK_DDR	F <sub>CLK_DDR</sub>	Output	Clock output from sensor clock channel, F <sub>CLK_DDR</sub> = F <sub>CLK_SER</sub> /2

CLK\_PIX is GMAX3412 internal pixel clock, where one pixel data is output per clock cycle from each output channel. CLK\_DDR is a double data rate clock output to the external system, which can be used for pixel data sampling.

The frequency of the internally generated high-speed clock CLK\_SER can be calculated by the PLL multiplication factor(M<sub>X</sub>) and PLL dividing factor(D<sub>YI</sub> and D<sub>YO</sub>), as shown below:

$$F_{CLK\_SER} = F_{CLK\_REF} \times \frac{M_X}{D_{YI} \times D_{YO}}$$

Where  $20\text{MHz} \leq F_{\text{CLK\_REF}} \leq 62.5\text{MHz}$ ,  $20\text{MHz} \leq \frac{F_{\text{CLK\_REF}}}{D_{YI}} \leq 62.5\text{MHz}$  and  $800\text{MHz} \leq F_{\text{CLK\_SER}} \times D_{Y0} \leq 1200\text{MHz}$ .

Details for PLL register settings are shown in Table 27.

Table 27 Registers for PLL setting

Address(hex)		Bit	Name	Description
SPI	I <sup>2</sup> C			
AB	2EAB	3:0	PLL_DIV_IN	Set PLL dividing factor D <sub>YI</sub> 0: D <sub>YI</sub> = 1 1: D <sub>YI</sub> = 2 2: D <sub>YI</sub> = 3 ... ... 14: D <sub>YI</sub> = 15 15: D <sub>YI</sub> = 16
A9	2EA9	6:0	PLL_MULT	Set PLL multiplication factor M <sub>X</sub> 0 ~ 11: not defined 12: M <sub>X</sub> = 12 13: M <sub>X</sub> = 13 ... ... 126: M <sub>X</sub> = 126 127: M <sub>X</sub> = 127
A7	2EA7	1:0	PLL_DIV_OUT	Set PLL dividing factor D <sub>Y0</sub> 0: D <sub>Y0</sub> = 1 1: D <sub>Y0</sub> = 2 2: D <sub>Y0</sub> = 3 3: D <sub>Y0</sub> = 4

## Reset Sequence

The sensor reset sequence is shown in Figure 31. All the signals in the figure should follow the corresponding minimal time delays for correct reset operation. All programming registers will be reset to their default value when SYS\_RST\_N is set to '0'. It is necessary to reconfigure the registers before image capture. If different CLK\_PIX frequency is required while the sensor running, the sensor reset sequence must be executed.

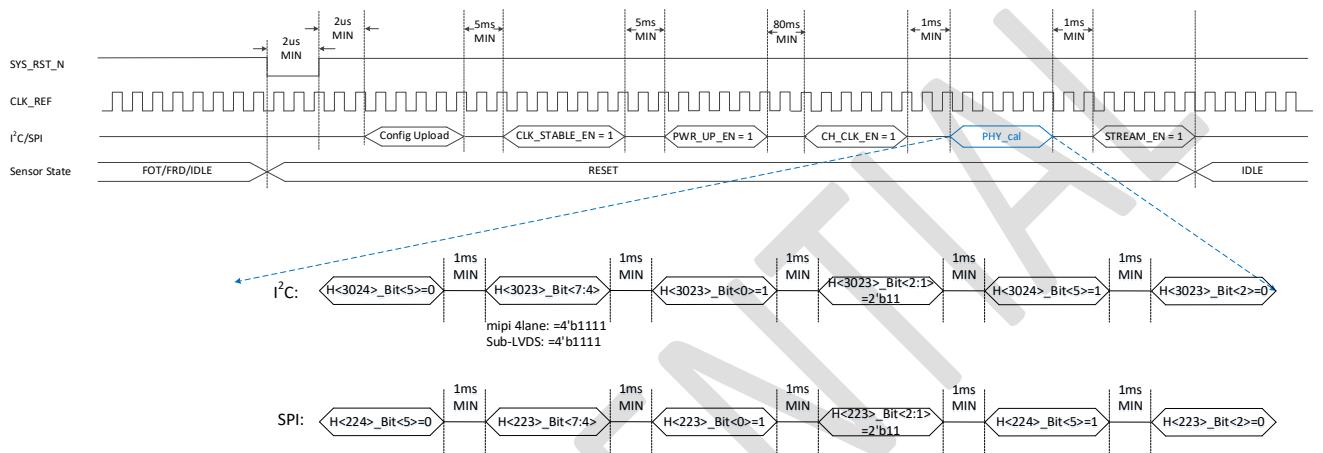


Figure 31 Sensor reset sequence

## Register Communication Timing

GMAX3412 has on-chip SPI/I<sup>2</sup>C for registers communication. There is a dedicated pin CCI\_EN (pin-P3) used to select communication protocol. Tie CCI\_EN low then SPI is used; otherwise tie this pin high.

After the sensor power on, all registers will be reset to default state. Some of the registers need to be re-configured before proper operation of the sensor. The read and write of these registers are through the SPI/ I<sup>2</sup>C interface. Details about the read and write operation is explained below.

## SPI Communication Operation

### SPI WRITE

The data is sampled by the GMAX3412 on the rising edge of SCK. The SCK has a maximum frequency of 10MHz. The XCE signal has to be high for one clock period before the first data-bit is sampled. XCE has to remain high for 1 clock period after the last data-bit is sampled.

During SPI write operation, the control bit A15 is set to low. Figure 32 and Figure 33 show the SPI write operation with continuous addresses and discontinuous addresses.

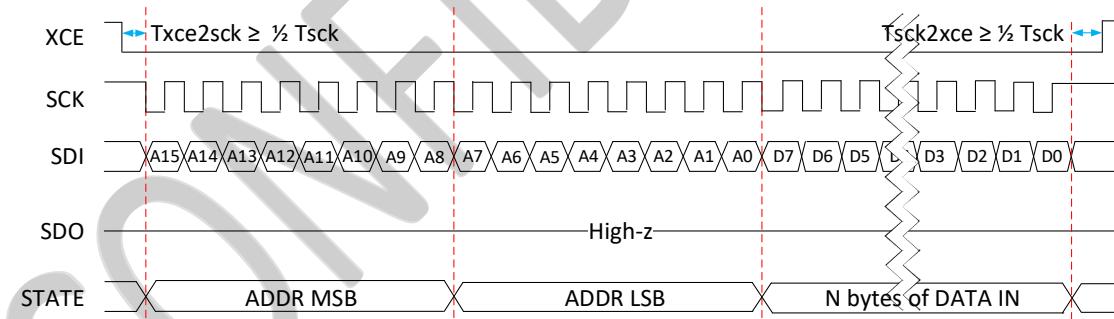


Figure 32 SPI Write operation timing with continuous addresses

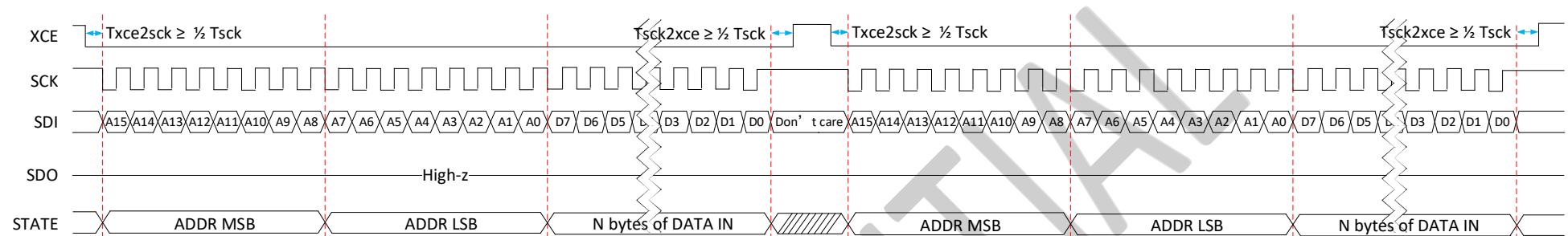


Figure 33 SPI Write operation timing with discontinuous addresses

### SPI Read

The control bit A15 is set to high in order to read the registers from the interface. The data is sent out from SDO in the falling edge of SCK with MSB first.

Like the write operation, it is also possible to read registers with continuous addresses or discontinuous addresses. The timing diagram of SPI read operation is shown in Figure 34 and Figure 35.

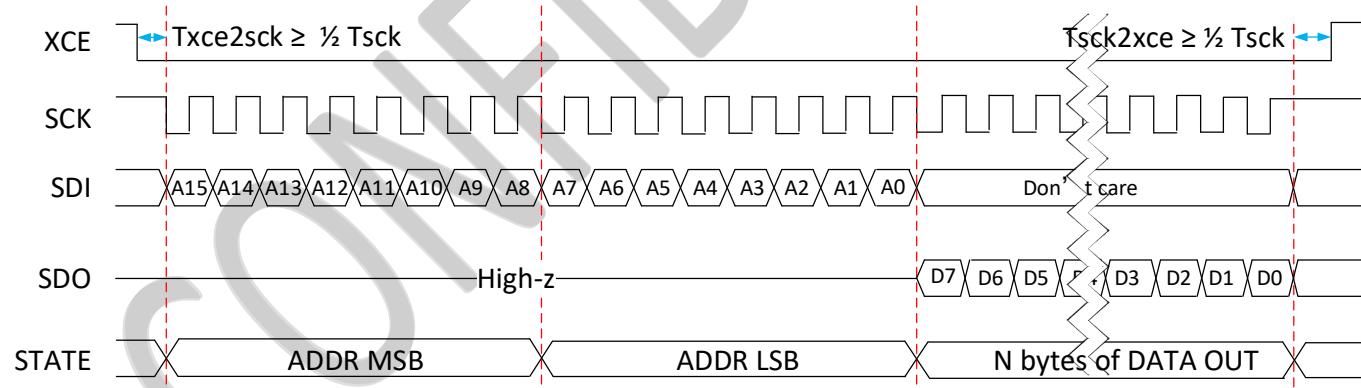


Figure 34 SPI Read operation timing with continuous addresses

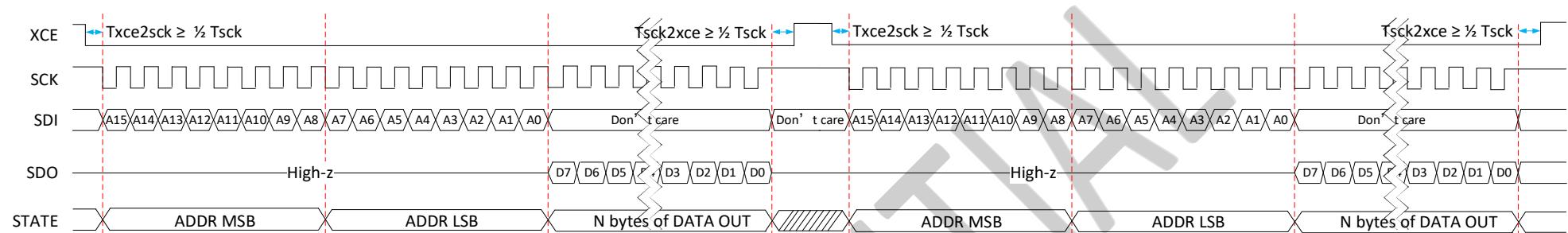


Figure 35 SPI Read operation timing with discontinuous addresses

## I<sup>2</sup>C Communication Operation

When sensor work under I<sup>2</sup>C communication, the PIN-M2 serves as SLAMODE, with which GMAX3412 can be used two kinds of slave address with common I<sup>2</sup>C bus as shown in Table 28.

There is a R/W bit follows SLAVE address. R/W bit is set to 0 indicates I<sup>2</sup>C write and 1 indicates I<sup>2</sup>C read.

Table 28 SLAMODE address

SLAMODE	SLAVE Address (7 bit)	Description
0	001_0000	Address 1
1	001_1010	Address 2

### I<sup>2</sup>C WRITE

After a write request with designating slave address, the master sets the address to M which is the designating address. Then the master can write the data in address M. After successful written, the master generates the stop condition to end the communication. The sensor address and data flow in write operation is shown in Figure 36. After each data byte is transferred, A(Acknowledge) or  $\bar{A}$ (Negative Acknowledge) is transferred from slave to master.

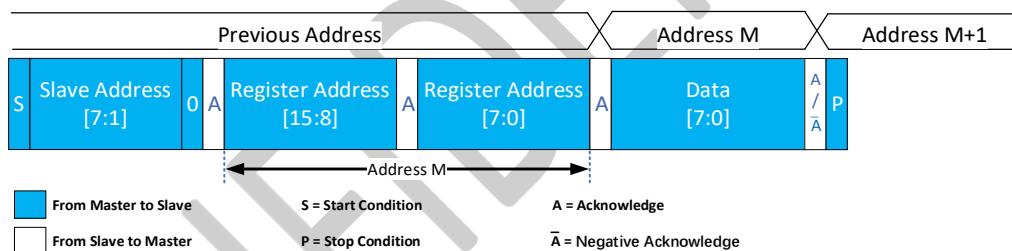


Figure 36 I<sup>2</sup>C single write

GMAX3412 also support sequential write as shown in Figure 37.

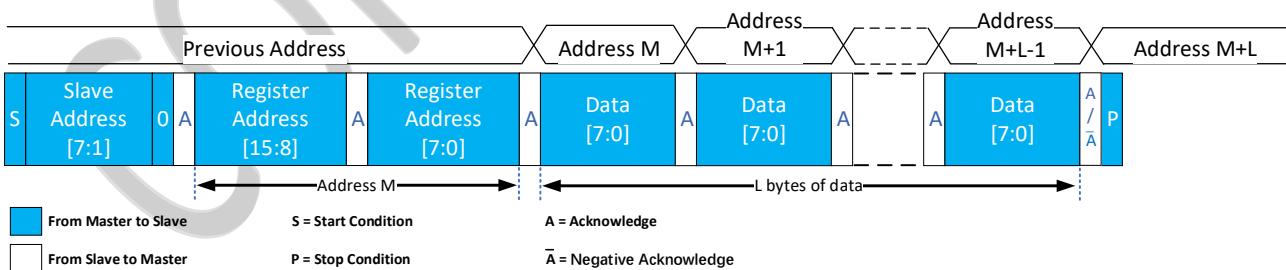


Figure 37 I<sup>2</sup>C sequential write

Data is transferred serially with MSB first. Serial data is transferred through pin SDA, and serial clock is transferred through pin SCL. As shown in Figure 38, serial data(SDA) is transferred at serial clock(SCL) cycle. During data transferred phase, SDA must be held while SCL is high. SDA could be changed only when SCL is low. The SCL has a maximum frequency of 400KHz.

As shown in Figure 38, the start condition 'S' is defined as SDA changing from high to low while SCL is high, and stop condition 'P' is defined as SDA changing from low to high while SCL is high. Repeated start condition 'Sr' is defined as a start condition, when it is generated, the stop condition has not been generated in the previous communication phase.

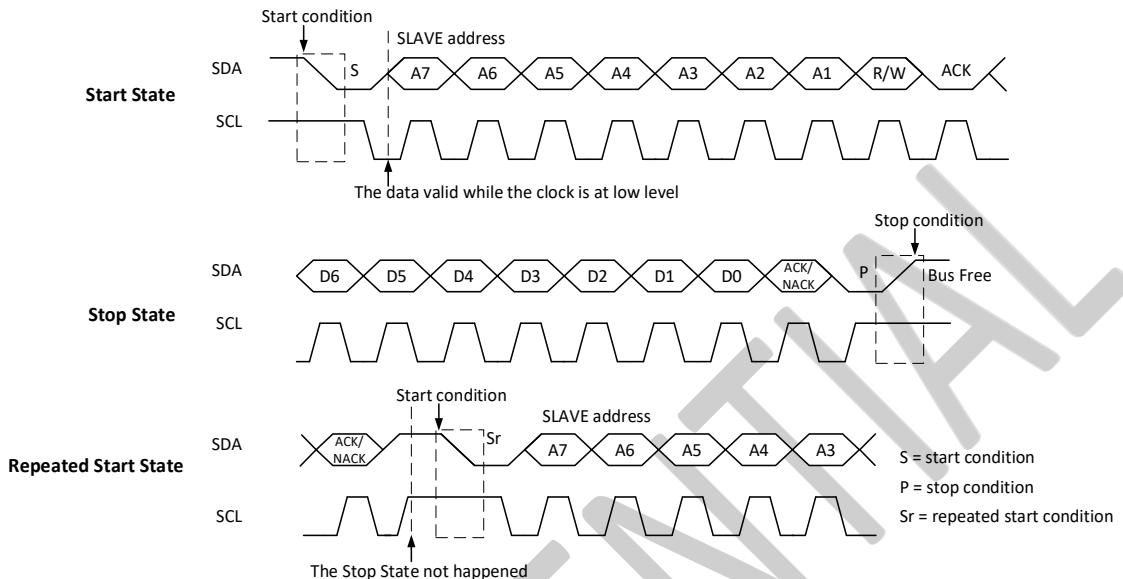


Figure 38 I<sup>2</sup>C operation timing

## I<sup>2</sup>C READ

Before reading the data, the master must set the designating address first. Figure 39 and Figure 40 describe single read and sequential read respectively.

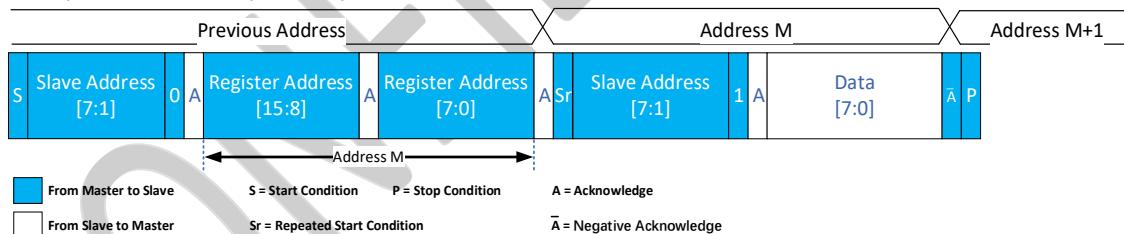


Figure 39 I<sup>2</sup>C single read

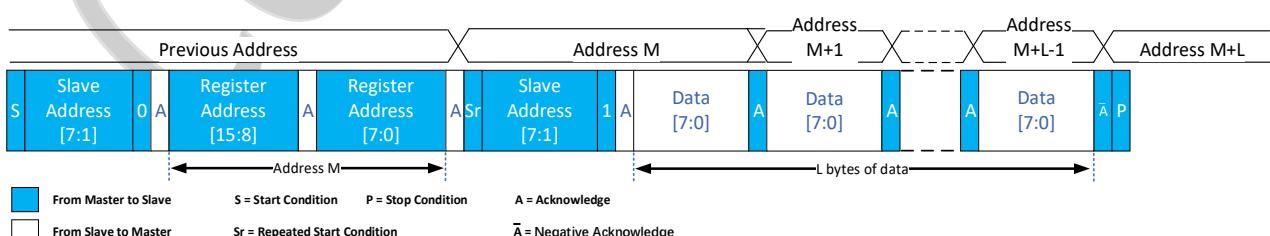


Figure 40 I<sup>2</sup>C sequential read

## Synchronization of Registers

GMAX3412 sensor on-chip registers are categorized into two types with the unit of byte. Although all of the registers will be uploaded into the sensor with SPI/ I<sup>2</sup>C write operation, some of them will not be functional until a trigger moment. Descriptions of these registers are listed in Table 29.

Table 29 Categories of GMAX3412 registers

Type	Trigger Moment	Address (hex)		Bit	Description
		SPI	I <sup>2</sup> C		
A	End of FOT	906	3706	3:0	High sign bit:black level offset value setting for odd column
		907	3707	all	Low sign bit:black level offset value setting for odd column
		A06	3806	3:0	High sign bit:black level offset value setting for even column.
		A07	3807	all	Low sign bit:black level offset value setting for even column.
		700	3500	0	Horizontal flip enable
		700	3500	3:1	Image test mode
		700	3500	7:4	Horizontal window number
		722:701	3522:3501	all	X window setting
		AE	2EAE	5:0	PGA gain setting
		904	3704	5:0	Digital gain setting for odd column.
B	Rising edge of TEXP1 and end of FOT	8	2E08	all	EXP0_F
		B:9	2E0B:2E09	all	EXP0_C
		C	2E0C	all	EXP1_F
		F:D	2E0F:2E0D	all	EXP1_C
		Rising edge of TEXP1	11:10	all	FRAME_NUM
	End of FOT	3C:1D	2E3C:2E1D	all	Y window setting
	Immediately after SPI/ I <sup>2</sup> C write			others	

Category A type registers will be reflected at the falling edge of TEXP1 with a fixed delay and globally controlled by the register REG\_HOLD. Setting REG\_HOLD=1 at the start of register communication period prevents the registers that are set thereafter from reflecting at the frame TEXP1 falling edge. After registers uploaded, setting REG\_HOLD = 0 and designating registers will be reflected at the falling edge of TEXP1 in the next frame.

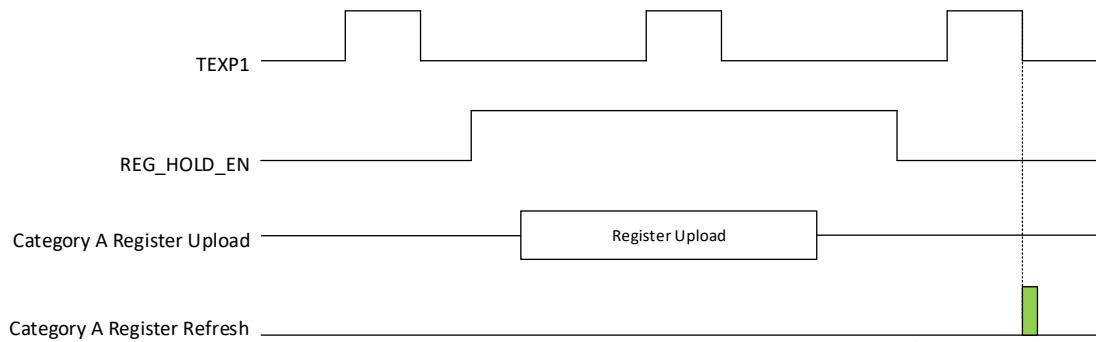


Figure 41 Category A register refresh timing

Table 30 register setting for group hold

Address (hex)		Bit	Name	Description
SPI	I <sup>2</sup> C			
1	2E01	0	REG_HOLD	0: invalid 1: valid (register hold)

Category B type registers will be reflected immediately when the communication is performed. Then the state of sensor will be changed. It's strongly recommended to reconfigure this type registers under the IDEL state when pixel is neither exposure nor reading out.

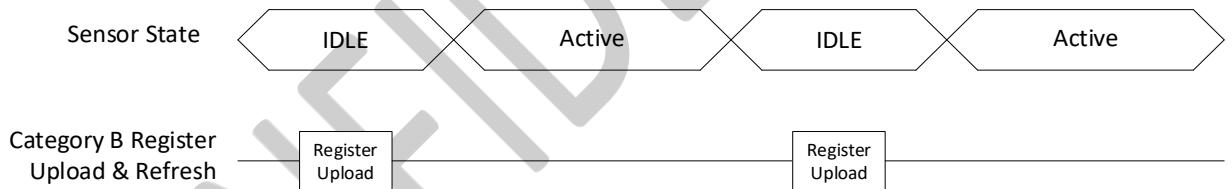


Figure 42 Category B register refresh timing

## Requesting Frames

After sensor power on sequence and register configuration, GMAX3412 will enter the IDLE state and wait for external trigger signal for image capture. The sensor starts exposure when high state of TEXP1 is detected. Once the exposure finishes, the charges collected in the photodiode will be transferred and stored in the memory cell inside each pixel. This period is named as frame overhead time(FOT). After this, the sensor enters frame readout state(FRD) and the image signals can be readout row by row. A second frame exposure can start when the sensor is in FRD state. The sensor enters IDLE again once frame readout is finished. When pin 'SYS\_RST\_N' is pulled low, the sensor will enter RESET state, with all on-chip registers reset to their default value. GMAX3412 will not response to any external trigger signal in RESET state. The four operation states is described in Table 31.

Table 31 Operation states of GMAX3412

Operation State	Description
RESET	When pin 'SYS_RST_N' is pulled low, sensor is in RESET phase. The sensor will not response to any external trigger in this state.
IDLE	In this state, the sensor configuration is ready. It waits for external trigger signal to start image capture. GMAX3412 is in IDLE state whenever it is not in RESET, FOT and FRD state.
FOT	Frame Overhead Time, in this state, the image signal are transferred globally in the storage node inside each pixel.
FRD	Frame Readout, in this state, the stored image signal is readout row by row

GMAX3412 sensor supports both internal and external exposure control. Details of them are described in below section.

**Note:**

- 1) The pulse width of external trigger signal TEXP1 must be at least 2 CLK\_PIX cycles.
- 2) The pulse width of external trigger signal TEXP2 must be at least 2 CLK\_PIX cycles.
- 3) The time from the rising edge of TEXP1 to the rising edge of TEXP2 must be at least 2 CLK\_PIX cycles.

## Internal Exposure Control

When GMAX3412 is working with internal exposure control, the exposure time is set through on-chip registers. Please refer to section 'Frame Number and Exposure Setting' for the relevant registers. GMAX3412 will start exposure when the high state of TEXP1 is detected.

Figure 43 shows the request of two frames with internal exposure. Figure 43(a) shows frame request when exposure time is shorter than the readout time. In this situation, the exposure of the second frame starts during the readout and ends immediately once readout is finished. Figure 43(b) shows frame request when exposure time is longer than readout time. In this situation, the second frame exposure starts with a fixed delay after FOT of the previous frame.

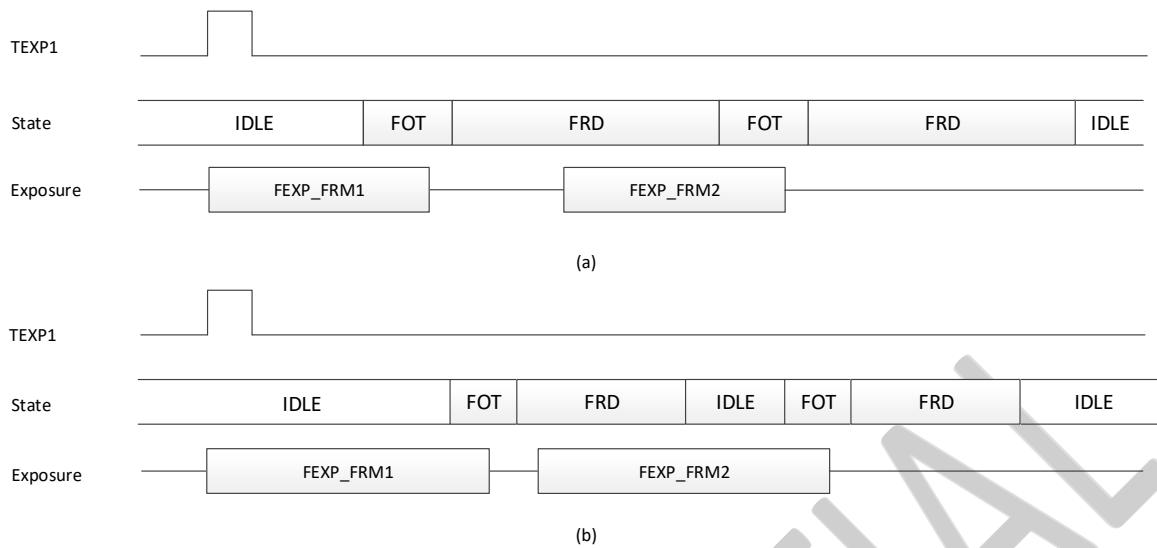


Figure 43 Frame request with internal exposure control

**Note:**

- 1) Frame exposure always extends into FOT state, details please refer to section “Exposure End Delay”.

It is possible that before the frame readout of previous requested frames, a second TEXP1 pulse is triggered as like shown in Figure 44. In this case, after frame readout of current frame, new frames will be requested. This new trigger will also update the exposure time and number of frames. Refer to section ‘Synchronization of Registers’ for more info.

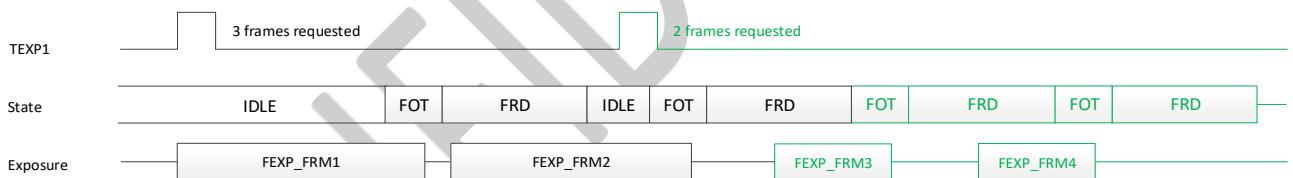


Figure 44 Trigger before readout of previous requested frames

## External Exposure Control

When GMAX3412 is working with external exposure control, only one frame can be output each time. Figure 45(a) shows one frame requested when the sensor is in IDLE state. Exposure starts immediately after detection of high state in TEXP1 signal, and it stops when a low state is detected.

Starting exposure in the FOT phase of previous frame is not allowed, otherwise the image sensor will not work properly.

Ending exposure after FRD of the previous frame is recommended, otherwise the exposure end will be delayed, as illustrated in Figure 45(b).

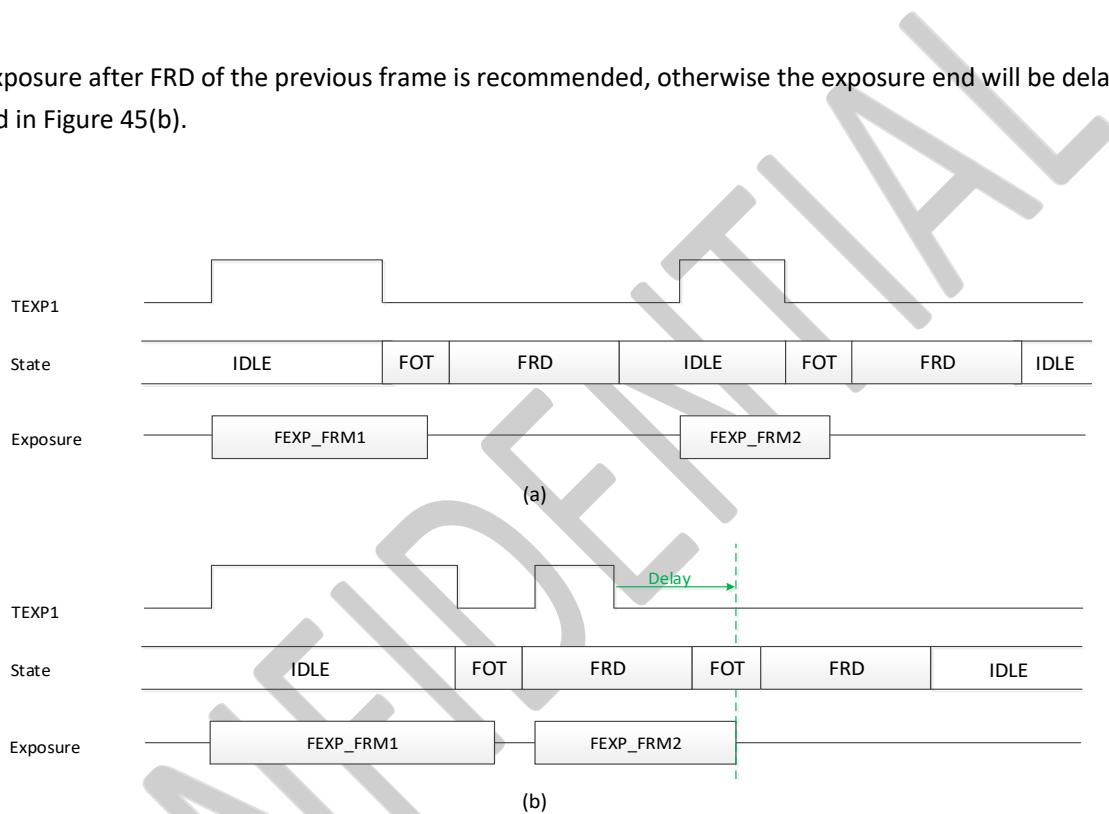


Figure 45 Two frame requests with external exposure

## Exposure Delay

The real exposure of GMAX3412 will always have a delay compared with external trigger signals. They are described in more detail below.

**Note:**

- 1) There is a maximum uncertainty of 1 CLK\_PIX cycles for detection of the external trigger signal.

## Exposure Start Delay

a. Internal Exposure

With internal exposure, the exposure start delay depends on the status of the sensor. We only provide the equation for this delay with trigger in IDLE state.

$$TD_{EXPS\_INT} = 4 \times T_{LINE} - \min (EXPO\_F \times 4 \times T_{CLK\_PIX}, T_{LINE} - T_{CLK\_PIX}), \text{ (Trigger in IDLE)}$$

b. External Exposure

The exposure start delay also depends on the sensor status with sensor in external exposure mode, as calculated below:

$$TD_{EXPS\_EXT} = \begin{cases} 0 & , \text{ (Trigger in IDLE)} \\ 2 \times T_{LINE} & , \text{ (Trigger in FRD)} \end{cases}$$

Register detail with  $TD_{EXPS\_EXT}$  triggered in IDLE is shown in Table 32.

Table 32: Register setting for External Exposure

Address (hex)		Bit	Name	Description
SPI	I <sup>2</sup> C			
6	2E06	2	EXT_IDLE_EXP_DELAY	0: $TD_{EXPS\_EXT} = 0$ (trigger in IDLE) 1: $TD_{EXPS\_EXT} = 2 \times T_{LINE}$ (trigger in IDLE)

## Exposure End Delay

The exposure time always extend into part of the FOT state both in internal exposure and external exposure mode. The exact exposure end moment will be 2500 CLK\_PIX cycles and 3160 CLK\_PIX cycles delayed after start of FOT in 12bit sub-LVDS mode and 12bit MIPI mode, and 3600 CLK\_PIX cycles in 10bit sub-LVDS mode.

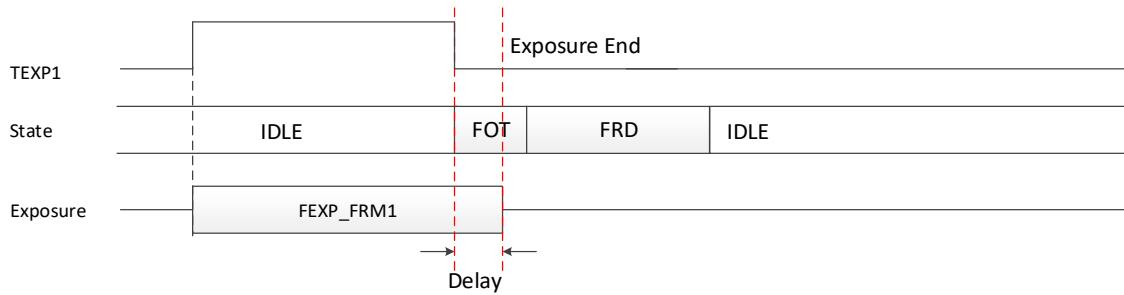


Figure 46 Exposure delay for GMAX3412 sensor

## Exposure Time Calculation

For internal exposure, the exposure time can be calculated as:

12bit sub-LVDS mode,

$$T_{EXP,INT} = EXP0\_C \times T_{LINE} + \min (EXP0\_F \times 4 \times T_{CLK\_PIX}, T_{LINE} - T_{CLK\_PIX}) + 2500 \times T_{CLK\_PIX}$$

12bit MIPI mode,

$$T_{EXP,INT} = EXP0\_C \times T_{LINE} + \min (EXP0\_F \times 4 \times T_{CLK\_PIX}, T_{LINE} - T_{CLK\_PIX}) + 3160 \times T_{CLK\_PIX}$$

10bit sub-LVDS mode,

$$T_{EXP,INT} = EXP0\_C \times T_{LINE} + \min (EXP0\_F \times 4 \times T_{CLK\_PIX}, T_{LINE} - T_{CLK\_PIX}) + 3600 \times T_{CLK\_PIX}$$

For external exposure, the exposure time can be calculated as:

12bit sub-LVDS mode,

$$T_{EXP,EXT} = T_{FR\_W} + 2500 \times T_{CLK\_PIX}$$

12bit MIPI mode,

$$T_{EXP,EXT} = T_{FR\_W} + 3160 \times T_{CLK\_PIX}$$

10bit sub-LVDS mode,

$$T_{EXP,EXT} = T_{FR\_W} + 3600 \times T_{CLK\_PIX}$$

With  $T_{FR\_W}$  the pulse width of  $TEXP1$ .

## Frame Rate Calculation

If exposure time is longer than the readout time of GMAX3412, the frame rate will depend on the exposure time.

The frame readout(FRD) time is equal to:

$$T_{RD} = N_{ROW} \times T_{LINE}$$

FOT time is equal to:

12bit mode,

$$T_{FOT} = 11 \times T_{LINE}$$

10bit mode,

$$T_{FOT} = 21 \times T_{LINE}$$

Then frame time(Internal Exposure Mode) can be calculated as:

$$T_{FRM} = \begin{cases} T_{RD} + T_{FOT} & N_{ROW} \geq T_{exp} + 6 \\ (T_{exp} + 6) \times T_{LINE} + T_{FOT} & N_{ROW} < T_{exp} + 6 \end{cases}$$

where  $T_{exp} = EXPO\_C$ .

## Reading Out The Sensor

GMAX3412 supports two types of data output interfaces: Sub-LVDS and CSI-2(MIPI). Register can be used to select the output interface, please refer to Table 33.

Please do not switch the output interface during operation, or the imaging characteristics cannot be guaranteed.

Table 33: Register setting for data output interface selection

Address (hex)		Bit	Name	Description
SPI	I <sup>2</sup> C			
200	3000	0	OUT_MODE_SEL	Output interface selection: 0: Sub_LVDS 1: CSI-2(MIPI)

## Sub-LVDS Output

There are sixteen sub-LVDS data channels in total. Together with the data channel, GMAX3412 has two sub-LVDS clock channel. The clock channel can be used to sample the image data.

- 16 data channels
- 2 clock channels

The data channels are used to transport the image data to the receiving end of the surrounding system. The clock channel outputs a Double Data Rate(DDR) clock which can be used at the receiving end to sample the image data. It is synchronous to the data channels with minimum skew.

**Note:**

- 1) The DDR clock generated by CLK\_OUT0 is used for sampling the image data from OUT<0>, OUT<2>, OUT<4>, OUT<6>, OUT<8>, OUT<10>, OUT<12>, OUT<14>, and CLK\_OUT1 is for OUT<1>, OUT<3>, OUT<5>, OUT<7>, OUT<9>, OUT<11>, OUT<13>, OUT<15>.

## Data Interface Training

For correct data receiving, it is recommended to train the output data interface(data channels) before image capture. It is possible to use the DDR clock channel to directly sample the data channel. Normally only word alignment is needed for this training process.

Described in section ‘Sensor Setting Flow’, a known training pattern(TP) will be output continuously on all data channels after STREAM\_EN release to state ‘1’. With this TP output, word alignment is possible.

Registers detail with data interface training are shown in Table 34.

Table 34 Register setting for data interface training

Address (hex)		Bit	Name	Description
SPI	I <sup>2</sup> C			
215	3015	3:0	Training Pattern	High sign bit:training pattern at channel output
214	3014	7:0		Low sign bit:training pattern at channel output

## SYNC Code

Sync code is added in the image sensor output to indicate the correct pixel data. The Sync code length is 40-bit and 48-bit for 10-bit out and 12-bit out respectively . So always 4-word in serial. There are four types of Sync codes used in GMAX3412 sensor. They are listed below in Table 35 and Table 36.

Table 35 Types of SYNC codes in GMAX3412 sensor

Sync code	Description
SOF	Start of Frame: Beginning of Image
EOF	End of Frame: End of Image
SOL	Start of Line: Beginning of horizontal line
EOL	End of Line: End of horizontal line

Table 36 Details of the SYNC codes

Sync code	First word		Second word		Third word		Fourth word	
	10-bit	12-bit	10-bit	12-bit	10-bit	12-bit	10-bit	12-bit
SOF	3FFh	FFFh	000h	000h	000h	000h	200h	800h
EOF	3FFh	FFFh	000h	000h	000h	000h	274h	9D0h
SOL	3FFh	FFFh	000h	000h	000h	000h	2ACh	AB0h
EOL	3FFh	FFFh	000h	000h	000h	000h	0D8h	B60h

Figure 47 illustrates the image data output format for GMAX3412 sensor. TP code is data word based and placed any moment when SYNC code and valid data are not output. The sensor will always output EB window, followed by UD window as described before in section ‘Widnowing’.



Figure 47 GMAX3412 image data output format

**Note:**

- 1) TP Row Number = 5 when exposure starts during readout in normal mode.
- 2) TP Row Number is between 5 and 10 when exposure starts during readout in Multi Region HDR or Multi-slope mode, exact value depending on the time from the rising edge of TEXP1 to the rising edge of TEXP2.
- 3) TP Row Number = 0 when exposure does not start during readout.

## Image Data Output Format

GMAX3412 array data output is split in 16 blocks. Figure 48 shows the column address and data word sequence in different sub-LVDS channels.



Figure 48 Data output format

In sub-LVDS output mode, the MSB and LSB sequence could be configured with register HLO\_ORDER, please refer to Table 37.

Table 37: Register setting for data output interface selection

Address (hex)		Bit	Name	Description
SPI	I <sup>2</sup> C			
210	3010	0	HLO_ORDER	Sub-LVDS ouptut mode: 0: MSB output first 1: LSB output first CSI-2(MIPI) output mode: Must be set to 1

## Channel Multiplexing

With the default setting, GMAX3412 use 16 channels to output the 12/10-bit image data. It supports to readout the full frame with reduced number of output channels. In this case, the register of LINE\_TIME, refer to section Line

Time, is needed to be adjusted proportionally and the frame rate will be reduced proportionally. All the sub-LVDS channels unused will automatically be switched off to save power.

Table 38 and Table 39 give more detailed information for channel multiplexing setting with register CHAN\_NUM. Taking 12bit as an example to show that the line time will increase with CHAN\_NUM decreasing. For example, when CHAN\_NUM is set to 8, OUT <0:15> will be used to output the full image, with each channel output 265 pixels per row and the LINE\_TIME should be set larger than 510. Figure 49 gives the number of pixels output by each channel in one line time.

Table 40 GMAX3412 channel output info with different setting for CHAN\_NUM @12bit mode

Address (hex)		Bit	Name	Value(hex)	Channal No.	Number of pixes per channel	Minimum value of LINE_TIME (12bit)
SPI	I <sup>2</sup> C						
209	3009	3:0	CHAN_NUM	8	OUT<0:15>	265	510
				7	OUT <0:13>	303	583
				6	OUT <0:11>	354	680
				5	OUT <0:9>	424	816
				4	OUT <0:7>	530	1020
				3	OUT <0:5>	707	1360
				2	OUT <0:3>	1060	2040
				1	OUT <0:1>	2120	4080
				0	OUT <0>	4240	8160

Table 41 GMAX3412 channel output info with different setting for CHAN\_NUM @10bit mode

Address (hex)		Bit	Name	Value(hex)	Channal No.	Number of pixes per channel	Minimum value of LINE_TIME (10bit)
SPI	I <sup>2</sup> C						
209	3009	3:0	CHAN_NUM	8	OUT<0:15>	265	250
				7	OUT <0:13>	303	286
				6	OUT <0:11>	354	334
				5	OUT <0:9>	424	400
				4	OUT <0:7>	530	500
				3	OUT <0:5>	707	667
				2	OUT <0:3>	1060	1000
				1	OUT <0:1>	2120	2000
				0	OUT <0>	4240	4000

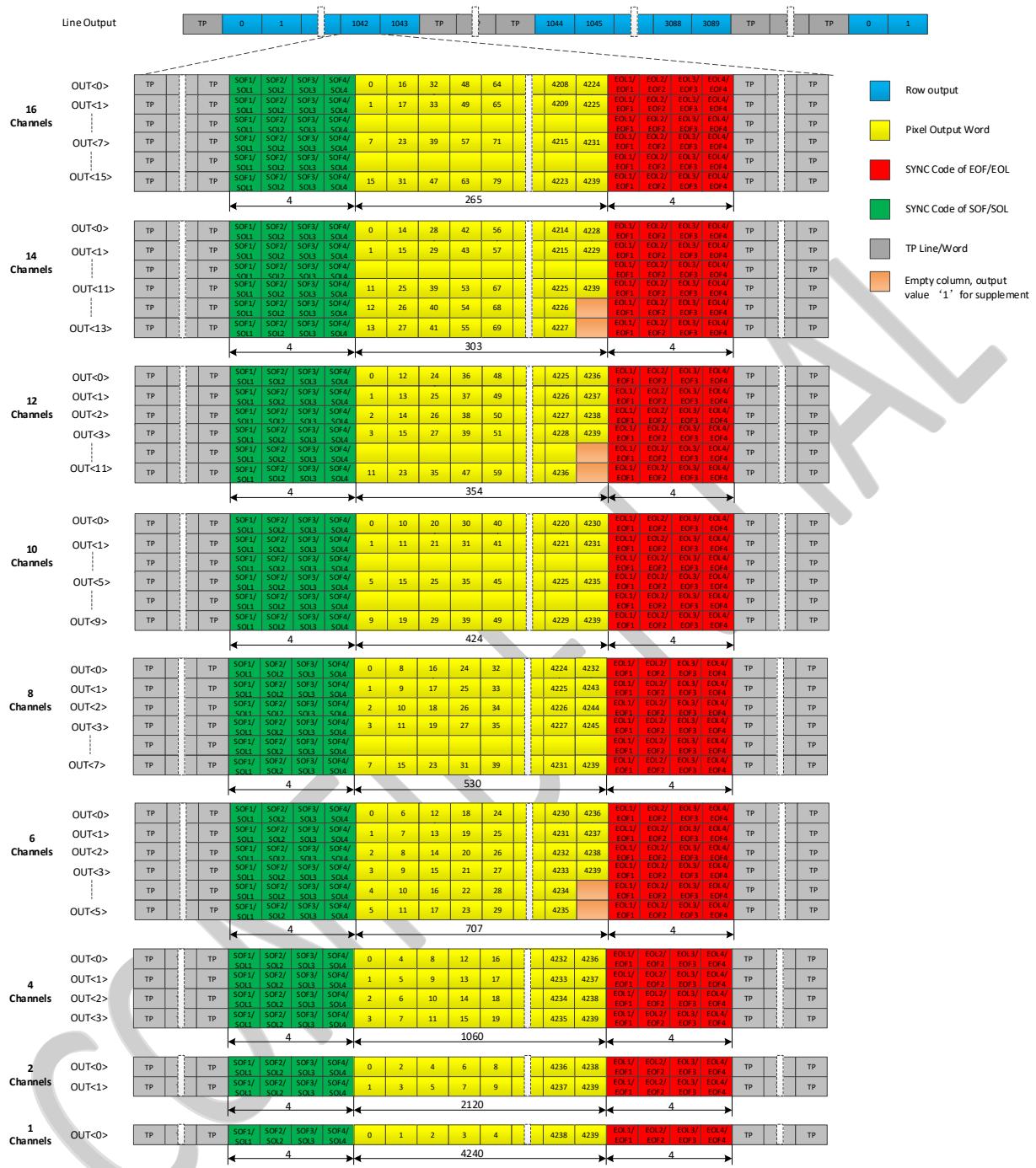


Figure 49 Pixel mapping with channel multiplexing

## MIPI Serial Output

In MIPI output mode, GMAX3412 has 4 lanes for data and 1 lane for clock.

- 4 data lanes
- 1 clock lane

The data lanes are used to transport the 12 bit image data to the receiving end of the surrounding system. The clock lane outputs a Double Data Rate(DDR) clock which can be used at the receiving end to sample the image data. It is synchronous to the data channels with minimum skew.

## Image Data Output Format

The image data output format with 4 lanes output is shown in Figure 50. Blank(B) code is data word based and placed any moment when packet header/footer code and valid data are not output.

In 4lane MIPI output mode, the register HLO\_ORDER listed in Table 37 must be set to 1. See Table 42 for more information of the registers.

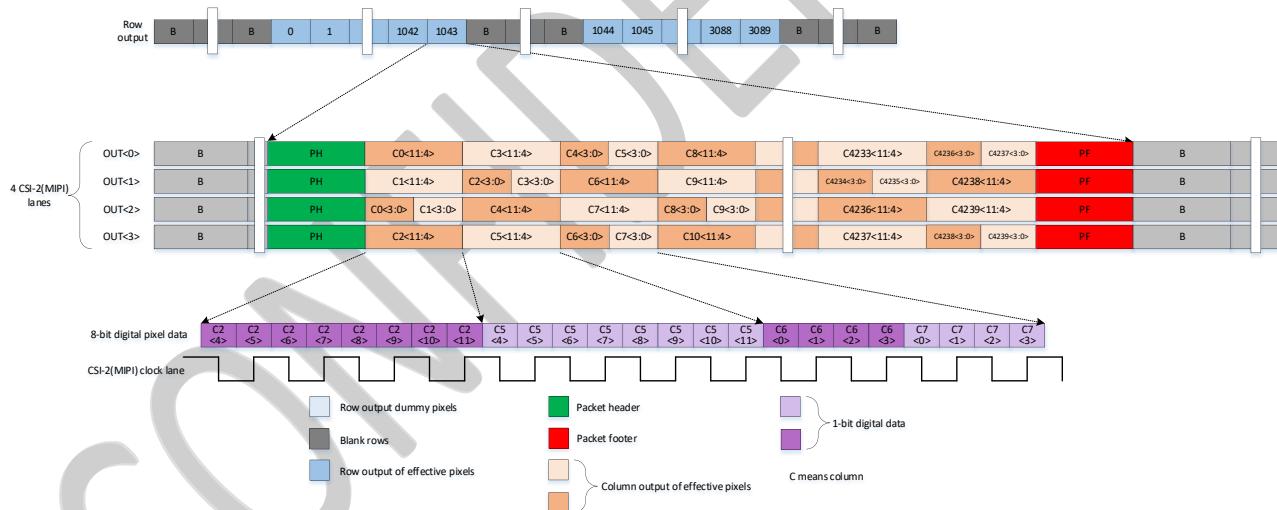


Figure 50: Image data output format of 4lane 12bit(CSI-2 serial output)

Table 42 Register setting for lane number of MIPI mode

Address (hex)		Bit	Name	Description
SPI	I <sup>2</sup> C			
204	3004	1:0	LANE_NUM	3h: 4lane, the minimum value of LINE_TIME is 1066 Others: prohibited
223	3023	7:4	MIPI_CHN_EN	Fh: 4lane Others: prohibited

## Description of Various Functions

### Minimum Exposure

With external exposure, GMAX3412 can be configured to capture image with exposure time smaller than the one specified in section ‘Exposure Time Calculation’. Registers related are listed in Table 43. The delay for exposure start will be 32  $T_{CLK\_PIX}$ , and for exposure end is 2  $T_{CLK\_PIX}$ . Triggering is only allowed when sensor is in IDLE state. The sensor enters FOT state right after detecting the falling edge of TEXP1 pulse.

Table 43 Register setting for working with minimum exposure

Address (hex)		Bit	Name	Description
SPI	I <sup>2</sup> C			
4	2E04	0	MIN_EXP_EN	0: Disable minimum exposure mode 1: Enable minimum exposure mode
3	2E03	0	INT_EXP_EN	0: External exposure 1: Internal exposure
54:51	2E54:2E51	all	MIN_EXP_TIMING	FFFFFFFh: minimum exposure mode Default: others

For minimum exposure, the exposure time is calculated by:

$$T_{EXP,MIN} = T_{FR\_W} - 30 \times T_{CLK\_PIX}$$

With  $T_{FR\_W}$  is the pulse width of TEXP1, which should be larger than  $(6.5\mu s + 30 \times T_{CLK\_PIX})$  in minimum exposure mode.

### Pins for Status Monitoring

In monitoring mode, set SDO\_TDIG\_SEL in Table 19 to 1. Then SDO\_TDIG (pin-M3) can be used to monitor the sensor status. User needs to set the correct registers for status monitoring.

Table 44 Register setting for status monitoring with digital output pins

Address (hex)		Bit	Name	Description
SPI	I <sup>2</sup> C			
47	2E47	all	TDIG	6: FOT 45: State'0' Others: N/A

## Gain Adjustment

### Digital Gain

The digital gain (GDIG) is set with the 2-bit coarse gain (DIG\_GAIN\_C\_\*) and 4-bit fine gain (DIG\_GAIN\_F\_\*) registers, expressed as:

$$GDIG = (2^{DIG\_GAIN\_C\_*}) \times (1 + DIG\_GAIN\_F\_*/16)$$

Figure 51 shows the possible gain steps.

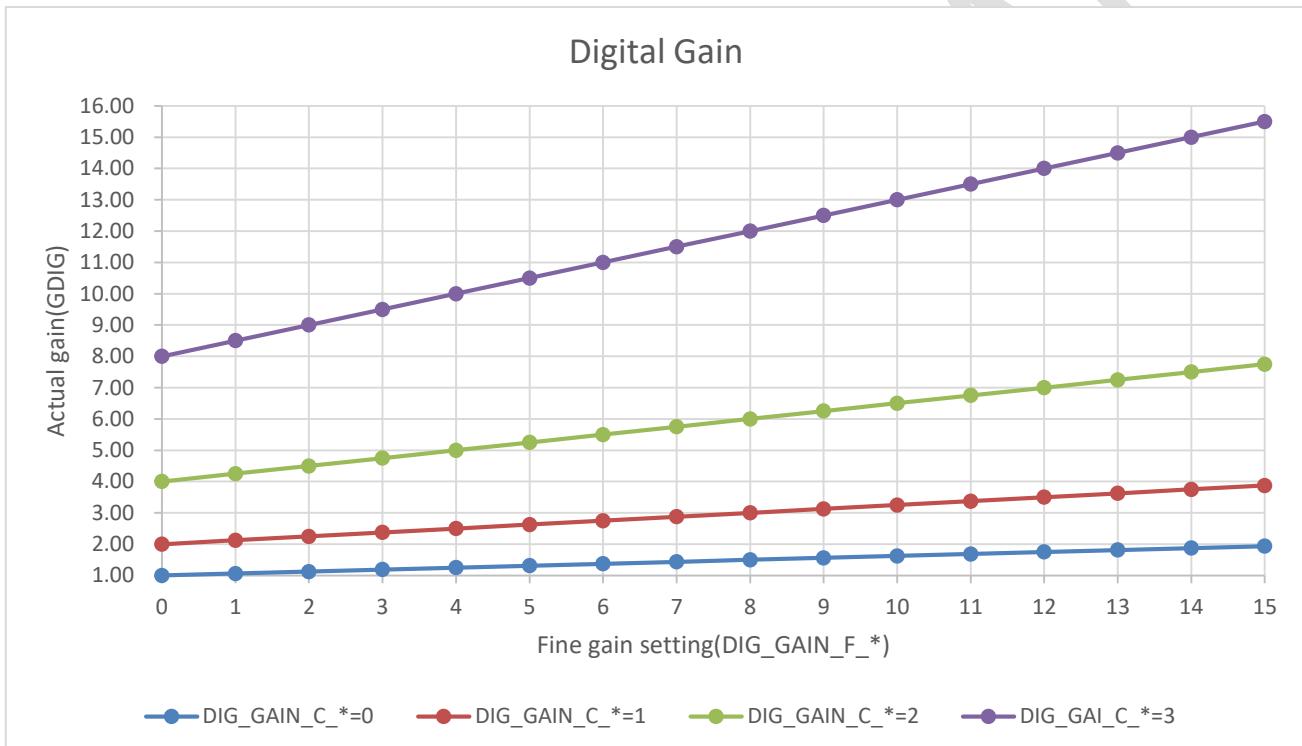


Figure 51: Digital gain setting

Table 45 Register for digital gain setting in GMAX3412

Address (hex)		Bit	Name	Description
SPI	I <sup>2</sup> C			
A04	3804	3:0	DIG_GAIN_F_EVEN	Digital fine gain adjustment for even column
A04	3804	5:4	DIG_GAIN_C_EVEN	Digital coarse gain adjustment for even column
904	3704	3:0	DIG_GAIN_F_ODD	Digital fine gain adjustment for odd column
904	3704	5:4	DIG_GAIN_C_ODD	Digital coarse gain adjustment for odd column

## PGA Gain

The PGA gain of the sensor can be adjusted by the register PGA\_GAIN. More information for the register is shown in Table 46. Table 47 gives commonly used PGA gain value and register value.

Table 46 Register for PGA gain setting in GMAX3412

Address (hex)		Bit	Name	Description	
SPI	I <sup>2</sup> C				
AE	2EAE	5:0	PGA_GAIN	PGA gain setting	

Table 47 Mapping of PGA gain and register value

Register value(hex)	Gain (dec)	Gain (dB)	Register value(hex)	Gain (dec)	Gain (dB)
3B	17.59	24.91	26	2.50	7.96
3A	14.42	23.18	25	2.36	7.46
39	12.19	21.72	24	2.24	7.00
38	10.53	20.45	23	2.13	6.57
37	9.27	19.34	22	2.03	6.15
36	8.20	18.28	21	1.93	5.71
35	7.38	17.36	20	1.85	5.34
34	6.67	16.48	1F	1.75	4.86
33	6.10	15.71	1E	1.67	4.45
32	5.58	14.93	1D	1.60	4.08
31	5.16	14.25	1C	1.53	3.69
30	4.74	13.52	1B	1.47	3.35
2F	4.40	12.87	1A	1.39	2.86
2E	4.10	12.26	19	1.33	2.48
2D	3.77	11.53	18	1.27	2.08
2C	3.53	10.96	17	1.22	1.73
2B	3.32	10.42	16	1.17	1.36
2A	3.11	9.86	15	1.12	0.98
29	2.95	9.40	14	1.07	0.59
28	2.78	8.88	13	1.03	0.26
27	2.64	8.43	12	1.00	0.00

**Note:**

- 1) In 12bit sub\_LVDS and 12bit MIPI mode, x1 to x17.59 PGA gain are supported.
- 2) In 10bit sub\_LVDS mode, x1 to x2.03 PGA gain are supported.

## Image Flipping

### Horizontal

GMAX3412 supports image flipping horizontally as shown in Figure 52. Please note that when register FLIP\_H as listed in Table 48 is enabled, the pixel mapping needs to be adapted as well. Figure 53 and Figure 54 give an example of pixel mapping when FLIP\_H is enabled in sub-LVDS output mode and MIPI output mode respectively.

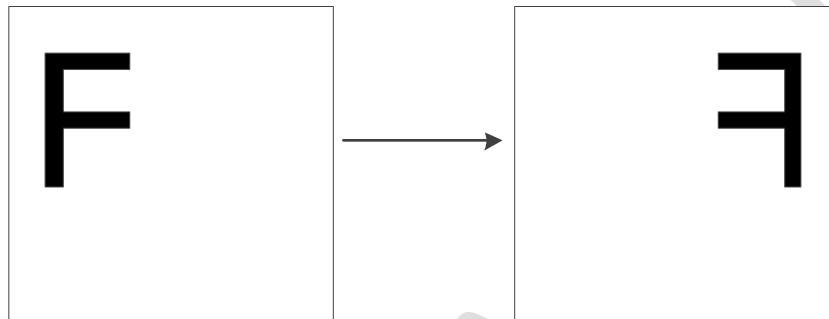


Figure 52 Image horizontal flipping

Table 48 Registers for image horizontal flipping

Address (hex)		Bit	Name	Description
SPI	I <sup>2</sup> C			
700	3500	0	FLIP_H	0: Disable image horizontal flipping 1: Enable image horizontal flipping

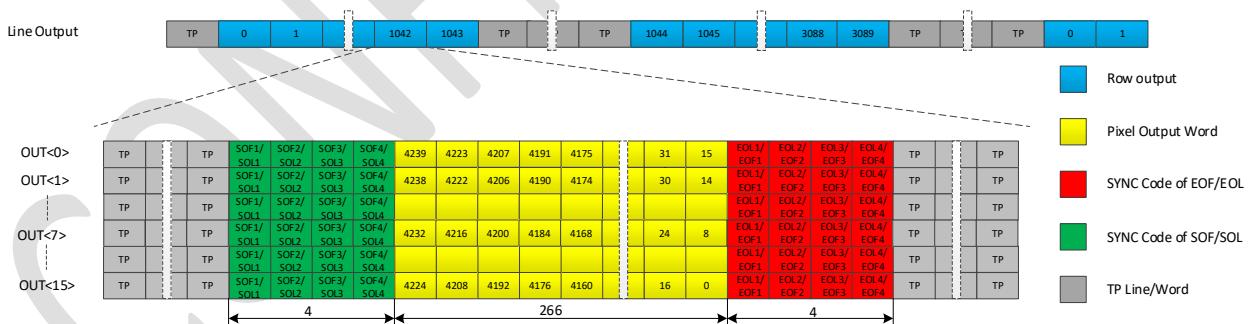


Figure 53 Pixel mapping when horizontal flipping is enabled in 16-channel sub-LVDS

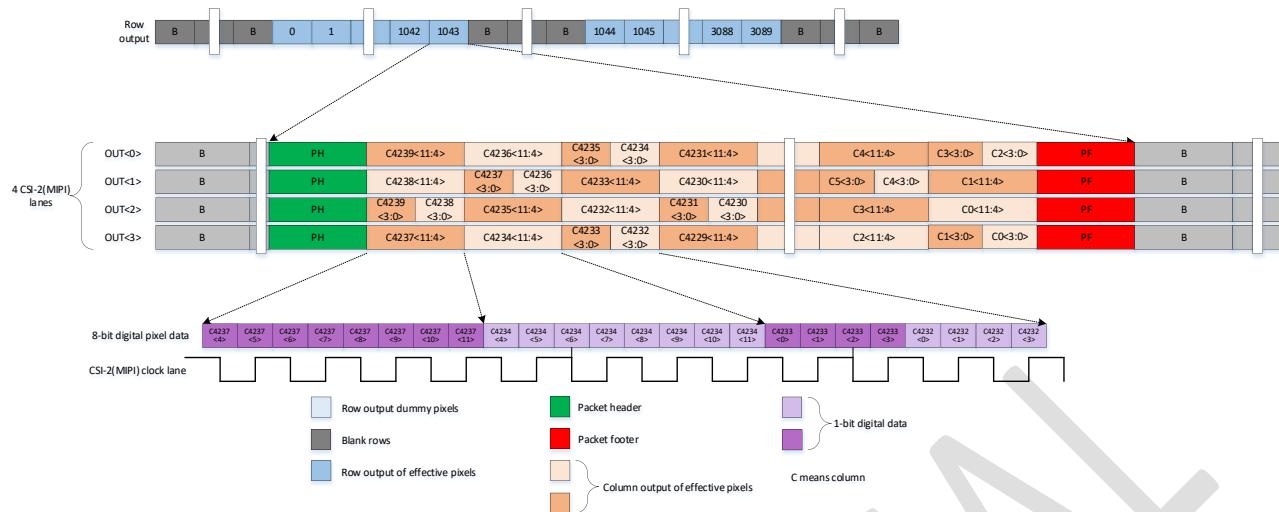


Figure 54 Pixel mapping when horizontal flipping is enabled in 4-lane MIPI

## Vertical

Image vertical flipping, as shown in Figure 55, can be enabled through register FLIP\_V.

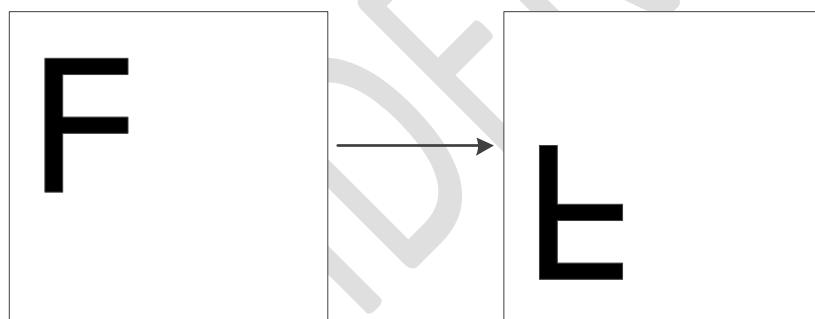


Figure 55 Image vertical flipping

Table 49 Registers for image vertical flipping

Table 10: Registers for Image Vertical Mapping				
Address (hex)		Bit	Name	Description
SPI	I <sup>2</sup> C			
5	2E05	0	FLIP_V	0: Disable image vertical flipping 1: Enable image vertical flipping

## Note:

- 3) Only rows in UD region of pixels can do vertical flipping, refer to Figure 3.

## Black Level

The black level for readout can be tuned by DOFF. The black level offset changes linearly with this number.

Table 50 Registers for dark offset setting of GMAX3412

Address (hex)		Bit	Name	Description
SPI	I <sup>2</sup> C			
907	3707	all	DOFF_ODD	Low sign bit :dark offset tuning for odd column
906	3706	3:0		High sign bit: dark offset tuning for odd column
A07	3807	all	DOFF_EVEN	Low sign bit :dark offset tuning for even column
A06	3806	3:0		High sign bit:dark offset tuning for even column

## Multiple Region HDR

GMAX3412 supports multiple region HDR by allowing two different exposure time for different vertical regions with the unit of 64 rows as shown in Table 51.

Table 51 Registers for multiple region HDR

Address (hex)		Bit	Name	Description
SPI	I <sup>2</sup> C			
B7	2EB7	all	MULTI_REGION<47:0>	For MULTI_REGION<N>, 0≤N≤47, 0: the exposure time of region N is controlled by TEXP1 1: the exposure time of region N is controlled by TEXP2 The address of region N is <64*N : 64*N+63>, except that the address of region 47 is <3008 : 3089>.
B6	2EB6	all		
B5	2EB5	all		
B4	2EB4	all		
B3	2EB3	all		
B2	2EB2	all		
B1	2EB1	0	MULTI_REGION_HDR_EN	0: multiple region function disable 1: multiple region function enable
8	2E08	all	EXPO_F	Fine setting for the long exposure time's rows when MULTI_REGION_HDR_EN=1
B:9	2E0B:2E09	all	EXPO_C	Coarse setting for the long exposure time's rows when MULTI_REGION_HDR_EN=1
C	2E0C	all	EXP1_F	Fine setting for the short exposure time's rows when MULTI_REGION_HDR_EN=1
F:D	2EOF:2E0D	all	EXP1_C	Coarse setting for the short exposure time's rows when MULTI_REGION_HDR_EN=1

In external exposure, the exposure time is set through TEXP1 and TEXP2. As illustrated in Figure 56, the output array is divided into 5 parts with two different exposure time. Each part contains several 64 rows. All the end time of exposure are aligned.

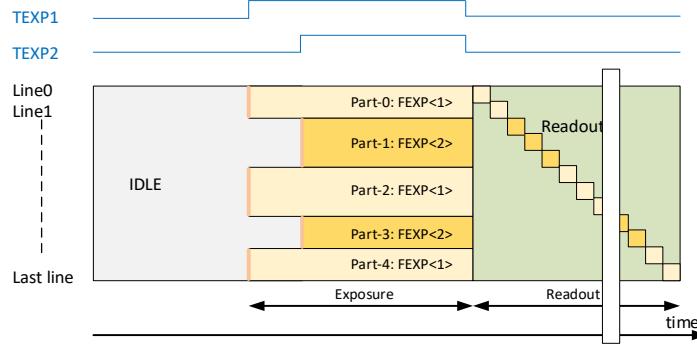


Figure 56 Introduction of multiple exposure HDR operation

**Note:**

- 1) In multiple region HDR mode ,at one frame time, PGA gain is same at all regions.
- 2) Not support multiple slope HDR function in multiple region HDR mode

## Multiple Slope HDR

The GMAX3412 supports multiple slope HDR function and in linear response there will be at most 2 slopes in one frame time. As illustrated in Figure 57, the bright pixel will be held to VGRSTL2 and the time depends on the rising edge of TEXP2 ,it won't be saturated at the end of the exposure. And the dark pixel have a normal response. Thus high dynamic range can be achieved. The placement of the knee-point in X axis depends on VGRSTL and VGRSTL2, the slope of the segments depends on the rising edge of TEXP2. The falling edge of TEXP2 are aligned.

Table 52 lists the registers related to multiple slope HDR for internal exposure mode. In external exposure, total exposure time is set through TEXP1, and knee-point depends on the rising edge of TEXP2.

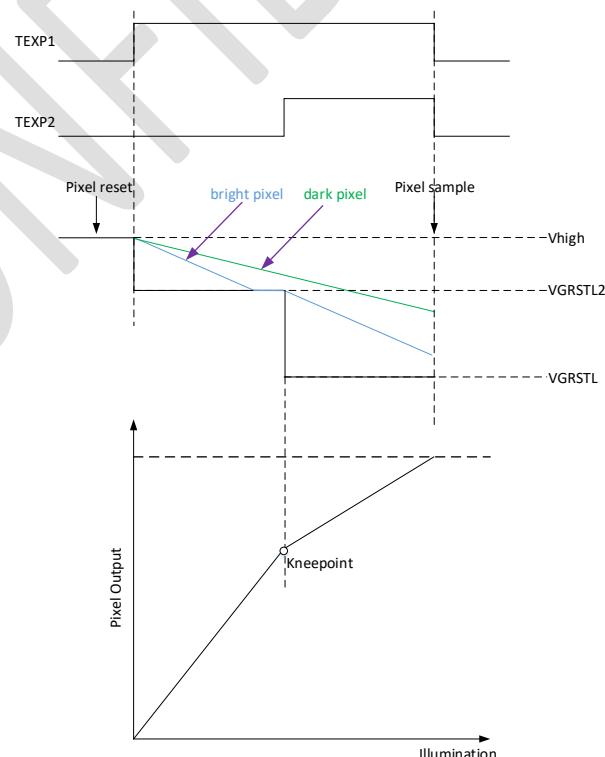


Figure 57 Introduction of multiple slope HDR function

Table 52 Registers for multiple slope

Address (hex)		Bit	Name	Description
SPI	I <sup>2</sup> C			
B8	2EB8	0	MULTI_SLOPE_EN	0: multiple slope function disable 1: multiple slope function enable
44F	324F	5:0	VGRSTL2	50mV per step, VGRSTL2 value decrease with register setting value increasing Default:011011(27):0V
416	3216	5:0	VGRSTL	50mV per step, VGRSTL value decrease with register setting value increasing Default:101000(40):-1.3V
8	2E08	all	EXPO_F	Fine setting for the total exposure time when MULTI_SLOPE_HDR_EN=1
B:9	2E0B:2E09	all	EXPO_C	Coarse setting for the total exposure time when MULTI_SLOPE_HDR_EN=1
C	2E0C	all	EXP1_F	Fine setting from the knee point to the end of exposure when MULTI_SLOPE_HDR_EN=1
F:D	2EOF:2E0D	all	EXP1_C	Coarse setting from the knee point to the end of exposure when MULTI_SLOPE_HDR_EN=1

## Test Image

GMAX3412 can be configured to output a test image for users to debug the surrounding system. The related registers to configure GMAX3412 is described in Table 53. The data of pixel(X, Y) is calculated by:

$$DN_{TI} = (X + Y) \% DN_{MAX}$$

Where  $DN_{MAX}$  is 4096 for 12-bit and 1024 for 10-bit. Output value  $DN_{TI}$  can't be 0 in LVDS mode. The test image is shown in Figure 58.

Table 53 Registers setting for GMAX3412 to output test image

Address (hex)		Bit	Name	Description
SPI	I <sup>2</sup> C			
700	3500	3:1	TEST_IMG_EN	0: Image capture 4: Test image out

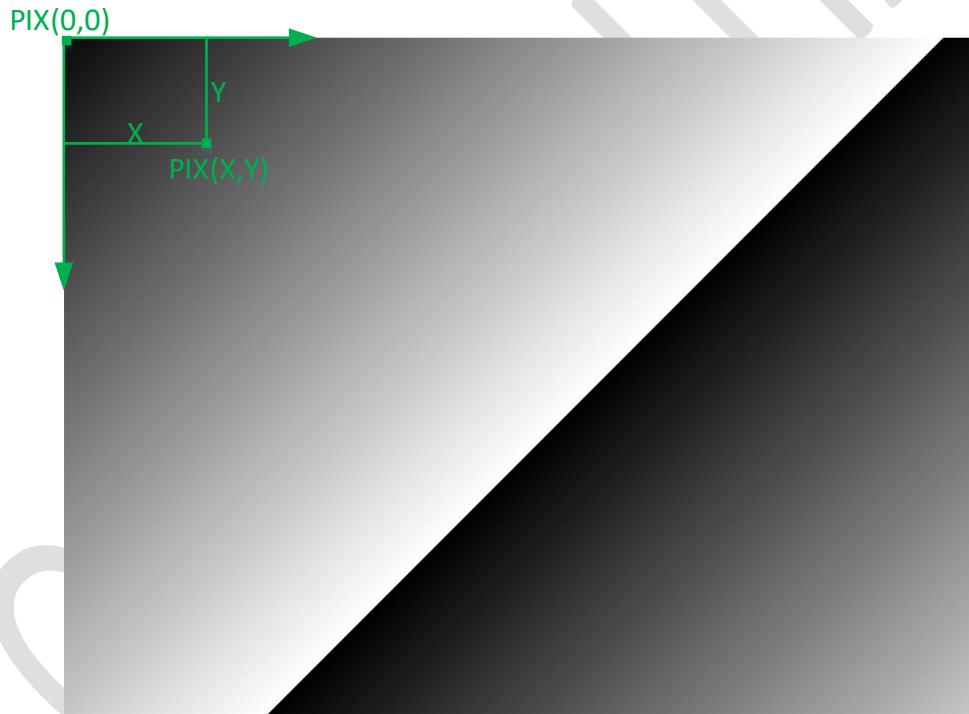


Figure 58 Test image output(12-bit)

## Temperature Readout

The temperature sensor locations on chip are shown in Figure 2.

The readout of digital temperature sensor is through register D\_TEMP. An example for the output of this temperature sensor (DN) versus the chip temperature would be shown in the graph below later. The temperature of the sensor can be obtained by using this fit line.

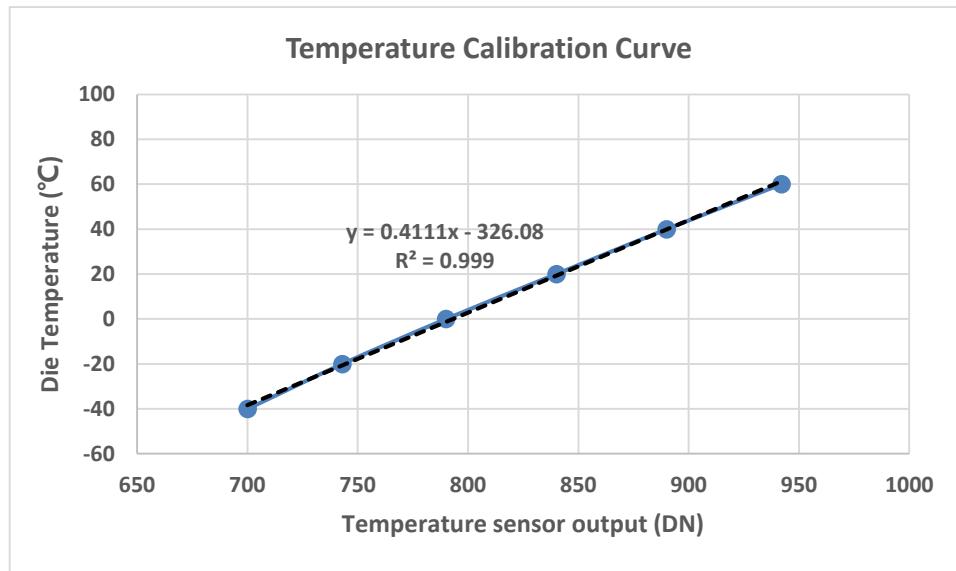


Figure 59 Calibration curve of the digital temperature sensor

### Note:

- 1) The fitting of the temperature output curve may be different from sensor to sensor, the user is advised to make calibration on individual sensor for best accuracy.
- 2) The curve has high correlation with CLK\_PIX frequency(100MHz in default), when a change of CLK\_PIX happens, this curve needs to be re-characterized
- 3) The SPI address of D\_TEMP is H<458:457>, and I<sup>2</sup>C address is H<3258:3257>.

## OTP Memory Readout

### SPI Interface

Reading out the OTP memory data occurs via the SPI interface. Figure 60 shows the single readout timing to read out the OTP memory.

- OTP Readout is initiated by writing the desired OTP address to SPI address 601h.
- Next, reading address 602h sends out the data on the programmed OTP address of the SPI register.
- To jump to another OTP address, a new OTP address has to be uploaded to SPI address 601h.

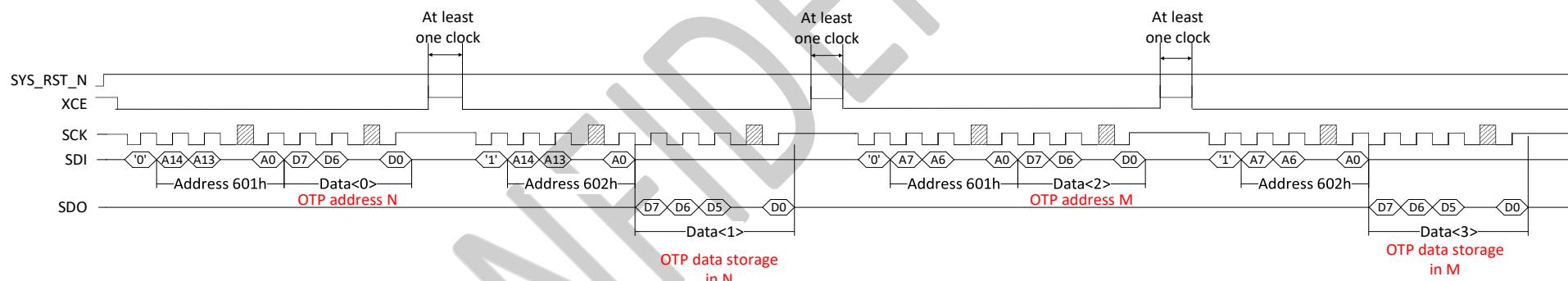


Figure 60 Single readout of OTP data in SPI

It is also possible to sequential readout the memory data. Figure 61 shows the operation timing.

- OTP Readout is initiated by writing the desired OTP address to SPI address 601h.
- Next, reading address 602h sends out the data on the programmed OTP address of the SPI register.
- The following read of address 602h returns the following byte, etc.

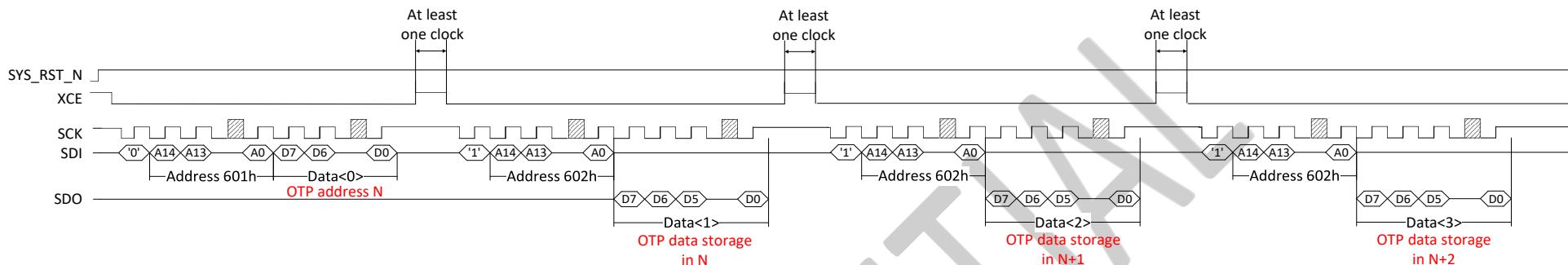
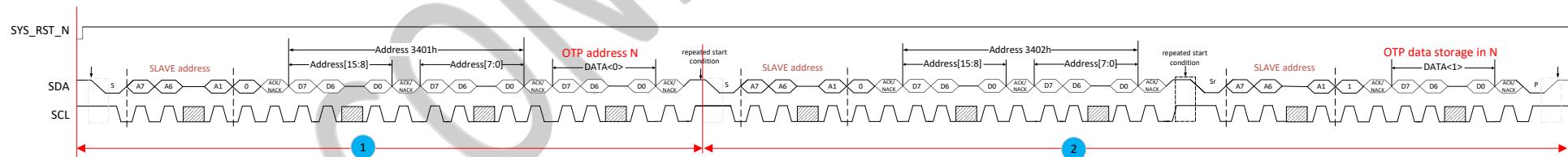


Figure 61 Sequential readout of OTP data in SPI

## I<sup>2</sup>C Interface

Figure 62 shows the readout timing to read out the OTP memory in I<sup>2</sup>C.

- OTP Readout is initiated by writing the desired OTP address to I<sup>2</sup>C address 3401h.
- Next, reading address 3402h sends out the data on the programmed OTP address of the I<sup>2</sup>C register.
- To jump to another OTP address, a new OTP address has to be uploaded to I<sup>2</sup>C address 3401h. Repeat ② in Figure 62 would to sequential readout the memory data.

Figure 62 Readout of OTP data in I<sup>2</sup>C

## OTP Data Description

T.B.D.

CONFIDENTIAL

## Blemish Specification

GMAX3412 sensor outgoing test is performed with the following sensor configuration.

Table 54 Sensor configuration

Test Configuration	Channels	Gain
12-bit sub-LVDS	16 CH	PGA gain x1, digital gain x1
10-bit sub-LVDS	16 CH	PGA gain x1, digital gain x1
12-bit MIPI	4 Lanes	PGA gain x1, digital gain x1

GMAX3412 mono sensors' defect limits only apply to Area A of 4096 x 3072 pixel array, color sensors' defect limits only apply to Area B of 4036 x 3012 pixel array.

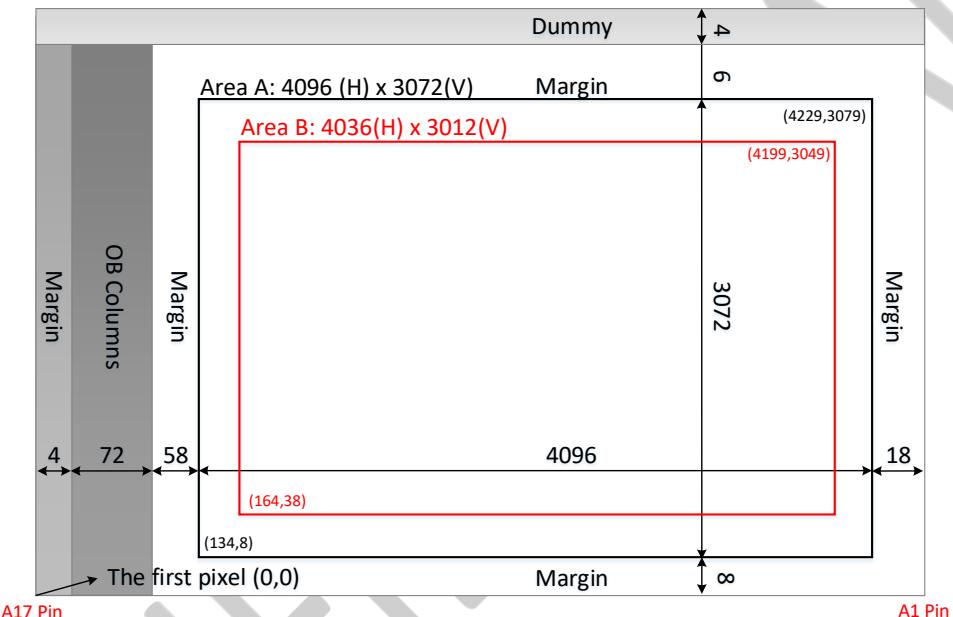


Figure 63 Defect controlled area

## Test images

Test images as listed in Table 2 are grabbed with GMAX3412 final tester at room temperature, under the illumination of a white LED light source with uniformity better than 98% across the image area, and the F number is 16.

Table 55 Test image Definition

Test Images	Description
Dark	2 images grabbed at shortest integration time in dark environment; Per pixel average is performed on these images to form the test image.
Grey	2 images grabbed at a typical integration time (T) to reach half-saturation in light environment; Per pixel average is performed on these images to form the test image.
Saturation	2 images grabbed at an integration time of 2 x T in light environment; Per pixel average is performed on these images to form the test image.

## Defect definitions

Table 56 Defect definitions

Defect Name	Description
Bad pixel in Dark image	Any pixel deviates more than +/-5% of the full swing <sup>(1)</sup> from the mean value of the Dark image.
Bad pixel in Grey image	Any pixel deviates more than +/-20% from the mean value of the Grey image.
Bad pixel in Saturation image	Any pixel deviates more than -20% from the mean value of the Saturation image.
Total defect pixels	The total number of non-overlapping bad pixels in Dark, Grey and Saturation image.
Cluster	Horizontal and vertical consecutive defect pixels are considered as a cluster.
Cluster (N)	Any cluster with size of N defect pixels is considered as cluster (N). For color sensors, the rule is applied within each color plane (R, Gr, B, Gb).
Defect Row/Column	Any row/column with its mean value deviating more than +/-3% of the full swing <sup>(1)</sup> from the mean value of the Dark image. Any row/column with its mean value deviating more than +/-5% from the mean value of the Grey image. Any row/column with its mean value deviating more than -5% from the mean value of the Saturation image. Or a row/column with more than 100 defect pixels.

<sup>(1)</sup> Swing is equal to the difference between the mean value of the Saturation image and the mean value of the Dark image.

## Defect limits

Maximum allowed defect numbers are indicated below.

Table 57 Defect limits

Item	Demo grade
Maximum # of defect pixels	720
Maximum # of defect row and column	0
Maximum # of Clusters ≥ size 4	0

## Storage Condition, Handling and Soldering

T.B.D.

CONFIDENTIAL

## Product Ordering Information

Part number	Blemish Grade	Chroma	Description	Marking Code
GMAX3412-AVM-NLV-BUD	Demo grade	Mono	Micro-lens, ceramic 176 pins LGA, Sealed D263T glass with AR coating. 128 fps @ 10bit 16 x Sub-LVDS 60 fps @ 12bit 16 x Sub-LVDS 30 fps @ 12bit 4 x MIPI	GMAX3412-AM
GMAX3412-AVC-NLV-BUD	Demo grade	Bayer RGB		GMAX3412-AC

## Packing and Tray Specification

T.B.D.

CONFIDENTIAL

## Rights

Gpixel reserves the right to change any information contained herein without notice.

CONFIDENTIAL

## For More Information

For additional information please visit [www.gpixel.com](http://www.gpixel.com) or contact us at [info@gpixel.com](mailto:info@gpixel.com).

For technical support, please contact [support@gpixel.com](mailto:support@gpixel.com).

For RMA, please contact [RMA@gpixel.com](mailto:RMA@gpixel.com).

### Gpixel Microelectronics Inc.

Building #5, Optoelectronic  
Information Industrial Park,  
#7691 Ziyu Road, Changchun,  
Jilin, China.

TEL. +86-431-85077785

### Gpixel Microelectronics Hangzhou Inc.

Room 3101-3109, 31 / F, Huaye  
Development Center, No. 599,  
Jianye Road, Binjiang District,  
Hangzhou China.

TEL.+86-571-87718606-888

### Gpixel NV

Copernicuslaan 60,  
2018 Antwerp, Belgium

TEL. +32-33034442

### Gpixel Japan Co., Ltd.

4<sup>th</sup> floor, 2-4-32 Aomi,  
Kotoku, Tokyo, 135-  
0064, Japan

TEL. +81-03-5962-1600