GMAX3412 FPGA Driver Code User Guide

V0.1

Change record

Version	Date (dd/mm/yyyy)	Comment
V0.1	13/10/2023	The first release

Content

1 Introduction

1.1 Overview

In order to support user design, the GMAX3412 sensor driver code in evaluation kit FPGA is provided for free. It is only used as a design reference or testing purposes and Gpixel assumes no responsibility for any damages resulting from the use of this code for purposes other than those stated.

Please refer to the GMAX3412 datasheet for detailed sensor's design requirements.

The sensor driver code includes clocking, initialization logic, SPI, exposure control, and LVDS receiver. And is designed based on Xilinx XCAU10P FPGA. Please note that the driver code not support as follows:

- MIPI interface.
- Channel multiplexing, only support 16 pairs of sub-LVDS.
- Internal exposure control. Only use the external exposure control.
- I2C interface

1.2 Resource Utilization

The resource utilization of driver code as follows.

Table 1 resource utilization

Name	Ultization
LUT	4421
LUTRAM	388
FF	4524
BUFG	9
PLL	1

2 Architecture

2.1 Architecture

The basic overview of gmax3412_sensor_driver is provided in Figure 1. The driver consists of the following parts:

- Clocking: the clocking module is used to generate all clocks within the driver and clk_ref (the sensor input clock).
- controller module: the controller implements the initialization of the sensor, including power-on, read OTP, config the sensor registers. After initialization, it dynamically detects external parameter changes to perform the related actions.
- spi module: the module is used to access the sensor registers with SPI interface.
- trigger module: generate the texp signal to control the sensor exposure.
- image receiver module: receive the image data from 16 pairs of SubLVDS signals. Including serdes, training, sync code detection, etc.

Note: Sub-LVDS output mode only support LSB output first

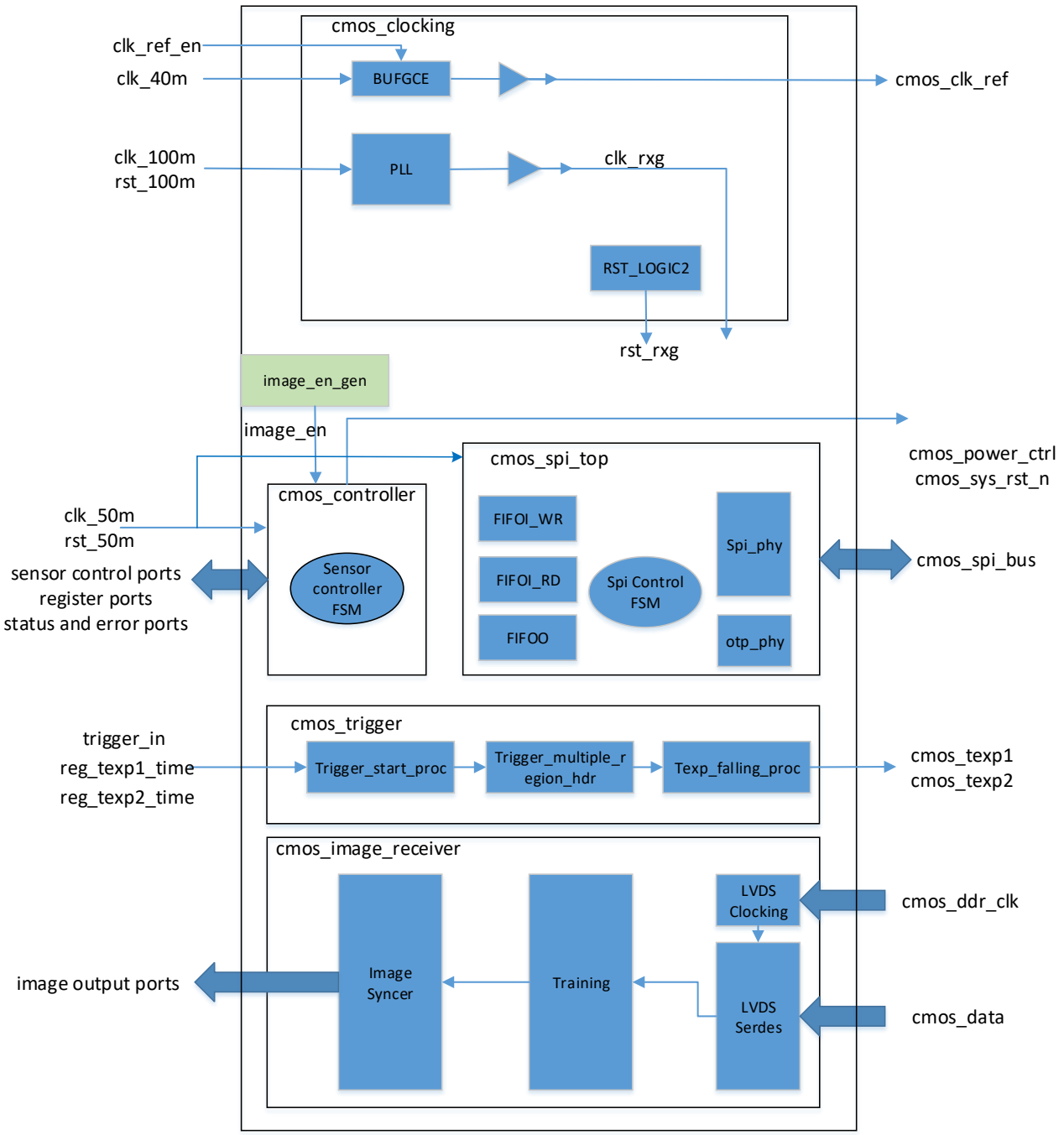

Figure 1 gmax3412_sensor_driver architecture

2.2 Parameter and Ports

The parameters and ports of the top module are described in Table 2 and Table 3.

Table 2 the parameters of the top module

No.	Name	Value	Description
1.	PWR_RAIL_NUM	4	don't change
2.	DATA_CHAN_NUM	16	don't change
3.	CLK_CHAN_NUM	2	don't change

4.	LT_PORT_WIDTH	16	don't change
5.	PG_PORT_WIDTH	6	don't change
6.	DGC_PORT_WIDTH	2	don't change
7.	DGF_PORT_WIDTH	4	don't change
8.	BL_PORT_WIDTH	12	don't change
9.	CHN_PORT_WIDTH	4	don't change
10.	WINL_PORT_WIDTH	16	don't change
11.	WINS_PORT_WIDTH	16	don't change
12.	WINS_X_PORT_WIDTH	13	don't change
13.	WINL_X_PORT_WIDTH	13	don't change
14.	TIMER_1MS	50000	don't change
15.	DATAIN_SWAP	16'b1010_1000_0001_0010	LVDS data swap: 1 is swapped and 0 is not swapped. bit[0] indicates the cmos_data_p/n[0]

Table 3 gmax3412_sensor_driver ports

No.	Name	Width	IO	Description
1.	clk_100m	1	I	Fixed 100MHz clock input
2.	rst_100m	1	I	sync reset with clk_100m, high is valid
3.	clk_40m	1	I	Fixed 40MHz clock input
4.	clk_50m	1	I	Fixed 50MHz clock input
5.	rst_50m	1	I	sync reset with clk_50m, high is valid
6.	cmos_power_ctrl	4	O	control the cmos power-on sequence,Strictly follow the sensor datasheet
7.	lvds_power_ctrl	1	O	0:MIPI 1:LVDS(only support lvds)
8.	cmos_clk_ref	1	O	cmos input clock, the typical value
9.	cmos_sys_rst_n	1	O	cmos system reset signal
10.	cmos_texp1	1	O	cmos external trigger
11.	cmos_texp2	1	O	cmos external trigger
12.	cmos_cci_en	1	O	0:SPI 1:IIC
13.	cmos_spi_csn	1	O	cmos spi communication signal
14.	cmos_spi_sclk	1	O	cmos spi communication signal
15.	cmos_spi_mosi	1	O	cmos spi communication signal
16.	cmos_spi_miso	1	I	cmos spi communication signal
17.	cmos_ddr_clk_p	2	I	clk_ddr_p
18.	cmos_ddr_clk_n	2	I	clk_ddr_n
19.	cmos_data_p	16	I	lvds_data_p
20.	cmos_data_n	16	I	lvds_data_n
21.	cmd_cmos_power_up	1	I	cmos power-up command,rising edge is valid
22.	cmos_power_up_done	1	O	pulled high after output power-on sequence
23.	cmd_rd_otp_done	1	O	read cmos otp complete signal,1:otp data effect
24.	otp_data	240	O	otp data

25.	cmd_cmos_init	1	I	registers initialization command
26.	cmos_init_done	1	O	after training pulled high
27.	cmd_cmos_reset	1	I	cmos reset command, rising edge is valid. Not debugged
28.	cmos_reset_done	1	O	cmos reset complete signal,pulled high after cmos reset
29.	cmd_cmos_power_off	1	I	cmos power_off command,rising edge is valid Not debugged
30.	cmos_power_off_done	1	O	cmos power_off complete signal,pulled high after cmos power_off
31.	acquisition_start	1	I	acquisition_start, rising edge is valid. The high pulse must more than 200ns
32.	acquisition_stop	1	I	acquisition_stop, risign edge is valid. The high pulse must more than 200ns
33.	pll_div_in	4	I	0(Fixed value)
34.	pll_mult	7	I	30(Fixed value)
35.	pll_div_out	2	I	0(Fixed value)
36.	reg_line_time	16	I	line time,step size is clk_pix
37.	reg_fot_time	32	I	step size is clk_50m
38.	reg_pga_gain	4	I	PGA gain setting;
39.	reg_digtal_gain_fine_even	4	I	When disable digital gain must be 0 ; when using digital gain step is 0.0625
40.	reg_digtal_gain_coarse_even	2	I	When disable digital gain must be 0 ; 2'd0 is prohibited when using digital gain,step is 2^N
41.	reg_digtal_gain_fine_odd	4	I	When disable digital gain must be 0 ; when using digital gain step is 0.0625
42.	reg_digtal_gain_coarse_odd	2	I	When disable digital gain must be 0 ; 2'd0 is prohibited when using digital gain,step is 2^N
43.	reg_target_black_lvl_even	12	I	dark offset tunning for even column
44.	reg_target_black_lvl_odd	12	I	dark offset tunning for odd column
45.	reg_test_en	3	I	0：image data；4：test image
46.	reg_flip_h	1	I	0：no horizintal flipping；1：horizintal flipping
47.	reg_flip_v	1	I	0：no vertical flipping； 1：enable vertical flipping
48.	reg_bit_width	2	I	0: 12bit; 2: 10bit;
49.	reg_color_en	1	I	0: Mono sensor; 1: Color sensor
50.	reg_min_exp_en	1	I	0: Disable minimum exposure mode; 1: Enable minimum exposure mode
51.	reg_min_exp_pulse	32	I	step size is clk_50m; In minimum exposure mode, TEXP minimum pulse width
52.	reg_multi_region_hdr_en	1	I	0: multiple region function disable1: multiple region function enable

53.	reg_multi_region	48	I	For MULTI_REGION<N>, 0≤N≤47,0: the exposure time of region N is controlled by TEXP1; 1: the exposure time of region N is controlled by TEXP2； The address of region N is <64*N : 64*N+63>
54.	reg_multi_slope_en	1	I	0: multiple slope function disable； 1: multiple slope function enable
55.	reg_texp1_time	32	I	step size is clk_50m;
56.	reg_texp2_time	32	I	step size is clk_50m;
57.	reg_vgrstl2	6	I	50mV per step, VGRST2 value decrease with register setting value increasing. Default:011011(27):0V
58.	reg_vgrstl	6	I	50mV per step, VGRSTL value decrease with register setting value increasing. Default:101000(40):-1.3V
59.	reg_win1_y_s	16	I	Start row address in UD window 1. Should be set between 0 and 3085
60.	reg_win1_y_l	16	I	Number of readout rows in UD window 1
61.	reg_win2_y_s	16	I	Start row address in UD window 2. Should be set between 0 and 3085
62.	reg_win2_y_l	16	I	Number of readout rows in UD window 2
63.	…	16	I	…
64.	…	16	I	…
65.	reg_win8_y_s	16	I	Start row address in UD window8. Should be set between 0 and 3085
66.	reg_win8_y_l	16	I	Number of readout rows in UD window 8
67.	reg_win_x_num	4	I	The front total number of open horizontal windows effective
68.	reg_win_all_len	13	I	the value = reg_win0_x_l + reg_win1_x_l + ... + reg_win7_x_l
69.	reg_win0_x_s	13	I	Start column address in UD window. Only valid when WIN_X_NUM >0,WIN0_X_S value must be even number.Should be set between 0 and 4239
70.	reg_win0_x_l	13	I	Number of readout columns in UD window.Only valid when WIN_X_NUM >0.Should be multiple of 16, minmum WIN0_X_L value is 32.
71.	reg_win1_x_s	13	I	Start column address in UD window. Only valid when WIN_X_NUM >1,WIN0_X_S value must be even number.Should be set between 0 and 4239.
72.	reg_win1_x_l	13	I	Number of readout columns in UD window.Only valid when WIN_X_NUM >1.Should be multiple of 16, minmum WIN0_X_L value is 32.

73.	…	13	I	…
74.	…	13	I	…
75.	reg_win7_x_s	13	I	Start column address in UD window. Only valid when WIN_X_NUM >7,WIN0_X_S value must be even number.Should be set between 0 and 4239
76.	reg_win7_x_l	13	I	Number of readout columns in UD window.Only valid when WIN_X_NUM >7.Should be multiple of 16, minmum WIN0_X_L value is 32.
77.	trigger_in	1	I	system external trigger signal
78.	clk_rxg	1	O	Pixel clock 10bit:120Mhz; 12bit:100Mhz;
79.	rst_rxg	1	O	High is valid
80.	fvalout	1	O	Frame effective signal, high level effective
81.	lvalout	1	O	Line effective signal, high level effective
82.	dataout	192	O	Output image data
83.	spi_wr_error	1	O	Register update error signal 1: error; 0: no error
84.	cmos_init_status	8	O	CMOS initialization status 1:suceess /yes；0：failure/no， bit[0]：cmos power on； bit[1]：release sys_rst_n; bit[2]：cmos init; bit[3]：cmos training done; bit[4]:cmos training success; bit[5]：cmos imaging; bit[7:6]：REV
85.	cmos_digital_temperature	16	O	CMOS temperature, read every 2 seconds, negative numbers displayed with complement, 1 bit/℃
86.	training_result	16	O	0:not started or failed；1：success,bit[0] corresponds channel 0,bit[15]corresponds channel 15
87.	……._r	…	O	Updated register value

3 User Flow

3.1 Initialization

After FPGA's configuration, the control flow as follows. When you detect the cmos_init_done, you can start the acquisition.

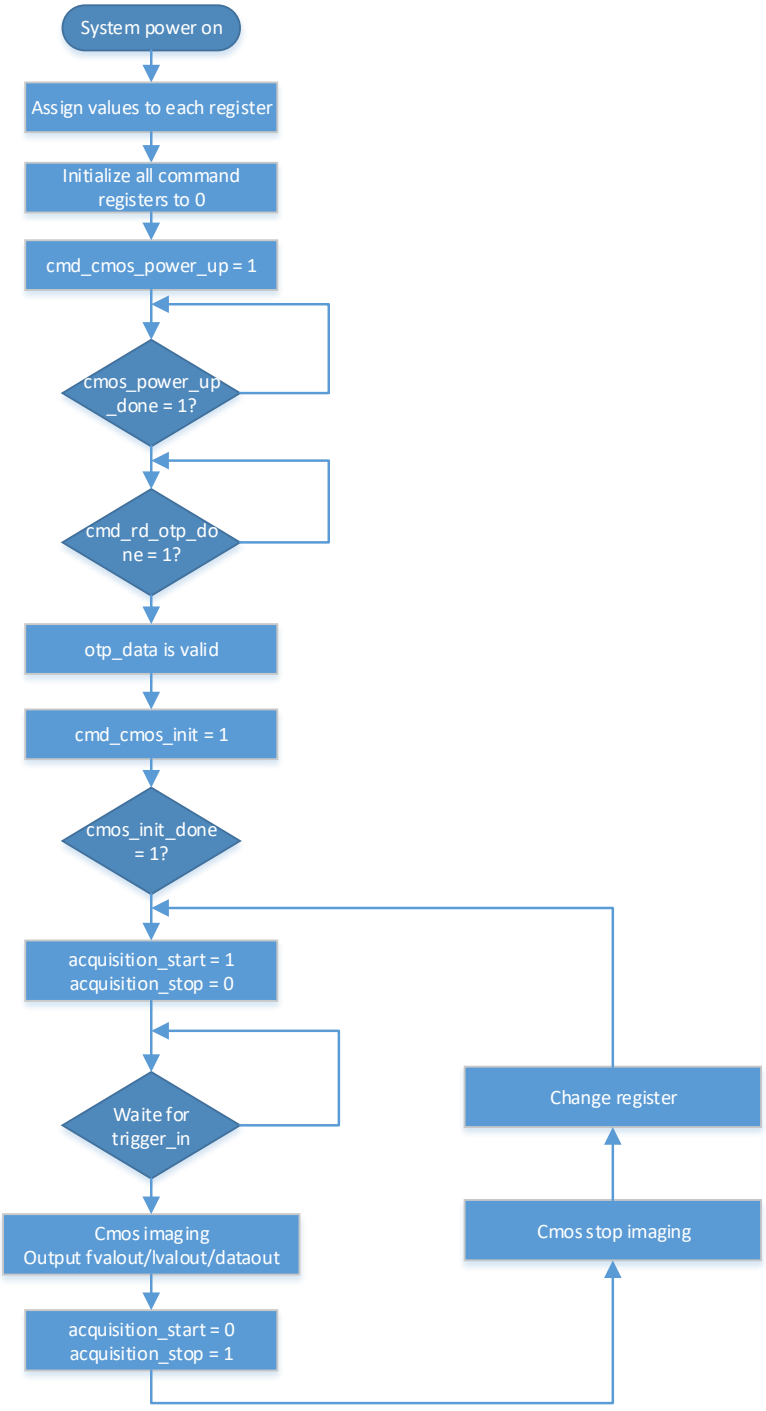

Figure 2 initialization process

Figure 3 shows the recommended initialization process. In order to make the power supply and signals more stable, the interval of each operation is lengthened appropriately, which is different from the datasheet. In applications, you can modify the parameters to change the power-on interval.

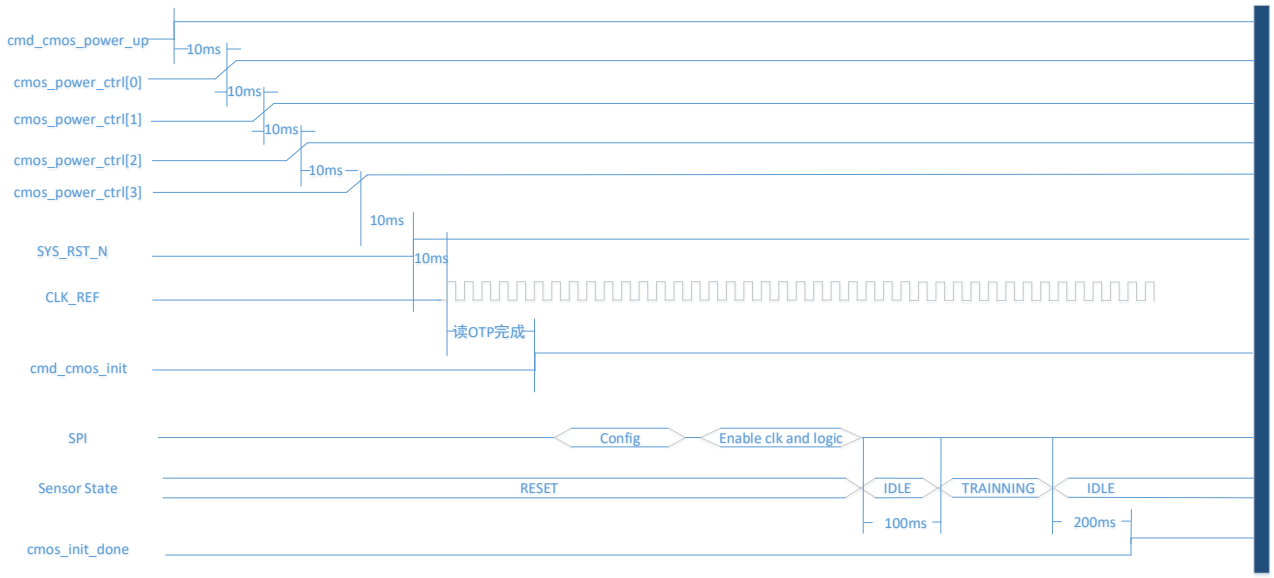

Figure 3 initialization process

3.2 Typical parameter setting

3.2.1 ROI

Table 4 ROI parameter

Vertical/horizontal	register	value	actually ROI value (display value)
vertical	reg_win1_y_s	ROI1_OffsetY + 8(no flip_v) ROI1_OffsetY + 6(flip_v)	ROI1_OffsetY
	reg_win1_y__l	ROI1_Height1	ROI1_Height
	reg_win2_y_s	ROI2_OffsetY + 8(no flip_v) ROI2_OffsetY + 6(flip_v)	ROI2_OffsetY
	reg_win2_y_l	ROI2_Height	ROI2_Height
	reg_win3_y_s	ROI3_OffsetY + 8(no flip_v) ROI3_OffsetY + 6(flip_v)	ROI3_OffsetY
	reg_win3_y_l	ROI3_Height	ROI3_Height
	reg_win4_y_s	ROI4_OffsetY + 8(no flip_v) ROI4_OffsetY + 6(flip_v)	ROI4_OffsetY
	reg_win4_y_l	ROI4_Height	ROI4_Height
	…	…	…
	…	…	…
	reg_win8_y_s	ROI8_OffsetY + 8(no flip_v) ROI8_OffsetY + 6(flip_v)	ROI16_OffsetY
	reg_win8_y_l	ROI8_Height	ROI16_Height
horizontal	reg_win1_x_s	ROI1_OffsetX + 134	ROI1_OffsetX
	reg_win1_x_l	ROI1_ Width 1	ROI1_Width
	reg_win2_x_s	ROI2_OffsetX +134	ROI2_OffsetX
	reg_win2_x_l	ROI2_ Width	ROI2_Width
	reg_win3_x_s	ROI3_Offset X +134	ROI3_OffsetX
	reg_win3_x_l	ROI3_ Width	ROI3_Width
	reg_win4_x_s	ROI4_Offset X +134	ROI4_OffsetY
	reg_win4_x _l	ROI4_ Width	ROI4_ Width
	…	…	…
	…	…	…
	reg_win8_x _s	ROI8_Offset X +134	ROI8_OffsetY
	reg_win8_x _l	ROI8_ Width	ROI8_ Width

3.2.2 Trigger_in

Trigger_in signal is used to control exposure, it is described in the following figure.

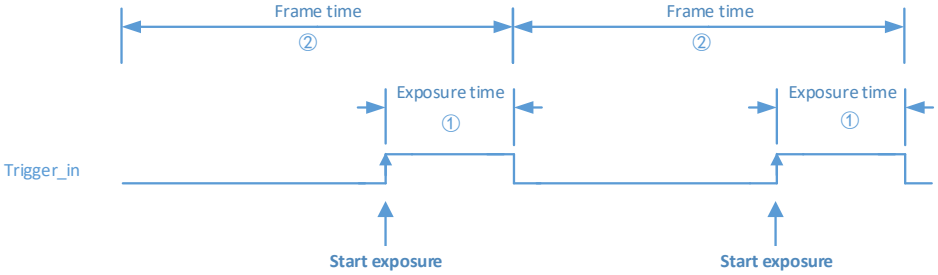

Figure 4 Trigger in signal

3.2.3 Multislope HDR/Multiregion HDR

The following figure is a typical example of Multislope HDR/Multiregion HDR, for reference design.

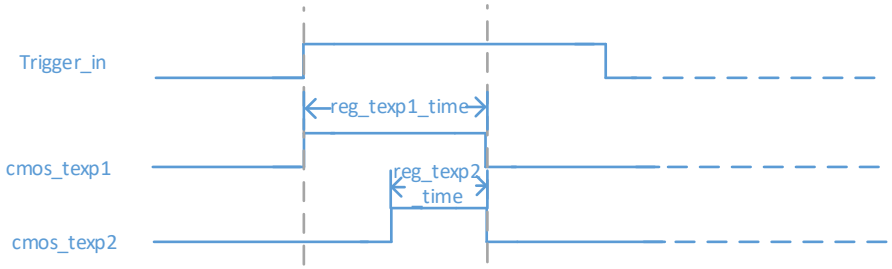

Figure 5 Multislope HDR/Multiregion HDR