NeuroCube: Low-Power Reconfigurable Neuromorphic Architecture Using Hybrid Memory Cube

Abstract

This document serves as a sample for submissions to MICRO 2014. We provide some guidelines that authors should follow when submitting papers to the conference.

1. Introduction

THIS PART IS FOR INTRODUCTION

1. Machine Learning is important application in RMS (Recognition/Mining/Synthesis)

2. However, it's impossible to operate current ML techniques in embedded system due to massive computation

3. As demands for ML in embedded system such as IoT/Mobile platform increases, low-power and high power-efficiency ML is required

4. Therefore, Specific Architecture for ML is required which is better than General Purpose Micro-Arch such as CUDA

5. Deep Learning Network: compsed of multiple different type of NN is powerful tool in ML

6. To operated diff. NNs with single ASIC, Reconfigurbility is important in Neuromorphic Architecture

2. Previous Work

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2.1. Neural network for machine learning

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2.2. Neuromorphic hardware implementation

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3. Reconfigurable Neuromorphic Architecture

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3.1. External memory

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3.2. Cache memory

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3.3. Processing elements

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3.4. Network-on-chip

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References

[1] K. Flautner *et al.*, "MICRO'47 Conference Site," 2014. Available: http://www.microarch.org/micro47/