Signetics

8T380
Bus Receiver

Quad Bus Receiver with Hysteresis-Schmitt Trigger
Product Specification

Logic Products

DESCRIPTION

The 8T380 is a quad 2-input bus receiver with hysteresis for use in I/O, data, and memory busses. Built-in hysteresis provides maximum noise immunity and a power-up or power-down sequence on the receiver will not affect the bus. LOW input current allows several drivers and receivers to communicate over a common bus in "Party line" fashion. The 8T380 is ideal as a Schmitt Trigger in analog interfaces that cannot tolerate the non-linear input impedance characteristics of standard TTL. Further, the LOW input requirements allow the 8T380 to be used as a CMOS to TTL interface. All inputs have clamping diodes to simplify systems design.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
N8T380	20ns (t_{PLH}) 16ns (t_{PHL})	25mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N8T380N
Plastic SO	N8T380D

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Out
L	L	H
L	H	L
H	L	L
H	H	L

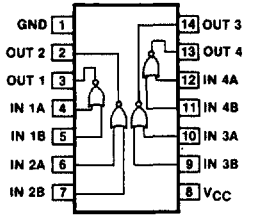
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

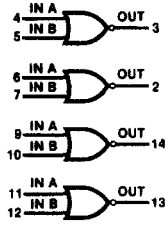
PINS	DESCRIPTION	8T
All	Input	1.2ul
All	Output	10ul

NOTE:
A unit load (ul) is 40μA I_{IH} and −1.6mA I_{IL}.

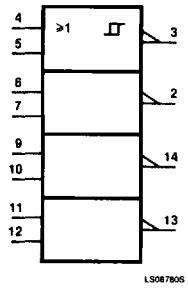
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		8T	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	V
I_{OL}	Continuous	30	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		8T			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0		2.5	V
V_{IL}	LOW-level input voltage	1.1		1.5	V
I_{IK}	Input clamp current			−12	mA
I_{OH}	HIGH-level output current			−400	μA
I_{OL}	LOW-level output current			16	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

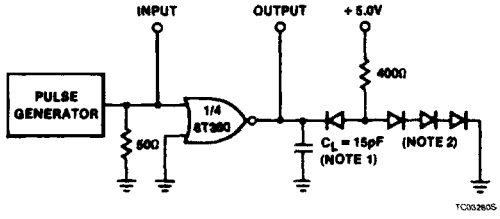
PARAMETER		TEST CONDITIONS[1]	8T380		UNIT
			Min	Max	
V_{IH}	Input HIGH voltage	Guaranteed input HIGH threshold voltage	2.0	2.5	V
V_{IL}	Input LOW voltage	Guaranteed input LOW threshold voltage	1.1	1.5	V
V_{IK}	Input clamp diode voltage	V_{CC} = MIN, I_{IK} = −12mA		−1.5	V
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, I_{OH} = −400μA	2.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, I_{OL} = 16mA		0.4	V
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 4.5V		50	μA
		V_{CC} = 0V, V_I = 4.5V		50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0V		−25	μA
I_{OS}	Short-circuit output current[2]	V_{CC} = MAX	−18	−55	mA
I_{CC}	Supply current (total)	V_{CC} = 5.25V		40	mA

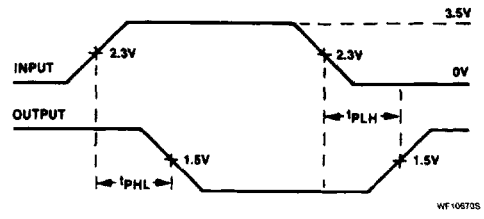
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	8T		UNIT
			C_L = 15pF, R_L = 400Ω		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Input to output	See Test Circuits and Waveforms		35 35	ns

TEST CIRCUITS AND WAVEFORMS





NOTES:
1. Including probe and jig capacitance
2. All diodes are 1N3064
3. Pulse generator characteristics

P.A. = 3.5V
Z_{OUT} = 50Ω
P_{RR} = 1MHz
$t_r = t_f \leq$ 10ns (10% to 90%)
Duty Cycle = 50%

TYPICAL APPLICATIONS

A generalized "Party Line" bus interface is shown in Figure 1. Each driver/receiver combination can communcicate with any other pair of all. Open collector NAND Gates such as the Signetics 7439 have adequate driver capability for the bus terminations as well as 20 driver/receiver pairs. In addition the bussing scheme is non-inverting as shown and bus drivers are activated by a logic "1" whereas bus receivers are activated by a Logic "0."

Each termination consisting of a 180Ω resistor to V_{CC} and 390Ω to ground is a 120Ω Thevenin's equivalent circuit. The maximum length of cable that can be driven is a complex relationship involving the type of cable used as well as the distribution of drivers and receivers on the bus. Using flat ribbon cable, a maximum reasonable length is 50 ft. minus the combined length of all taps or stubs.

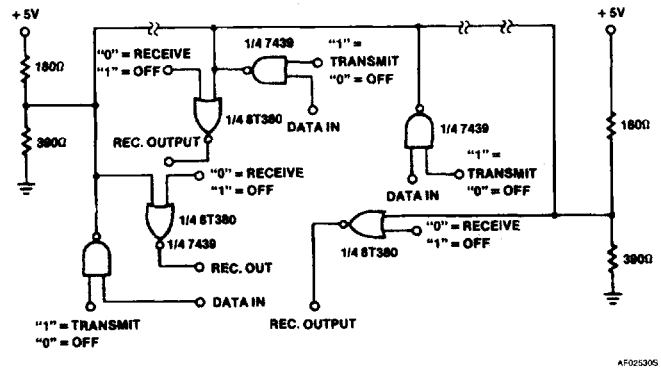


Figure 1

SCHMITT TRIGGER

The receiver transfer curve shown in Figure 2a makes the 8T380 ideal in a variety of Schmitt Trigger and waveshaping applications such as Figure 2b.

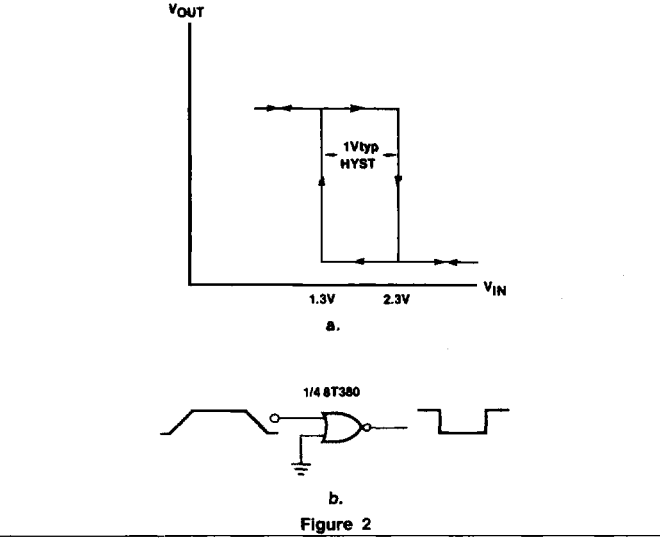


Figure 2

MOS/CMOS INTERFACE

The input current which is only 50μA MAX in the logical "1" state and no current in the logical "0" state marks the 8T380 an ideal MOS/CMOS interface element.

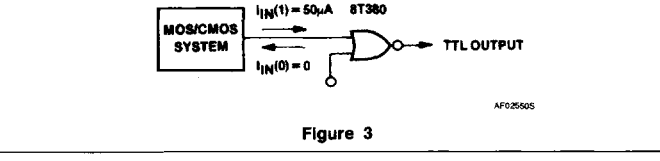


Figure 3

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