**Follow-up questions from 1st session; class to answer/discuss:**

1. For equity order books: what is a best practice: build in FPGA or build with overclocked servers? Why?
2. Would 5 million FPGA gates (up from 2 or 3 million) benefit equity order book builds?
3. What are benefits of Intel core – FPGA cache coherency?
4. Please define what Corvil describes as “Speed II” or “Meta-Speed”.
5. Why does Corvil state that Meta-Speed is more important today than pure raw speed?
6. What are 2 drivers for trading firms to architect for less latency jitter and more deterministic latencies?
7. What are common inputs to real time Alpha seeking strategies?
8. Why are more firms conducting Transaction Cost Analyis (TCA) I real time?
9. For Machine Learning (ML) / Neural Networks (NN): describe difference between “trained” and “test” data.
10. True/False: Layer 1 switches inspect packets.
11. True/False: Corvil only provides network analytics
12. True/False: FPGA’s can complete Monte Carlo risk/price analysis faster than GPU’s
13. How many times faster is a SuperMicro overclocked server core than an FPGA core?
14. How many levels of parallelization must FPGA’s achieve in order to match performance of overclocked servers?
15. Why do overclocked servers experience periodic latency jitter, while FPGA’s do not?
16. Please describe how Metamako Meta-Mux switch order aggregation works for routing orders to exchanges in CoLo.
17. Describe a “partial” FPGA solution for Electronic Trading (ET).
18. Describe how xCelor new Layer5 switch works.
19. Describe Algo-Logic’s TCP EndPoint
20. For which market data feed does Algo-Logic build FPGA based Feed Handlers (FH), order books, and order flow.
21. What FPGA vendor has complete FH, order book, order-flow infrastructure solution? For how many feeds? What vendor(s) can it partner for a complete solution for all FH’s?
22. Describe a hedge fund’s trader ecosystem.
23. Describe a market maker’s trader ecosystem.
24. What real time metrics are critical to guide a market maker’s order flow decisions and hence profitability.
25. True/False: Fixnetics cache coherency is between a core on one socket and an FPGA on another socket
26. True/False: Wall Street IT analysts have high confidence in Intel doubling speed of their CPU cores process speeds over next 2-3 years.
27. How do Metamako and Fixnetics partner?
28. Which programming tool (Verilog or OpenCL) allow programmers to map FPGA bit registers within their programming “modules” or “classes”.
29. What electronic trading organizations will prosper in space of ULL ET now & in future? Which may very well fail, even disappear? Why is role of ROI critical?
30. Why is it difficult to conduct proper and accurate projections of ROI on future infrastructure investments?
31. What are the key advantages of FPGA’s for ET? What are FPGA pitfalls? How are they being addressed or mitigated?

\*\*\*\* Also – please send in Homework #1 via email before Tuesday June 6:

As mentioned at end of class yesterday, this should be a proposed “pilot” in CoLo for an exec broker to quickly test a partial FPGA solution ….. before assessing plans to further implement more FPGA solutions. Get creative and propose servers/switches/apps that merit tests to evaluate improvements in deterministic latencis.

***HOMEWORK #1 – Design (white board picture or Visio) -partial FPGA Pilot architecture with requirements of:***

* ***Only 1 Multi-Layer FPGA switch in Colo for raw direct market data feeds***
* ***No other FPGA devices***
* ***Choose servers for FH normalization, book builds, risk checks, FIX Order generation;***
* ***Choose servers/switches for exchange & client connectivity;***

***1-pager: per limitations in requirements – argue how your architecture addresses ULL and deterministic latencies.***