Enhancement mode NFET Inverter
Introduction and Physical Properties

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1) NFET Cell Description

The Enhancement mode NFET Inverter cell is a 1 input 1 output device. When used in a digital circuit it acts as a logic NOT gate. 2 inverter circuits can be used as a buffer and a repeater since the output flows from V_{dd} and ground and not from the input.

2) NFET Cell Symbol

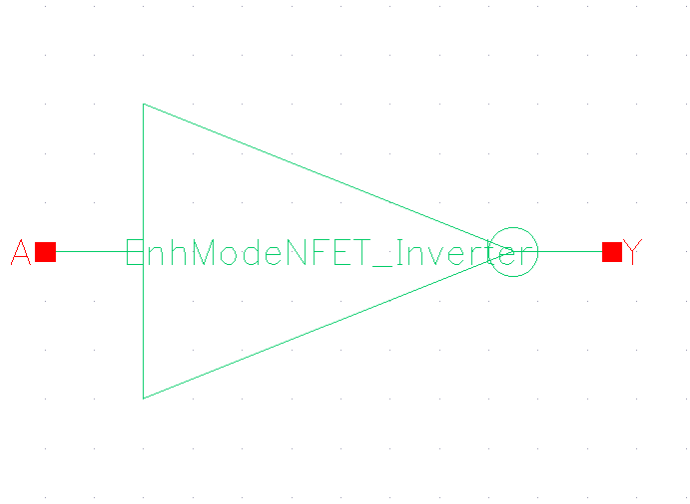

Figure 1: Symbol for Enhancement mode NFET Inverter

3) NFET Cell Truth Table

Cell Truth Table	
Inputs	Outputs
0	1(degraded)
1	0

4) NFET Cell Schematic Diagram

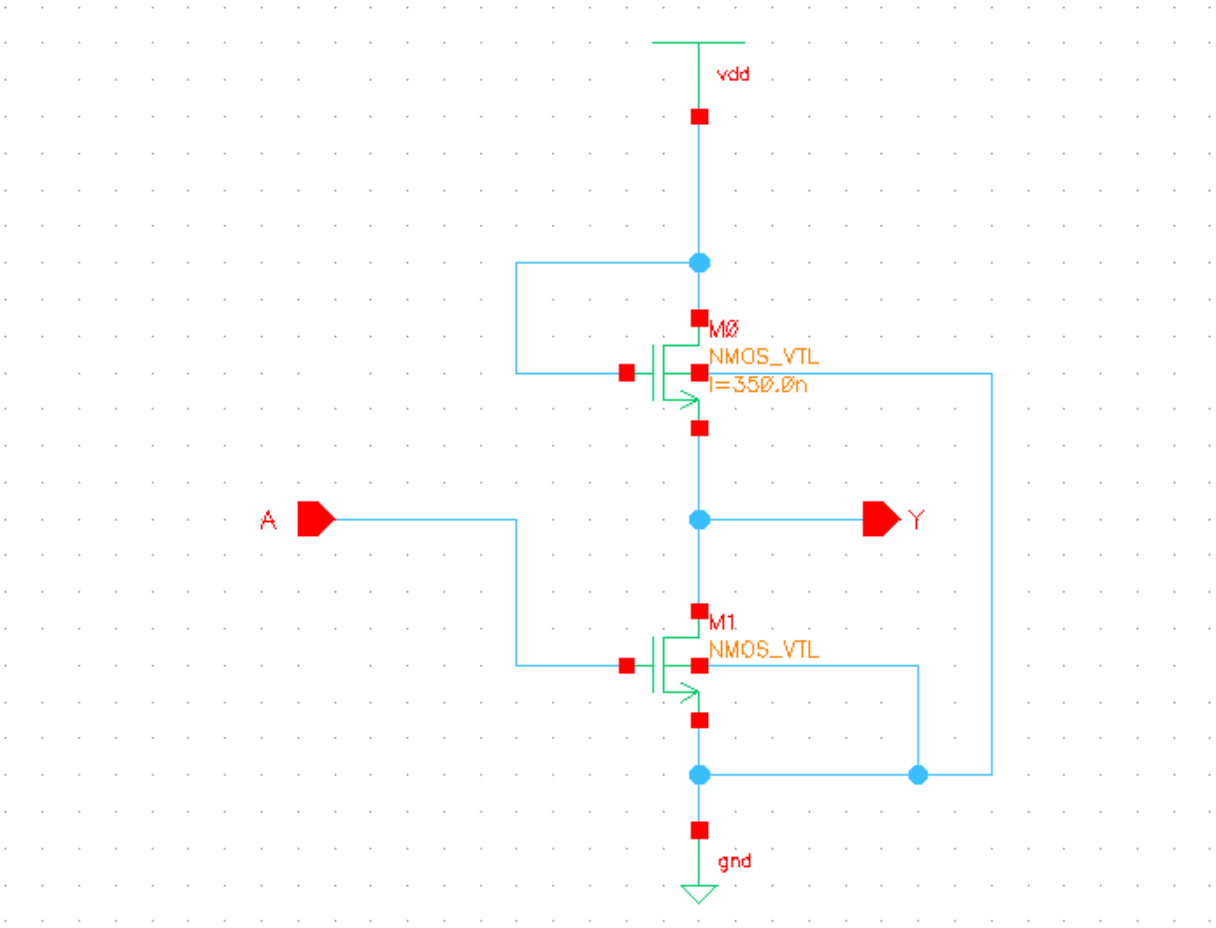

Figure 2: Circuit for Enhancement mode NFET Inverter

5) NFET Transistor Dimensions

Transistor Dimensions		
Transistor Instance Number	Length (nm)	Width (nm)
NMOS (M0) Pullup	350	90
NMOS_(M1) Pulldown	50	90

Performance Analysis

6,7) NFET Output Rise/Fall Time Data

Input X: Output Rise Time Data t_r (ps)					
Input Rise/ Fall Time	Output Load (FOx)				
	0	1	2	4	8
40				511.1	

Input X: Output Fall Time Data t_f (ps)					
Input Rise/ Fall Time	Output Load (FOx)				
	0	1	2	4	8
40				68.02	

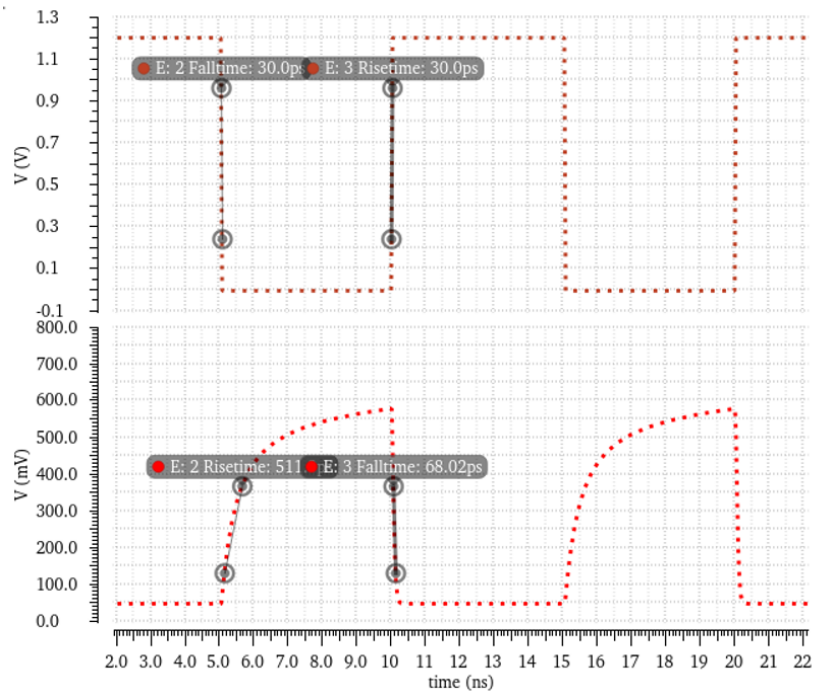

Figure 3: NFET Plot of The Input and Output Waveforms with Rise and Fall Times

8,9) NFET Propagation Delays

Data Worst Case Low to High Propagation Delay Data t_{plh} (ps)					
Input Rise/ Fall Time	Output Load (FOx)				
	0	1	2	4	8
40				NA	

Data Worst Case High to Low Propagation Delay Data t_{phl} (ps)					
Input Rise/ Fall Time	Output Load (FOx)				
	0	1	2	4	8
40				NA	

NA due to not reaching 1.2V

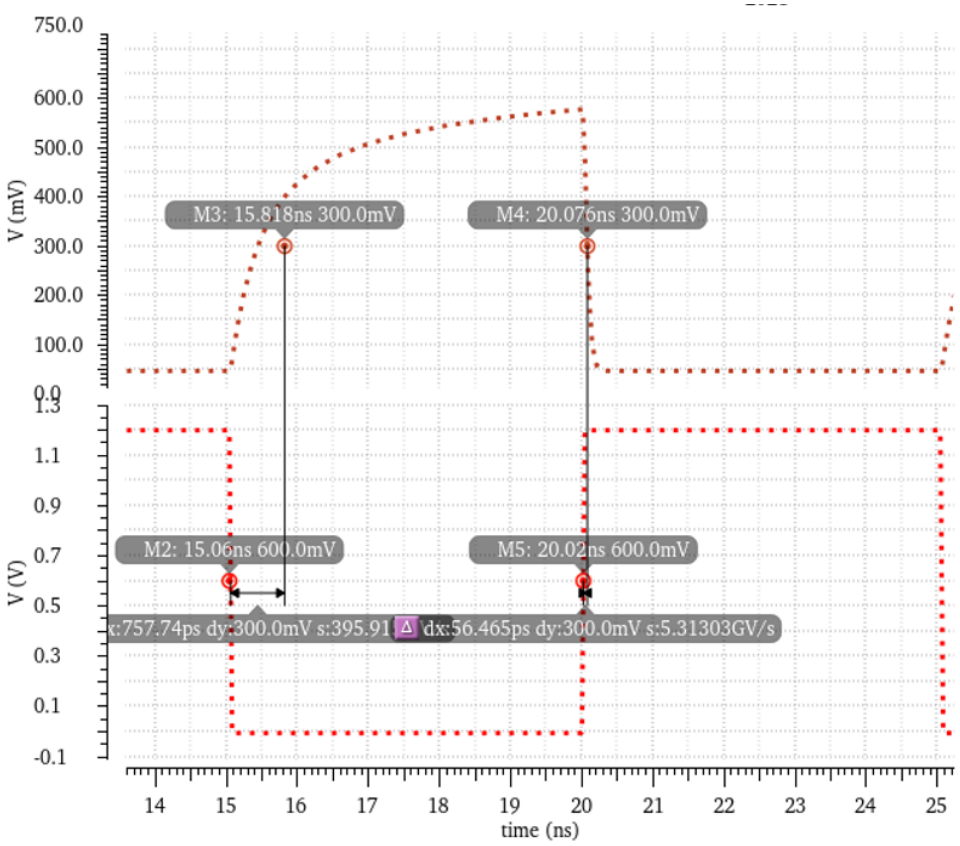

Figure 4: Plot of The Input and Output Waveforms with Propagation Delay Times

10.) NFET Inverter DC Analysis

Type	V_{IH_DC} (mV)	V_{IL_DC} (mV)	V_{OH_DC} (mV)	V_{OL_DC} (mV)
NFET	624.0	344.8	508.5	117.8

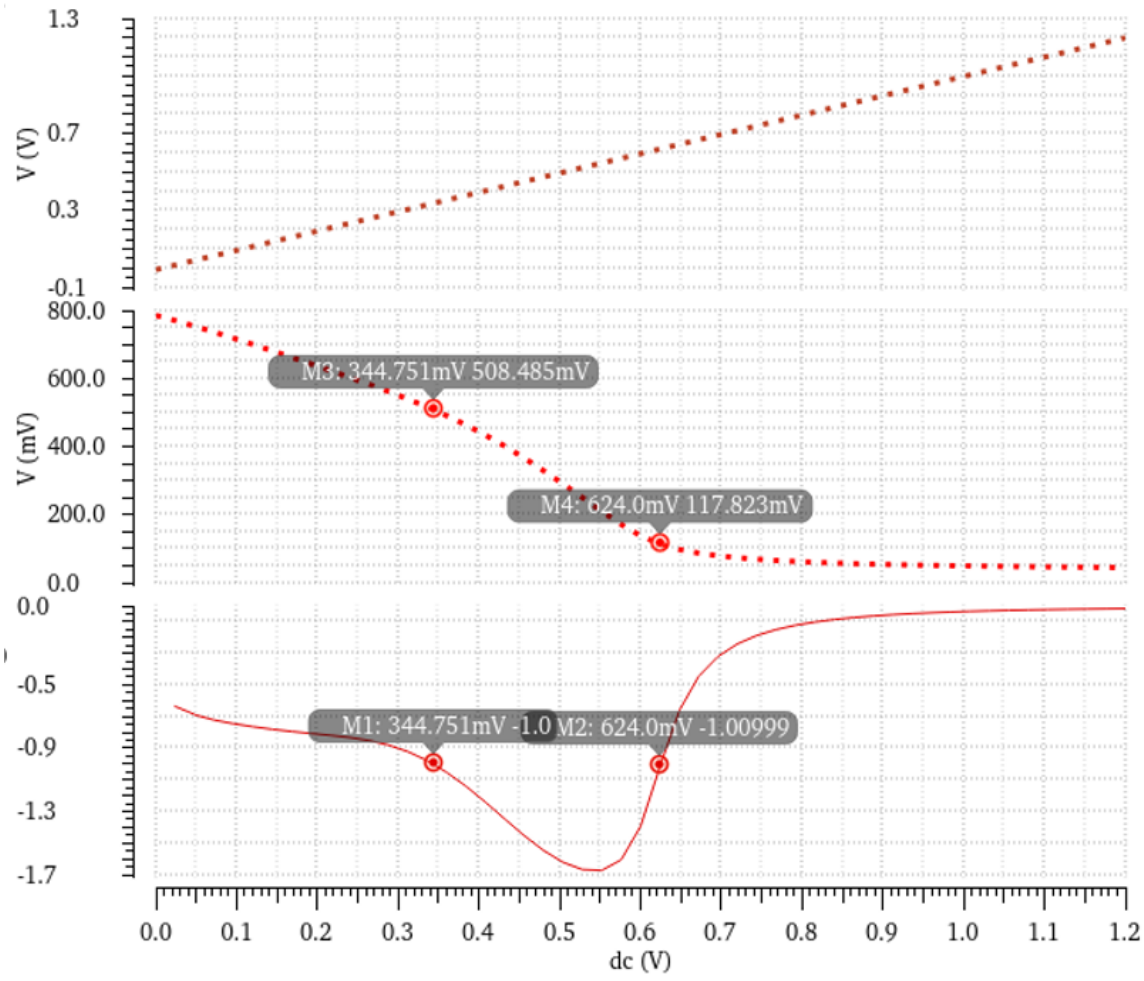

Figure 5: Plot of DC Sweep with the Derivative of the Output Response

Group 17
10/29/2021
Introduction and Physical Properties

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1) NFET Long-Gate Cell Description

The Enhancement mode NFET Long-Gate Inverter cell is a 1 input 1 output device. When used in a digital circuit it acts as a logic NOT gate. 2 inverter circuits can be used as a buffer and a repeater since the output flows from V_{dd} and ground and not from the input. This Inverter has a larger gate to better the transient resonse.

2) NFET Long-Gate Cell Symbol

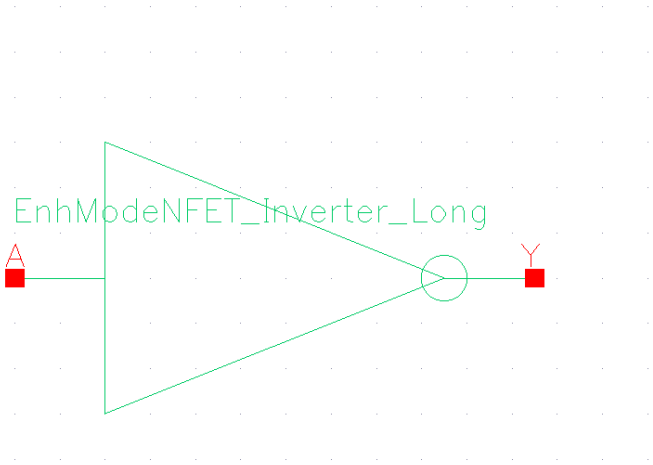

Figure 6: Symbol for Enhancement mode NFET Long-Gate Inverter

3) NFET Long-Gate Cell Truth Table

Cell Truth Table	
Inputs	Outputs
0	1(degraded)
1	0

4) NFET Long-Gate Cell Schematic Diagram

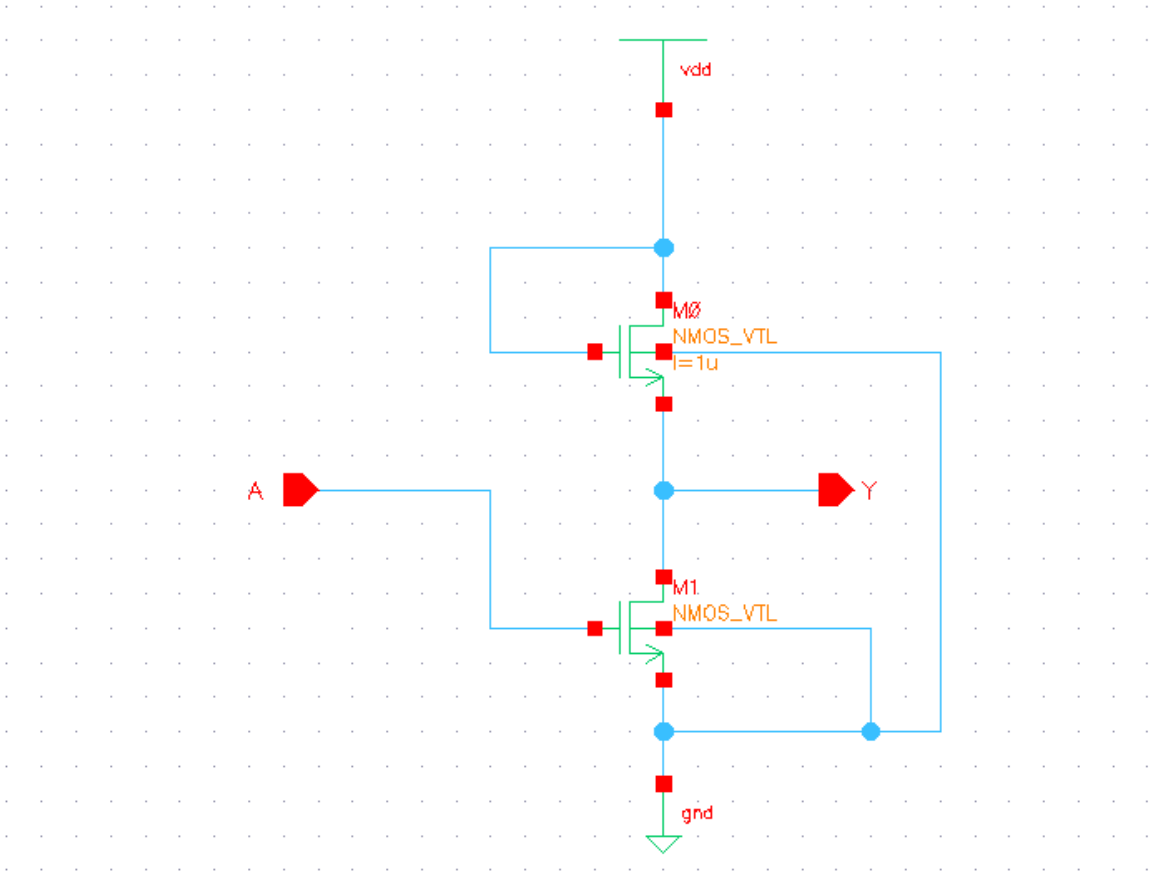

Figure 7: Circuit for Enhancement mode NFET Long-Gate Inverter

5) NFET Long-Gate Transistor Dimensions

Transistor Dimensions		
Transistor Instance Number	Length (nm)	Width (nm)
NMOS (M0) Pullup	1000	90
NMOS_(M1) Pulldown	50	90

Performance Analysis

6,7) NFET Long-Gate Inverter Cell Output Rise/Fall Time Data

Input X: Output Rise Time Data t_r (ps)					
Input Rise/ Fall Time	Output Load (FOx)				
	0	1	2	4	8
40				1158	

Input X: Output Fall Time Data t_f (ps)					
Input Rise/ Fall Time	Output Load (FOx)				
	0	1	2	4	8
40				72.77	

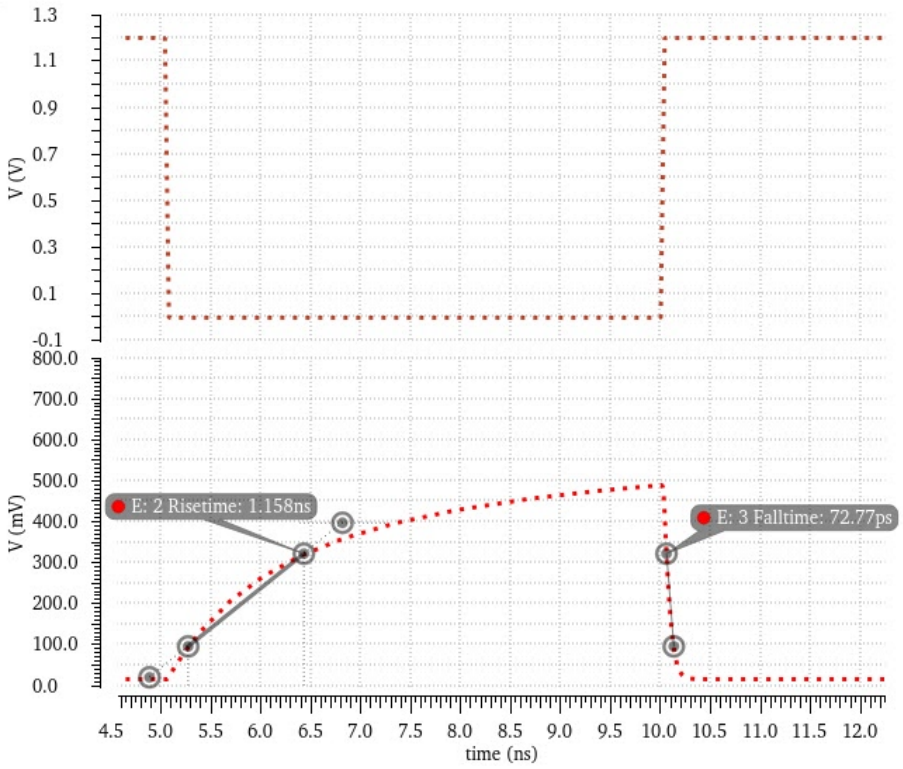

Figure 8: Plot of The Input and Output Waveforms with Rise and Fall Times

8,9) NFET Long-Gate Inverter Cell Propagation Delays

Data Worst Case Low to High Propagation Delay Data t_{plh} (ps)					
Input Rise/ Fall Time	Output Load (FOx)				
	0	1	2	4	8
40				NA	

Data Worst Case High to Low Propagation Delay Data t_{phl} (ps)					
Input Rise/ Fall Time	Output Load (FOx)				
	0	1	2	4	8
40				NA	

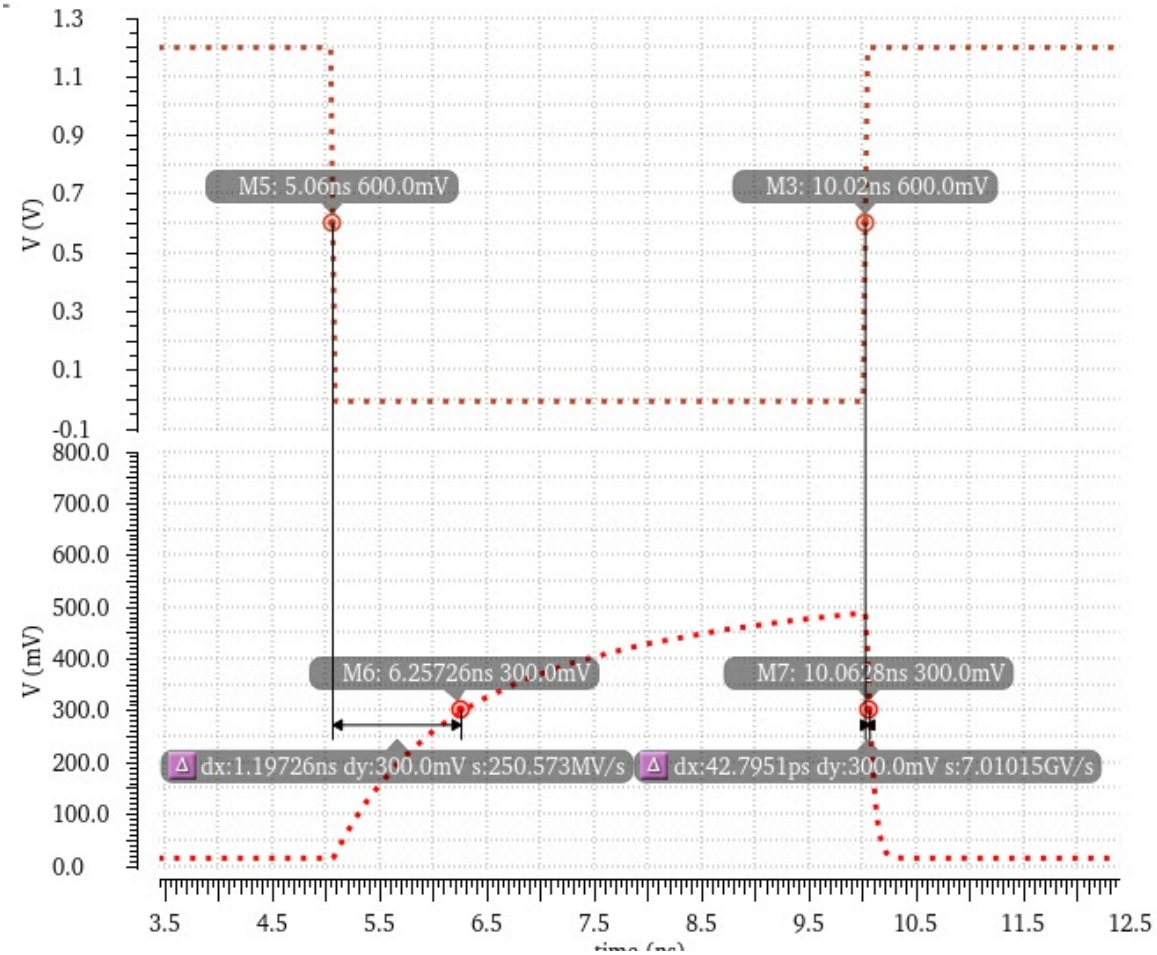

Figure 9: Plot of The Input and Output Waveforms with Propagation Delay Times

NA due to not reaching 1.2V

10.) NFET Long-Gate Inverter Cell DC Analysis

V_{IH_DC} (mV)	V_{IL_DC} (mV)	V_{OH_DC} (mV)	V_{OL_DC} (mV)
550.6	270.7	528.8	66.0

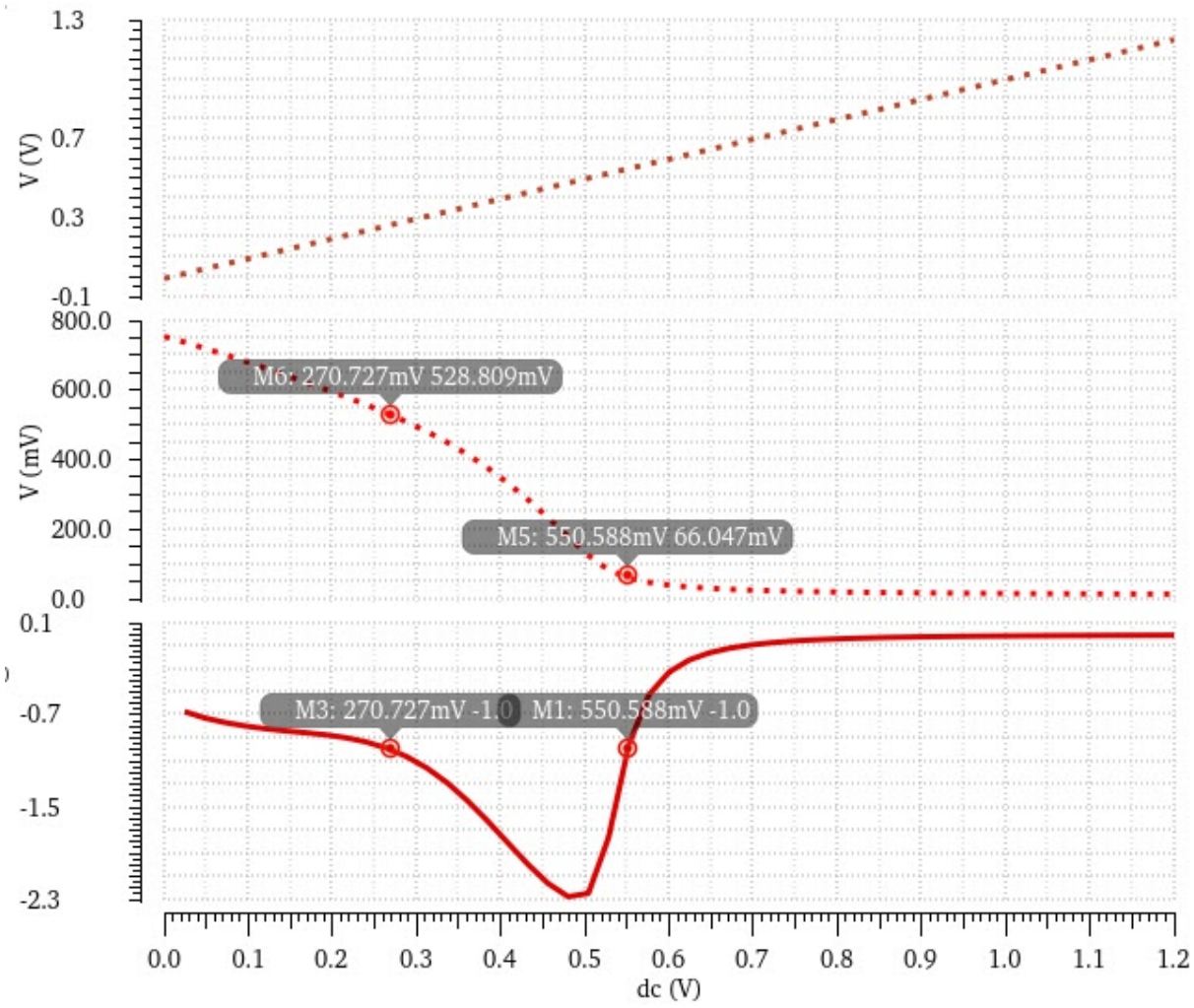

Figure 10: Plot of DC Sweep with the Derivative of the Output Response