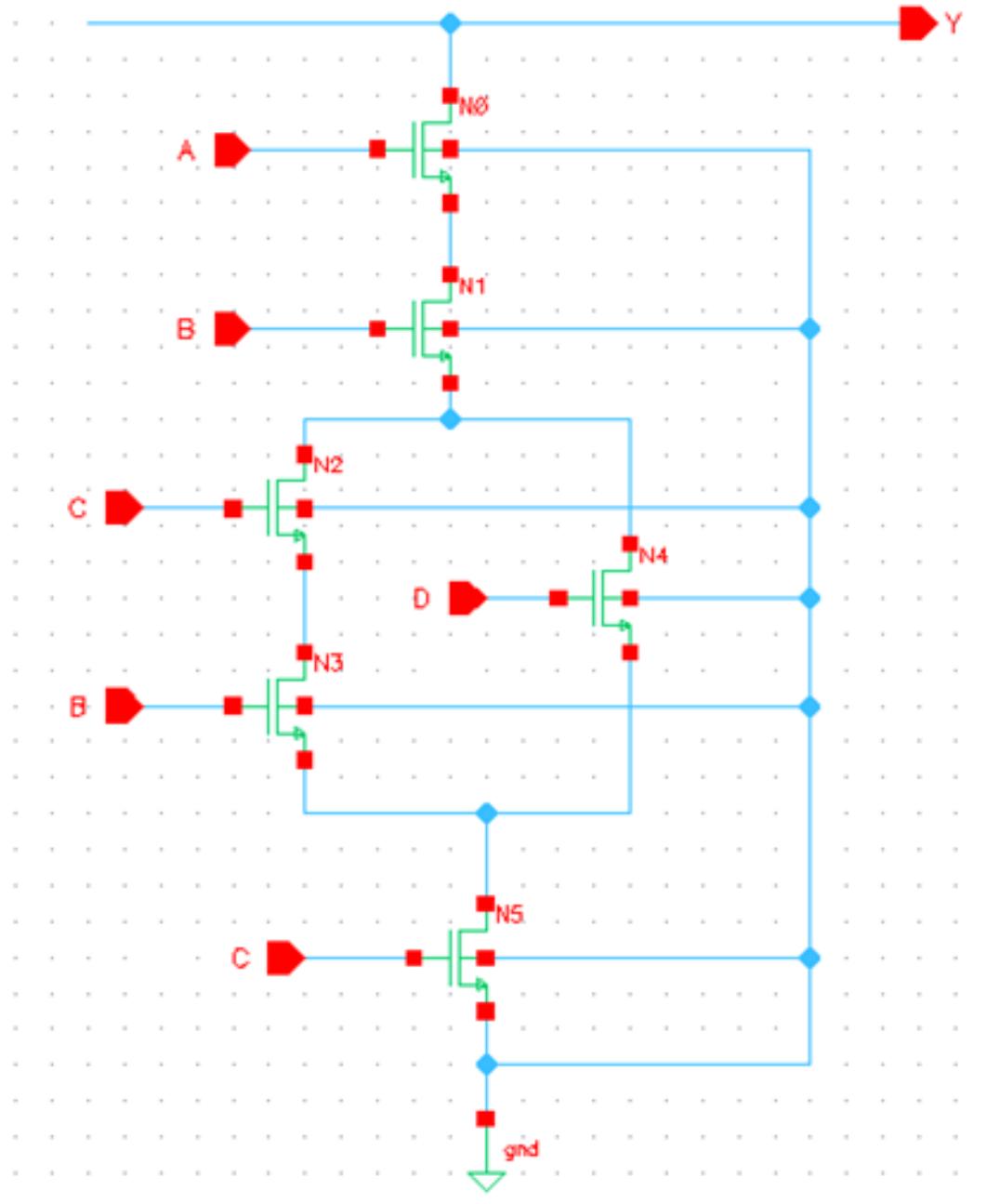


# Digital IC Design 1

## Lab 2: Part 2 - CMOS Compound Gate Report

### Original CMOS Compound Gate

Consider the NMOS stack of compound gate shown below.



### Minimization and Cell Discovery

### NMOS Stack of the CMOS Compound Gate

$$\begin{aligned}
 Y &= \overline{\overline{A} \overline{B} ((C \overline{B}) + D) C} \\
 &= \overline{\overline{ABC}((C \overline{B}) + D)} \\
 &= \overline{\overline{ABCCB} + \overline{ABCD}} \\
 &= \overline{\overline{ABC} + \overline{ABCD}} \\
 &= \overline{\overline{ABC} (1 + D)} \\
 &= \overline{\overline{ABC}}
 \end{aligned}$$

### PMOS Stack of the CMOS Compound Gate

$$Y = \overline{\overline{A}} + \overline{\overline{B}} + \overline{\overline{C}}$$

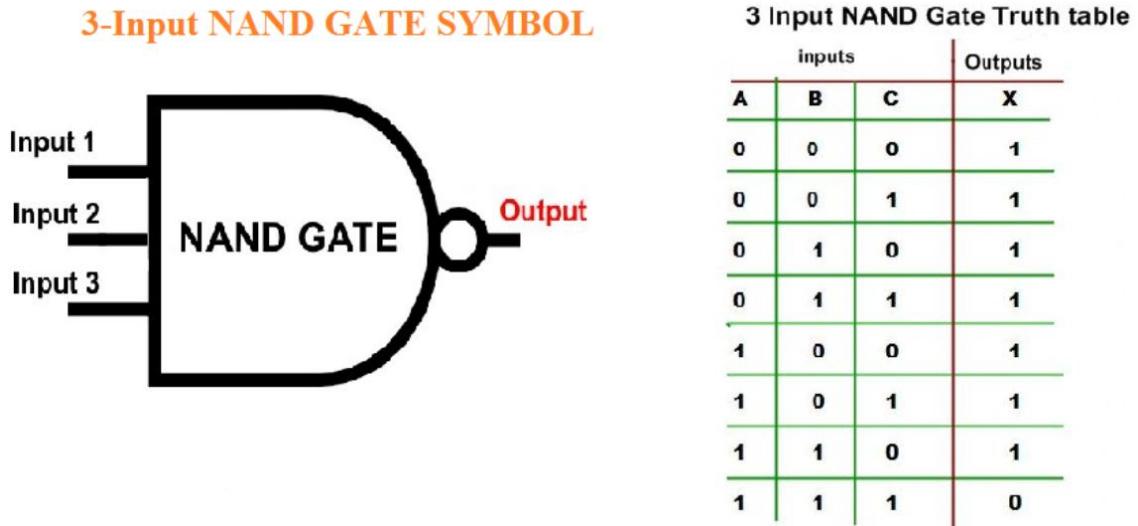
Therefore, after minimizing the original CMOS compound gate, the team discovered the circuit is equivalent to a 3-input NAND gate.

### Introduction and Physical Properties

#### Cell Description

This lab will be analyzing the compound gate design that has 4 states. The first two stages are buffers, the third stage will be a 3-input NAND gate as DUT, and the last stage is different fanout loads.

The three input NAND gate takes three inputs and if any input contains 0 the output is 1, else if all inputs are 1, the output is 0. The NAND gate is one of the universal gates. The IC 7400 consists of 4 NAND gates. Any logic function can be implemented with a combination of NAND gates though it may be slower than using other gates. It can model an AND OR or NOT gate.



#### Cell Symbol

The CMOS Inverters are used as buffers. The NAND gate can be used for any logic design. DUT and CMOS inverter. The CMOS inverter is used for the buffers and on the other FO configurations. The A,B,C/input pins are connected to the sources, a VDD pin is connected to 1.2 V DC voltage. A GND pin will be connected to low voltage/or the ground, and the output/Y pin produces a signal read after it travel through the CMOS inverter and NAND gate

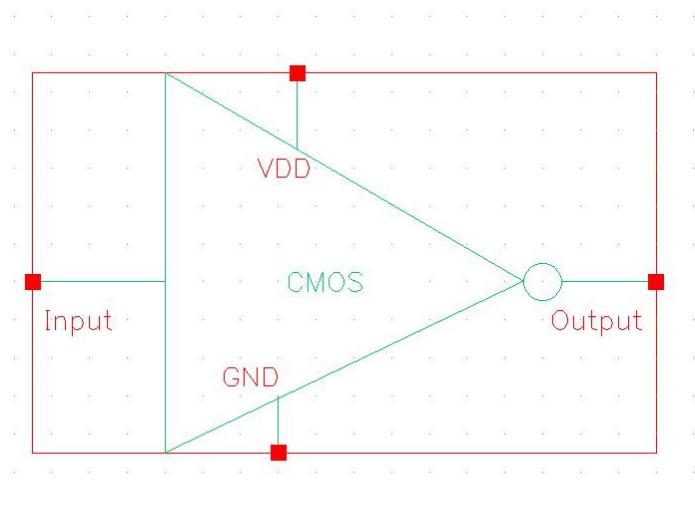


Fig 2: CMOS Inverter symbol

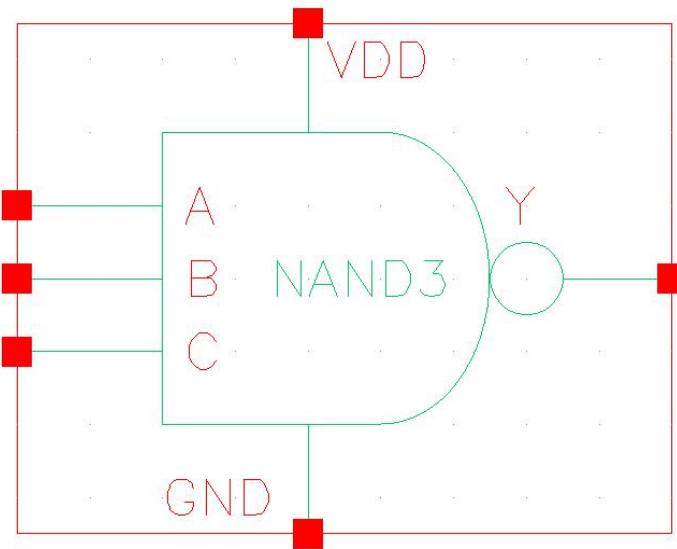


Fig 3: 3 input NAND gate as a DUT

### **Cell Truth Table**

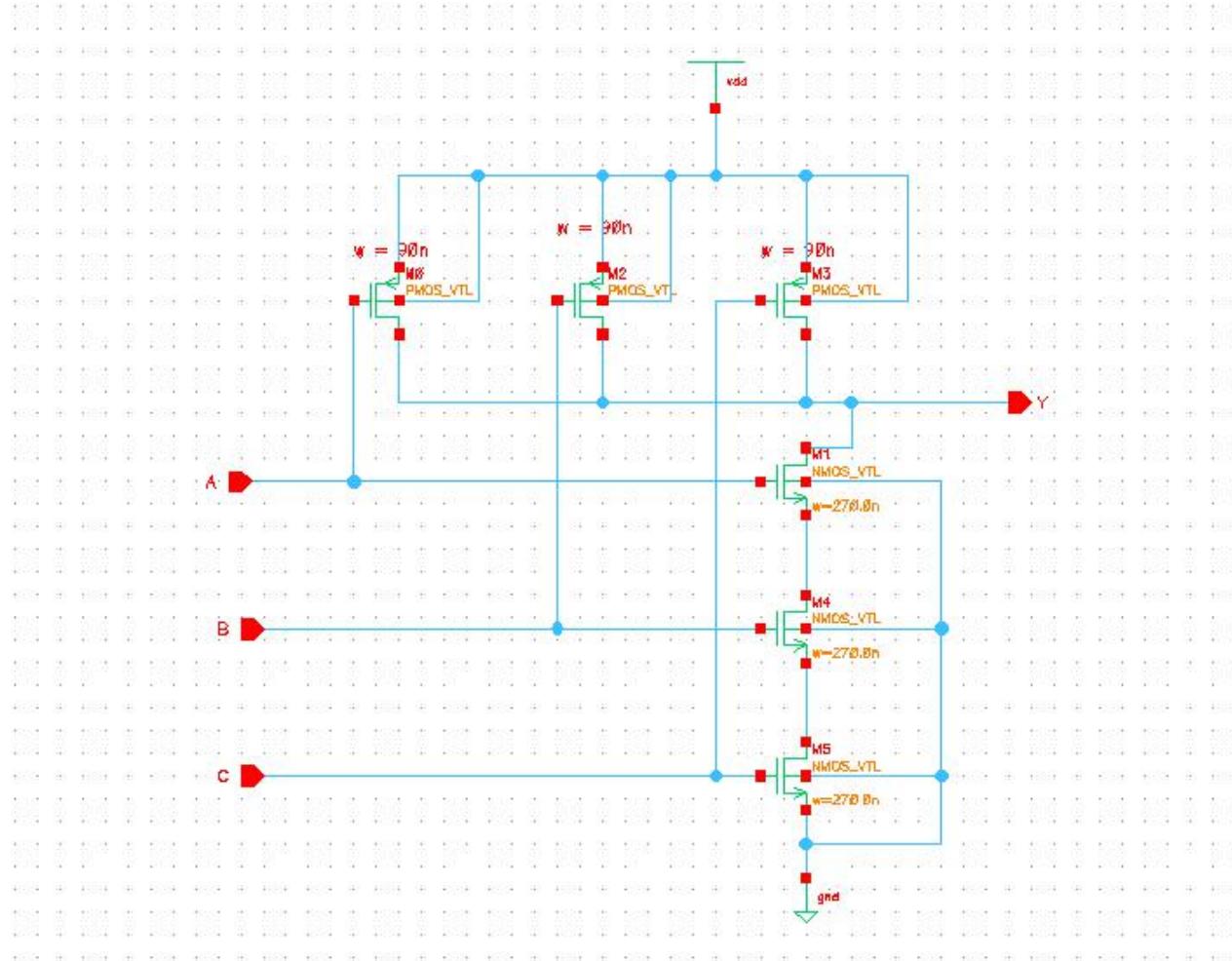
Complete the truth table (sample given below) for all cell outputs using {0, 1} for the input low and high, respectively and {L, H} for the output low and high, respectively. Repeat rows and columns as needed.

<b>DUT Truth Table</b>			
<b>A</b>	<b>B</b>	<b>C</b>	<b>DUT Outputs {L,H}</b>
0	0	0	1
0	0	1	1
0	1	1	1
0	1	0	1
1	1	0	1
1	0	1	1
1	1	1	0

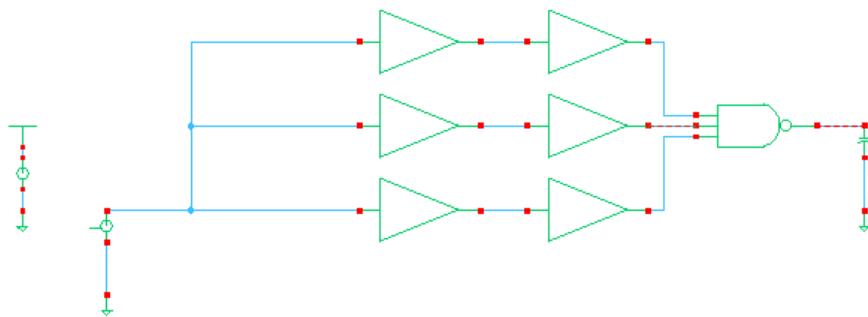
*Table 1: Truth table of the NAND3 gate*

### **Cell Schematic Diagram**

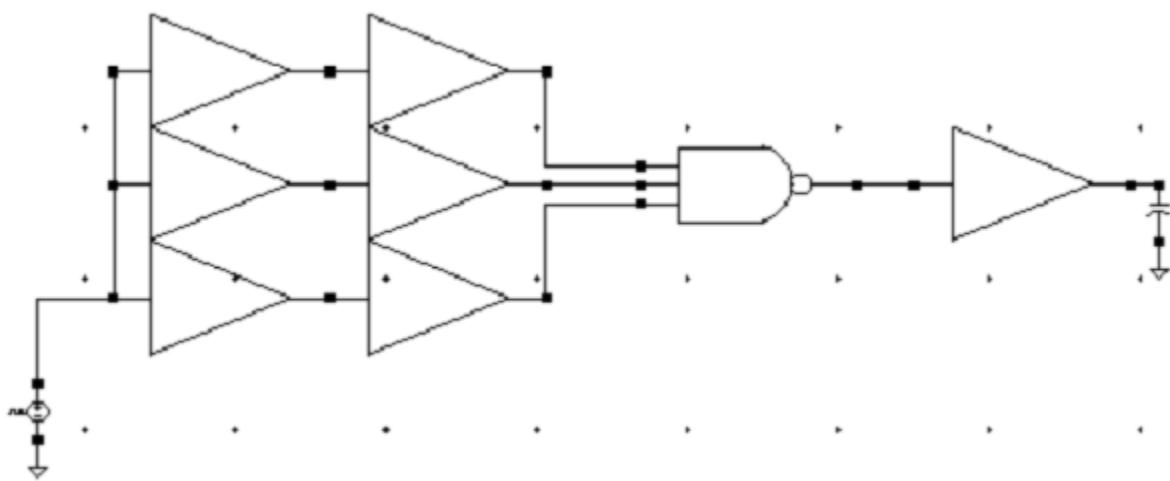
The DUT or NAND3 gate has 3 input signals that have 3 NMOS transistors connected in series and 3 PMOS transistors connected in parallel. The designs have different fanouts such as FO\_0, FO\_1, FO\_2, FO\_4, FO\_8. As expected, the inputs' rise time and fall time of the NAND3 gate should meet around 50ps.



**Fig 4: NAND3 schematic**



*Figure 5: Example Schematic FO\_0.*



*Figure 6: Example Schematic FO\_1*

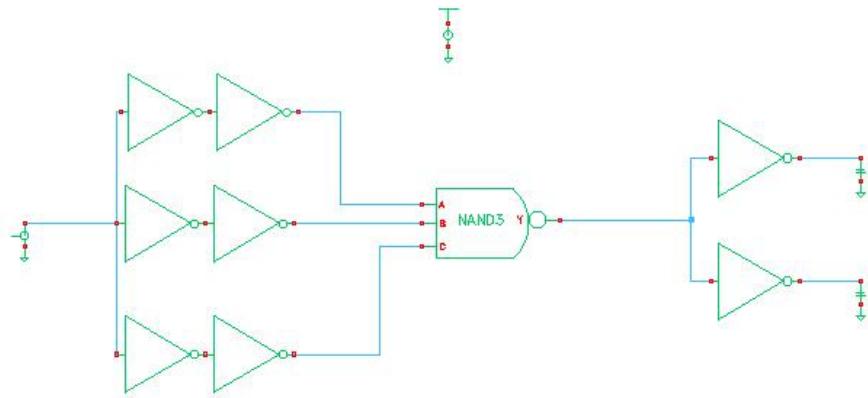


Figure 8: Example Schematic FO\_2

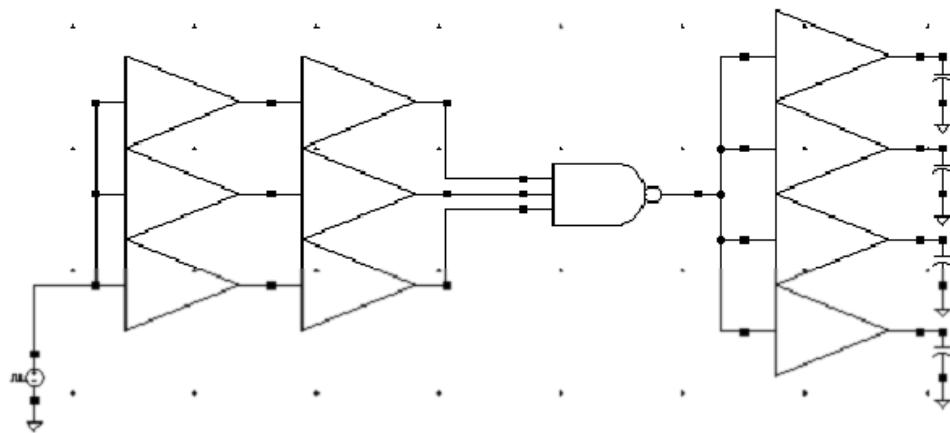
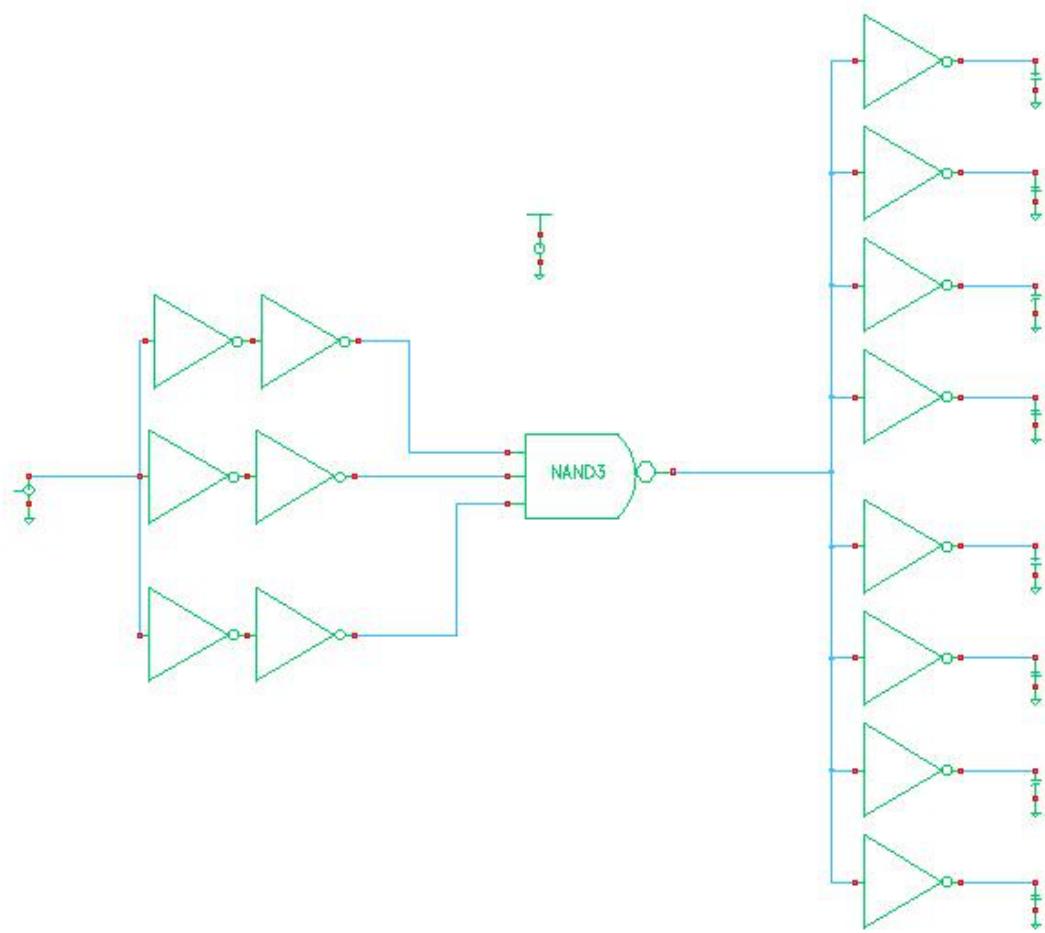


Figure 9: Example Schematic FO\_4



*Figure 10: Example Schematic FO\_8*

### Cell Layout Diagram and Dimensions

Record the transistor length and width dimensions (nm).

Transistor Dimensions											
FO Type		FO_0		FO_1		FO_2		FO_4		FO_8	
Type	Transistor Type	Length [nm]	Width [nm]								
CMOS Inverter	PMOS	50	90	50	90	50	90	50	90	50	90
	NMOS	50	90	50	90	50	90	50	90	50	90
NAND3 Gate/DUT	PMOS	50	90	50	90	50	90	50	90	50	90
	NMOS	50	270	50	270	50	270	50	270	50	270

*Table 2: Transistor Dimensions*

Fanouts all use the same 50 nm length and 90 nm width.

### Performance Analysis

#### Rise and Fall Times

These tables below shows the measured rise and fall times for different fanouts

FO Type	DUT		
	Width (nm)		PMOS
			90
	Length (nm)		NMOS
			270
	Rise Time		PMOS
			50
	NMOS		NMOS
			50
	Rise Time		2.3491n s

FO_0	Vpulse (ns)	Fall Time	2.6515n s
	Tr (input) (ps)	A	50.45
		B	52.17
		C	53.36
	Tf (input) (ps)	A	51.25
		B	50.59
		C	50.81
	Tr (output) (ps)	Y	137.5
	Tf (output) (ps)	Y	95.63

Table 3 : FO\_0 Rise and Fall Times

FO Type	DUT		
FO_1	Width (nm)	PMOS	90
		NMOS	270
	Length (nm)	PMOS	50
		NMOS	50
	Vpulse (ns)	Rise Time	1.62
		Fall Time	2.5
	Tr (input) (ps)	A	54.17
		B	46.05
		C	45.97

	<b>Tf (input) (ps)</b>	<b>A</b>	53.39
		<b>B</b>	49.8
		<b>C</b>	49.78
	<b>Tr (output) (ps)</b>	<b>Y</b>	
	<b>Tf (output) (ps)</b>	<b>Y</b>	

**Table 4 : FO\_1 Rise and Fall Times**

<b>FO Type</b>	<b>DUT</b>		
<b>FO_2</b>	<b>Width (nm)</b>	<b>PMOS</b>	90
		<b>NMOS</b>	270
	<b>Length (nm)</b>	<b>PMOS</b>	50
		<b>NMOS</b>	50
	<b>Vpulse (ns)</b>	<b>Rise Time</b>	1.6
		<b>Fall Time</b>	2.4
	<b>Tr (input) (ps)</b>	<b>A</b>	52.94
		<b>B</b>	44.62
		<b>C</b>	45.27
		<b>A</b>	51.25

	<b>Tf (input) (ps)</b>	<b>B</b>	48.11
		<b>C</b>	48.13
	<b>Tr (output) (ps)</b>	<b>Y</b>	14.93
	<b>Tf (output) (ps)</b>	<b>Y</b>	17.95

Table 6 : FO\_2 Rise and Fall Times

<b>FO Type</b>	<b>DUT</b>		
<b>FO_4</b>	<b>Width (nm)</b>	<b>PMOS</b>	90
		<b>NMOS</b>	270
	<b>Length (nm)</b>	<b>PMOS</b>	50
		<b>NMOS</b>	50
	<b>Vpulse (ns)</b>	<b>Rise Time</b>	1.8
		<b>Fall Time</b>	2.65
	<b>Tr (input) (ps)</b>	<b>A</b>	52.04
		<b>B</b>	47.49
		<b>C</b>	47.91
	<b>Tf (input) (ps)</b>	<b>A</b>	53.78
		<b>B</b>	50.89
		<b>C</b>	50.88
	<b>Tr (output) (ps)</b>	<b>Y</b>	21.51
	<b>Tf (output) (ps)</b>	<b>Y</b>	17.13

Table 7 : FO\_4 Rise and Fall Times

FO Type	DUT		
FO8	Width (nm)	PMOS	90
		NMOS	270
	Length (nm)	PMOS	50
		NMOS	50
	Vpulse (ns)	Rise Time	2
		Fall Time	2.4
	Tr (input) (ps)	A	50.94
		B	48.75
		C	49.96
	Tf (input) (ps)	A	50.16
		B	48.06
		C	48.08
	Tr (output) (ps)	Y	22.92
	Tf (output) (ps)	Y	26.41

Table 8: FO\_8 Rise and Fall Times

**Propagation Delays**

These tables below shows the measured propagation delays for different fanouts

<b>Data Worst-Case Low to High Propagation Delay Data <math>t_{plh}</math> (ns)</b>					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	91.99	18.52	20.137	23.51	10.945

*Table 9: Data Worst-Case Low to High Propagation Delay Data  $t_{plh}$  (ns)*

<b>Data Worst Case High to Low Propagation Delay Data <math>t_{phl}</math> (ns)</b>					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	106.94	19.138	20.48	24.577	16.268

*Table 10: Data Worst Case High to Low Propagation Delay Data  $t_{phl}$  (ns)*

### Simulation plots

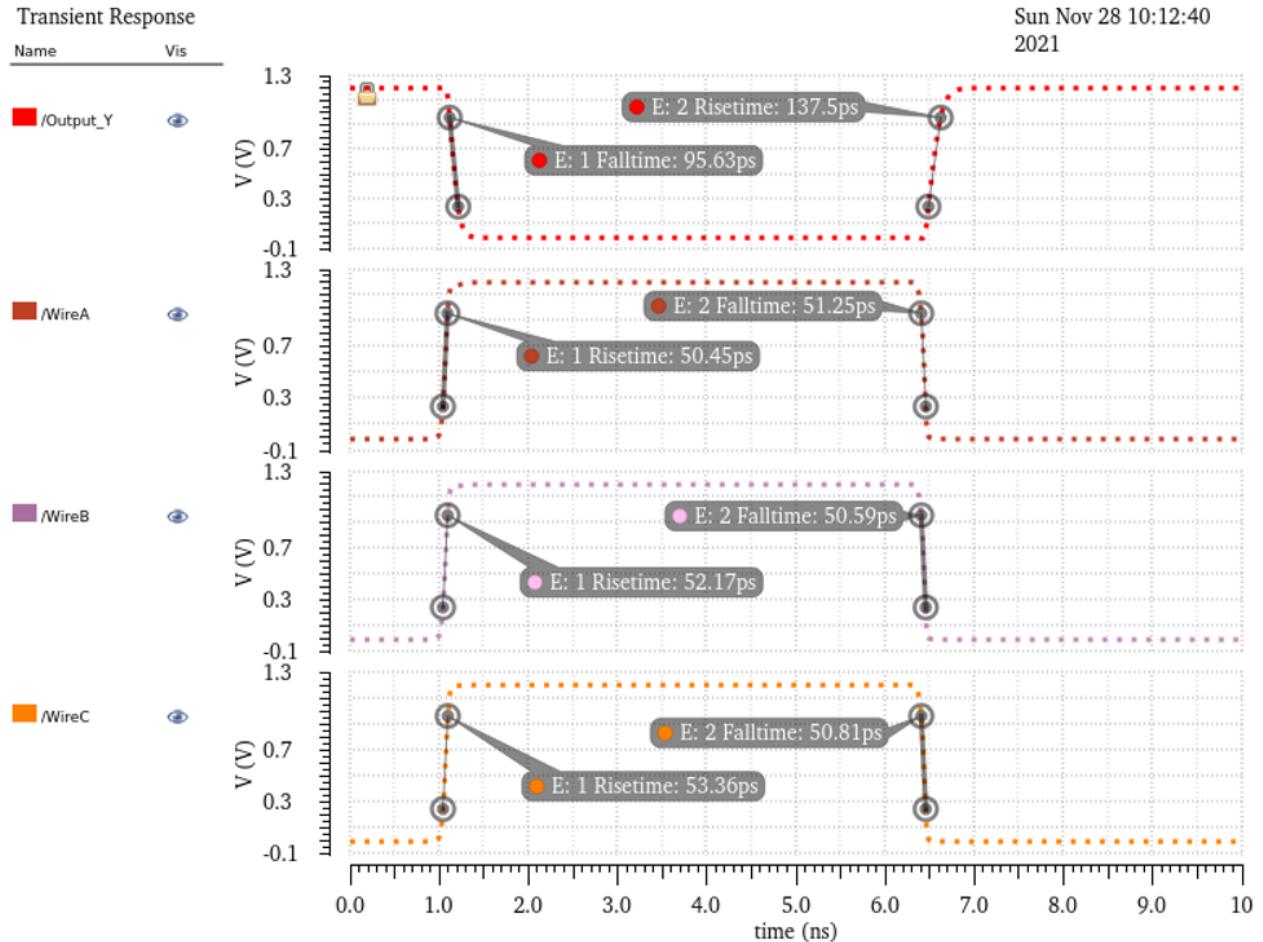


Figure 11: FO\_0 Raise Times and Fall Times

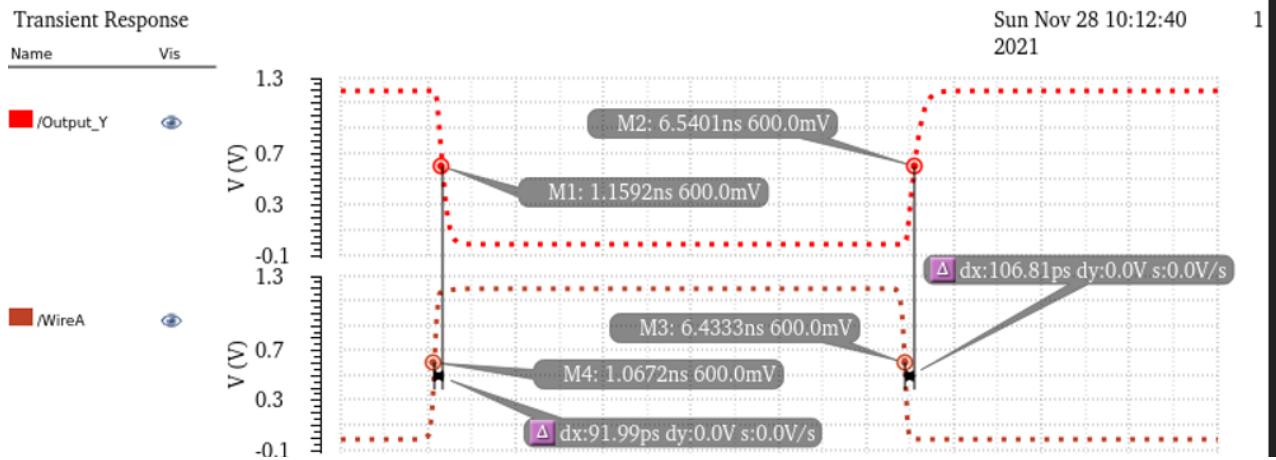


Figure 12: FO\_0 Transition Delta A to Y

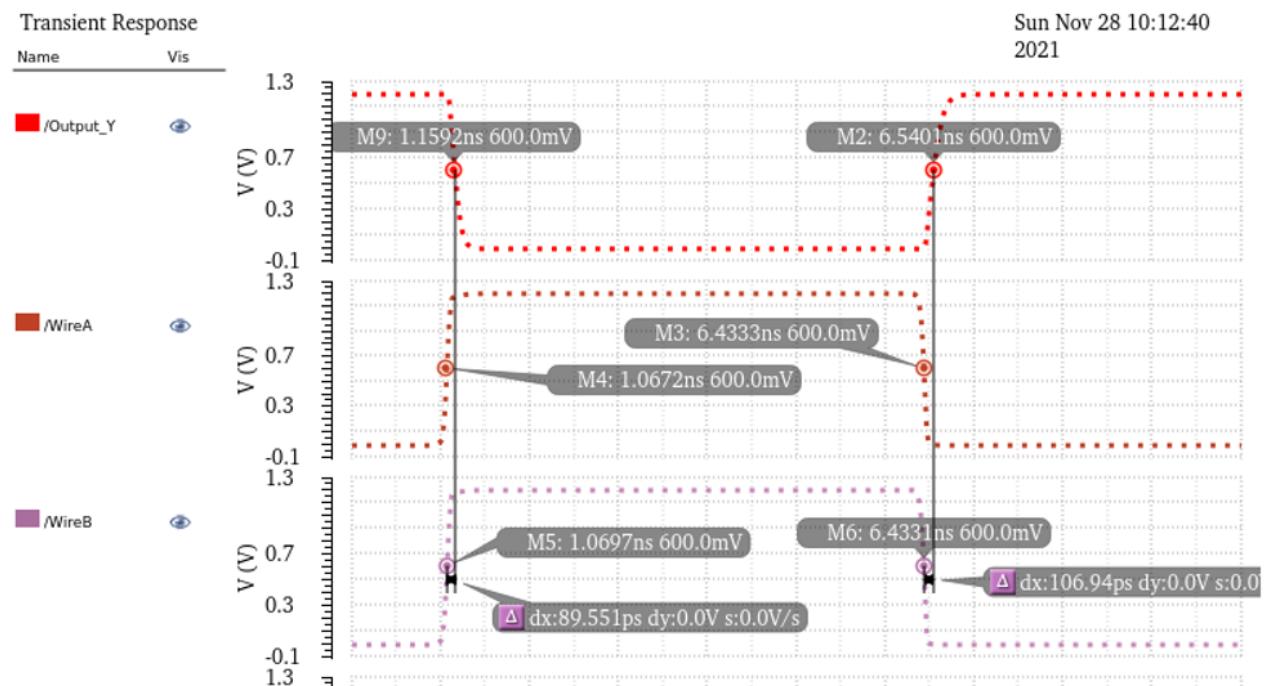


Figure 13: FO\_0 Transition Delta B to Y

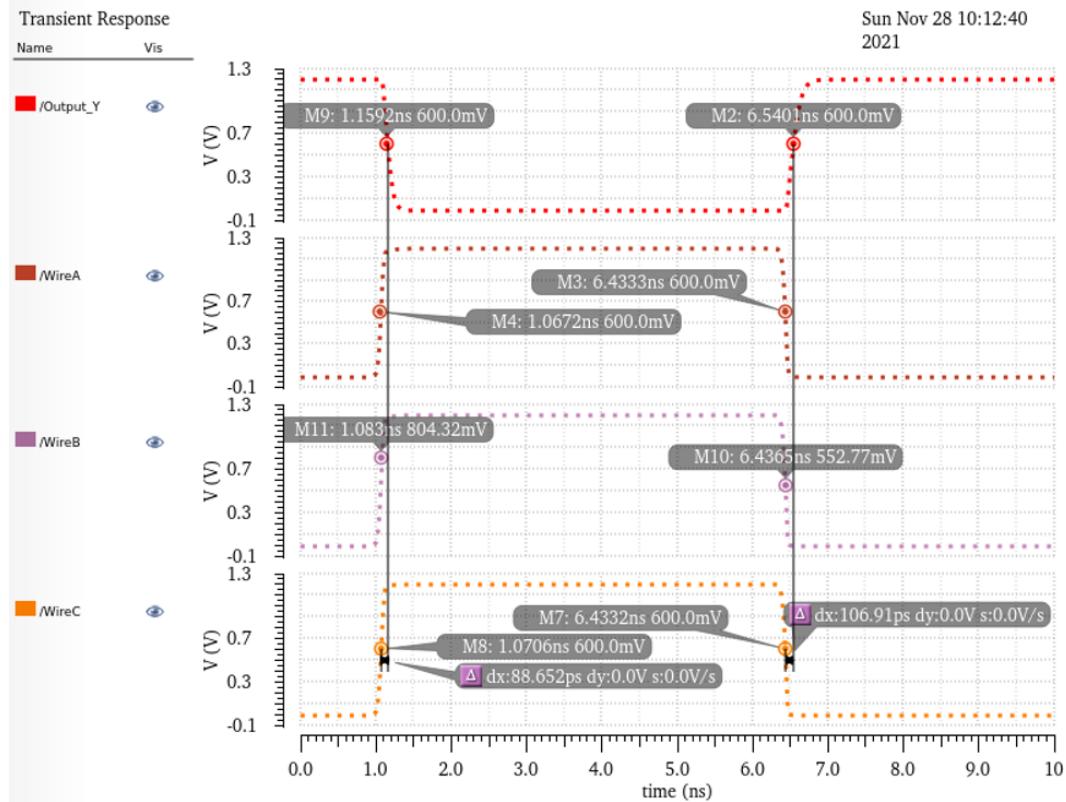


Figure 14: FO\_0 Transition Delta C to Y

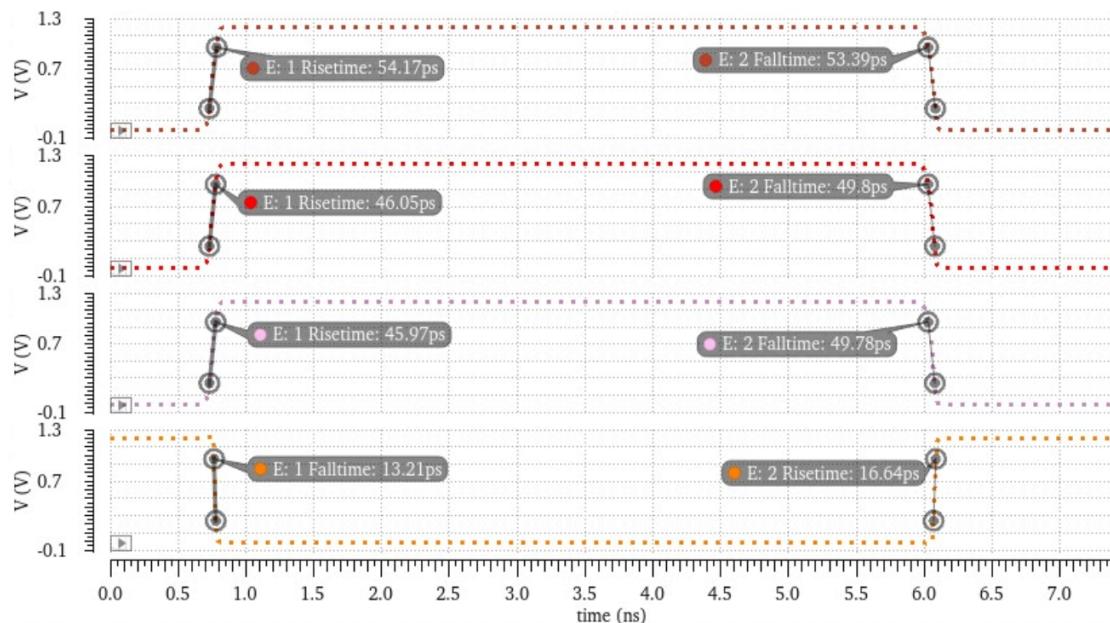
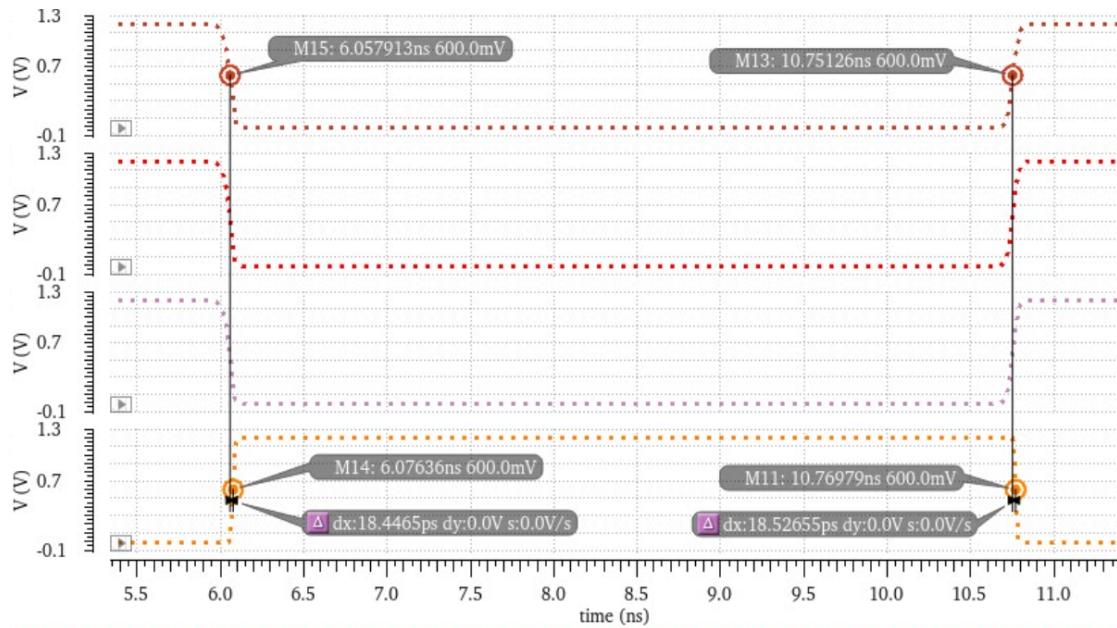
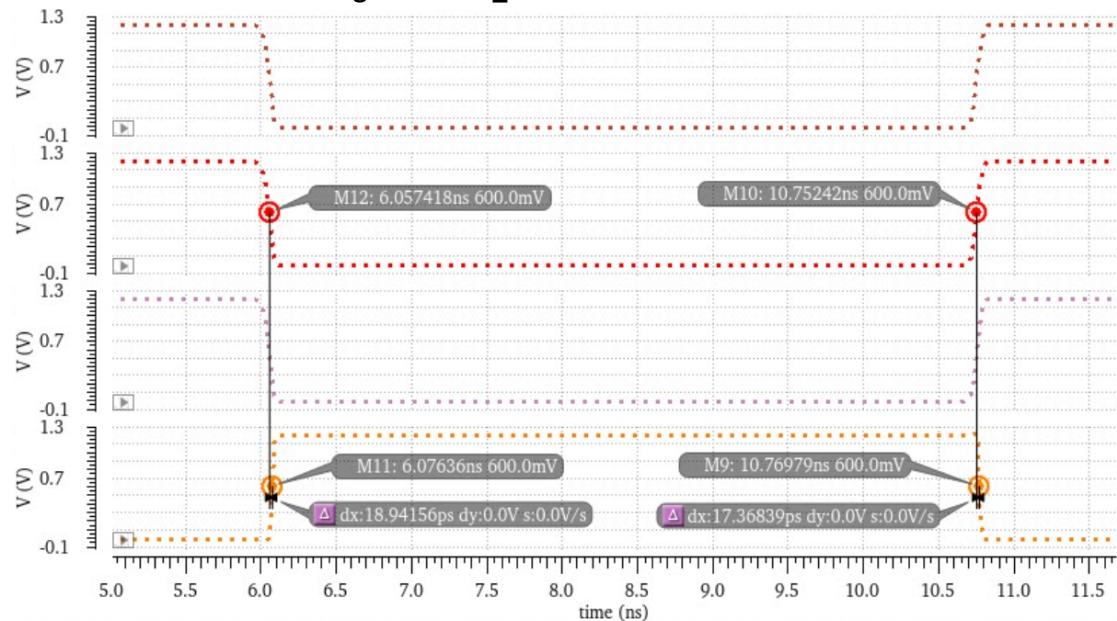
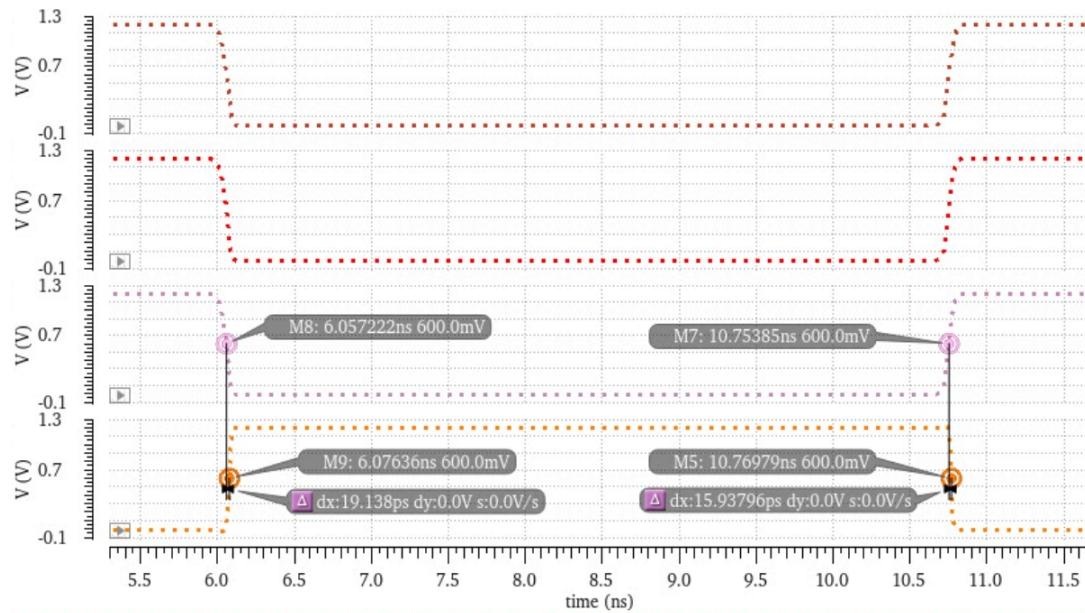
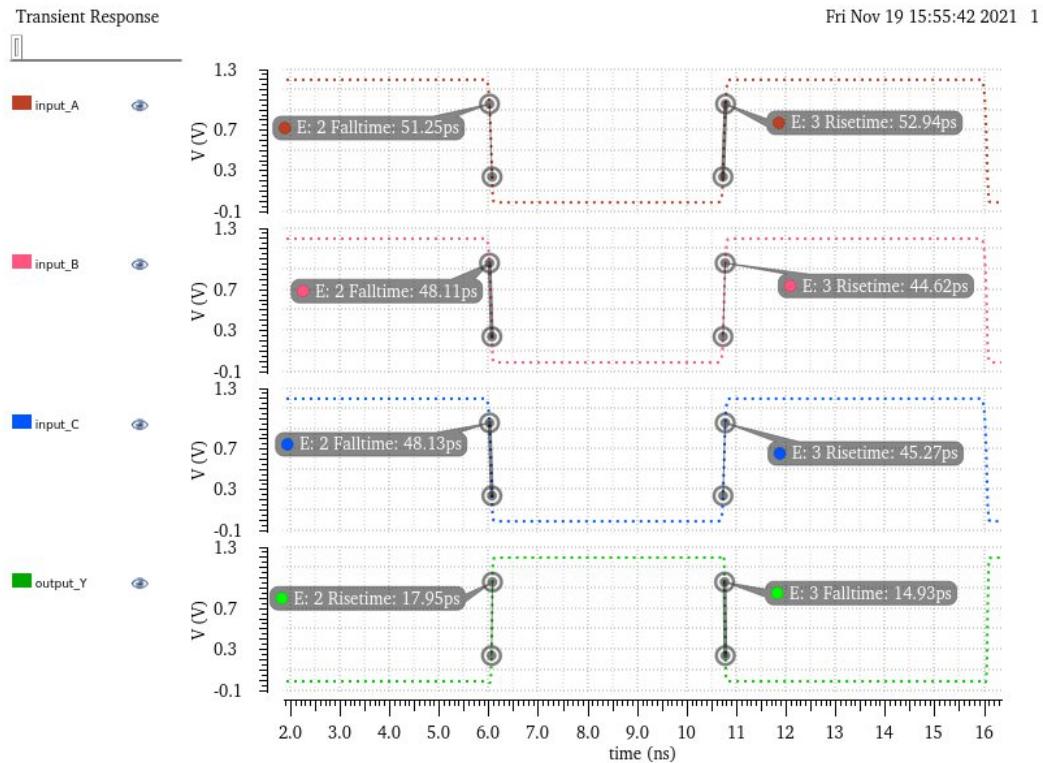


Figure: FO\_1 Raise Time and Fall Time

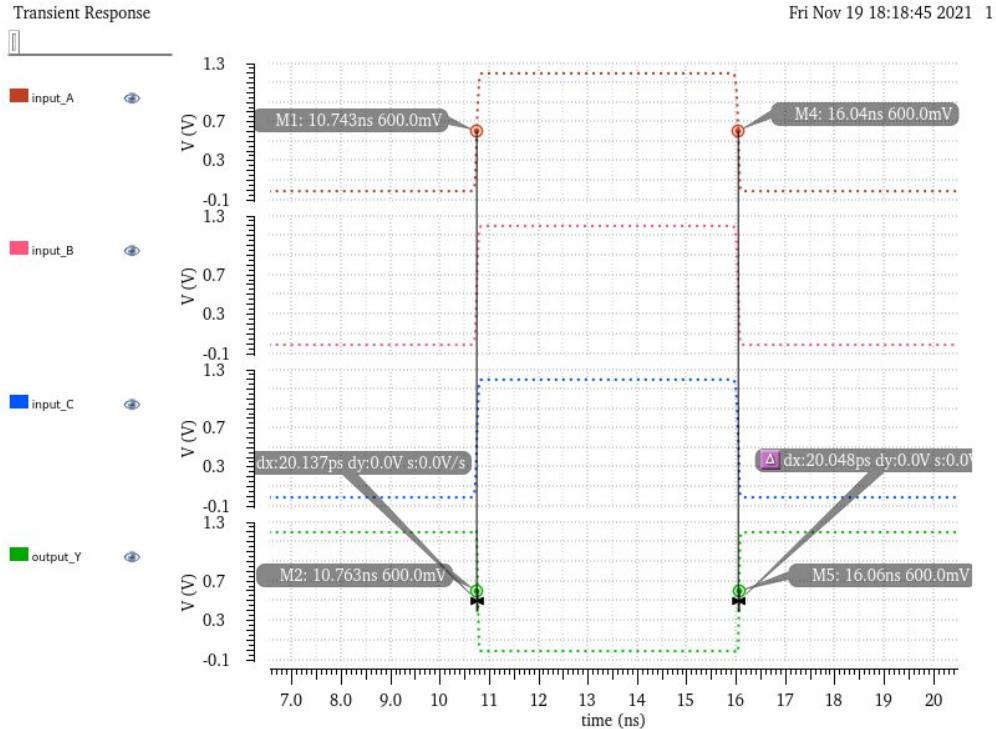
**Figure 15: FO\_1 Transition Delta A to Y****Figure 16: FO\_1 Transition Delta B to Y**



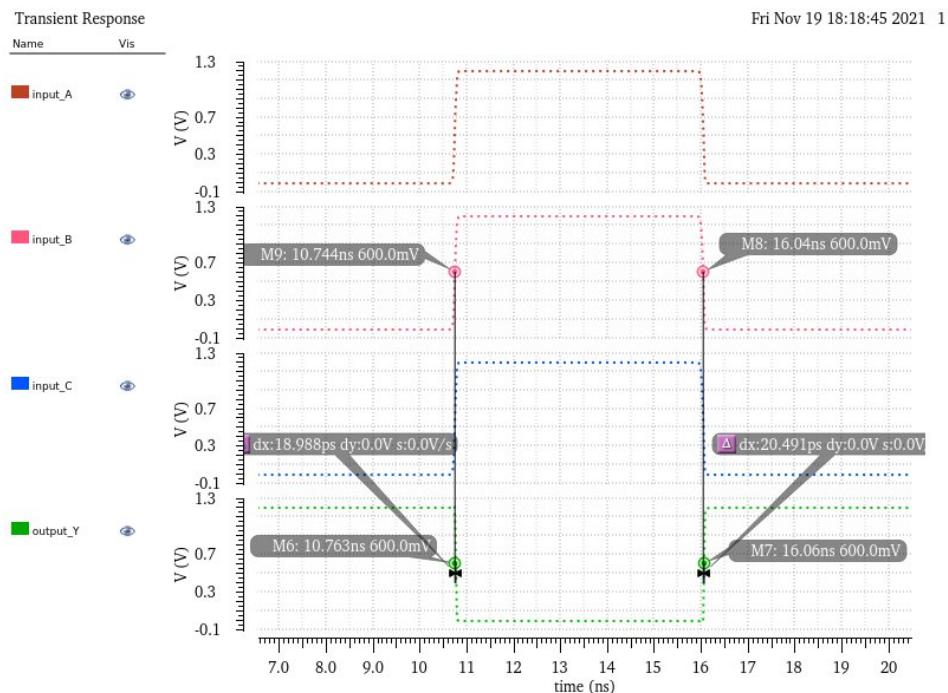
**Figure 17: FO\_1 Transition Delta C to Y**



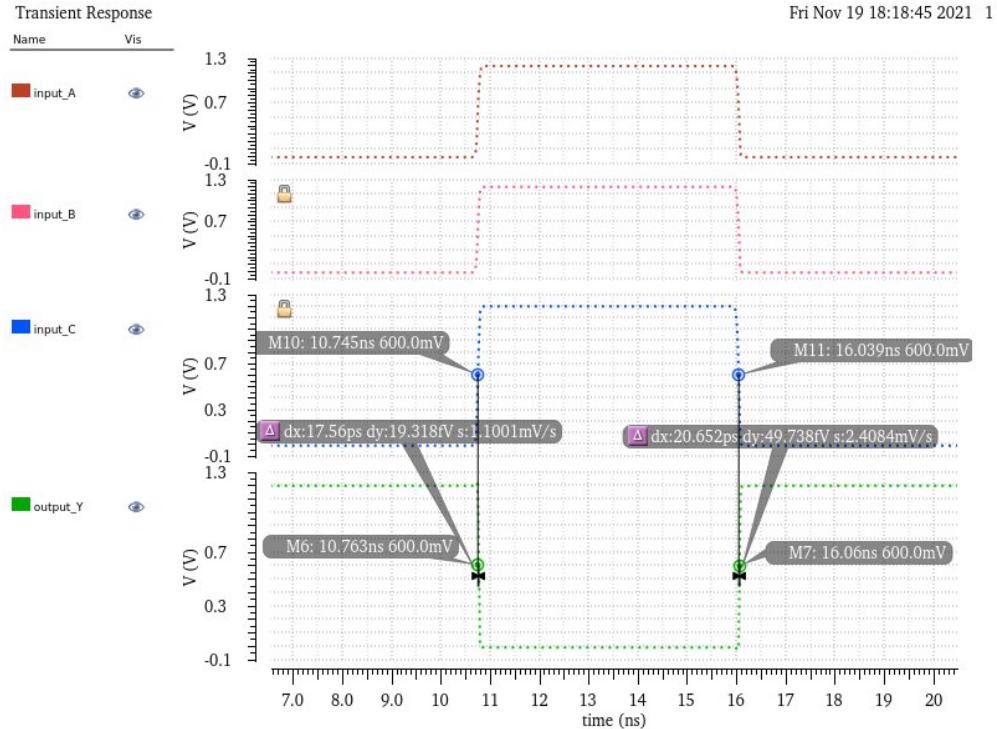
**Fig 18: FO\_2 - Tr and Tf of the 3 inputs A, B, C and output Y  
(Tr and Tf of Y < 30ps)**



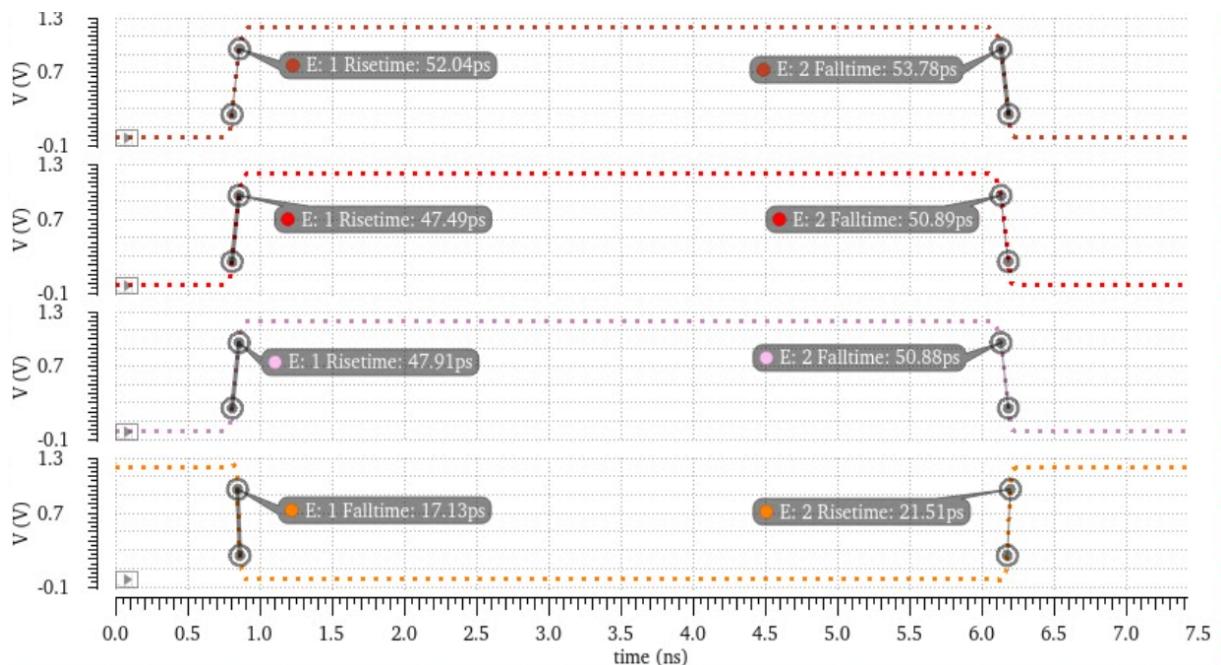
**Fig 19: FO 2 - Tphl and Tplh of the input A and the output Y**  
**(Tphl and Tplh of Y and input A < 35 ps)**



**Fig 20: FO 2 - Tphl and Tplh of the input B and the output Y**  
**(Tphl and Tplh of Y and input A < 35 ps)**



**Fig 21: FO\_2 - Tphl and Tplh of the input C and the output Y**  
**(Tphl and Tplh of Y and input A < 35 ps)**



**Figure 22: FO\_4 Raise Time and Fall Times**

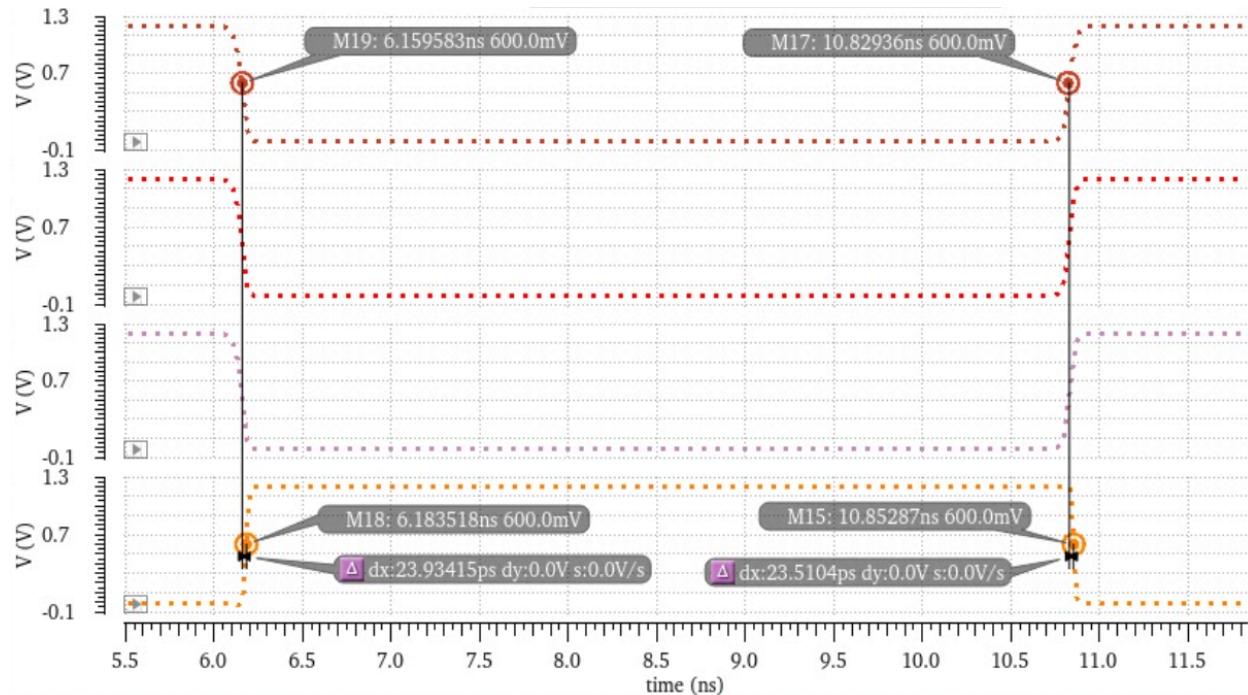


Figure 23: FO\_4 Transition Delta A to Y

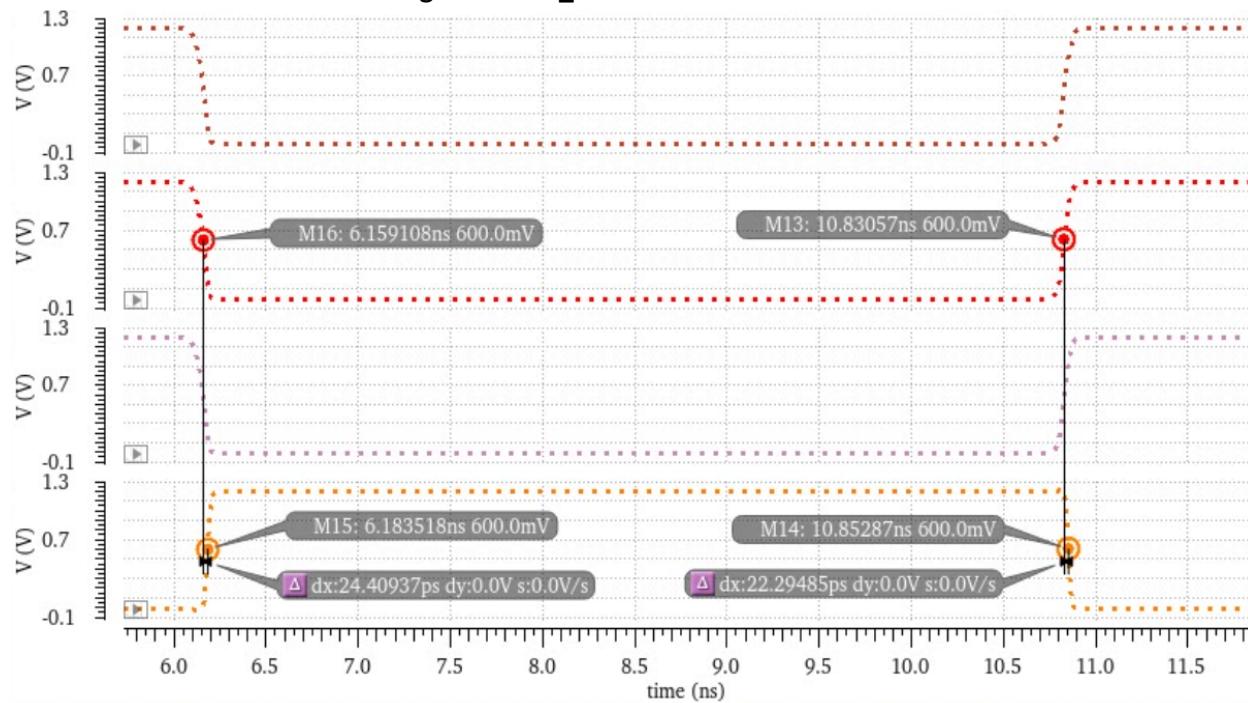


Figure 24: FO\_4 Transition Delta B to Y

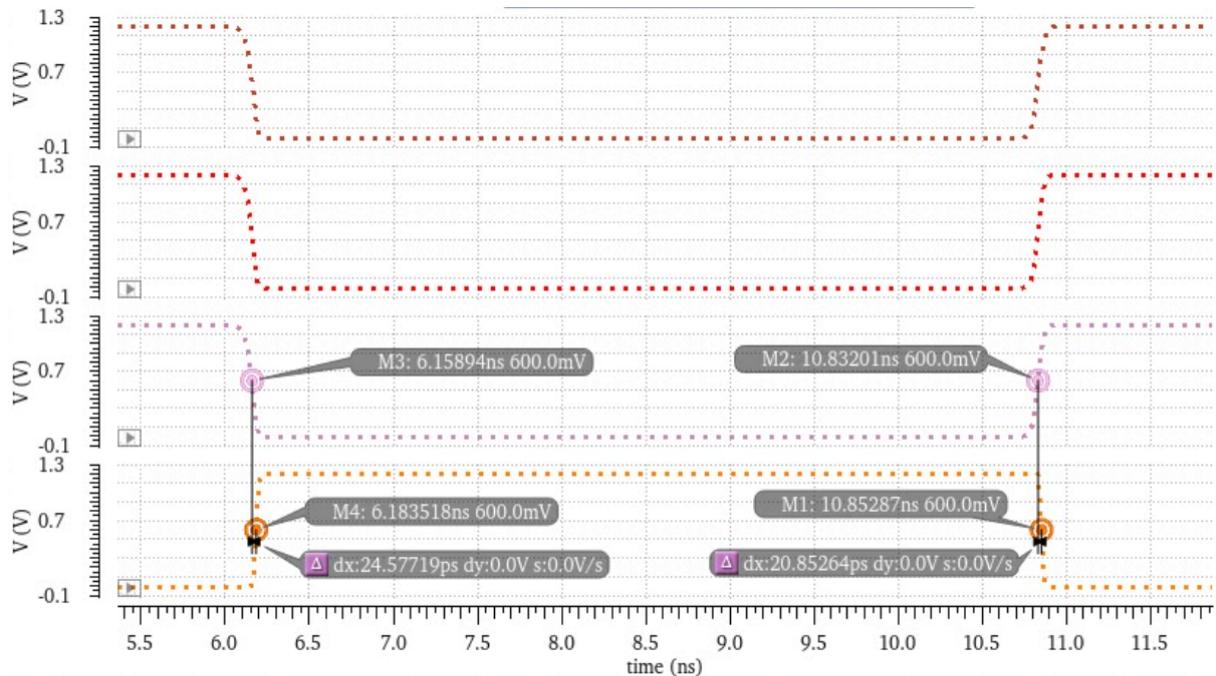


Figure 25: FO\_4 Transition Delta C to Y

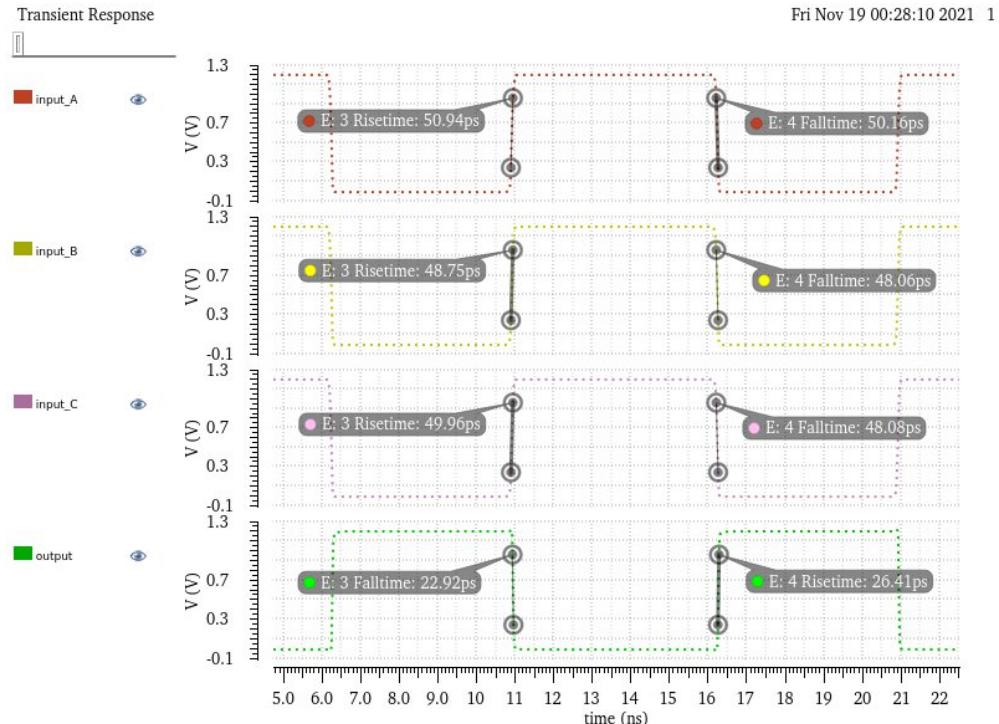
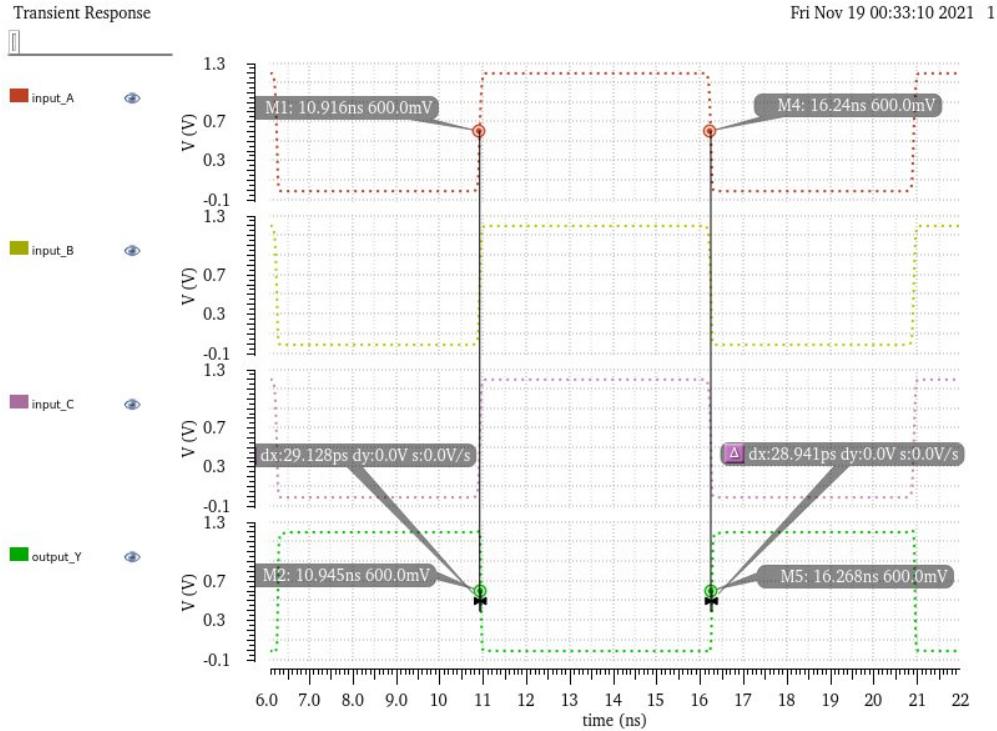
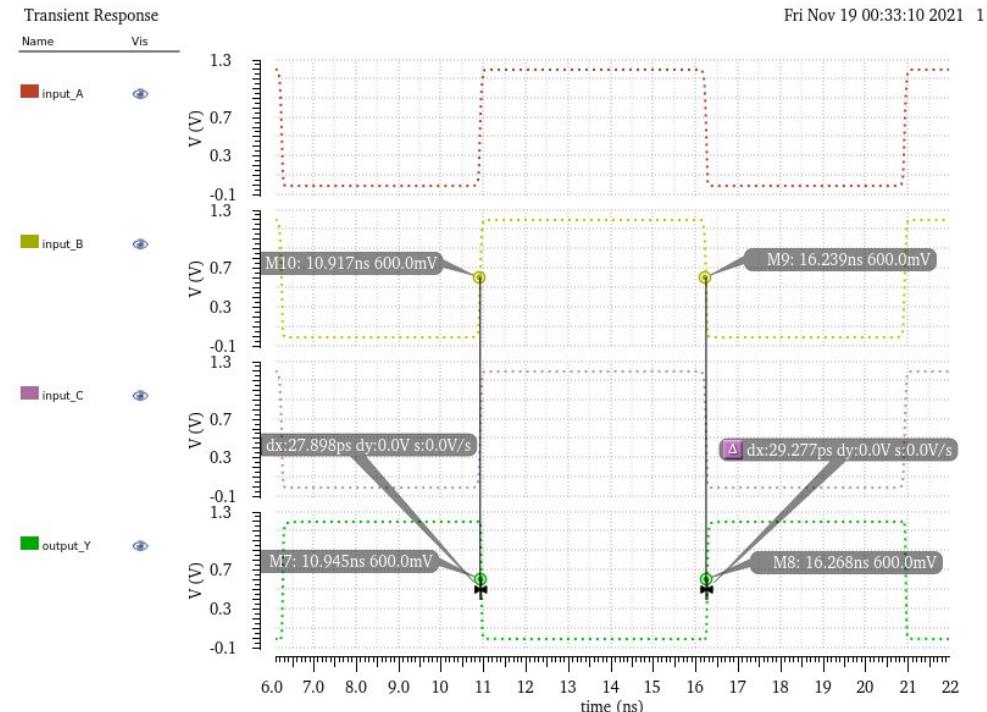


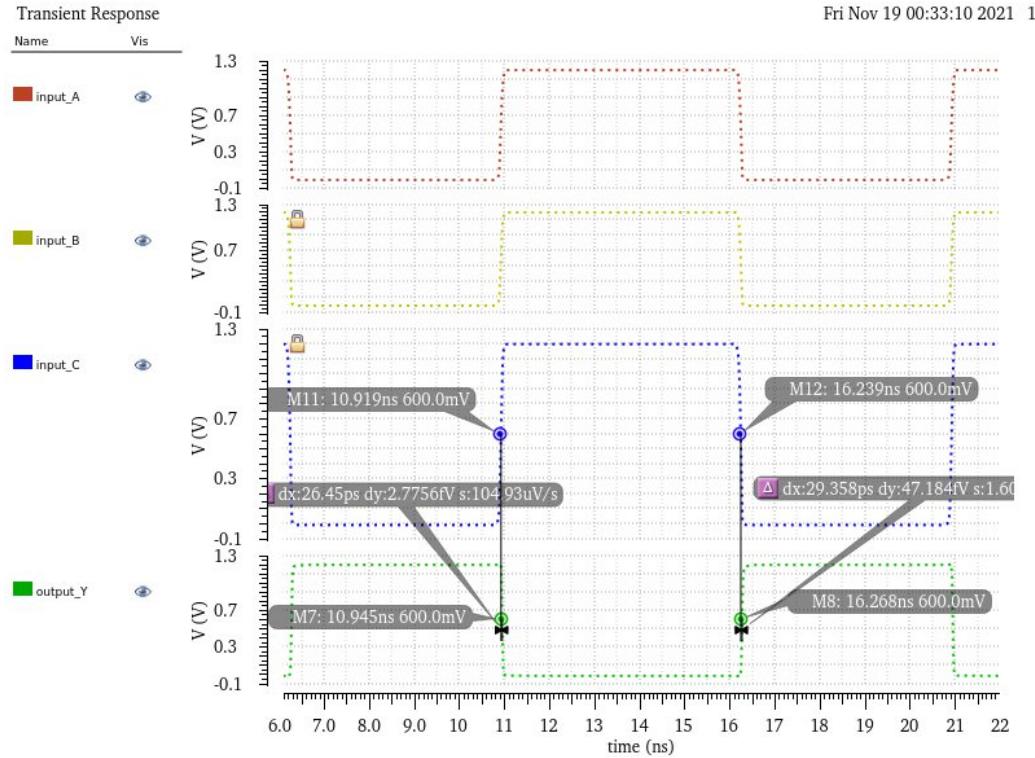
Fig 26: FO\_8 - Tr and Tf of the 3 inputs A, B, C and output Y  
(Tr and Tf of Y < 30ps)



**Fig 27: FO 8 - Tphl and Tplh of the input A and the output Y**  
**(Tphl and Tplh of Y and input A < 35 ps)**



**Fig 28: FO 8 - Tphl and Tplh of the input B and the output Y**  
**(Tphl and Tplh of Y and input A < 35 ps)**



**Fig 29: FO\_8 - Tphl and Tplh of the input C and the output Y**

(Tphl and Tplh of Y and input A < 35 ps)

#### Table of Simulated Results

For various transistor widths and their corresponding tr, tf, tphl and tplh. Highlight the row you selected as shown below.

	CMOS inverter PMOS and NMOS width variation table							
	DUT		Rise/Fall and delay times					
	Width PMOS	Width NMOS	Vpulse		Rise time (ps) (20% to 80%)	Fall time (ps) (80% to 20%)	Propagation (ps) Low to high	Propagation (ps) High to low
	$W_p$ (nm)	$W_N$ (nm)	Rise time (ns)	Fall time (ns)	$T_r$	$T_f$	$T_{plh}$	$T_{phl}$
F00	90	270			137.5	95.63	91.99	106.94
F01	90	270			16.64	13.21	18.52	19.138
F02	90	270	3	2.4	17.95	14.93	20.137	20.48

	90	90	2.7	2.7	22.15	34.0	40.55	20.58
F04	90	135	2.5	2.3	21.15	25.21	30.23	21.38
	90	180	2.5	2.3	20.92	22.05	21.52	16.17
	90	225	2.3	2.2	20.39	20.1	23.57	22.73
	90	270	1.8	2.65	21.51	17.13	23.51	24.557
F08	90	270	2	2.4	22.92	26.41	10.945	16.268

**Please answer the following question:**

Josh modeled the first inverter lab portion. Alex, Nguyen and Joe modeled the second half of the lab compound. All team members contributed to the lab report.

**Conclusion**

We selected the PMOS width to be 90 and the NMOS width to be 270. We chose this size because, in the worst case scenario, there are 3 NMOS transistors in series. Also, In the worst case, there is 1 PMOS in series. Thus the width of the NMOS gate should be 3 times the size as the PMOS. Additionally these values meet the required timing specifications, as seen in the table above.

- Calculate the number of transistors in the longest path of your minimized compound gate **for P(1) and N(3)** stacks separately. Call it MaxSeriesN and MaxSeriesP (worst case)
- Consider the sizes of PFET and NFET obtained in inverter DUT sizing. Call it invP and invN.
- The initial sizing of the compound gate should be:

$$\text{All PFETs widths} = \text{MaxSeriesP} * \text{invP} = 1 * 90\text{nm} = 90\text{nm}$$

$$\text{All NFETs widths} = \text{MaxSeriesN} * \text{invN} = 3 * 90\text{nm} = 270\text{nm}$$

This was used as the default for the first DUT sizing.