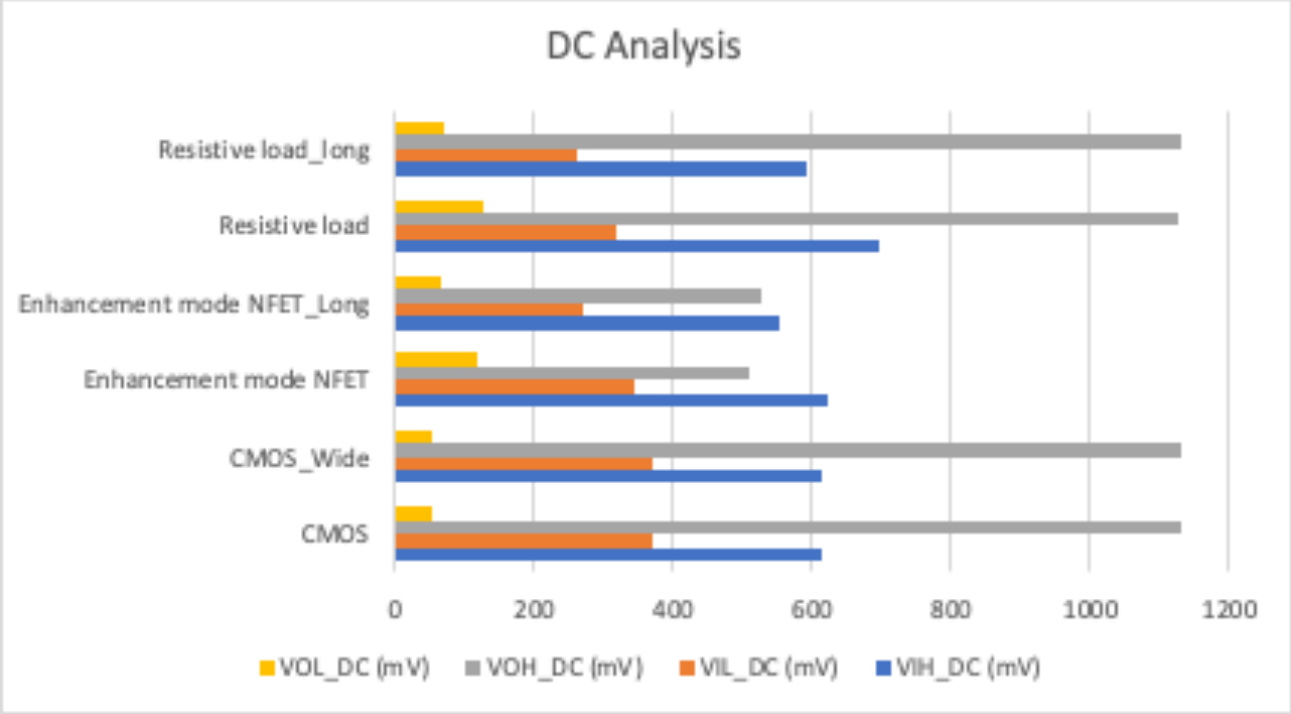
Questions

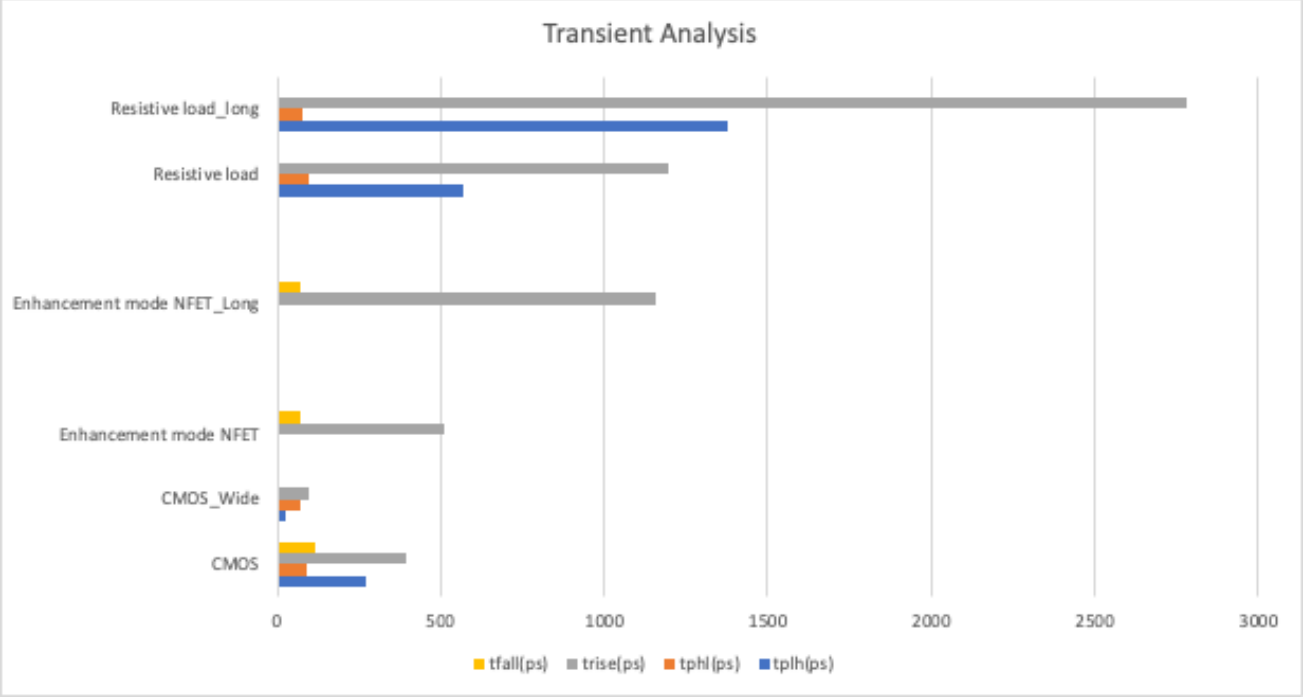
DC Analysis

Type	V_{IH_DC} (mV)	V_{IL_DC} (mV)	V_{OH_DC} (mV)	V_{OL_DC} (mV)
CMOS	613.3	369.4	1129.1	53.07
CMOS_Wide	614.0	369.6	1128.8	53.9
Enhancement mode NFET	624	344.8	508.5	117.8
Enhancement mode NFET_Long	550.6	270.7	528.8	66.0
Resistive load	695.8	316.4	1125	128.5
Resistive load_long	593	261	1131	69.6



Transient Analysis

Type	tp_{lh}(ps)	$\boldsymbol{tp_{hl}}$(ps)	$\boldsymbol{t_{rise}}$(ps)	$\boldsymbol{t_{fall}}$(ps)
CMOS	273.3	92.4	394.6	115.4
CMOS_Wide	27.66	70.85	94.72	29.35
Enhancement mode NFET	NA (didn't reach 1.2V)	NA (didn't reach 1.2V)	511.1	68.02
Enhancement mode NFET_Long	NA (didn't reach 1.2V)	NA (didn't reach 1.2V)	1158	72.77
Resistive load	567	95	1194	120
Resistive load_long	1378	80	2783	112



1. **Explain in your own words the variation of the DC output voltages V_{OH} and V_{OL} for the four inverters? In particular focus on the differences noted earlier in the NFET connected inverters.**

V_{OL} : The CMOS devices both match and are the strongest low out of the six device. Out of the other four devices, the 'long' models almost match the CMOS devices.

V_{OH} : is only weak in the Enhancement mode inverter. This is likely due to the fact that the input VDD is divided over the pullup NMOS device.

It is clear the DC analysis of the Complementary MOS configuration is most ideal. While the NMOS devices are very similar with the output signal being the distinct difference. Where the resistive long model closely resembles the characteristics of the CMOS.

Explain in your own words the variation of the switching times for all the inverters?

Output propagation delay

t_{phl} high to low: The enhancement inverter has a severely reduced output, leaving it out of the comparison. With all other devices being comparable.

t_{plh} low to high: The wide CMOS_Wide has the fastest propagation delay, due to its dimensions. The wider channel allows more current and voltage propagation. Conversely, the Resistive long device has a higher resistance and path, for this reason the I/O is significantly delayed.

Rise and fall time

t_{rise}: The rise time on the resistive loads are significantly longer. This is due to the large resistances converting energy to heat. This results in less energy being delivered to the output from the drain. Thus, It takes longer to build up a potential. V=J/C

Note: Calculation for resistor long was close but could have been closer.

t_{fall}:

The differences are due to nmos and pmos requiring different voltage gate levels for 1 and 0 and also that these also give a strong 1 or strong 0 respectively. This is what gave the NFET a quicker response time for the high end on DC but slower than the CMOS for the OH. The resistive OL values were similar to the NFET because they have a similar pulldown mechanic.

2. **List out the major drawbacks and benefits of using a NFET load and resistor for signal inversion from area, VTC (Voltage Transfer Characteristic), noise margin, leakage and fabrication point of view. Why do you think CMOS has become so popular in recent times?**
   Low static power consumption and also has high noise immunity. CMOS doesn't have resistors so it uses less energy than a resistor inverter. They also have less complexity and create less heat. CMOS can propagate 0 and 1 but NMOS can only do logic 1 or VDD-Vt. CMOS can switch to a VOL the fastest and rise time is also the fastest. It takes less energy in switching time.

3. **What happens if PMOS and NMOS are interchanged in an inverter connection?**

   The three possible CMOS inverter configurations
   1. NMOS pull up and PMOS pull down: signal is buffer, with weak logic 1.
   2. NMOS pull up and pull down: the signal is inverted with a weak logic 1.
   3. PMOS pull up and pull down: the output is always logic 1.

   Where should you measure the output to get the desired inverted signal after interchanging their positions?

   There is no inverted signal as the circuit becomes a buffer instead of an inverter by switching the pmos and nmos.

4. **What are the roles and responsibilities of each member of your lab team? Who did what part of the lab?**
   a. Alex Beaulier - NFET Long and Normal Simulations.
   b. Joseph Wetzel - CMOS wide and Normal Simulations
   c. Josh Horejs - Resistive loads
   d. All members - Final questions document