

# CMOS Inverter

## Introduction and Physical Properties

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### 1) CMOS Inverter Cell Description

The CMOS Inverter cell is a 1 input 1 output device. When used in a digital circuit it acts as a logic NOT gate. 2 inverter circuits can be used as a buffer and a repeater since the output flows from  $V_{dd}$  and ground and not from the input.

### 2) CMOS Inverter Cell Symbol

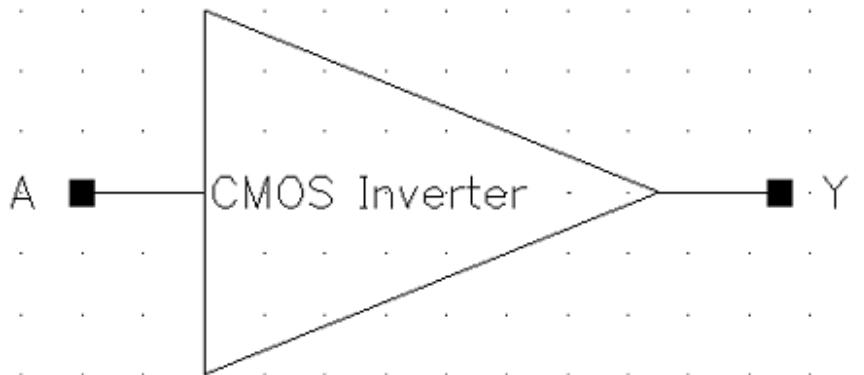
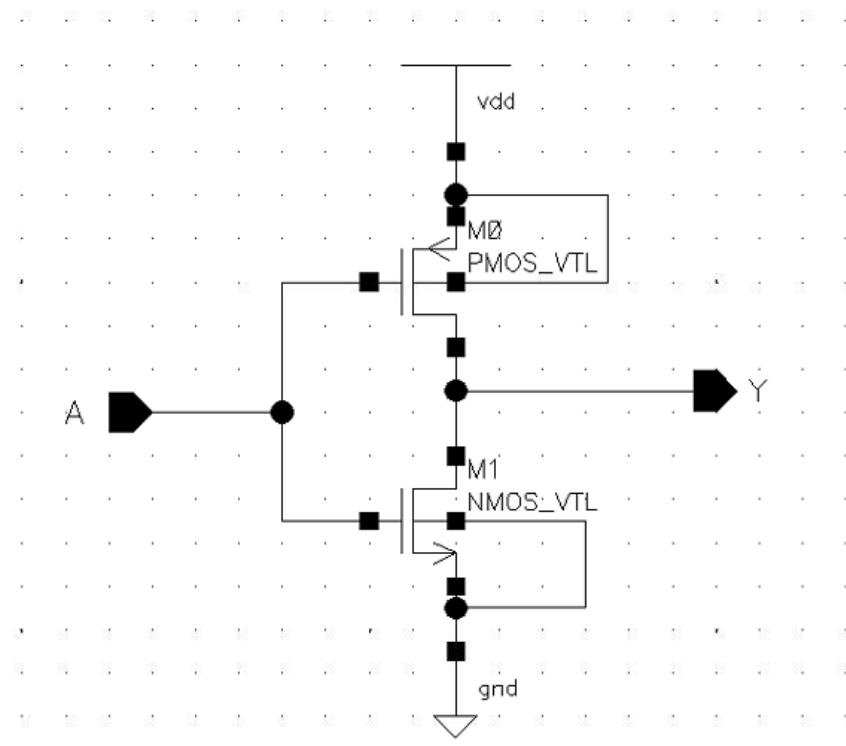


Figure 1: Symbol for CMOS Inverter

### 3) CMOS Inverter Cell Truth Table

CMOS Inverter Cell Truth Table	
Inputs	Outputs
0	1
1	0

### 4) CMOS Inverter Cell Schematic Diagram



**Figure 2: Circuit for CMOS Inverter**

## 5) Transistor Dimensions

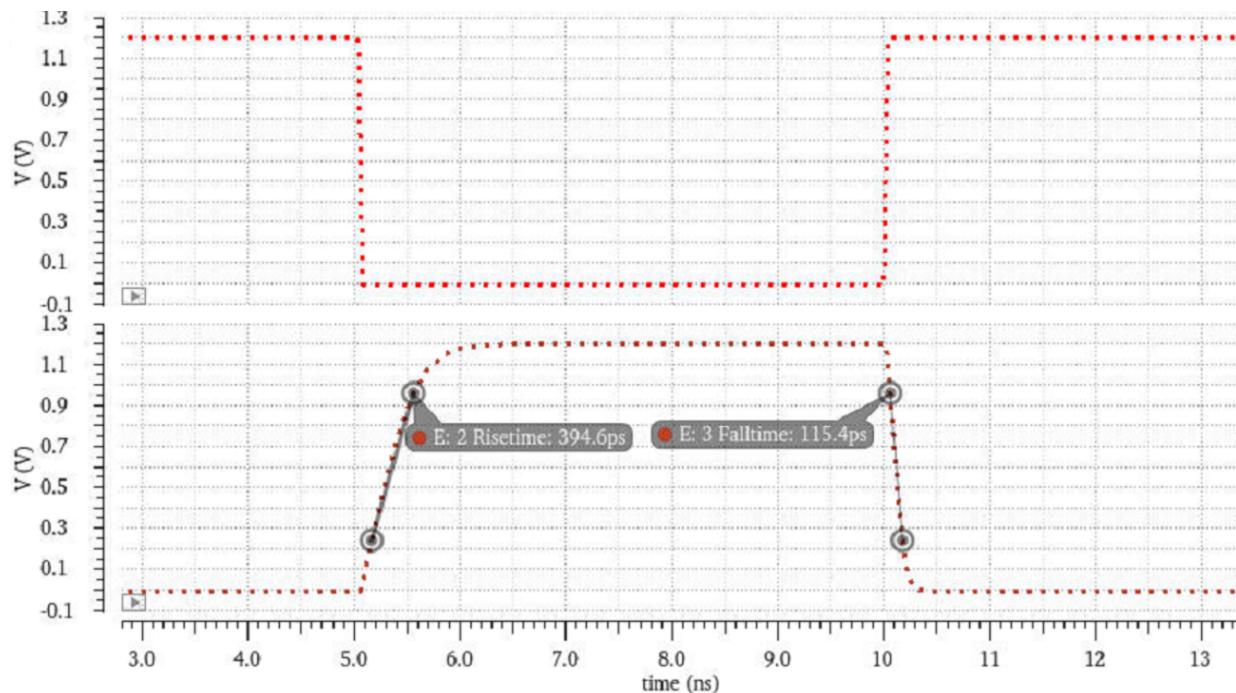
Transistor Dimensions		
Transistor Instance Number	Length (nm)	Width (nm)
NMOS (M1)	50	90
PMOS (M0)	50	90

## Performance Analysis

### 6,7) CMOS Inverter Cell Output Rise/Fall Time Data

Input X: Output Rise Time Data $t_r$ (ps)					
Input Rise/ Fall Time	Output Load (FO <sub>x</sub> )				
	0	1	2	4	8
40				394.6	

Input X: Output Fall Time Data $t_f$ (ps)					
Input Rise/ Fall Time	Output Load (FO <sub>x</sub> )				
	0	1	2	4	8
40				115.4	



**Figure 3: Plot of The Input and Output Waveforms with Rise and Fall Times**

## 8.9) CMOS Inverter Cell Propagation Delays

Data Worst Case Low to High Propagation Delay Data $t_{plh}$ (ps)					
Input Rise/ Fall Time	Output Load (FO <sub>x</sub> )				
	0	1	2	4	8
40				273.3	

Data Worst Case High to Low Propagation Delay Data $t_{phl}$ (ps)					
Input Rise/ Fall Time	Output Load (FO <sub>x</sub> )				
	0	1	2	4	8
40				92.4	

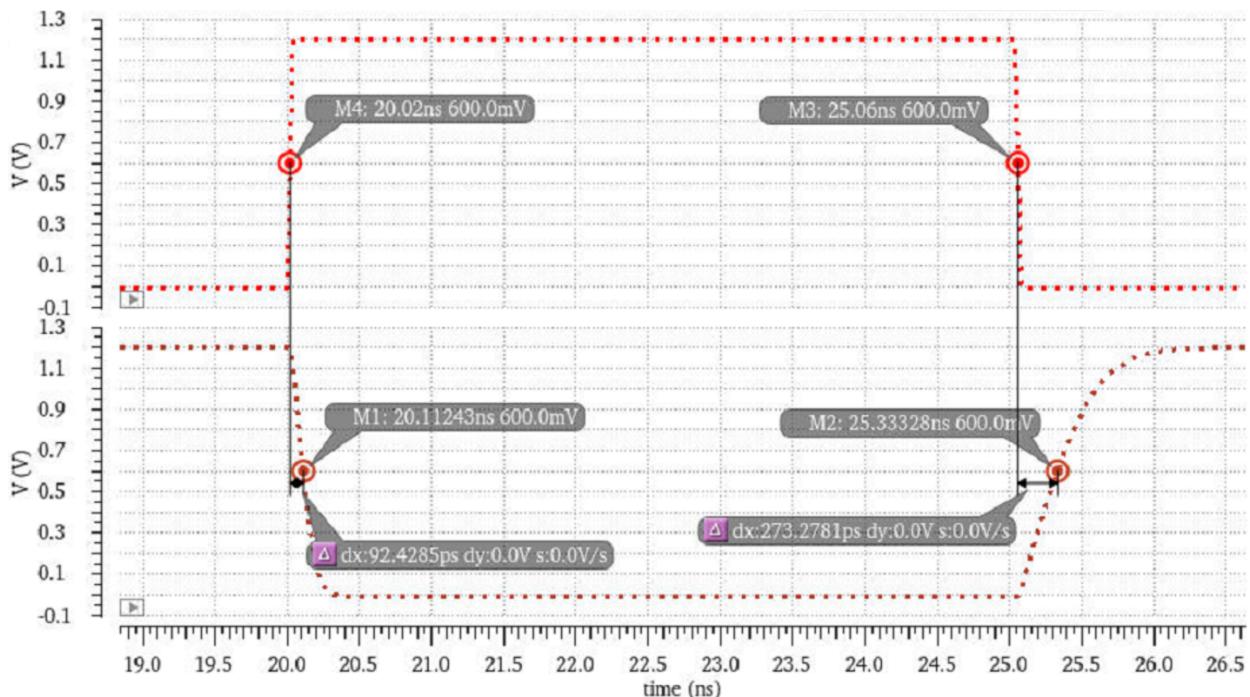
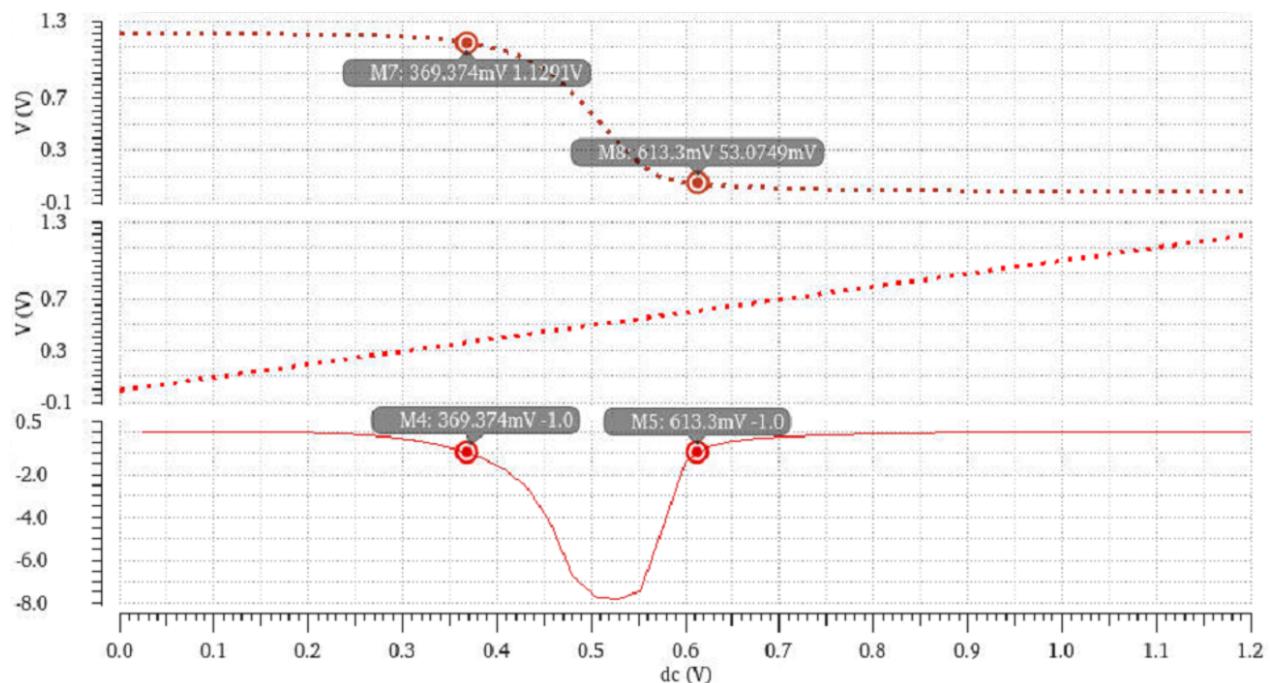


Figure 4: Plot of The Input and Output Waveforms with Propagation Delay Times

## 10.) CMOS Inverter Cell DC Analysis

Type	$V_{IH\_DC}$ (mV)	$V_{IL\_DC}$ (mV)	$V_{OH\_DC}$ (mV)	$V_{OL\_DC}$ (mV)
CMOS	613.3	369.4	1129.1	53.07



**Figure 5: Plot of DC Sweep with the Derivative of the Output Response**

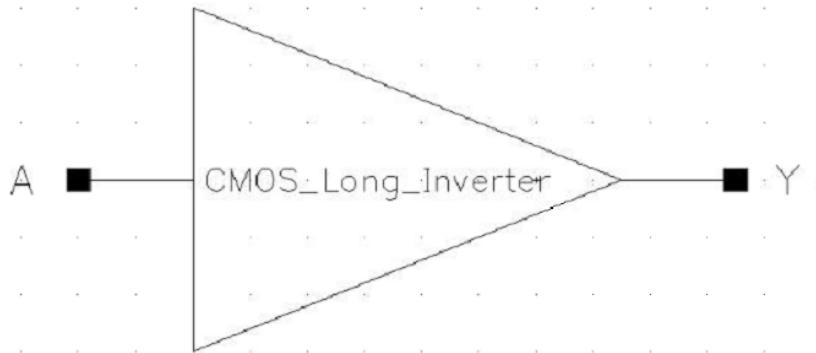
CMOS Long-Gate Inverter  
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10/29/2021  
Introduction and Physical Properties

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### 1) CMOS Long-Gate Inverter Cell Description

The CMOS Long-Gate Inverter cell is a 1 input 1 output device. When used in a digital circuit it acts as a logic NOT gate. 2 inverter circuits can be used as a buffer and a repeater since the output flows from  $V_{dd}$  and ground and not from the input. This Inverter has a larger gate to better the transient response.

### 2) CMOS Long-Gate Inverter Cell Symbol



**Figure 6: Symbol for CMOS Long-Gate Inverter**

### 3) CMOS Long-Gate Inverter Cell Truth Table

Cell Truth Table	
Inputs	Outputs
0	1
1	0

#### 4) CMOS Long-Gate Inverter Cell Schematic Diagram

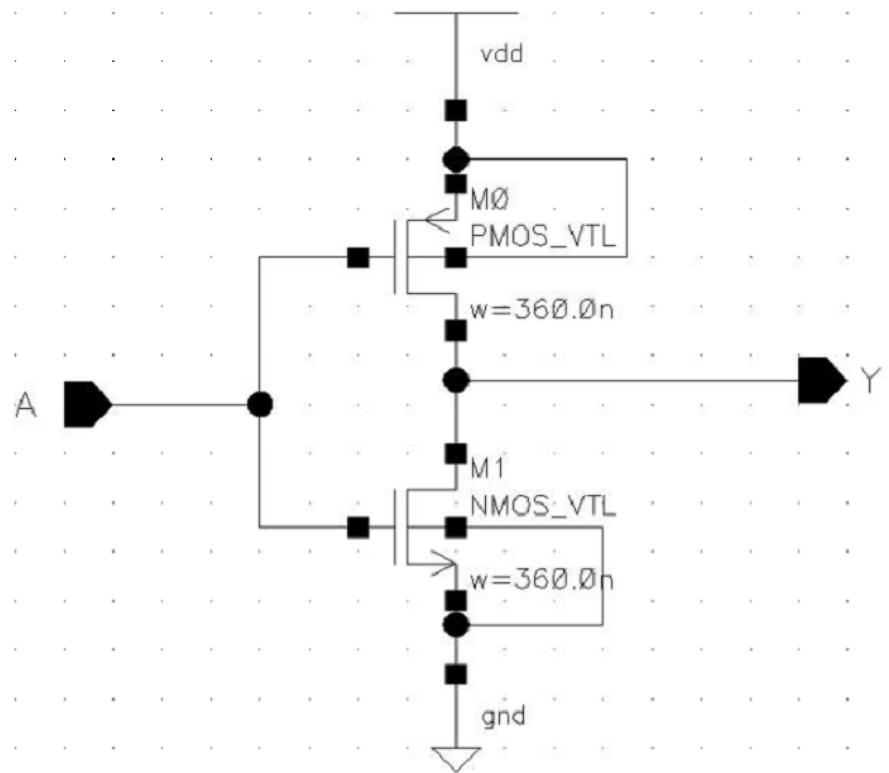


Figure 7: Circuit for CMOS Long-Gate Inverter

#### 5) Transistor Dimensions

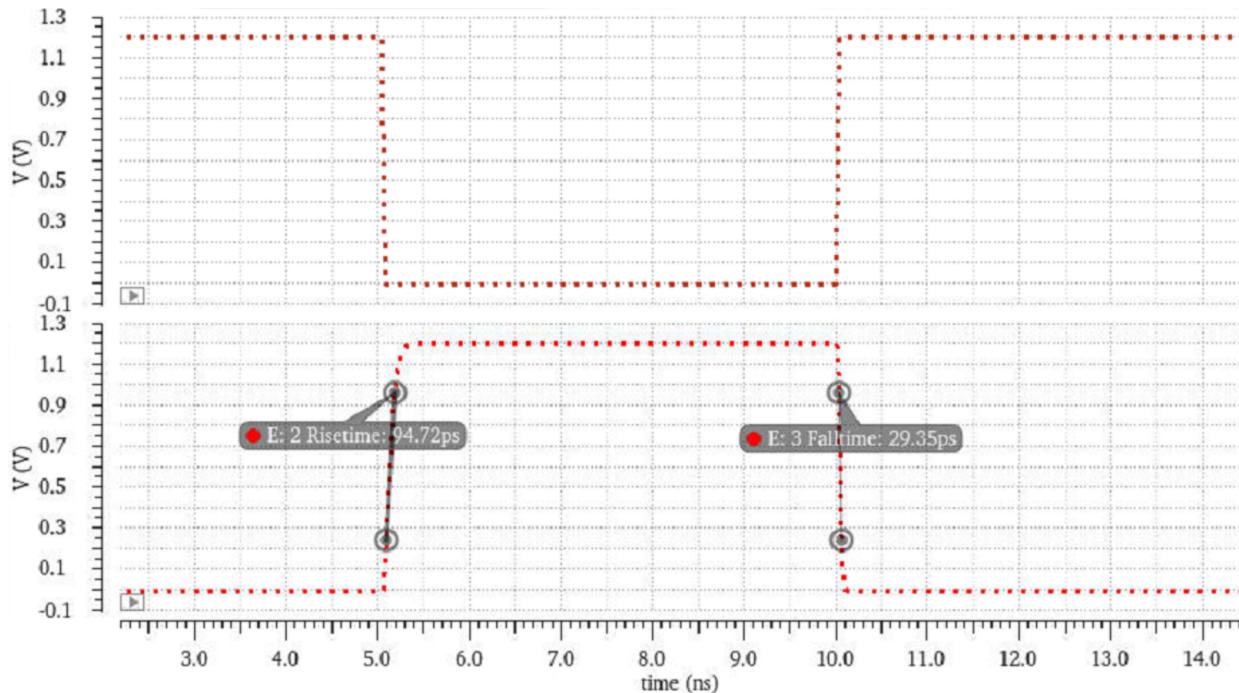
Transistor Dimensions		
Transistor Instance Number	Length (nm)	Width (nm)
NMOS (M1)	50	360
PMOS (M0)	50	360

## Performance Analysis

### 6,7) CMOS Long-Gate Inverter Cell Output Rise/Fall Time Data

Input X: Output Rise Time Data $t_r$ (ps)					
Input Rise/ Fall Time	Output Load (FO <sub>x</sub> )				
	0	1	2	4	8
40				94.72	

Input X: Output Fall Time Data $t_f$ (ps)					
Input Rise/ Fall Time	Output Load (FO <sub>x</sub> )				
	0	1	2	4	8
40				29.35	



**Figure 8: Plot of The Input and Output Waveforms with Rise and Fall Times**

## 8,9) CMOS Long-Gate Inverter Cell Propagation Delays

Data Worst Case Low to High Propagation Delay Data $t_{plh}$ (ps)					
Input Rise/ Fall Time	Output Load (FOx)				
	0	1	2	4	8
40				27.66	

Data Worst Case High to Low Propagation Delay Data $t_{phl}$ (ps)					
Input Rise/ Fall Time	Output Load (FOx)				
	0	1	2	4	8
40				70.85	

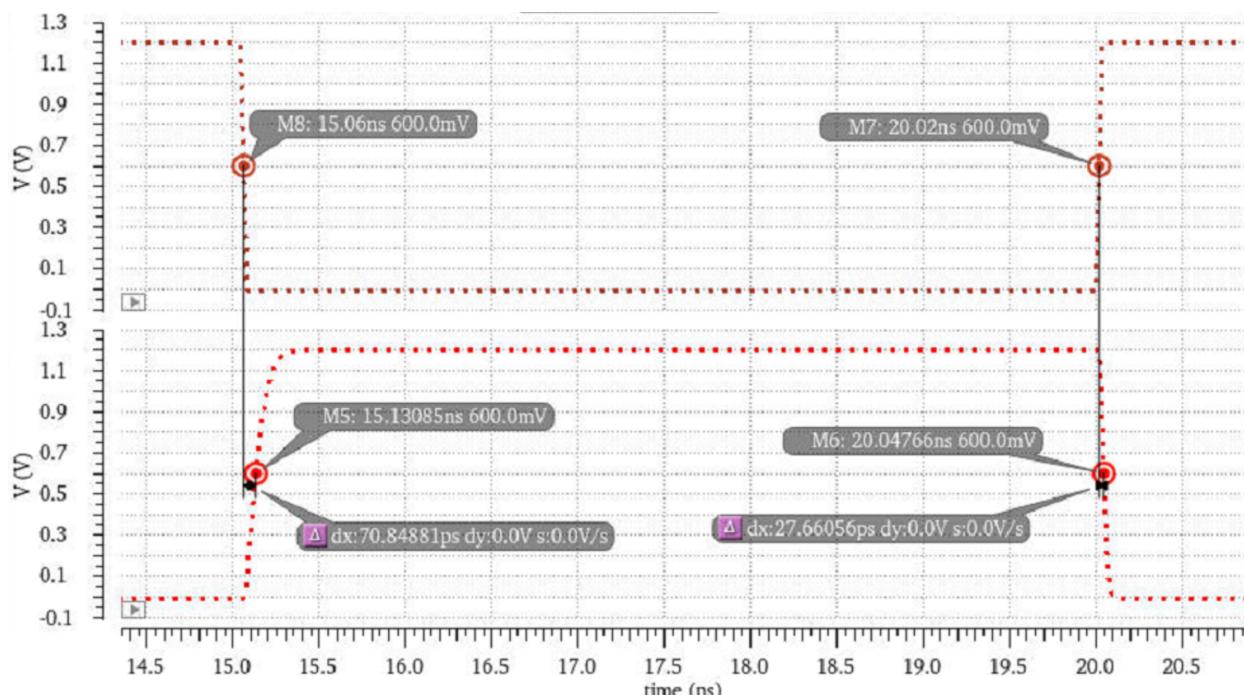
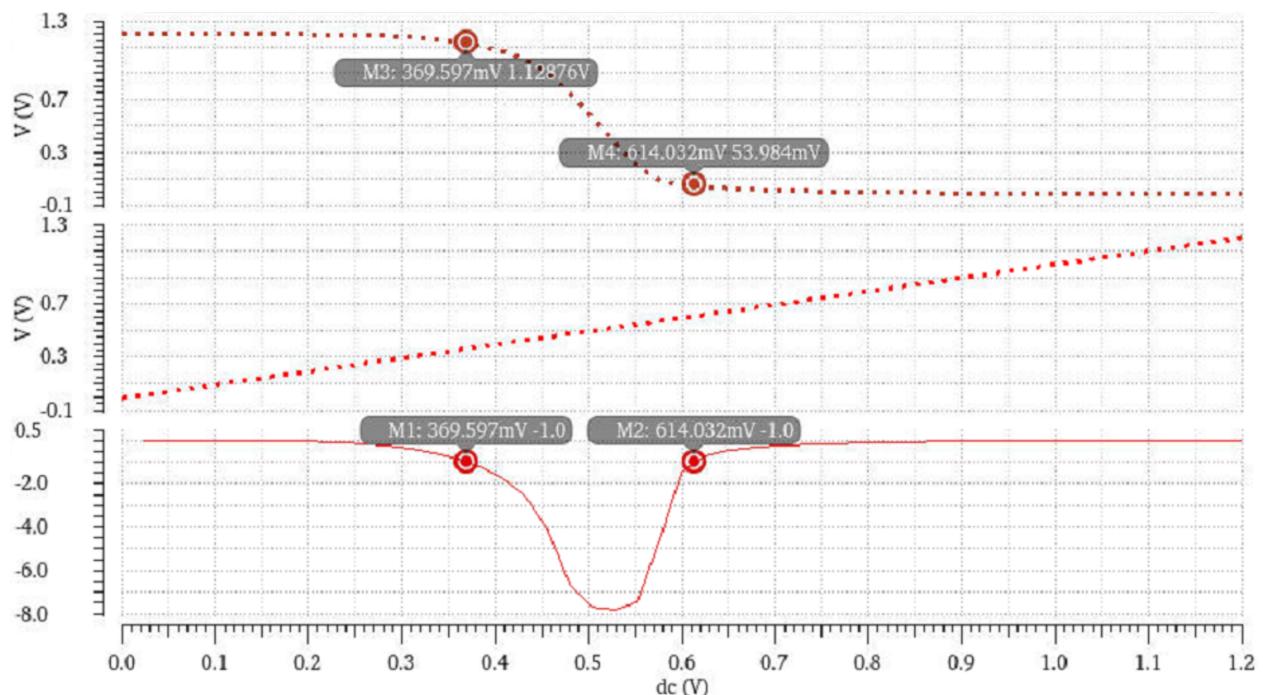


Figure 9: Plot of The Input and Output Waveforms with Propagation Delay Times

## 10.) CMOS Long-Gate Inverter Cell DC Analysis

Type	$V_{IH\_DC}$ (mV)	$V_{IL\_DC}$ (mV)	$V_{OH\_DC}$ (mV)	$V_{OL\_DC}$ (mV)
CMOS Long	614.0	369.6	1128.8	53.9



**Figure 10: Plot of DC Sweep with the Derivative of the Output Response**