Resistive Load Inverter
Introduction and Physical Properties

1) Cell Description

By using the equivalent resistance of the enhancement NMOS inverter, the Id is equivalent. The NMOS being a normally closed switch, an input low, allows VDD propagation to the output. When the input is high the NMOS creates a direct path to ground causing a logical low.

2) Cell Symbol

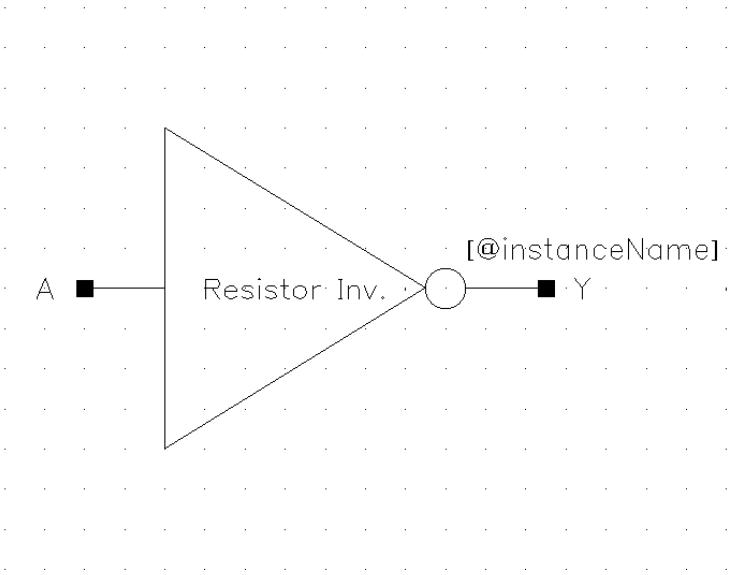

Figure 1: Symbol for Resistive Load Inverter

3) Cell Truth Table

Cell Truth Table	
Inputs	Outputs
0	1
1	0

4) Cell Schematic Diagram

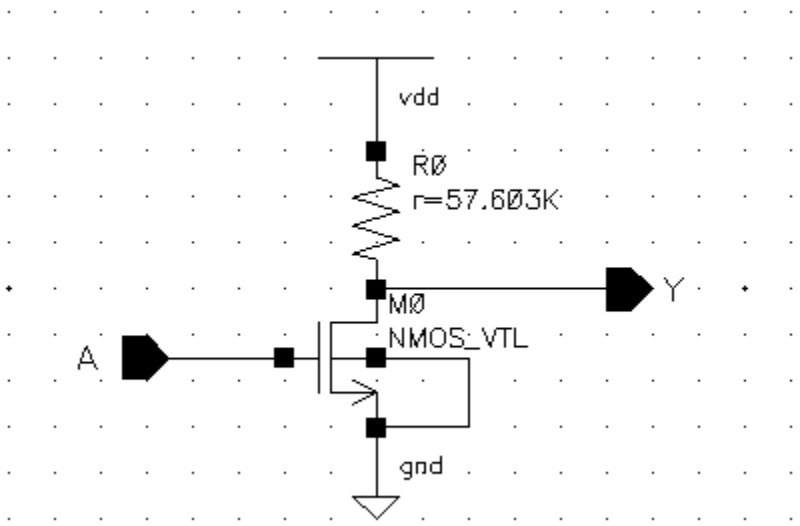

Figure 2: Circuit for Resistive Load Inverter

5) Transistor Dimensions

Transistor Dimensions		
Transistor Instance Number	Length (nm)	Width (nm)
NMOS (M0)	90	50

Performance Analysis

6,7) Output Rise/Fall Time Data

Input X: Output Rise Time Data t_r (ps)					
Input Rise/ Fall Time	Output Load (FOx)				
	0	1	2	4	8
40				1,194	

Input X: Output Fall Time Data t_f (ps)					
Input Rise/ Fall Time	Output Load (FOx)				
	0	1	2	4	8
40				120	

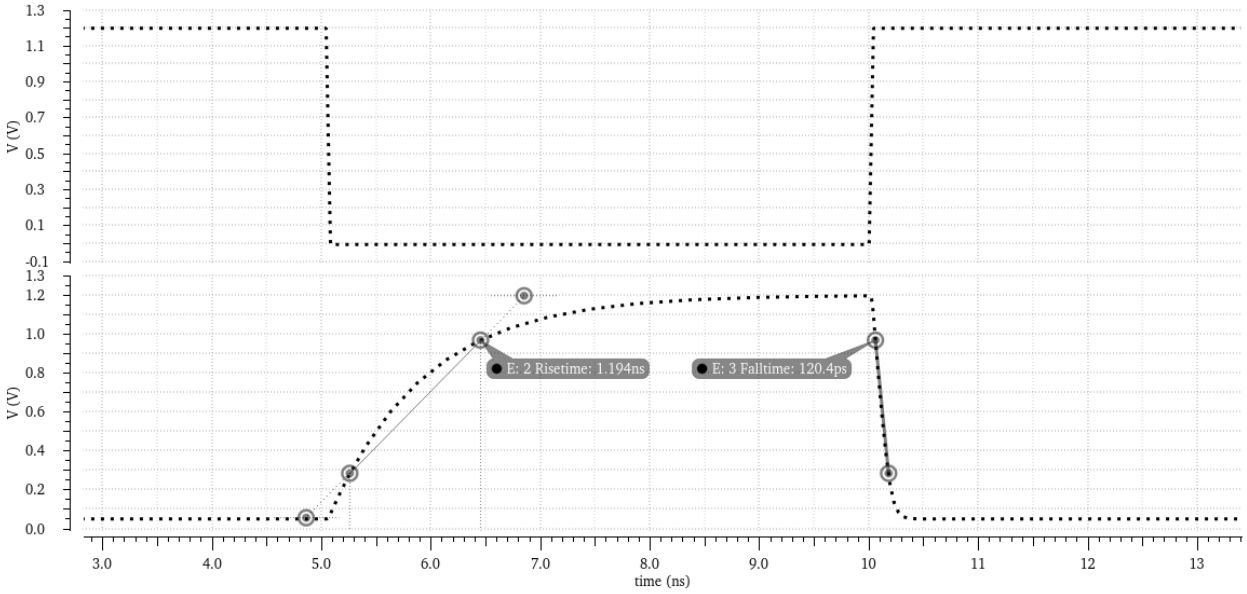

Figure 3: Plot of The Input and Output Waveforms with Rise and Fall Times

8,9) Propagation Delays

Data Worst Case Low to High Propagation Delay Data t_{plh} (ps)					
Input Rise/ Fall Time	Output Load (FOx)				
	0	1	2	4	8
40				95	

Data Worst Case High to Low Propagation Delay Data t_{phl} (ps)					
Input Rise/ Fall Time	Output Load (FOx)				
	0	1	2	4	8
40				567	

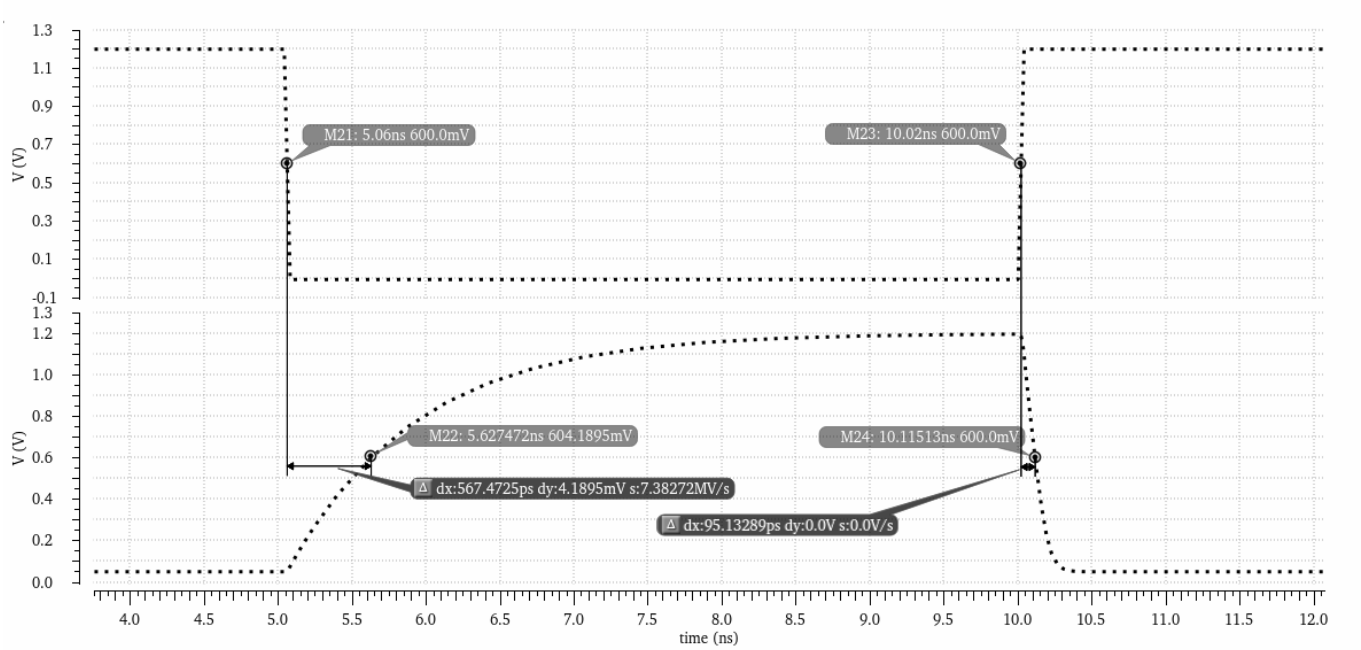

Figure 4: Plot of The Input and Output Waveforms with Propagation Delay Times

10.) DC Analysis

V_{IH_DC} (mV)	V_{IL_DC} (mV)	V_{OH_DC} (mV)	V_{OL_DC} (mV)
695.8	316.4	1125	128.5

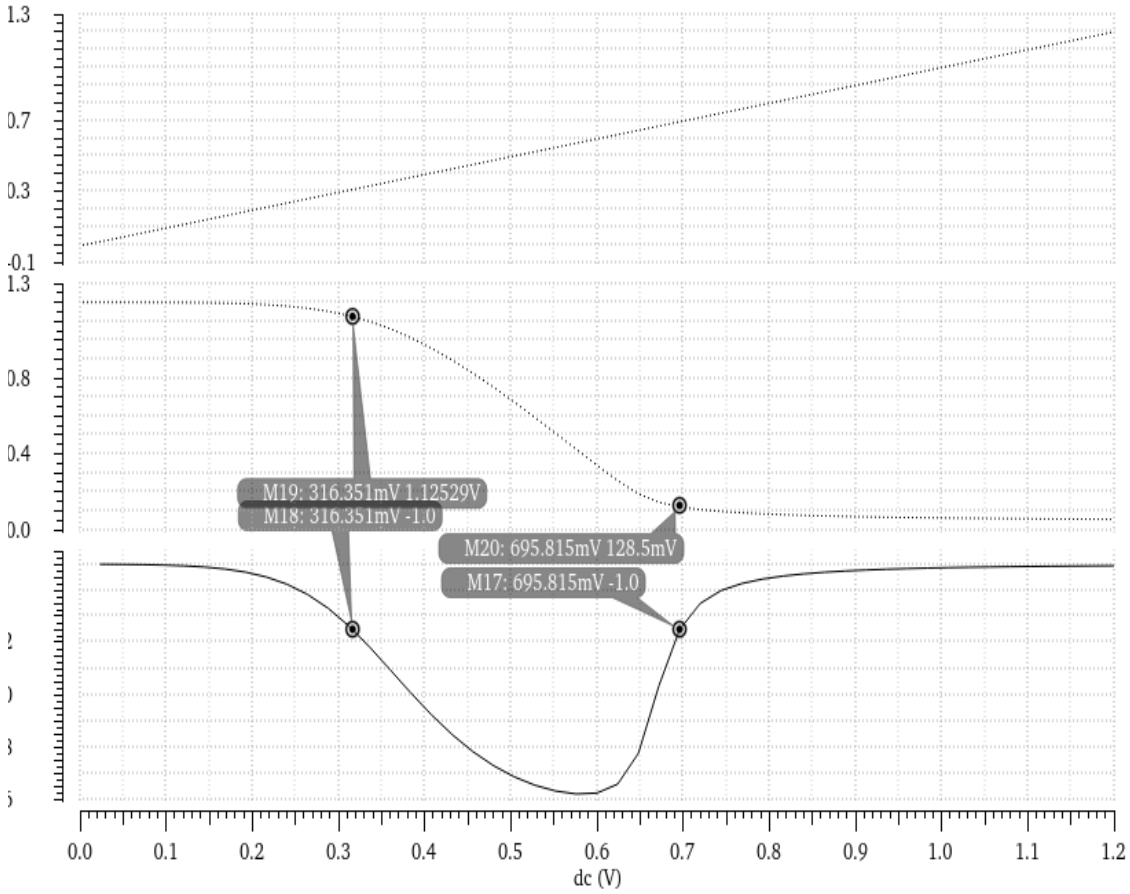

Figure 5: Plot of DC Sweep with the Derivative of the Output Response

Long-Gate Resistive Load Inverter
Joseph Wetzel, Alex Beaulier, Josh Horejs
Group 17
10/29/2021
Introduction and Physical Properties

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1) Cell Description

By using the equivalent resistance of the enhancement NMOS inverter, the Id is equivalent. The 'enhancement' NMOS being a normally off switch, an input low, allows VDD propagation to the output. When the input is high the NMOS creates a direct path to ground causing a logical low.

2) Cell Symbol

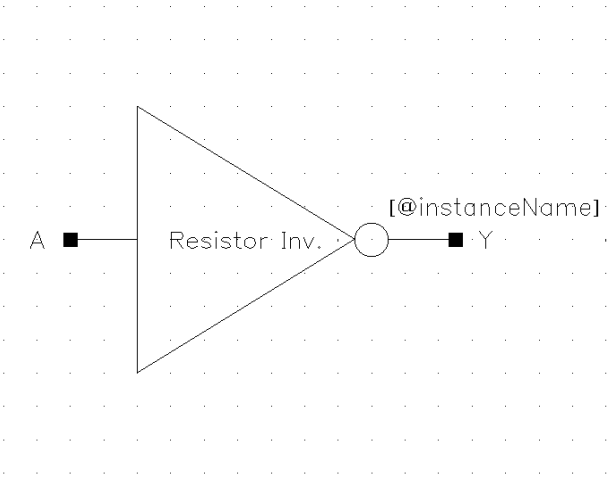

Figure 6: Symbol for Resistive Load Long-Gate Inverter

3) Cell Truth Table

Cell Truth Table	
Inputs	Outputs
0	1
1	0

4) Cell Schematic Diagram

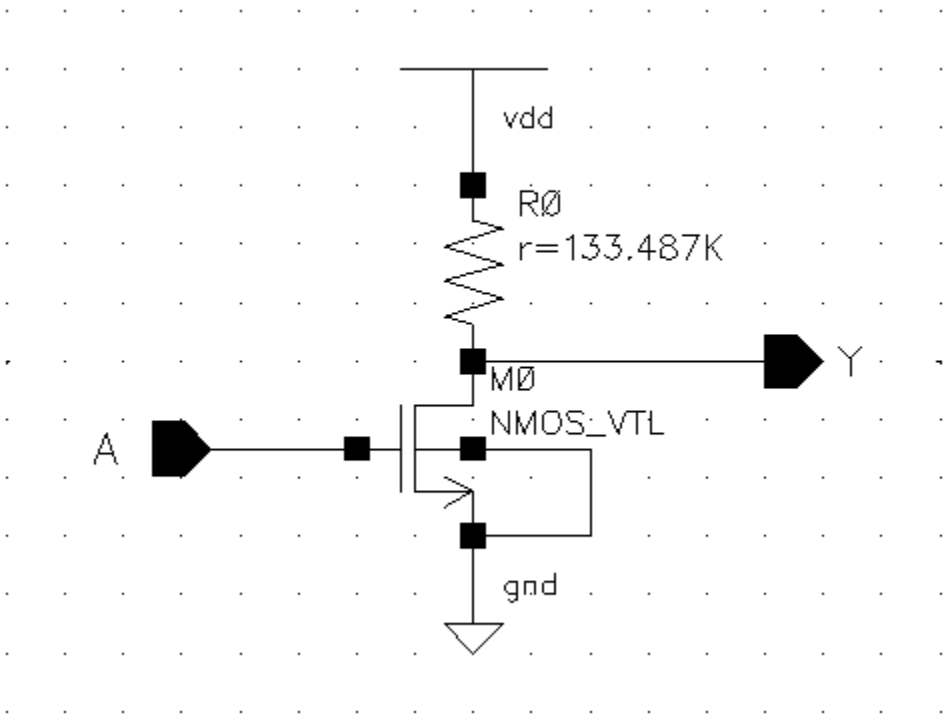

Figure 7: Circuit for Resistive Load Long-Gate Inverter

5) Transistor Dimensions

Transistor Dimensions		
Transistor Instance Number	Length (nm)	Width (nm)
NMOS	90	50

Performance Analysis

6,7) Output Rise/Fall Time Data

Input X: Output Rise Time Data t_r (ps)					
Input Rise/ Fall Time	Output Load (FOx)				
	0	1	2	4	8
40				2783	

Input X: Output Fall Time Data t_f (ps)					
Input Rise/ Fall Time	Output Load (FOx)				
	0	1	2	4	8
40				112	

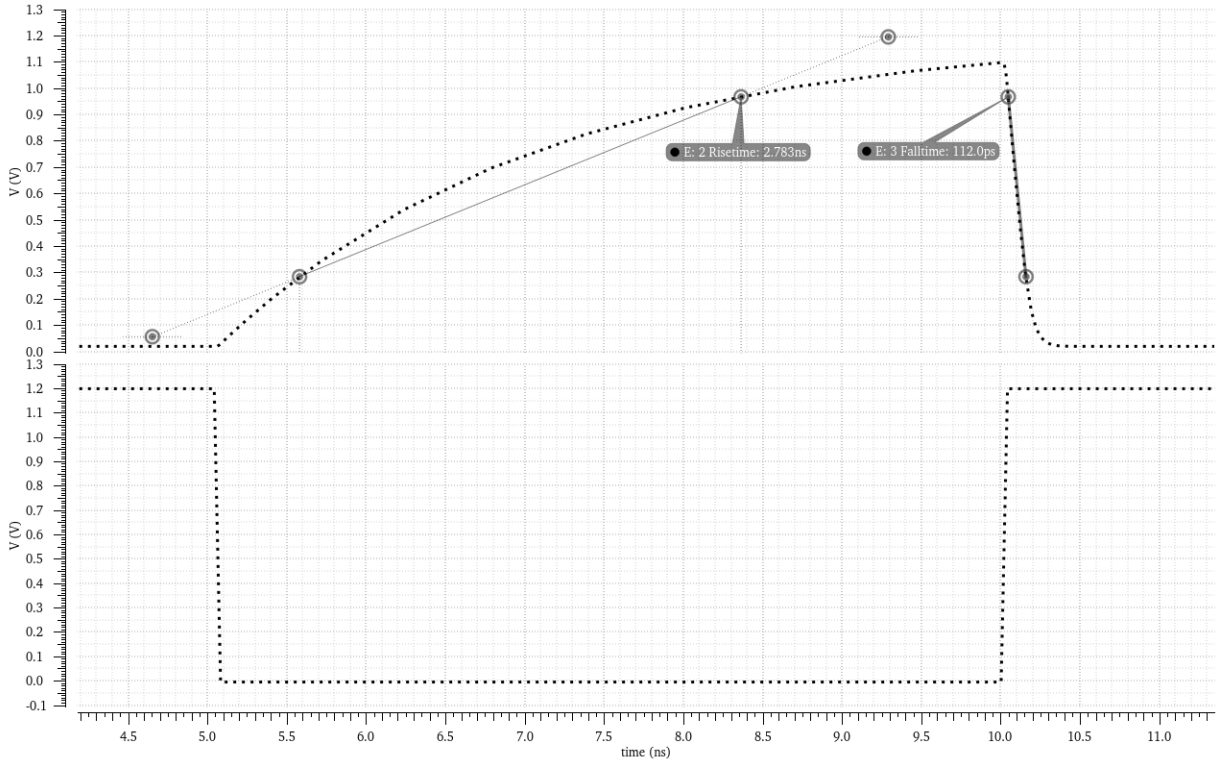

Figure 8: Plot of The Input and Output Waveforms with Rise and Fall Times

8,9) Propagation Delays

Data Worst Case Low to High Propagation Delay Data t_{plh} (ps)					
Input Rise/ Fall Time	Output Load (FOx)				
	0	1	2	4	8
40				1378	

Data Worst Case High to Low Propagation Delay Data t_{phl} (ps)					
Input Rise/ Fall Time	Output Load (FOx)				
	0	1	2	4	8
40				80	

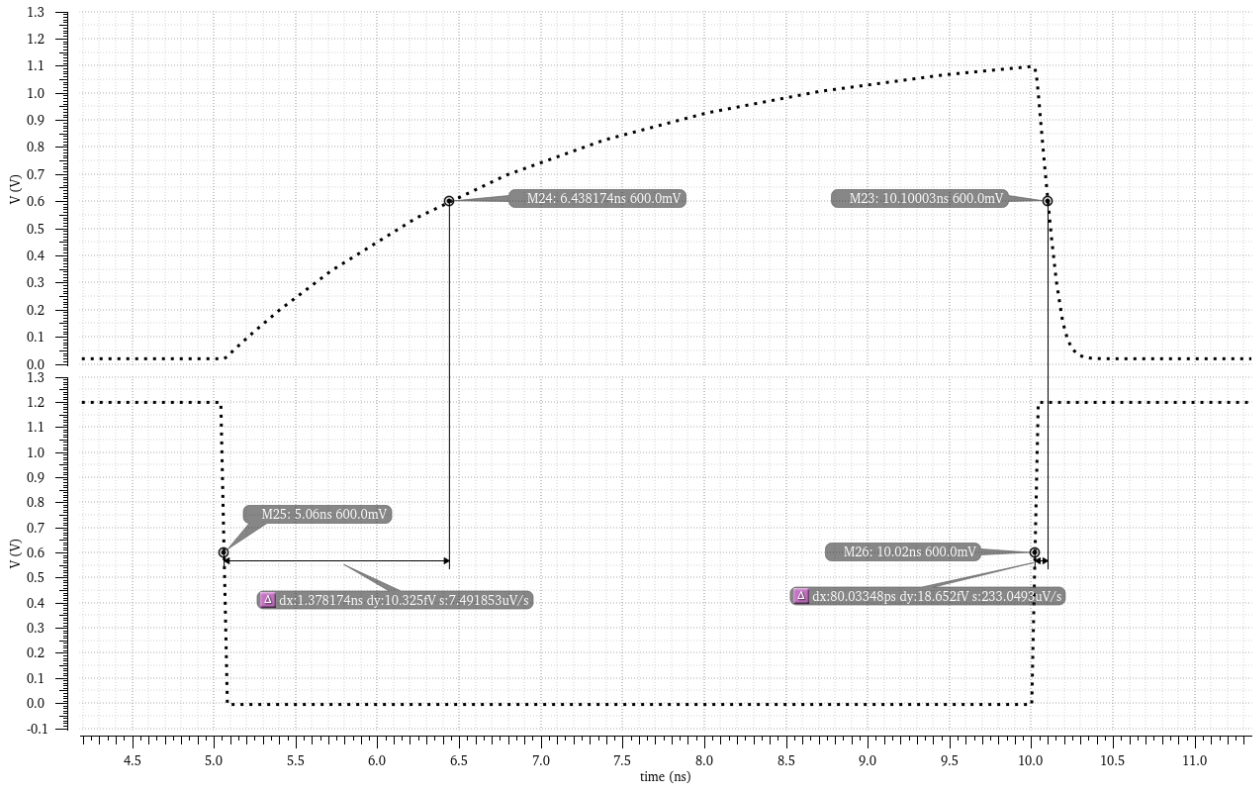

Figure 9: Plot of The Input and Output Waveforms with Propagation Delay Times

10.) DC Analysis

V_{IH_DC} (mV)	V_{IL_DC} (mV)	V_{OH_DC} (mV)	V_{OL_DC} (mV)
593	261	1,131	69.6

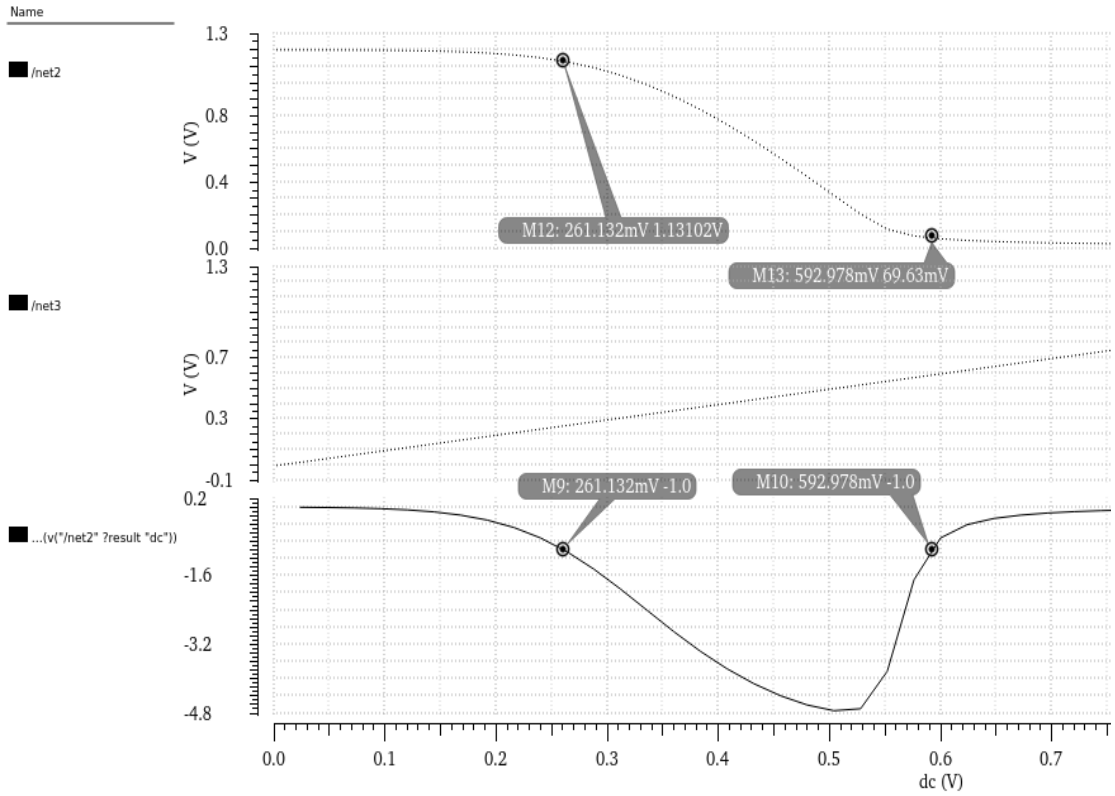

Figure 10: Plot of DC Sweep with the Derivative of the Output Response

Calculating NMOS Equivalent Resistance

Finding the correct R value

Starting with the base NMOS device, the equivalent resistance is found as follows, from page (pg149):

$$t_{pd} = ln(2)RC$$

The following circuit is used to find the exact equivalent resistance of one NMOS using capacitive decay.

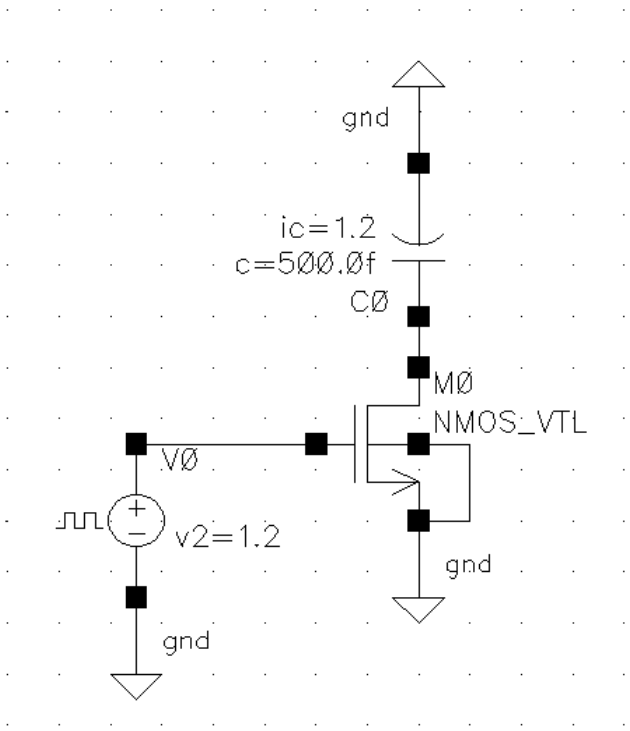

Figure: Schematic of single unaltered NMOS(L=50nm by W=90nm**)**

The propagation delay time or t_{pd} is found below.

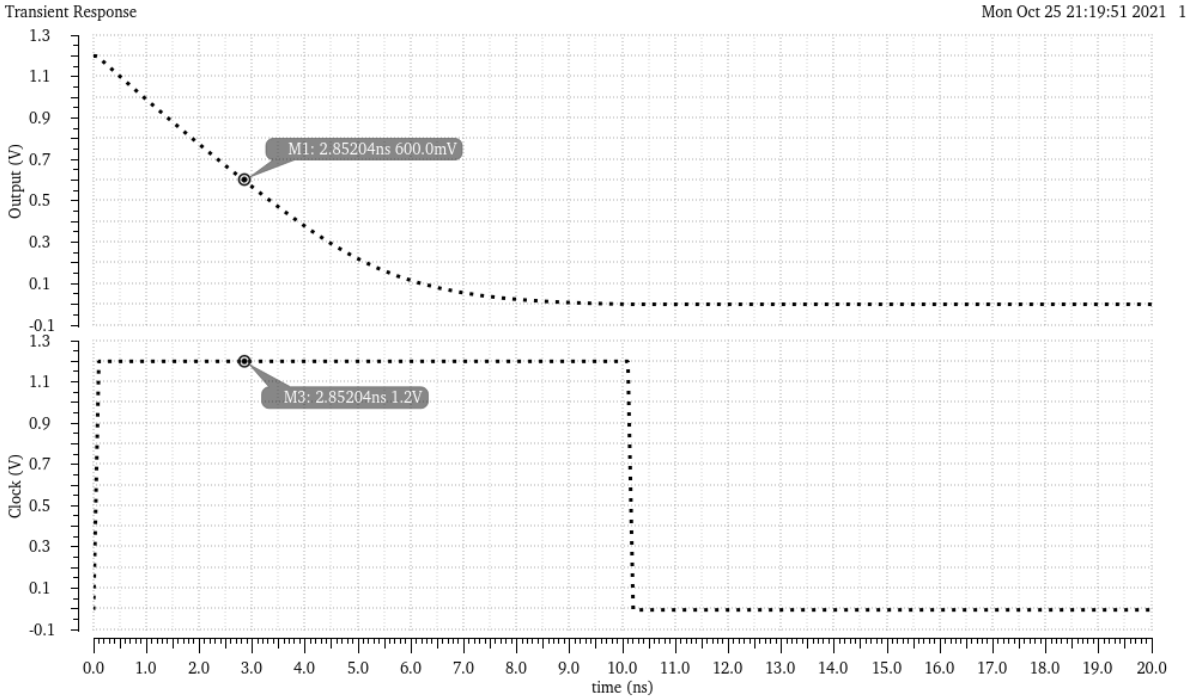

Figure: Finding t_{pd} using capacitive decay.

With C and t_{pd} , R is found for an unedited L=50nm by W=90nm device.

$$t_{pd} = t_{pd}(\sim 600mV)$$

$$\begin{aligned} R_{NMOS} &= t_{pd}/(ln(2)C) \\ &= 2.85ns/(ln(2) \bullet 500fF) \\ &= 8229\ \Omega \end{aligned}$$

Resistance is proportional to length with respect to width as follows:

$$R \quad \propto L/W$$

The first resistor inverter length is increased by a factor of 7.

7•8229 Ω = 7 • 50nm / 90nm ≅ 57603 Ω

The second resistor inverter length is increase by a factor of 20.

20•8229 Ω = 20 • 50nm / 90nm ≅ 164580 Ω

This method worked for ball park figures but using the exact tpd analysis worked much better in the end.