Digital IC Design 1

Lab 2: Part 1 - Inverter Report

Introduction and Physical Properties

Cell Description

The inverter acts individually as a logical inverter. However, the double inverter in series acts as a logical buffer that has multiple purposes, with signal integrity being at the top of the list of applications.

Cell Symbol

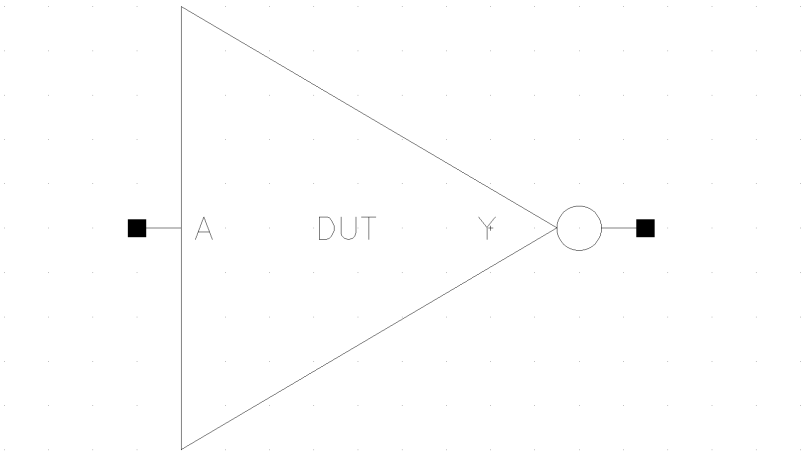

Figure 1: Cell symbol of the device under test.

Cell Truth Table

Logic table of DUT output. The DUT in this case is an inverter.

CMOS Inverter Cell Truth Table	
Inputs	Outputs
0	1
1	0

Cell Schematic Diagram

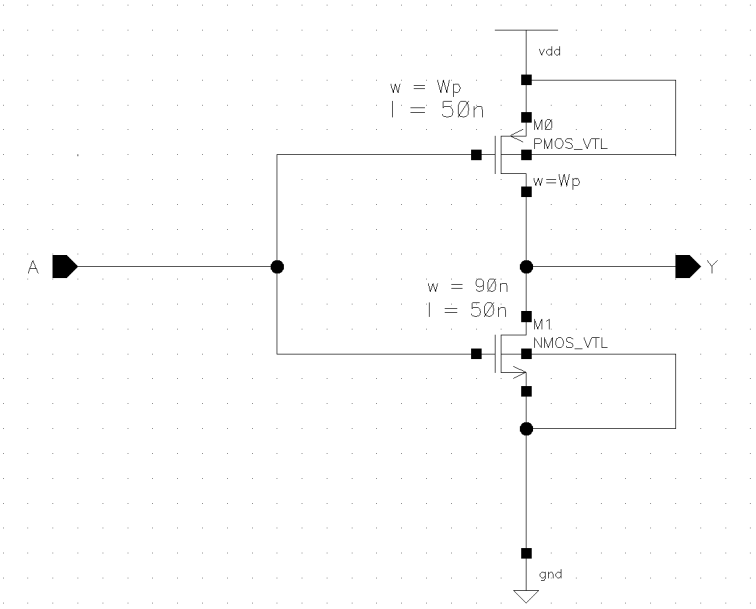

Figure 2: Circuit for CMOS Inverter as the DUT. Wp denotes variable PMOS width.

Cell Layout Diagram and Dimensions

Transistor Dimensions				
	PMOS		NMOS	
Transistor Instance Number	Length (nm)	Width (nm)	Length (nm)	Width (nm)
Device Under Test	50	135	50	90

Unit design	50	90	50	90

Performance Analysis

Rise and Fall Times

Input L: Output Rise Time Data t_r (ps)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	256	18.2	21.3	27.7	39.1

Stack Input Combination: $Y = \bar{A}$

Stack S, Input H: Output Fall Time Data t_f (ps)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	117	15.2	16.8	19.9	25.3

Stack Input Combination: $Y = \bar{A}$

Propagation Delays

Data Worst-Case Low to High Propagation Delay Data t_{plh} (ps)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	182.3	19.6	22.8	28.7	38

Worse Case Input Combination: $Y = \bar{A}$

Data Worst-Case High to Low Propagation Delay Data t_{phl} (ps)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	100.4	7.95	10.6	15.2	22.1

Worse Case Input Combination: $Y = \bar{A}$

Simulation FO0 load:

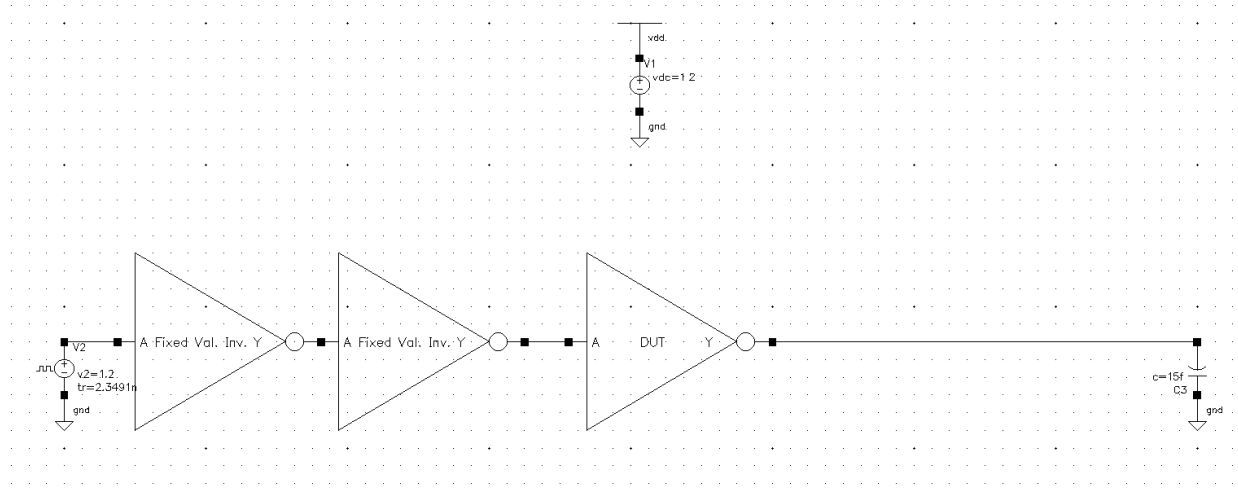

Figure 3: Schematic of DUT with FO0 load.

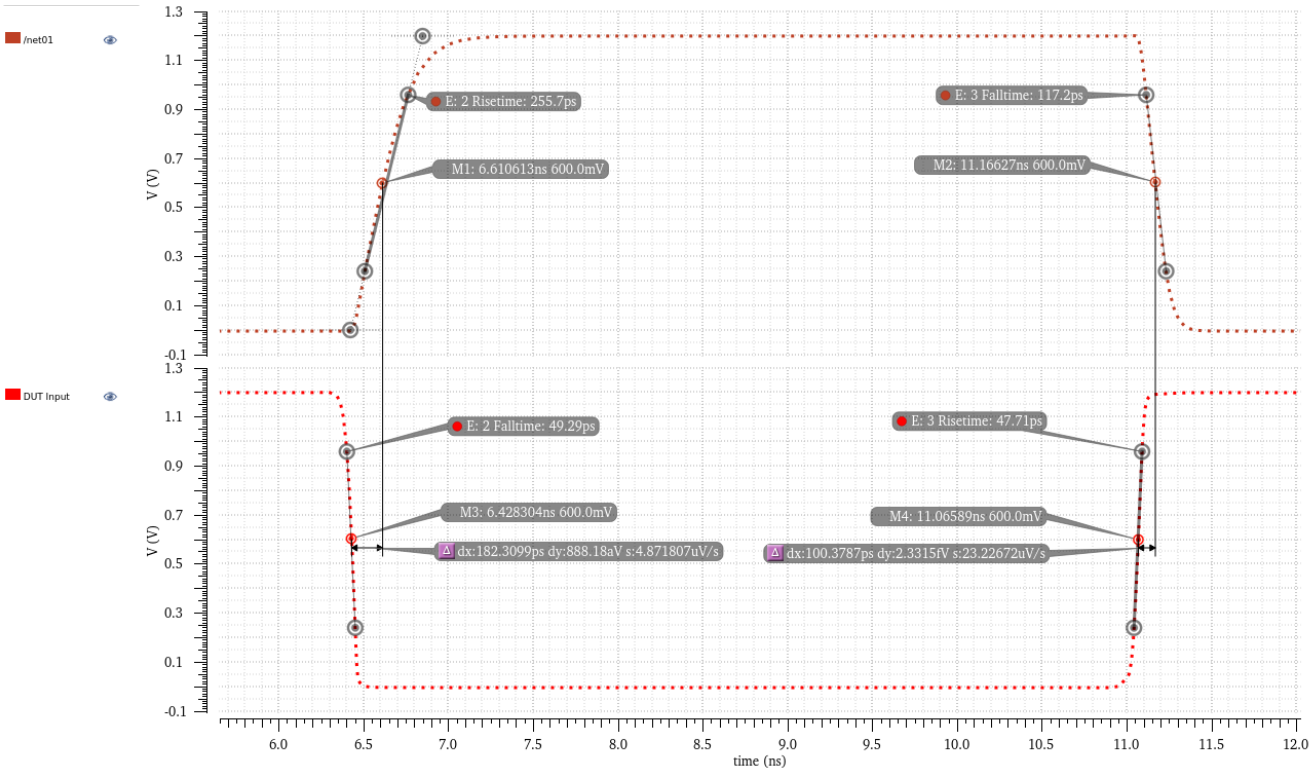

Figure 4: Graph of DUT under a FO0 load.

Simulation FO1:

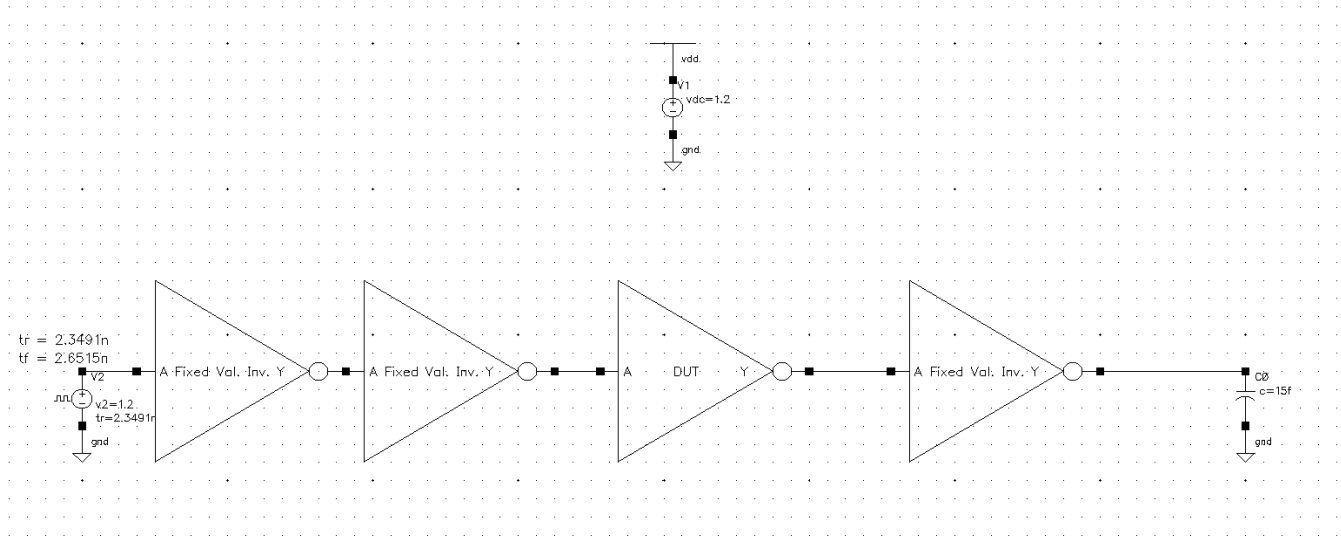

Figure 5: Schematic of DUT with FO1 load.

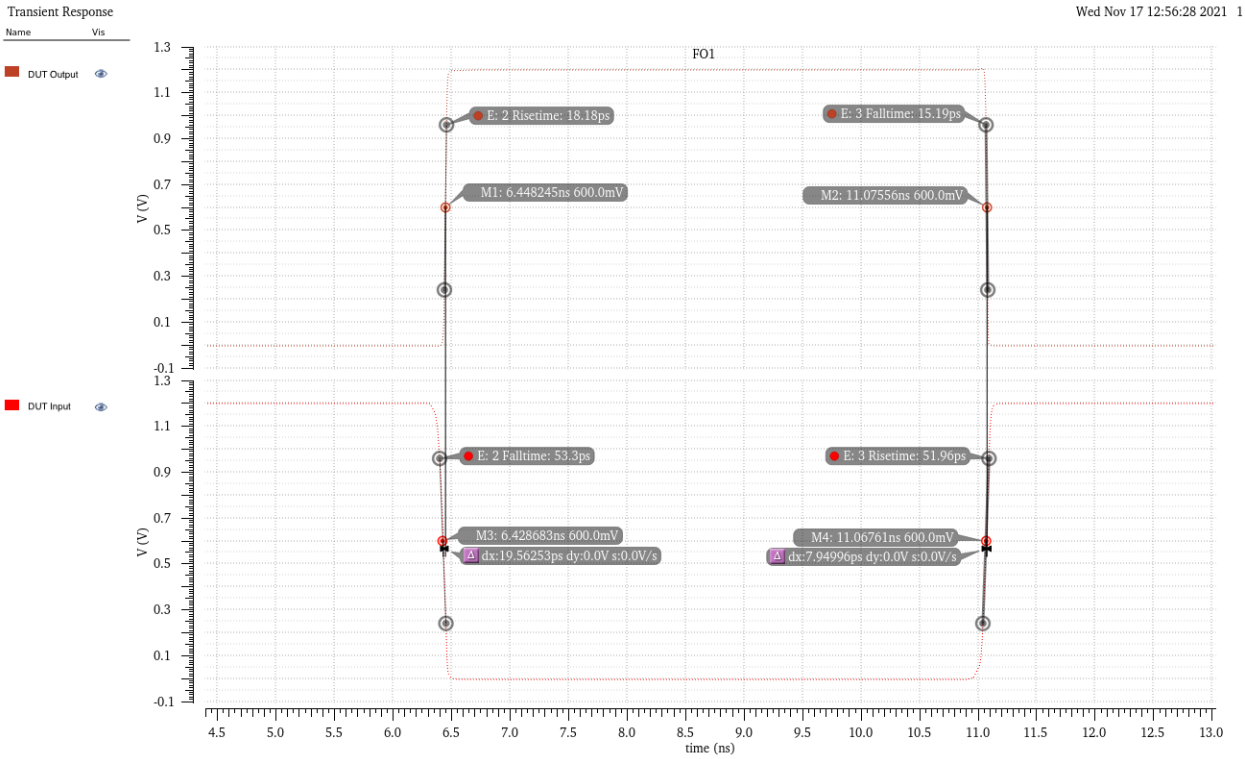

Figure 6: Graph of DUT under a FO1 load.

Simulation FO2:

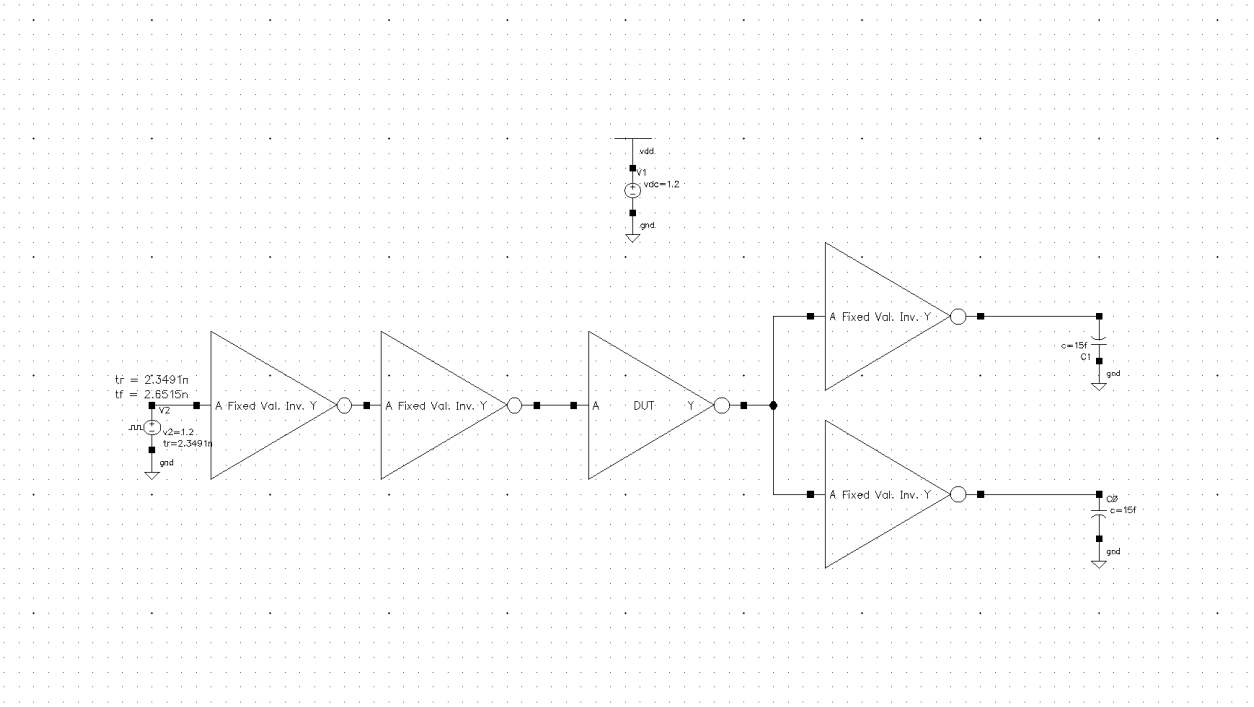

Figure 7: Schematic of DUT with FO2 load.

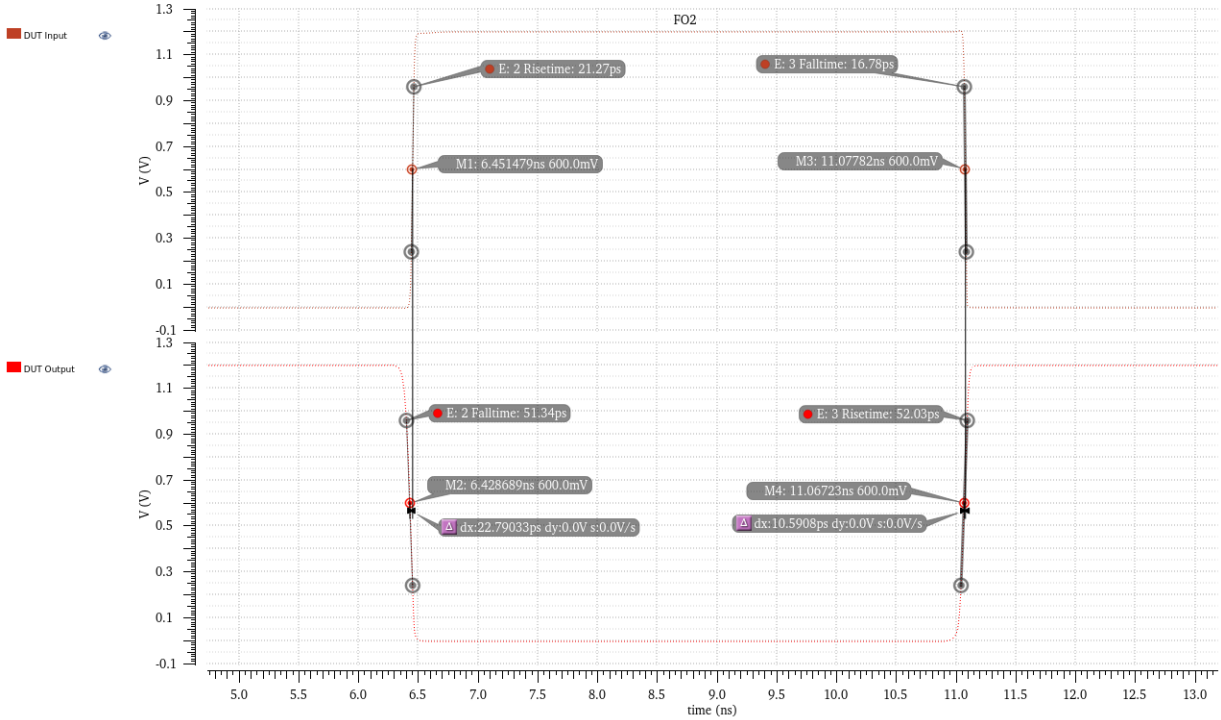

Figure 8: Graph of DUT under a FO2 load.

Simulation FO4:

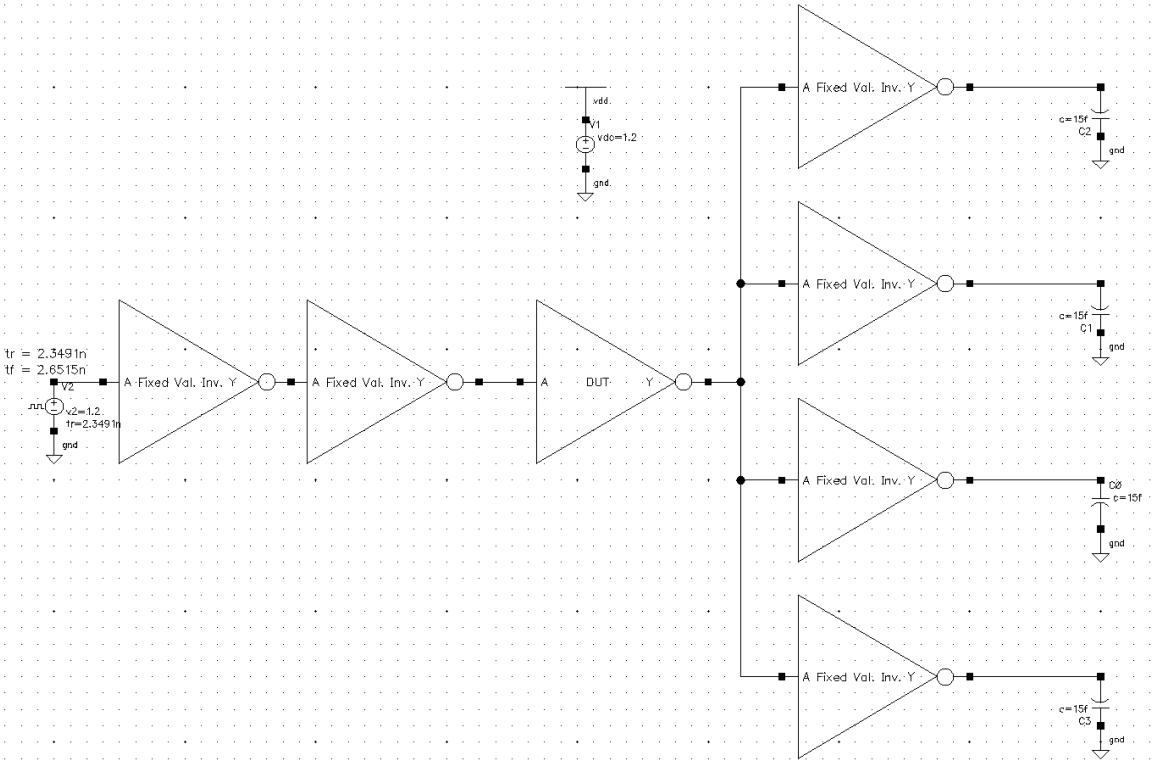

Figure 9: Schematic of DUT with FO4 load.

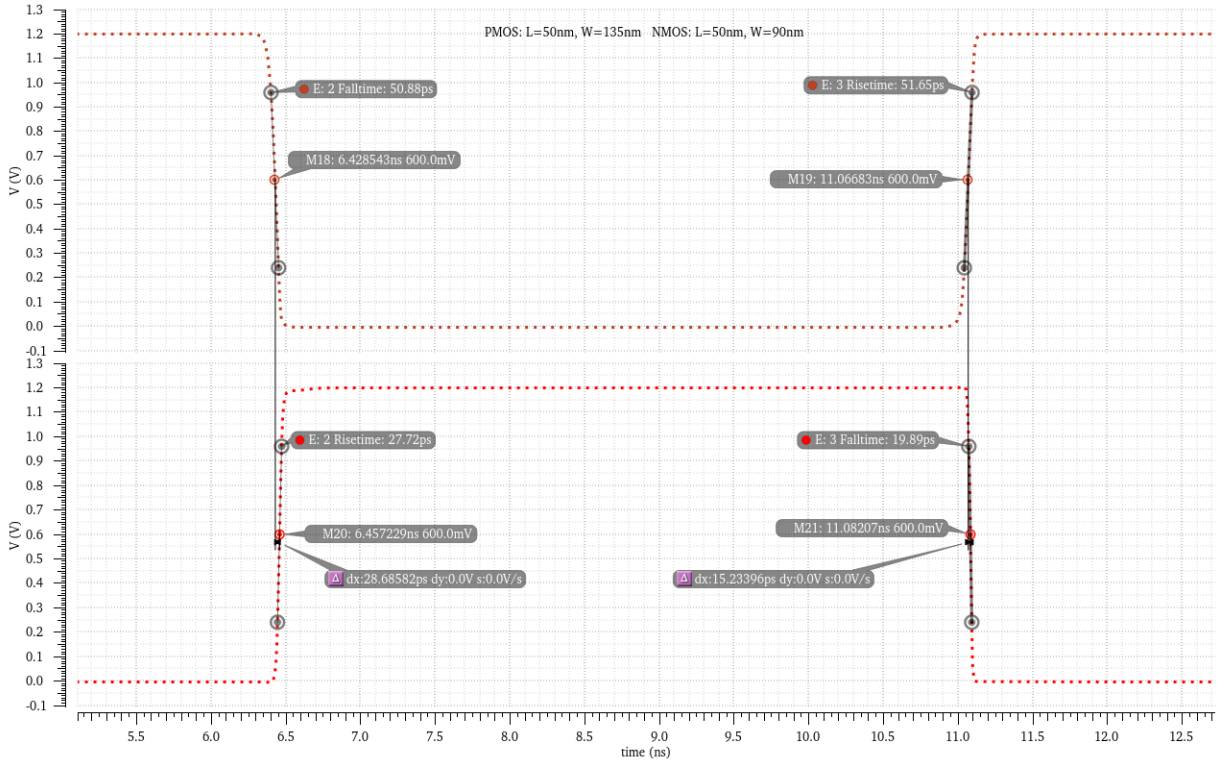

Figure 10: Graph of DUT under a FO4 load.

Simulation FO8:

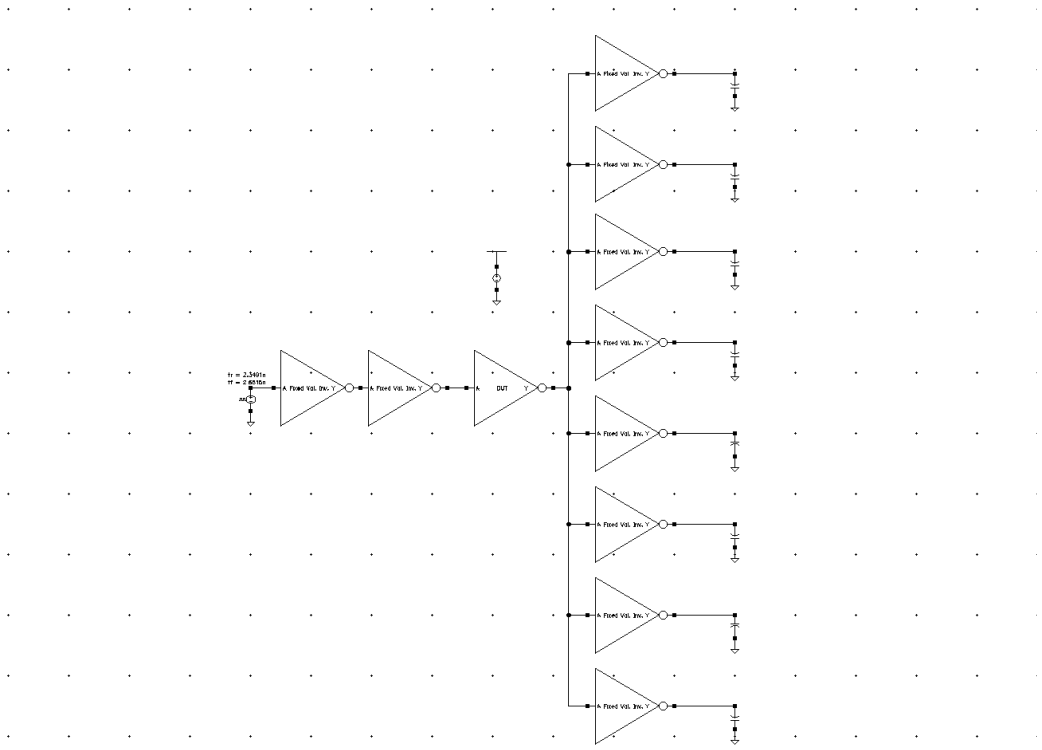

Figure 11: Schematic of DUT with FO8 load.

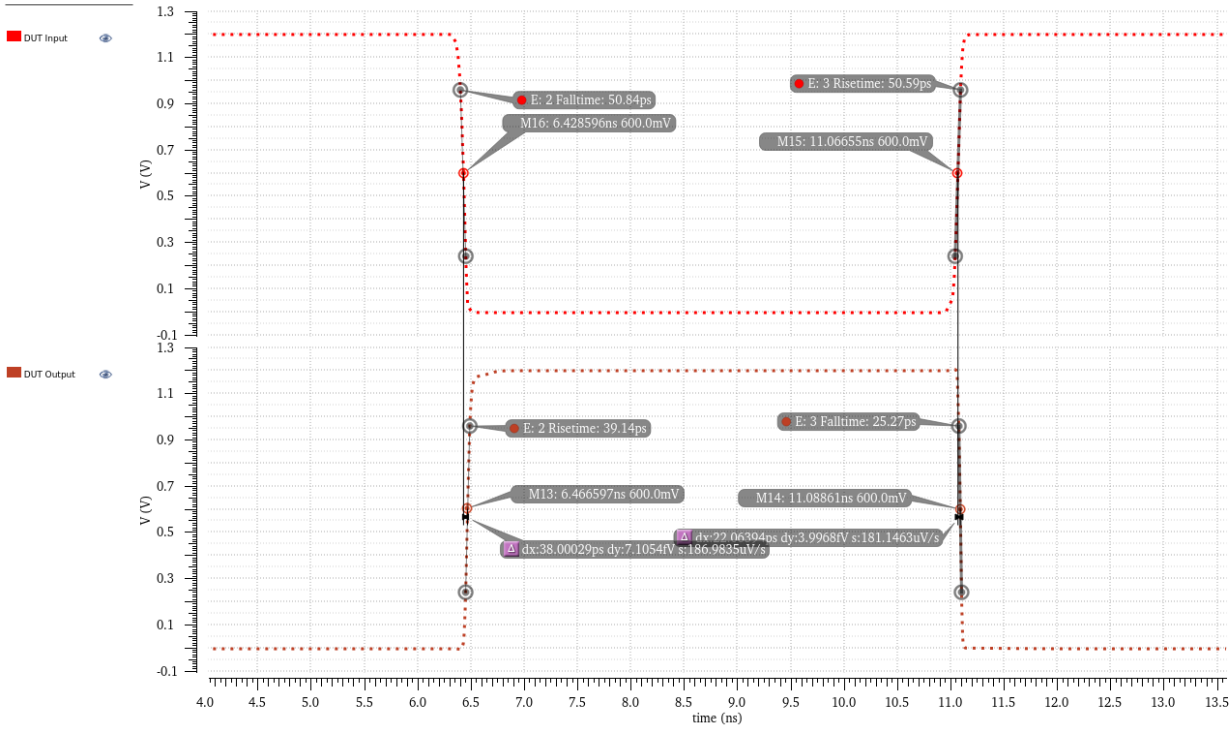

Figure 12: Graph of DUT under a FO8 load.

Table of Simulated Results the CMOS inverter with a FO4

CMOS inverter with load FO4 testing variable PMOS values at 45nm increments					
DUT		Transient Analysis (ps)			
Width NMOS	Width PMOS	Rise time (20% to 80%)	Fall time (80% to 20%)	Propagation Low to high	Propagation High to low
Wn	Wp	Tr	Tf	Tplh	Tphl
90	90	35.4	19.3	36.1	14.2
90	135	27.7	19.9	28.7	15.2
90	180	24.2	20.2	24	15.7
90	225	22.2	20.2	21.2	16.7
90	270	56.7	58.72	19.2	17.6

Table 1: Transient analysis results for varied Wp at increments of 45nm. Green indicates favorable results while red indicates non-ideal results.

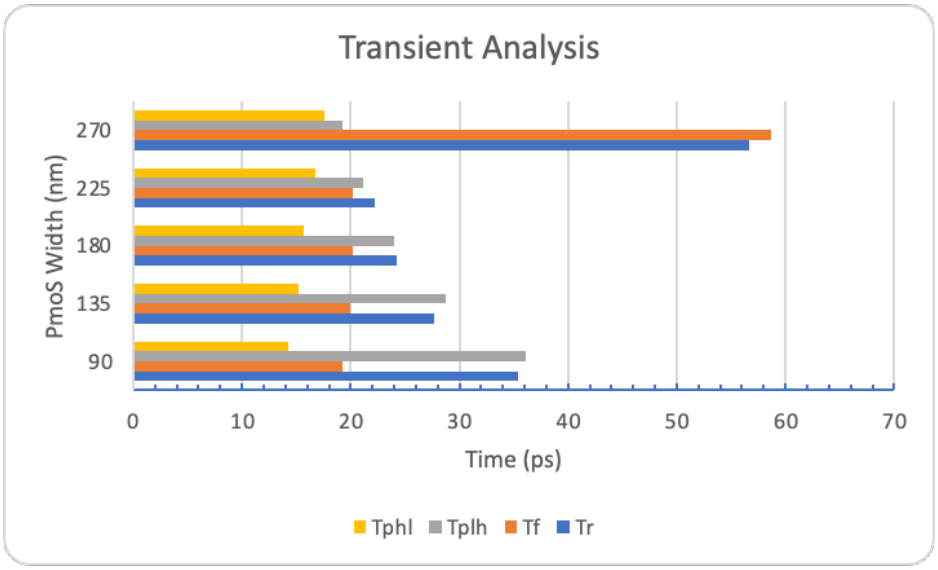

Figure 13: Plot of Transient analysis Table 1.

Conclusion

The original design decision to increase the PMOS width to 135nm was based on the timing requirements, characteristics of NMOS and PMOS proportional dimensions, and final design footprint. Based on the F04 PMOS width analysis, PMOS device widths: 135nm, 185nm, and 225nm would achieve the required sizing and timing.
PMOS width of 225nm would be an ideal match for the timing requirements.
PMOS width of 135nm is best for a small footprint.

After completing the analysis, it became clear PMOS width of 180nm is between the two undesired timing requirements at 90nm and 270nm. At 180nm the design would yield a favorable Tf, Tr, Tphl, Tplh time and would allow a margin of error between the two undesirable extreme values(90nm and 270nm).