TOP PADS

AnalogIO.SchDoc

DigitalIO.SchDoc

Power.SchDoc

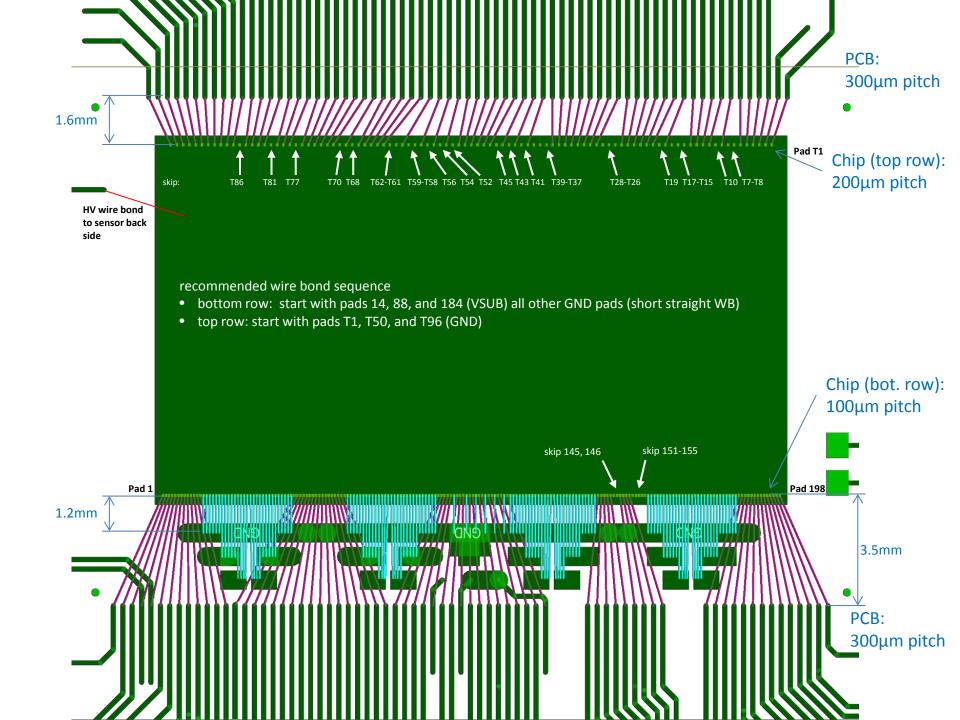
ANALOG IO

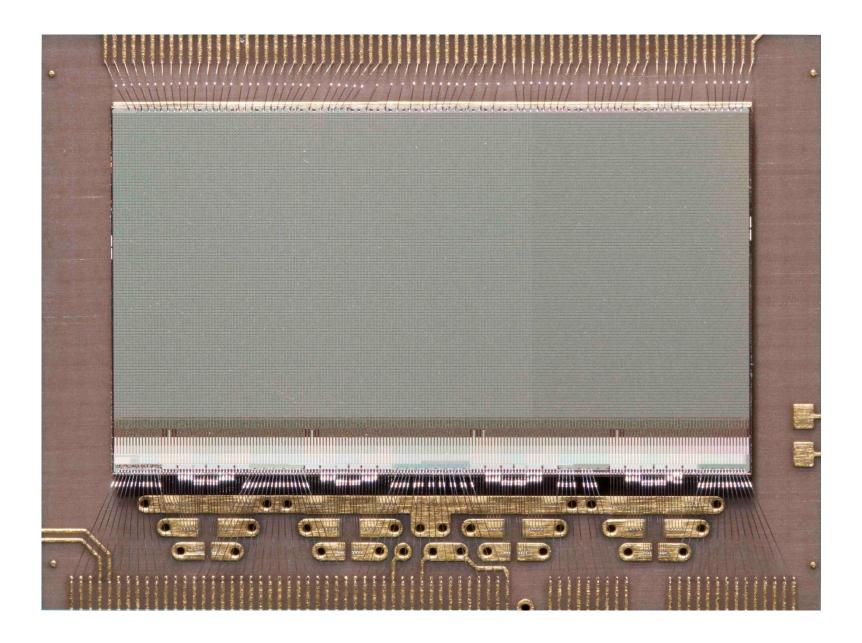
DIGITAL IO

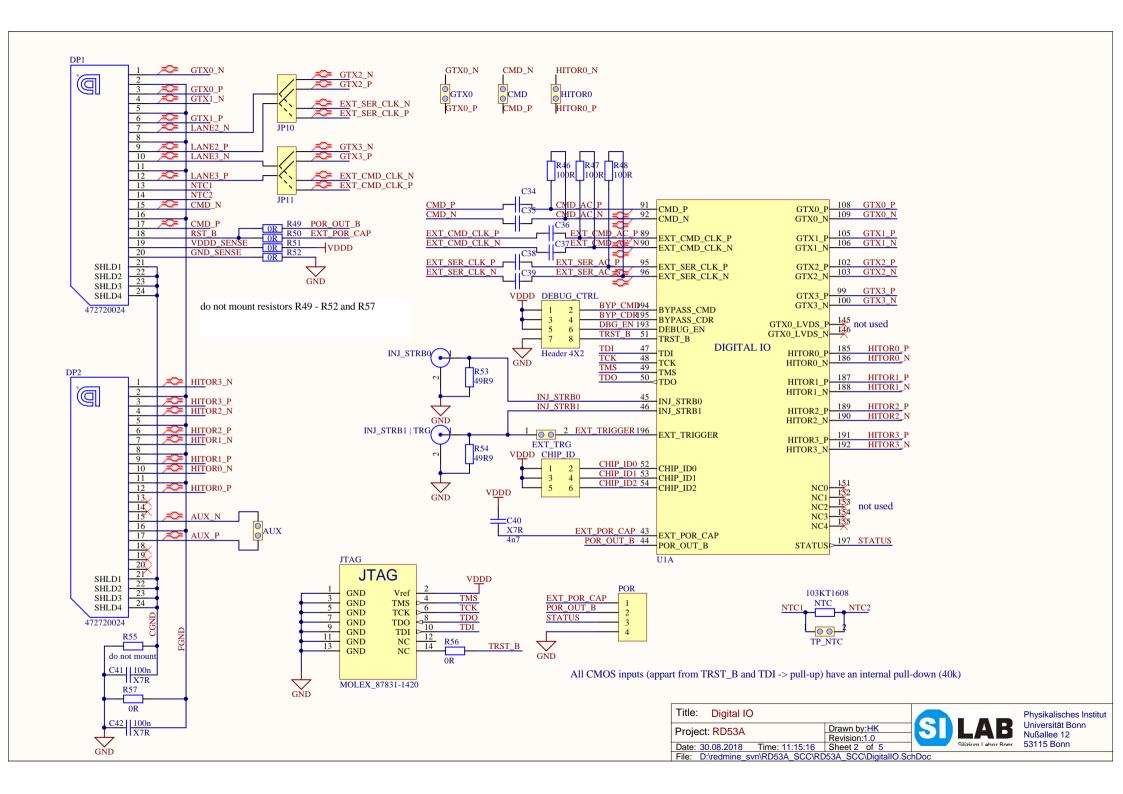
POWER

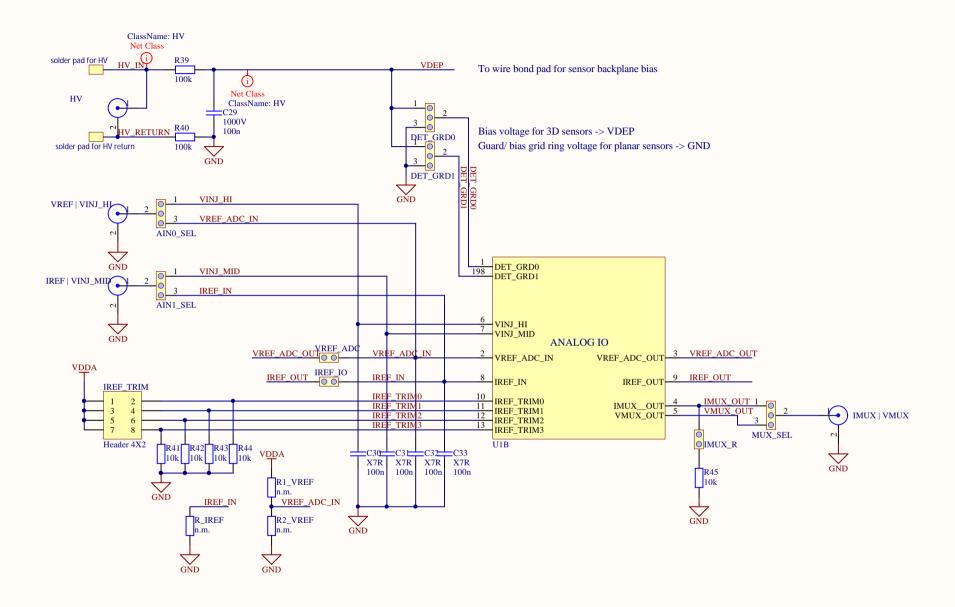
Title: RD53A Single Chip Card

Project: RD53A | Drawn by:HK | Revision:1.0 |
Date: 30.08.2018 | Time: 11:15:16 | Sheet 1 of 5 |
File: D:\text{Vedmine_svn\RD53A_SCC\RD53A_SCC\RD53A_SCC\RD53A_SCC\Top.SchDoc} | Physikalisches Institut Universität Bonn Nußallee 12 |
53115 Bonn

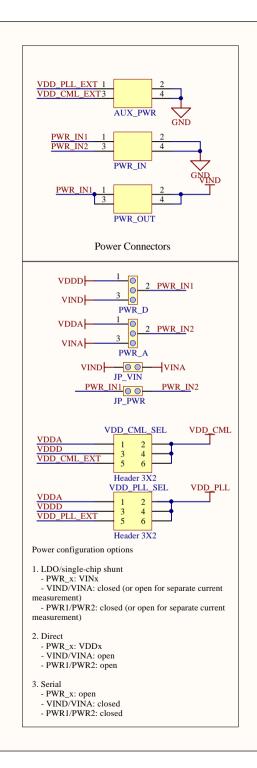


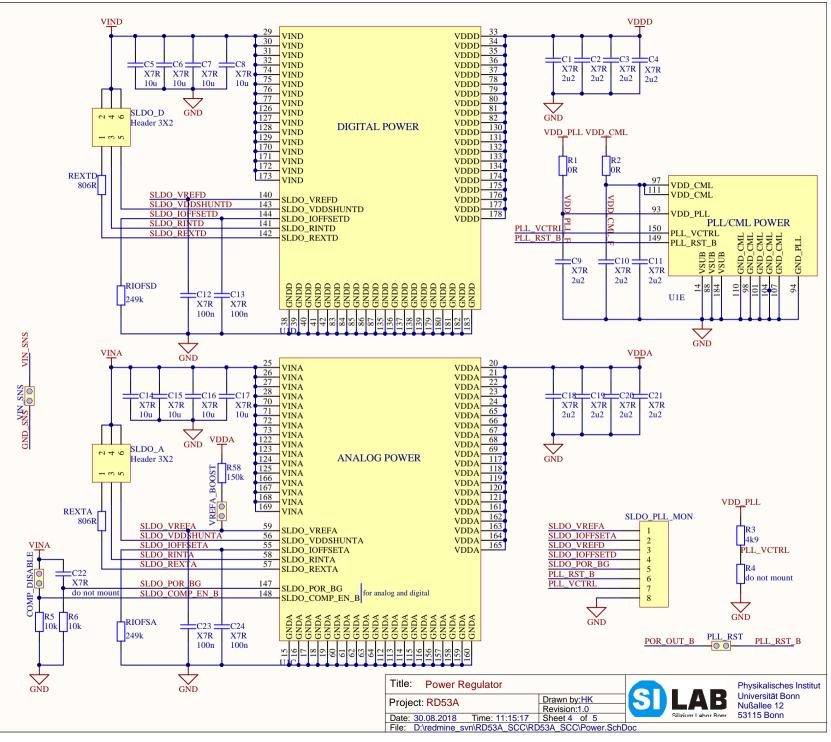


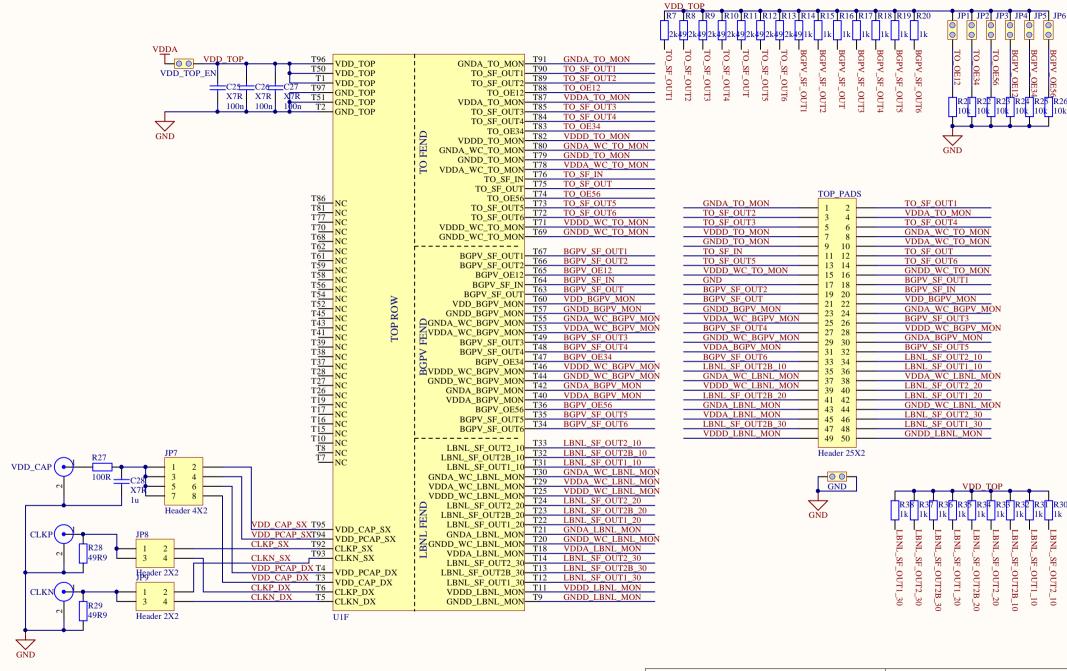




Title: Analog IO				Physikalisches Institut
Project: RD53A	Drawn by:HK Revision:1.0	21	LAB Silizium Labor Ronn	Universität Bonn Nußallee 12 53115 Bonn
Date: 30.08.2018 Time: 11:15:16	Sheet 3 of 5			
File: D:\redmine_svn\RD53A_SCC\RD53A_SCC\AnalogIO.SchDoc				







Title: Top Row Test Pads Physikalisches Institut Universität Bonn Drawn by:HK Project: RD53A Nußallee 12 53115 Bonn Date: 30.08.2018 Time: 11:15:17 Sheet 5 of 5 File: D:\redmine svn\RD53A SCC\RD53A SCC\TopRow.SchDoc

BGPV_OE34

LBNL_SF_OUT1_10

LBNL

_SF_OUT2

