RD53A Single Chip Card Configuration (Rev. 0.2c and 0.2d)

1. Assembly modifications

NEEDED to configure data link / clocking debug mode

- **JP10, JP11**: 1x3 solder jumper to select LANE2 and LANE3 use (mount 0 Ohm 0603 SMD resistors to make connections – already mounted on SCC revision 0.2d for 4-lane mode)

RECOMMENDED configuration

- PLL_RST: mount and close jumper to connect PLL_RST_B to POR_OUT_B
- REXTA, REXTD: mount to set current for shunt operation (**806 Ohm**)
- RIOFSA, RIOFSD: mount to set offset voltage point for shunt operation (**249 kOhm**)
- R3: to bias the PLL_VCTRL input mount **4.99 kOhm** resistor
- Remove (not mount): R51, R52, R55, and R57 (R49 and R50 are not mounted by default)
- Remove C22

Assemble as needed for debugging and optional operation modes

- PWR_OUT: Power connector for serial powering chain
- JP1, JP2, JP3, JP4, JP5, JP6: Output enable jumpers for the top row (test pads)
- JP7, JP8, JP9: pin headers for cap measurement circuit on top row
- VDD_TOP_EN: jumper to enable top row power supply
- VDD_CAP, CLKN, CLKP, INJ_STRB0, INJ_STRB1|TRG, IREF|VINJ_MID, HV, IMUX|VMUX, VREF|VINJ_HI: LEMO connectors for debugging
- EXT_TRG: jumper to connect EXT_TRIGGER to LEMO
- MUX_SEL: 1x3 jumper to select between IMUX and VMUX output for IMUX|VMUX LEMO connector
- IMUX_R: jumper to enable pull-down resistor for IMUX out to voltage conversion
- AIN0_SEL, AIN1_SEL: 1x3 jumpers to select analog input options (VINJ_x, xREF)
- R1_VREF, R2_VREF: optional voltage reference generation for on-chip ADC
- R_IREF: voltage divider for optional reference current generation for bias generation
- R3, R4: voltage divider for setting the PLL control voltage at PLL reset (PLL_RST_B)
- R49, R50: optional 0 Ohm resistors to connect external reset to either POR_RST_B or EXT_POR_CAP
- R55: connection between DP connector shield and local GND **(remove)**
- R56: connection between JTAG reset (TRST_B) and pin 14 of JTAG connector
- DET_GRD0, DET_GRD1: 1x3 jumper to select sensor guard ring connection
- AUX: AUX lane from 2nd DP connector, solder short wires to supply EXT_SER_CLK or EXT_CMD_CLK (JP10, JP11) if LANE2/LANE3 from DP1 are used for data.

Meant as test points:

GND, GTX0, HITOR0, CMD, TP_NTC, TOP_PADS

2. Jumper configuration

Default settings given below assume operation in **LDO mode** and no debug or overwrite settings applied. Jumper settings needed for operation a marked bold.

- **PWR_A, PWR_D**: Selects external power supply (PWR_IN) connection to the chip (VINx or VDDx)

Setting	Function	Default
VDDx	Direct powering	open
VINx	LDO or Shunt-LDO operation	**closed**

- **SLDO_A, SLDO_D**: Set position VDD_SHNT to enable shunt mode and set RINT or REXT (on bottom side of SCC) for selection of the current setting resistor.

Setting	Function	Default
VDD_SHNT	Enable shunt regulator	**open**
RINT	Select internal resistor for current setting	249 kOhm
REXT	Select external resistor for current setting	806 Ohm

- **VDD_CML_SEL**: Select CML driver power supply

Setting	Function	Default
VDDA	Operate CML driver from VDDA supply	**closed**
VDDD	Operate CML driver from VDDD supply	open
VEXT	Operate CML driver from external supply (AUX_PWR)	open

- **VDD_PLL_SEL**: Select PLL driver power supply

Setting	Function	Default
VDDA	Operate PLL driver from VDDA supply	**closed**
VDDD	Operate PLL driver from VDDD supply	open
VEXT	Operate PLL driver from external supply (AUX_PWR)	open

- **JP_PWR**: Shorts PWR_IN1 and PWR_IN2 input lines from the external power supply

Setting	Function	Default
Open	PWR_IN1 and PWR_IN2 are not connected to allow individual current sensing with direct powering	
Closed	PWR_IN1 and PWR_IN2 are shorted	**closed**

- **JP_VIN**: Shorts VIND and VINA, open in direct powering (or for individual current sensing in shunt mode)

Setting	Function	Default
Open	VINA and VIND are independent to allow individual current sensing	
Closed	VINA and VIND are shorted	**closed**

- **COMP_DISABLE**: SLDO compensation scheme

Setting	Function	Default
Open	New SLDO compensation scheme enabled	open
Closed	New SLDO compensation scheme disabled	

- **VREF_ADC**: ADC voltage reference selection

Setting	Function	Default
Open	Connect external voltage source to ADC reference input VREF_ADC_IN (via LEMO VREF|VINJ_HI)	
Closed	Use internal ADC voltage reference VREF_ADC_OUT	**closed**

- **IREF_IO**: Bias generator reference current selection

Setting	Function	Default
Open	Connect external current source to current reference input IREF_IN (via LEMO VREF|VINJ_MID) or use R_IREF	
Closed	Use internal current reference IREF_OUT	**closed**

- **IREF_TRIM**: Trim bits for internal current reference

Setting	Function	Default
[3:0]	Close jumper to set bit to high	1000

- **CHIP_ID**: Chip address selection

Setting	Function	Default
[2:0]	Close jumper to set bit to high	none

- **DEBUG_CTRL**: Enable debug modes (enabled when jumper is closed)

Setting	Function	Default
BYP_CMD	Bypass command decoder (use EXT_TRIGGER)	open
BYP_CDR	Bypass CDR (use EXT_CMD_CLK)	open
DBG_EN	Enable further debug options (see chip manual)	open
TRST_B	Enable further debug options (see chip manual)	open

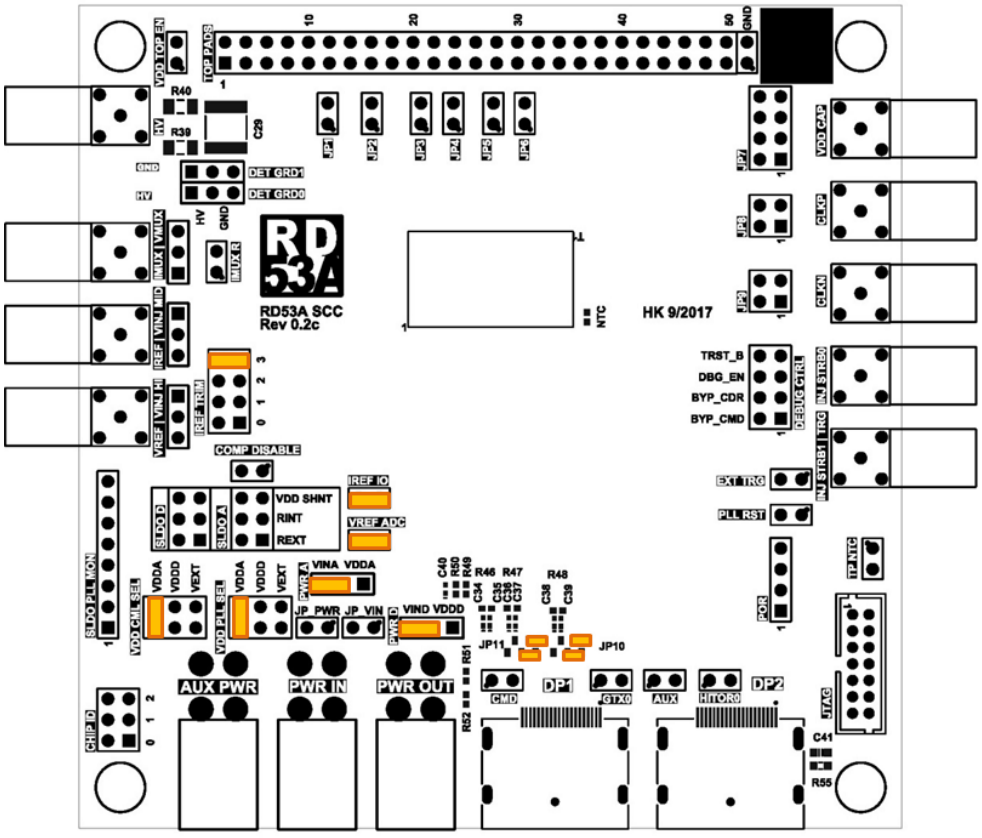

*Fig. 1: Jumper configuration for LDO mode (**default**).*

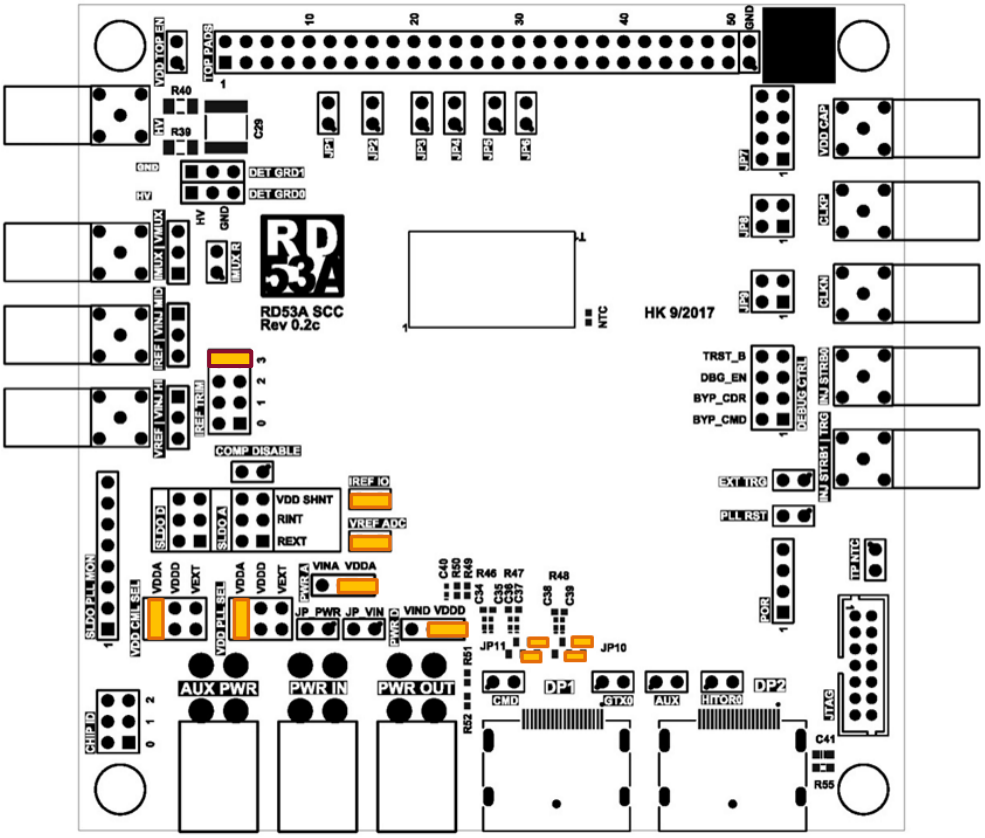

Fig. 2: Jumper configuration for direct powering.

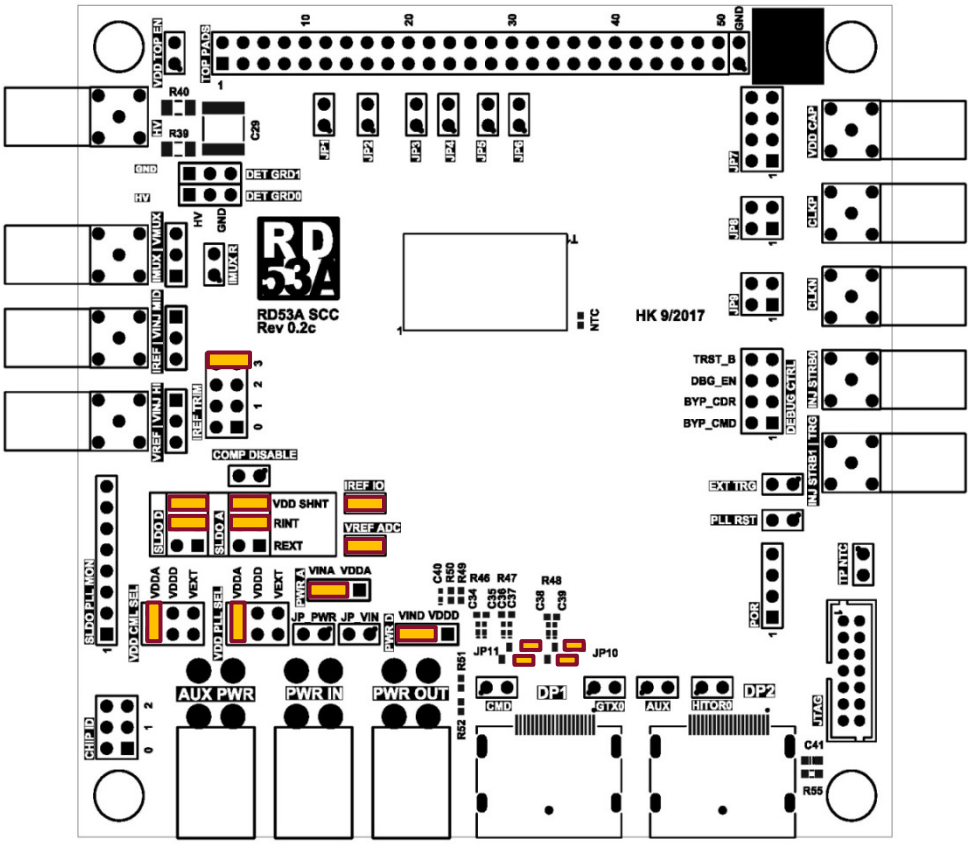

Fig. 3: Jumper configuration for shunt-mode with internal current setting resistor (RINT).

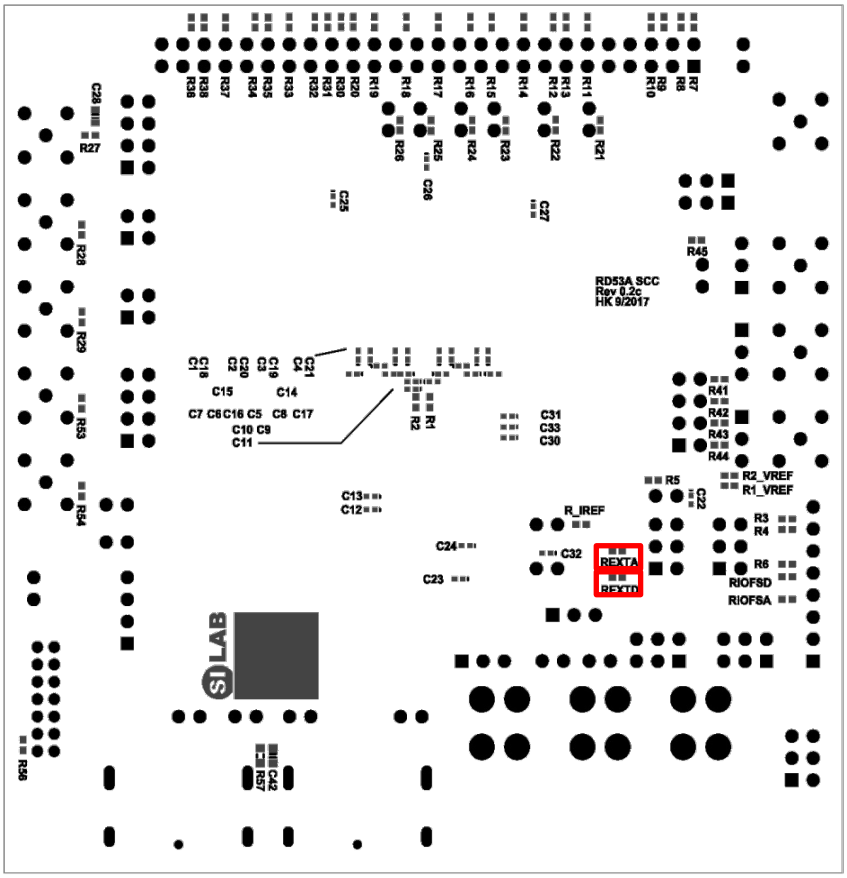

Fig. 4: Location of the shunt current setting resistors REXTA and REXTD on the bottom side of the SCC.

3. Powering Options

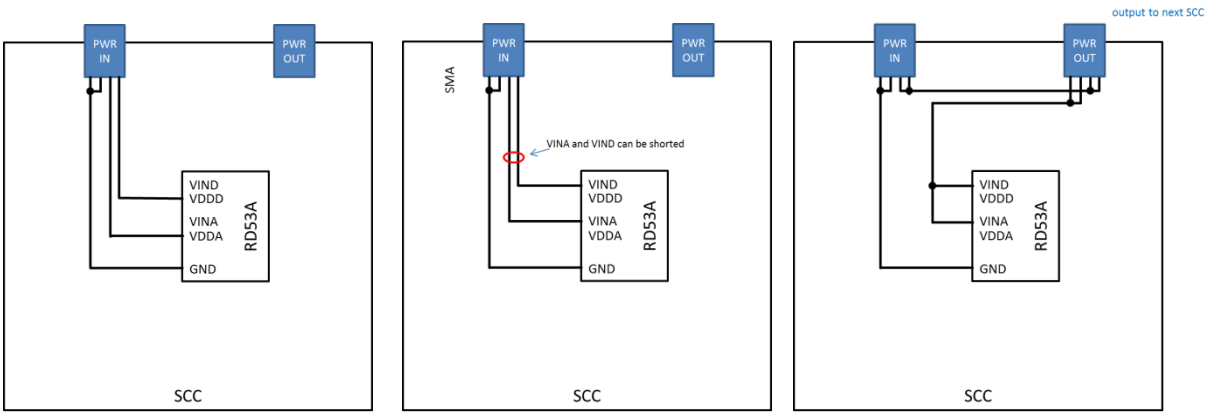

Fig. 5: Connectivity for power options: direct powering (left), single-chip shunt (or LDO only) (middle), and serial powering (right).

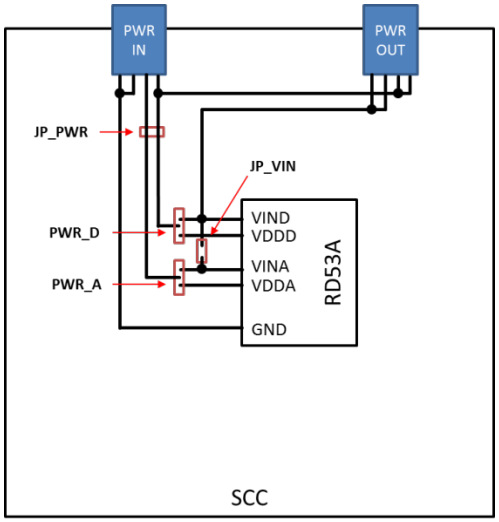

Fig. 6: Jumper implementation (JP_PWR, JP_VIN, PWR_A, and PWR_D)

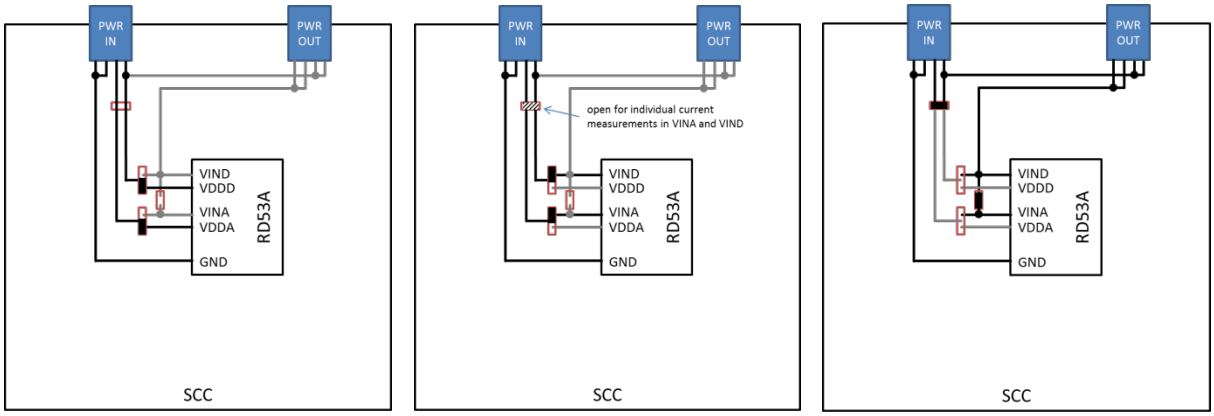

Fig. 7: Jumper settings for: direct powering (left), single-chip shunt (or LDO only) (middle), and serial powering (right).

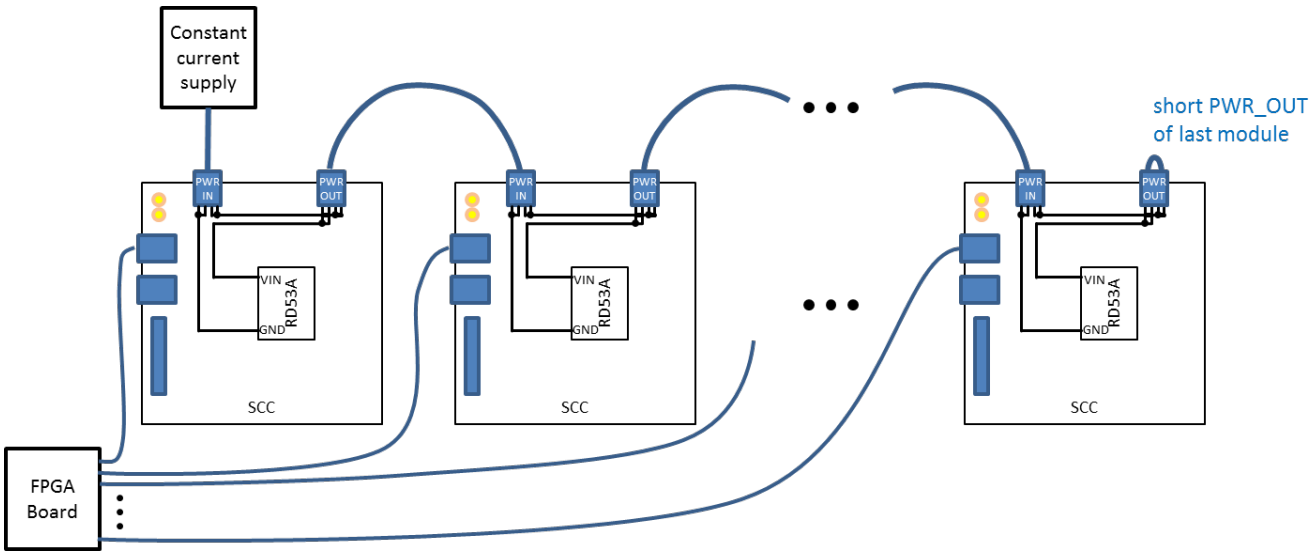

Fig. 8: Serial power chain setup. All connections to common FPGA board need to be galvanic-isolated.

4. Errata

SCC Revision 0.2c

- Issue: Wire bond pad for sensor backside bias is missing
  Work-around: Use DET_GRD1 net (close DET_GRD1 jumper) to apply the depletion voltage. Wire bond sensor backside (instead of chip pad 198) to the DET_GRD1 pad on the PCB. To reduce the risk of sparking don't place STATUS wire bond (chip pad 197) and remove part of the STATUS trace on the PCB.