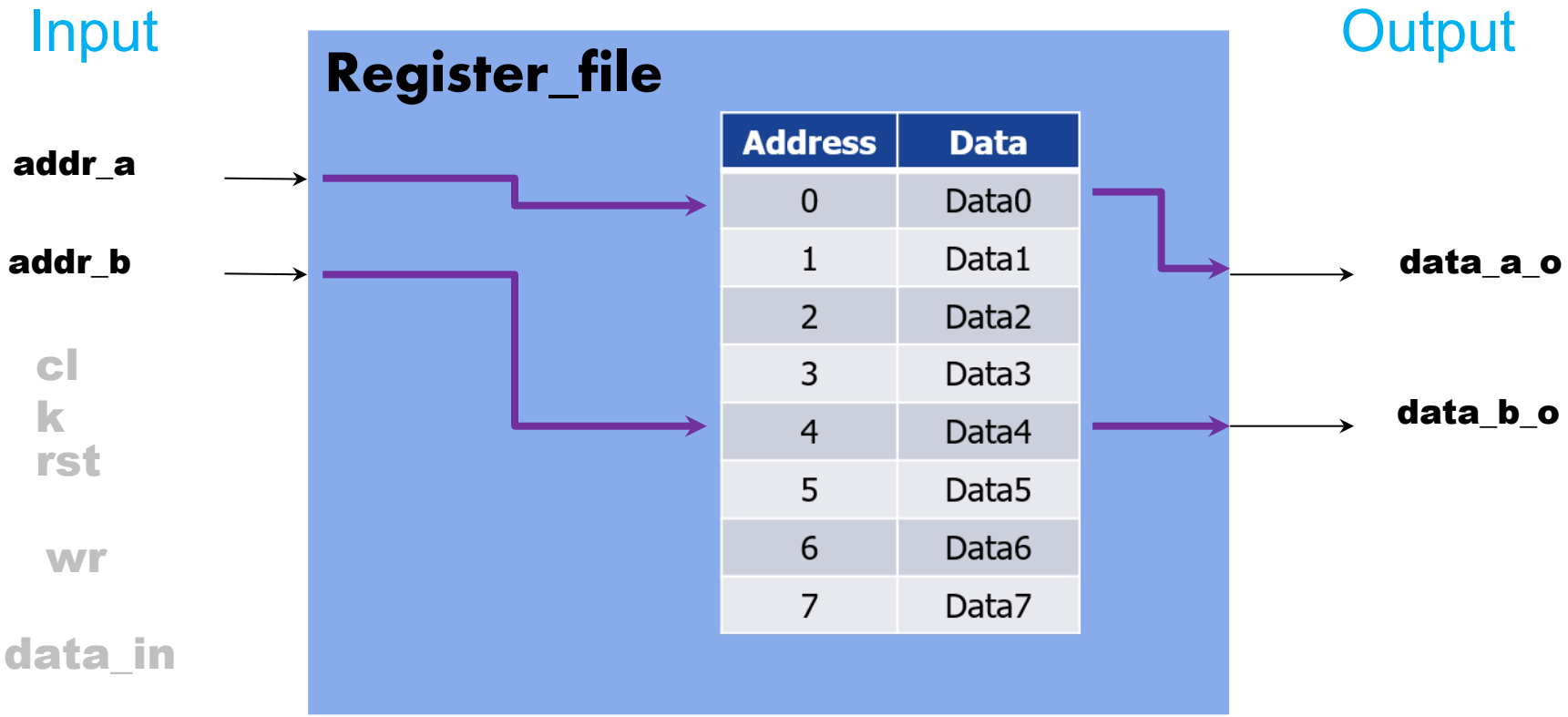
Lab 1: Register File Setup

~~9/19 - 9/27 (11:59:59 pm)~~

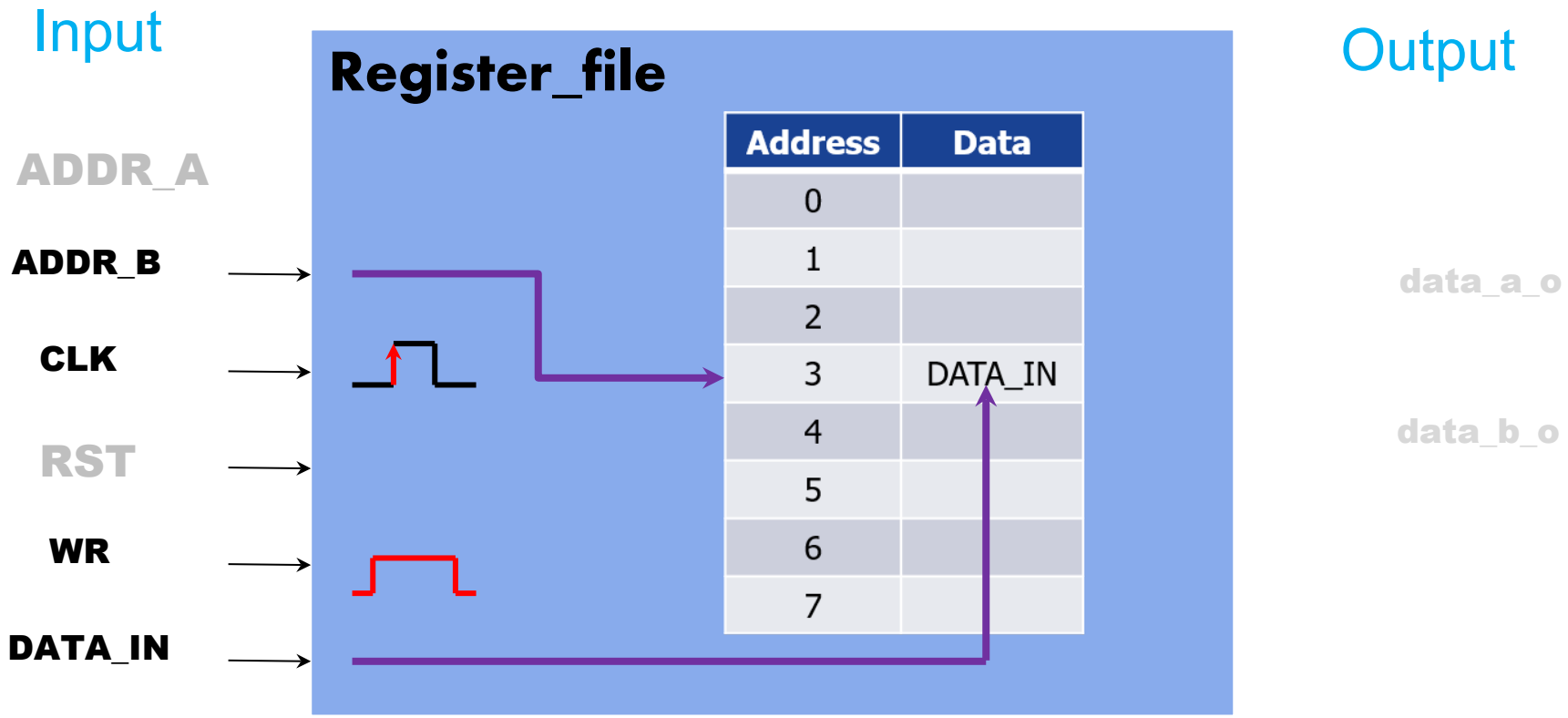
TODO: Design a Register File for Processor

- Design a 16-bit register file contains ***8 registers***
- Output can be read at once without waiting clock edge



TODO: Design a Register File for Processor

- Design a 16-bit register file contains ***8 registers***
- Write must be synchronous to clock edge



Assignment

- In your report…
  - Design and ***explain*** your RF code (register_file.v) - 50%
  - Run testbench and validate waveforms (test_register_file.v) - 50%
    - Please attach your capture of waveforms

Desired Waveform