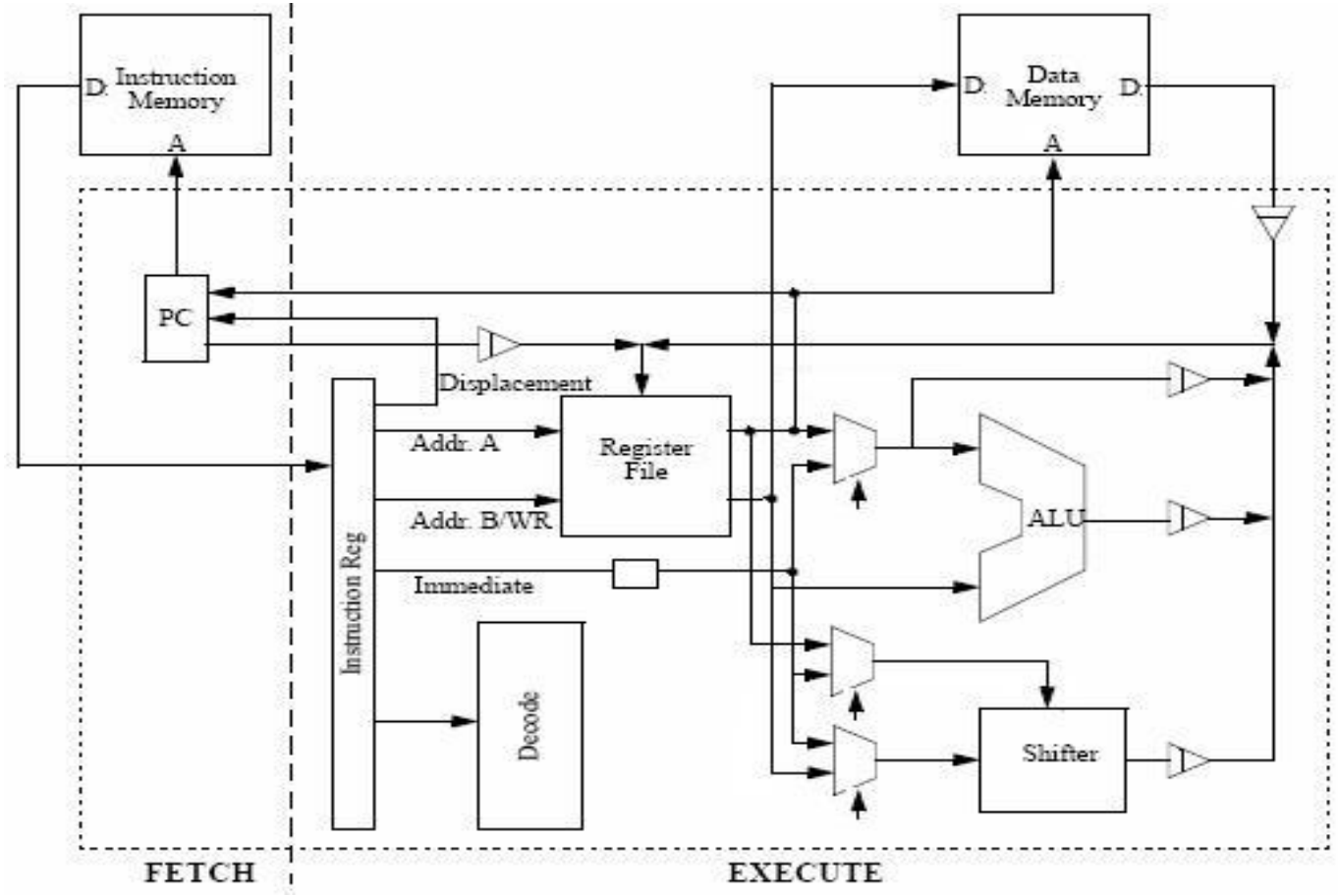
Lab 4: Integration

~~11/28 – 12/13 (11:59:59 pm)~~

It’s Time to Integrate Modules!

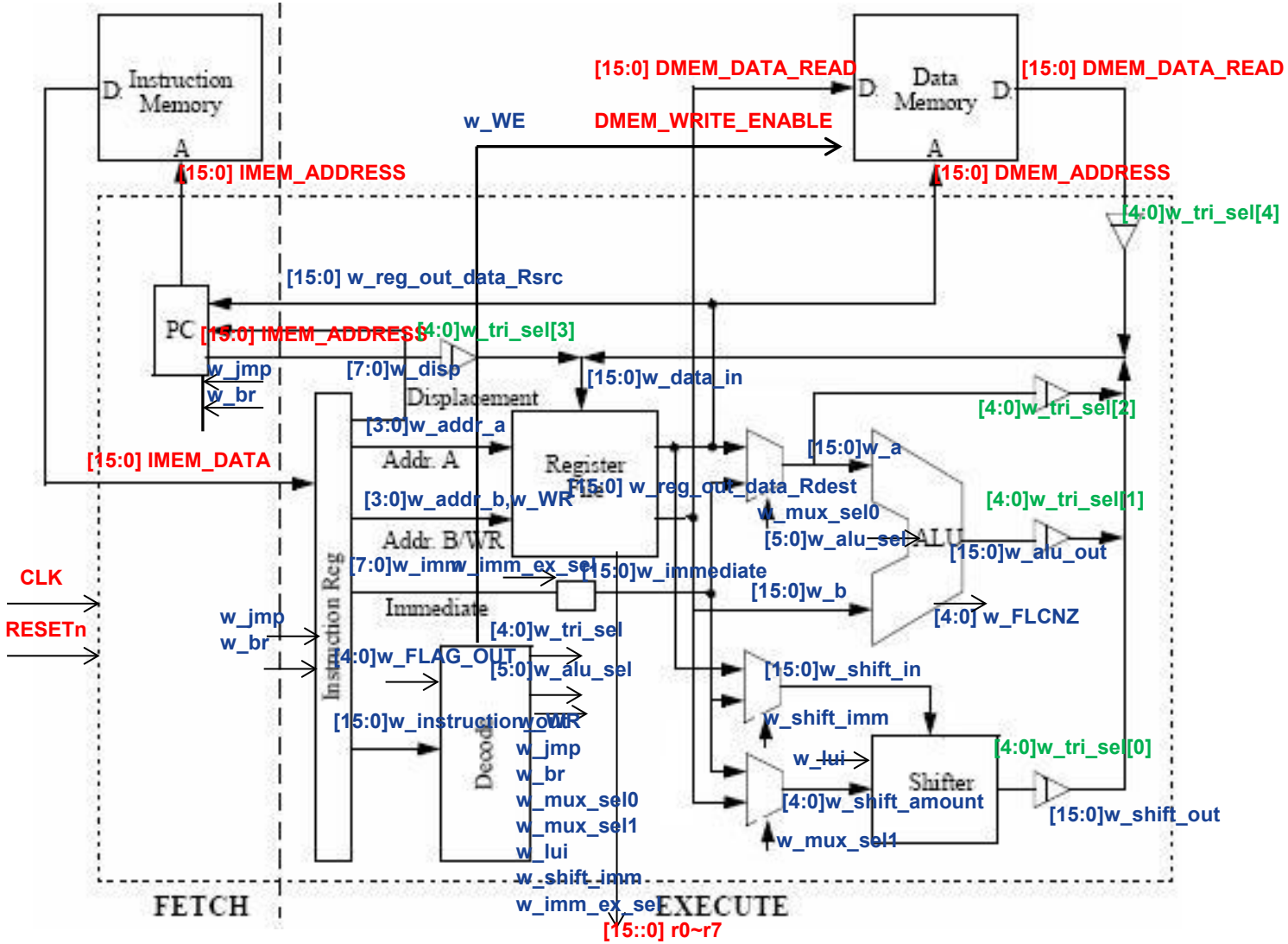
- It’s time to let your efforts bear the fruit!



Task is Simple

- We provided top module, test bench, instruction memory, and data memory
- If you verified your design carefully and modularly, you can integrate it easily!
- Please note that MUXs and TRI-state buffers are also implemented and provided as well

Processor Signals



Assignment

- In your report…
  - Translate binary in imem_img into human-readable assembly – 30%
  - Integrate the code and explain it (top_processor.v) – 30%
  - Run testbench and validate waveform (test_top.v) – 40%
    - Please attach your capture of waveforms

Desired Waveform

Desired Waveform