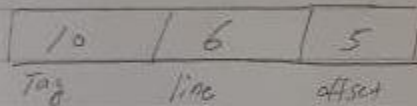


## Q1. (10pts) Cache and Memory mapping

1) Direct mapping

Given 2M memory capacity  $\rightarrow 2^{21}$ Cache consists of 64 blocks  $\rightarrow 2^6$ block contains 32 bytes  $\rightarrow 2^5$ 

①



② What is the tag, line, and offset for the address

\$123A63, in hexadecimal

0001	010	011	1010	0110	0011
2	4	7	1	3	

Tag: 0x 247

line: 0x 13

offset: 0x 03

2) Full associative mapping

Same Given

①



② \$123A63

0001	0010	0011	1010	0110	0011
9	1	1	0	3	

Tag: 0x 9103

offset: 0x 03

3) 4-way set association mapping  
Same Given

1)

12	4	5
Tag	Set	offset

2) What is the tag, set, and offset for  
\$ 123463

0001 0010 0011 1010 0110 10011

Tag: 0x 91D  
Set: 0x 3  
offset: 0x 03

## Q2. (10 pts) Cache hit and miss

1, What is the hit ratio for the entire memory reference sequence given (in bold)?

Q2 Cache hit and Miss

256 byte of memory  $\rightarrow 2^8$

16 byte - direct-mapped cache with 4 byte per block  
to  $2^4$   $2^4$

1)

4	2	2
Tag	line	offset

• What is the hit ratio for the entire memory reference sequence given

(1)

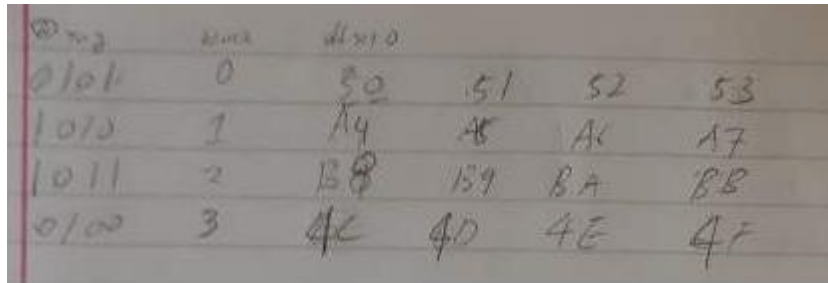
Tag	Block#	offsets	11	2	3
1110	0	E0	E1	E2	E3
0001	1	14	15	16	17
1011	2	18	19	20	21
0110	3	22	23	24	25

5

D  $\frac{5}{14} = 0.357$

	tag	line	block
0x91	1001	0001	M
0xA8	1010	1000	M
0xA9	1010	1001	M
0xAA	1010	1011	M
0xAD	1010	1101	M
0x93	1001	0011	M
0x6E	0110	1110	M
0xB9	1011	1001	M
0x17	0001	0111	M
0xE2	1110	0010	M
0x4E	0100	1110	M
0x4F	0100	1111	M
0x50	0101	0000	M
0xA4	1010	0100	M

2. What memory blocks will be in the cache after the last address has been assessed?



A handwritten table with four rows and six columns. The first column contains binary strings, the second contains decimal numbers, and the remaining four columns contain hexadecimal addresses. The first row has a circled 'Q2' in the first column. The second row has '50' under the third column, which is underlined. The third row has 'B8' under the third column, which is underlined. The fourth row has '4C' under the third column, which is underlined.

Q2	Block	Address			
0101	0	<u>50</u>	51	52	53
1010	1	<u>A4</u>	A5	A6	A7
1011	2	<u>B8</u>	B9	BA	BB
0100	3	<u>4C</u>	4D	4E	4F

Q3. (10 pts) Virtual memory and cache

### Q3 Virtual memory and cache

- 256 k byte virtual address space
- Each frame 32 k byte
- 128 k byte physical address

1) Virtual  $2^{18}$ , Physical  $2^{17}$ , Each frame  $2^{15}$

Virtual	Physical
3   15	2   15

2. Split the bits in memory address based on the cache

Physical  $2^{17}$ , 32 k byte direct mapped cache, block size 256 k byte

$2^{17}$	$2^{11-8=3}$	$2^8$
6	3	8
Line	offset	

3) Suppose the processor has requested to access a memory at 0x 32764

1) Show the change of TLB, TLB LRU, page table and Mem LRU. Also state whether page fault happens or not

State of work 0x 32764  
 0011 0110 0111 0110 0100  
 6

1) Search TLB  $\rightarrow$  not exist

2) Search page table  $\rightarrow$  not exist  $\rightarrow$  **Page fault**

3) So find victim page (Mem LRU)

Update **MEM LRU stack** at

6
0
5
4

**Update Page table** (This to be updated)

Virtual/Physical	Physical/Frame	Valid
0	2	1
1	—	0
2	—	0
3	—	0
4	0	1
5	3	1
6	1	1
7	—	0

⑤ Update TLB

Virtual page #	Physical page #	valid
6	1	1
0	2	1

⑥ Update TLB LRU stack

6
0

Final answer for

1)

TLB	Virtual page	Physical page	valid
	6	1	1
	0	2	1

TLB LRU Stack

6
0

Page table

Virtual page #	Physical page #	valid
0	2	1
1	—	0
2	—	0
3	—	0
4	0	1
5	3	1
6	1	1
7	—	0

Mem LRU stack

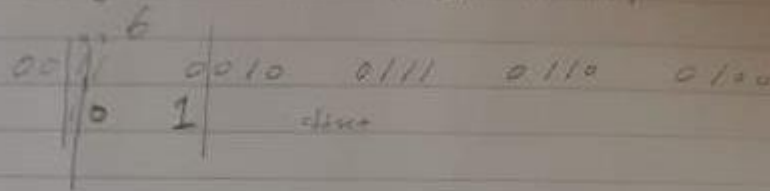
6
0
5
4

page fault

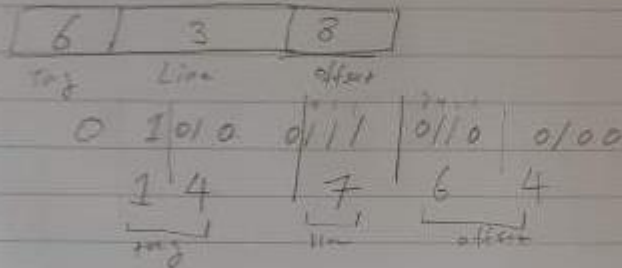
2) Show the changes in Cache.

2) Show the changes in Cache & Ox 32764

Cache



Cache



Cache

Line #	Tag	Data Block
0	10	.
1	0A	.
2	5C	.
3	14	.
4	28	.
5	04	.
6	37	.
7	14	.

1 - 1 = word

0 - 1 = word

0 - 2 = word

Extra credit

1) Suppose you want to write 101 to the word 0 (addr 0). How would you set the value in each case?

Reset	S1	S0	B#2	B#1	B#0	W#
0	1	1	1	0	1	1

4 But clock has to be triggered!

2) Suppose you want to read a data from address 1. Give correct values in each case

Reset	S1	S0	B#2	B#1	B#0	W#
0	0	1	X	✓	X	0

↑  
flush