修 士 論 文 概 要 書

MASTER'S THESIS ABSTRACT

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分野 Field	System LSI	氏 名 Name	ジャン モウフウ 姜　孟冯	指導教員 Supervisor	吉村　猛　㊞
研究 Research	Optimization technologies				
研究題目 Theme	Scheduling with Multiple Supply Voltages in High-Level Synthesis				

1. 研究の内容 Research Contents

(A)概要（背景・目的・目標・結果）Abstract (Background/Purpose/Target/Result)

As the semiconductor technology advances, power dissipation becomes a more and more critical problem in the design of both portable and desktop systems. An effective way to reduce power consumption is to lower the supply voltage level of a circuit. Reducing the supply voltage, however, causes an increase of the circuit delay and reduction of the throughput. In order to maintain the throughput, there is a way to use resources operating at multiple supply voltages.

The goal is to minimize power/energy consumption under both resource and latency constraints when the resources operating at multiple voltages (5V, 3.3V, and 2.4V). In particular, the final scheduling wonder modules on the critical paths to be assigned to the higher voltage levels (thus meeting the latency constraint)while modules on noncritical paths to be assigned to the lower voltage levels (thus reducing the power consumption).

The proposed algorithm Iterative Refinement Multiple Voltage Scheduling (IRVMS) can be treated as an iteration containing two phases: In Phase I, a Min-Cut based Voltage Assignment is used. It initializes the operations in the lowest voltages and tries to shorten the nodes in each of the critical paths gradually as little power increase as possible. In Phase II, ASAP/ALAP Scheduling is performed first and then do the List Scheduling by the priority which is defined as the latency weighted depth of each node. From the result of scheduling, we count the unallocated resources in each control step and make use of this information in the Voltage Assignment phase of the next cycle, thus we will have a heuristic approach to help us to increase the voltages of useful nodes.

From the experiment results, the average power saving is 22.5% under the time constraint $T_{cons}=1.5T_{LB}$ while the power saving can be 46.21% when $T_{cons}=2T_{LB}$ by using constrained resources.

(B)新規性・有効性について/Originality/Effectiveness

Use scheduling with multiple supply voltage to improve the reduction of power consumption.

Implement multiple voltage scheduling method in an iterative refinement way.

Explore the interaction between voltage assignment and scheduling in Multiple Voltage Scheduling.

The effectiveness of Multiple Voltage Scheduling in power saving can be seen from the experiment results.

(C)本人が具体的に研究した項目について/Research items specifically you have done

1. Read books and papers about some basic conception such as high-level-synthesis, scheduling, binding, level shifter, multiple supply voltages and so on.

2. Learn algorithms on VLSI and train programming skills so as to prepare for the final coding challenge.

3. Find a min cut based voltage assignment method which can be used in my field and make some improvement on it to better the solution under resource constraints

4. Code my own algorithm, modified it constantly in many details and get a final result under both latency and resource constraints

2. 研究発表等（学術論文誌、国際学会発表、国内学会発表、特許、その他の活動）
Publications (Journal, International conference, Domestic conference, Patent, Others)