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RESEARCH ARTICLE

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A power-efficient current-mode neural/muscular stimulator design for peripheral nerve prosthesis

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Summary

This paper presents a 16-channel power-efficient neural/muscular stimulation integrated circuit for peripheral nerve prosthesis. First, the theoretical analysis is presented to show the power efficiency optimization in a stimulator. Moreover, a continuous-time, biphasic exponential-current-waveform generation circuit is designed based on Taylor series approximation and implemented in the proposed stimulation chip to optimize the power efficiency. In the 16-channel stimulator chip design, each channel of the stimulator consists of a current copier, an exponential current generator, an active charge-balancing circuit, and a 24-V output stage. Stimulation amplitude, pulse width, and frequency can be set and adjusted through an external field-programmable gate array by sending serial commands. Finally, the proposed stimulator chip has been fabricated in a 0.18-μm advanced complementary metal-oxide-semiconductor process with 24-V laterally diffused metal oxide semiconductor option. The maximum stimulation power efficiency of 95.9% is achieved at the output stage with an electrode model of 10-kΩ resistance and 100-nF capacitance. Animal experiment results further demonstrate the power efficiency improvement and effectiveness of the stimulator.

KEYWORDS

electrode, exponential current, neural/muscular stimulator, optimization, peripheral nerve prosthesis, power-efficient

1 | INTRODUCTION

Neural and muscular stimulators have been widely used in biomedical applications for decades such as cardiac pacemakers, cochlear implants, retinal prosthesis, and brain stimulation.[1-4] Early development of such stimulators involves off-the-shelf electronic components and table-top instruments, which leads to heavy and bulky devices suited only for stationed clinical use powered by mains.[5] With fast development of semiconductor technology and transistor size shrinking in advanced complementary metal-oxide-semiconductor (CMOS) process over the years, battery-powered or wirelessly powered implantable neural/muscular stimulation devices have emerged as a powerful technology to assist disabled patients to improve the quality of their daily life.[6-8] One example is bionic neural link for peripheral nerve prosthesis,[9] which includes amplifiers and microstimulators to acquire neural signals from proximal nerve trunk near the injury point and to trigger muscle contraction at distal end, respectively. Implantable neural/muscular stimulation chips play an important role in the bionic neural link and other biomedical applications.

One of the major concerns in developing implantable stimulation system is the power efficiency (PE), which is defined as the ratio of power delivered to the load (P_{load}) to the total power consumed by the stimulator (P_{tot}). Stimulation PE is becoming increasingly important due to the limited power budget in the implantable circuit and systems nowadays. It determines the battery lifetime or the required coil size for wireless power transfer. Stimulator with high power-efficiency also generates less heat and reduces the risk of tissue damage.[10] The techniques of improving PE of the stimulator will be introduced separately in section 2. Another concern of the stimulator design is the stimulation safety. Compared with the monophasic stimulation, biphasic stimulation provides better safety because the tissue potential can be timely recovered.[11] To further remove the residue charge due to current mismatch in biphasic stimulation, researchers have proposed current matching and charge balancing techniques[12,13] to improve the stimulator design. A simple way to remove residue charge is shorting stimulation and reference electrodes after each stimulation to make the tissue potential recovered back to its reference level. However, the recovery time is depended on tissue-electrode RC time constant, which is usually large (~ms) and thus limits the maximum stimulation frequency. Active charge balancing can quickly remove the residue charge by inserting a series of positive or negative pulses within a very short duration after each stimulation, realizing the safety without compromising the stimulation frequency much.

An additional design consideration of the stimulator is its stimulation effectiveness. Based on the previous researches,[14,15] muscle stimulation usually requires an output current of several hundred micro amperes while the nerve stimulation needs smaller amplitude due to its high sensitivity, which requires a stimulator with adjustable stimulation parameters (ie, current amplitude, pulse width, and frequency). On the other hand, the tissue-electrode interface usually has high impedance, which requires large voltage compliance at the output stage of the stimulator to deliver large enough current to the load.[16,17]

This paper presents an integrated power-efficient 16-channel neural/muscular stimulator by using a new technique to improve the PE. By theoretically analyzing and optimizing the PE of a current-mode stimulator, we find that exponential waveform is the ideal current waveform for stimulation. Thus, a continuous-time exponential current generator is proposed and implemented in the neural/muscular stimulator integrated circuit (IC). Besides PE, the proposed stimulator IC also features stimulation safety and effectiveness. It includes active charge balancing circuits and biphasic current drivers to avoid tissue damage and also has 24-V output stages to provide large voltage compliance with 1.8-mA maximum output current. Moreover, the current copying technique is used and DAC sharing by multiple channels is realized in this stimulator design, to save the chip area and further improve the PE. Finally, the stimulator is fabricated by using Global Foundry 180-nm CMOS process and tested in the in vivo experiments, which demonstrate the improved PE and effectiveness of the chip by using proposed technique. The remaining part of the paper is organized as follows. The PE analysis and optimization is presented in Section 2. System architecture and circuit implementation are described in Section 3. Section 4 presents the measurement and experiment results, followed by the conclusion in Section 5.

2 | ANALYSIS AND OPTIMIZATION OF POWER EFFICIENCY IN STIMULATORS

Stimulator ICs can be used in bionic neural link for peripheral nerve prosthesis, as mentioned in section 1 and shown in Figure 1A. When the compound action potentials from proximal nerve trunk are detected by front-end circuit of the bionic neural link, the stimulators are triggered to generate stimulus to the distal nerve or muscles, bypassing the injury gap. For the stimulator IC design, there are 3 different stimulation modes to choose—voltage mode, charge mode, and current mode,[18] as shown in Figure 1B to D. The voltage-mode stimulator (Figure 1B) generates a voltage directly on the tissue load. Considering the output current branch as the output stage only, the PE of the output stage is given by

$$\mathrm{PE}(t) = \frac{P_{\mathrm{load}}(t)}{P_o(t)} = \frac{V_{\mathrm{load}}(t)\cdot I_o(t)}{V_{\mathrm{stim}}(t)\cdot I_o(t)} = \frac{V_{\mathrm{load}}(t)}{V_{\mathrm{stim}}(t)}, \tag{1}$$

in which $V_{\mathrm{load}}(t)$ is the voltage over the load, $V_{\mathrm{stim}}(t)$ is the stimulation voltage, and $I_o(t)$ is the resultant current in the output stage, respectively. It is known that the voltage-mode stimulation provides the highest PE[19,20] because ideally, V_{load} equals to V_{stim} at the output stage of the stimulator. Nonetheless, its uncontrolled or inaccurate controlled current and charge injection makes the voltage-mode stimulation inappropriate for clinical applications. The charge-mode stimulation as shown in Figure 1C has accurate control over the amount of injected charge.[21] However, it requires area-consuming capacitors (~μF), which prevents its adoption in implantable applications particularly when the multichannel stimulation is required. The above-mentioned deficiencies of voltage-mode and charge-mode stimulation methods make

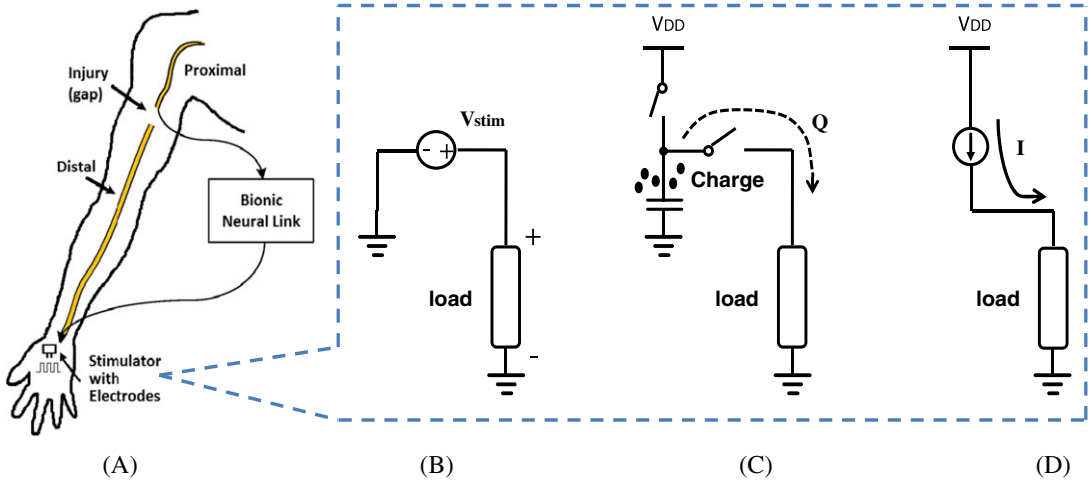


FIGURE 1 (A) Application of the stimulator IC used in bionic neural link for peripheral nerve prosthesis. Conceptual diagrams of the stimulators based on (B) voltage-mode, (C) charge-mode, and (D) current-mode stimulation [Colour figure can be viewed at wileyonlinelibrary.com]

the current-mode stimulation the most widely adopted method in stimulator designs.[22-24] For PE of current-mode stimulator, also considering the output current branch as the output stage only, the PE is expressed as

$$\mathrm{PE}(t) = \frac{P_{\mathrm{load}}(t)}{P_o(t)} = \frac{V_{\mathrm{load}}(t)\cdot I_{\mathrm{stim}}(t)}{V_{\mathrm{DD}}\cdot I_{\mathrm{stim}}(t)} = \frac{V_{\mathrm{load}}(t)}{V_{\mathrm{DD}}}, \tag{2}$$

in which I_{stim} is the stimulation current and V_{DD} is the supply voltage of the output stage. $V_{\mathrm{load}}(t)$ is determined by the load impedance and stimulation current, which is always smaller than V_{DD}. Thus, the current-mode stimulator usually has the lowest PE.

The low-PE of current-mode stimulators comes from the need of accommodating variable load impedances and stimulation strengths caused by varying stimulation interface conditions between electrodes and stimulation sites. The PE degrades dramatically when the voltage across the load $V_{\mathrm{load}}(t)$ is low due to small load impedance or low stimulation current, as illustrated in Figure 2A. To overcome this issue, a supply adaptation technique was proposed,[22,23] which adjusts the supply voltage according to the voltage across the stimulation load. By doing so, the overhead voltage of the current driver circuit can be maintained low and would not deteriorate the PE. This technique can improve the PE significantly provided the supply voltage can be controlled in fine steps. However, the DC-DC conversion process required in the supply adaptation has limited PE and response time. To generate large number of varying fine supply steps over time, it necessitates significant silicon area and/or off-chip components. To reduce the system complexity and requirement, a simplified adaptation method is used in Lee et al[10] shown in Figure 2A, which only adjusts the supply voltage according to the maximum voltage on the load. In this method, according to Figure 2A, the intrinsic capacitive characteristics of the interface between the stimulation electrode and tissue degrades the PE when constant stimulation current is applied, as indicated by the shaded area in Figure 2B. To mitigate this PE degradation, a discrete-time current waveform optimization method in Halpern and Fallon[25] can be used to reduce the required maximum voltage. However,

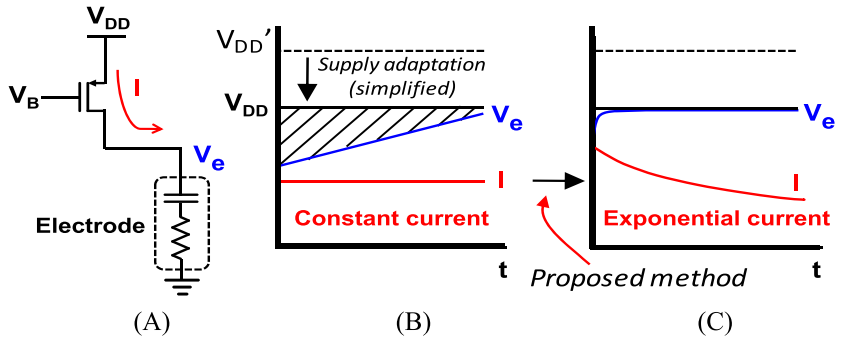


FIGURE 2 (A) Simplified model of the current-mode stimulator, (B) power waste (shaded area) in the simplified supply adaptation method, and (C) concept of the proposed exponentially decaying current for high-power-efficiency current-mode stimulation [Colour figure can be viewed at wileyonlinelibrary.com]

the limitation of this method is that it requires large computing resource to calculate the optimized current values in each discrete time step, and the current in each time step is still constant; thus, PE still degrades in each time step.

To achieve maximum PE, the current-mode stimulator must maintain a constant voltage on the stimulation electrode and minimize the power wasted by the current driver overhead voltage, as illustrated in Figure 2C. We propose an assumption that the electrode voltage can become constant if the output current is exponential and time continuous. If the assumption is true, then the PE can be maximized by adding an exponential current generator as the stimulus source in the stimulator. To theoretically valid this assumption, we analyze and optimizing the PE of a current-mode stimulator in the following part of the section, trying to prove that the exponential waveform is the ideal current waveform for stimulation.

As mentioned above, the conventional constant stimulation current will degrade the PE of the current-mode stimulator because of the intrinsic capacitance associated with the electrode-tissue interface. The voltage (V_e) on stimulation electrode is

$$V_e(t) = I(t)\times R_L + \int_0^t \frac{I(t)}{C_L} dt \tag{3}$$

To maximize the PE, a constant voltage is preferred on the stimulation electrode. Based on the circuit model in Figure 2A, the constant load voltage can be realized during stimulation when the following equation is fulfilled:

$$\frac{dV_e(t)}{dt} = \frac{d}{dt}\left(I(t)\times R_L + \int_0^t \frac{I(t)}{C_L} dt\right) = 0 \tag{4}$$

where $V_e(t)$, $I(t)$, R_L, and C_L are the electrode voltage, stimulation current, load resistance, and load capacitance, respectively. By solving 4, $I(t)$ can be expressed as

$$I(t) = I_0 \exp\left(-\frac{t}{R_L C_L}\right) \tag{5}$$

where I_0 is the initial value of the stimulation current. As such, the solution proves the assumption that an exponentially decaying stimulation current can realize optimized PE. From 5, we can conclude that the exponential current pulse is 1 of the most promising waveforms in neural stimulation so long as its time constant is optimized.[4] The theoretical analysis shows that the use of exponentially decaying stimulation current makes the electrode voltage nearly constant and hence minimizes the voltage headroom consumed by the current driving transistors at the stimulator output stage over the pulse duration.

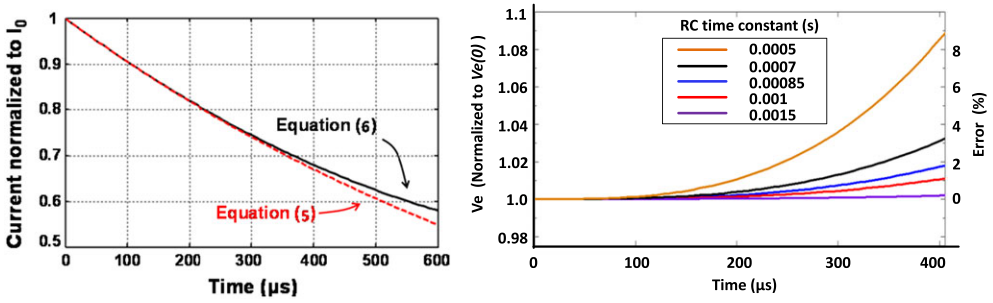
3 | CIRCUIT IMPLEMENTATION FOR EXPONENTIAL CURRENT GENERATION

To construct the exponential current waveform in 5 by an IC with required time constant $R_L C_L$, we use second-order Taylor series approximation (t is small) and high order terms are neglected as shown in the following equation.

$$I(t)\approx I_0\left(1 + \left(-\frac{1}{R_L C_L}\right)t + \frac{1}{2}\left(\frac{1}{R_L C_L}\right)^2 t^2\right) \quad = \frac{I_0}{2}\left(1 + \left(1-\frac{1}{R_L C_L}t\right)^2\right) \tag{6}$$

The error of 6 when compared with 5 is less than 6% in the range of $t < 600$ μs as shown in Figure 3A, when the typical values of 10 kΩ and 100 nF are used for the parameters R_L and C_L, respectively. For typical neural/muscular stimulation pulses whose widths are smaller than 300 μs, the approximated exponential current given by 6 can be regarded as the ideal exponential waveform. To verify the effectiveness of the approximation in the voltage waveform optimization explained in Section 1, Figure 3B shows the electrode voltage V_e calculated by integrating the approximated exponential current in 6. Different $R_L C_L$ are used for covering the range of load variation from −50% to +50% of the default $R_L C_L$ value (1 ms), and it is found that the electrode voltage, *Ve*, is nearly constant (variation less than 4%) for $t < 300$ μs. The error is neglectable (<2%) when the load varies from −30% to +50% for a time duration within 300 μs.

The circuit shown in Figure 4 can be used to implement the approximated exponential current described in 6. The transistors M_1 and M_2 have the identical size. Using the long-channel MOS transistor model and ignoring the channel length modulation effect, the output current I_{out} can be expressed as



(A) (B)

FIGURE 3 (A) Comparison between the ideal exponential current waveform and its second-order Taylor series approximation (approximated exponential current waveform) and (B) electrode voltage calculated by integrating the approximated exponential current [Colour figure can be viewed at wileyonlinelibrary.com]

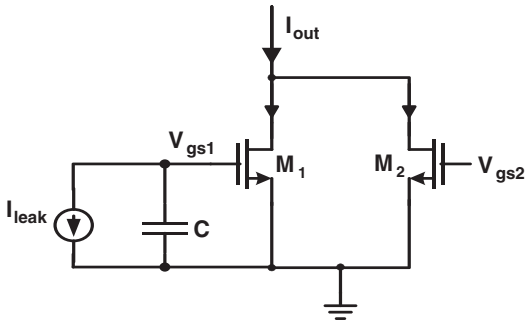


FIGURE 4 Proposed current generation circuit to output approximated exponential current using Taylor series approximation

$$I_{\text{out}}(t) = \frac{\beta}{2}\left(V_{\text{gs1}(0)} - V_{\text{thn}}\right)^2 + \frac{\beta}{2}\left(V_{\text{gs2}(0)} - V_{\text{thn}} - \frac{I_{\text{leak}}}{C}t\right)^2 = \frac{2\beta\left(V_{\text{gs}(0)} - V_{\text{thn}}\right)^2}{4}\left(1 + \left(1 - \frac{I_{\text{leak}}}{C\left(V_{\text{gs}(0)} - V_{\text{thn}}\right)}t\right)^2\right) \tag{7}$$

where β is the MOS transistor transconductance parameter, $V_{\text{gs}(0)}$ ($=V_{\text{gs1}}(0) = V_{\text{gs2}}(0)$) is the initial gate-source voltage of M_1 and M_2, and V_{thn} is the threshold voltage of NMOS transistors. Equating 7 with 6, the values of design parameters such as β, $V_{\text{gs}(0)}$, C, and I_{leak} can be determined to produce a desired exponential current waveform for stimulation, resulting in a nearly constant V_e and optimized PE. It should be noted that in the circuit implementation the matching of transistor (M_1 and M_2) sizes is important as large layout mismatch will cause nonideality. It is found from simulation that the PE has a degradation of 0.05% to 0.35% when the mismatch is set from ±1% to ±5%. A good matching (<±1%) of transistors in the circuit layout placement will make the PE degradation neglectable.

4 | SYSTEM ARCHITECTURE AND CIRCUIT IMPLEMENTATION

The system architecture of the 16-channel power-efficient stimulator IC is shown in Figure 5. It consists of a global digital controller (GDC), a 6-bit DAC, a bias generation circuit, and 16 stimulation channels. The stimulation channels can be selectively powered down to minimize the overall power consumption. Each channel consists of a current copier, an exponential current generator, a high-voltage current driver (HVCD) and an active charge-balancing (ACB) circuit. The GDC is always kept on to receive and decode the commands. The 6-bit DAC is shared by 16 channels to save the chip area and power and controlled by the GDC to generate the reference current for the current copier in each channel. The pseudo-exponential current generator provides the nonconstant current close to the exponential waveform for high PE.[26] A nanocurrent generator is needed for providing the leakage current I_{leak} in the pseudo-exponential current generator shown in Figure 4. Finally, the generated biphasic exponential current is amplified and delivered to the

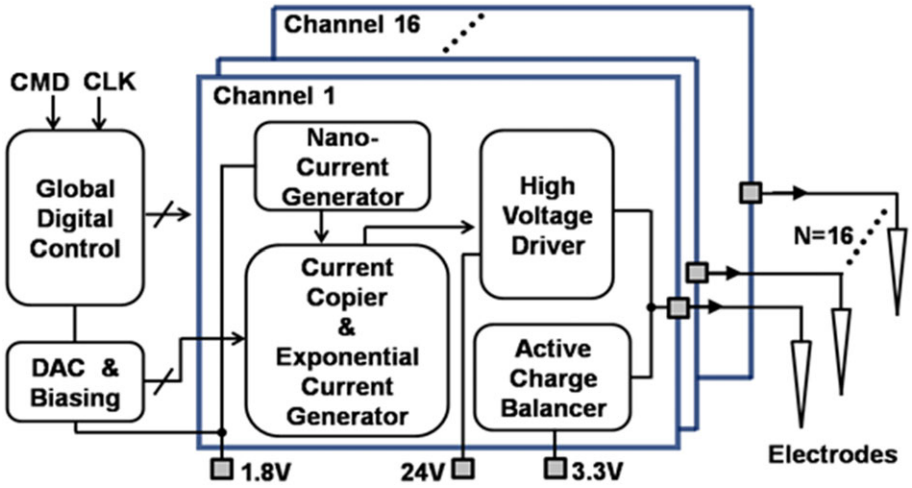


FIGURE 5 System architecture of the 16-channel power-efficient stimulator IC [Colour figure can be viewed at wileyonlinelibrary.com]

stimulation site by the HVCD with 24-V compliance. The ACB circuit removes the residual charge produced by the mismatched biphasic stimulation current by using a pulse insertion technique.[13]

4.1 | Current copier and exponential current generator

The current copier and the exponential current generator are key circuit blocks in our design. The current copier[27] enables DAC-shared simultaneous multichannel stimulation, and the exponential current generator produces the optimized current waveform required for high-PE. The circuit schematic of a single stimulation channel is shown in Figure 6 A. In the current copier and exponential current generator, a switched transistor array M_C is used to generate the

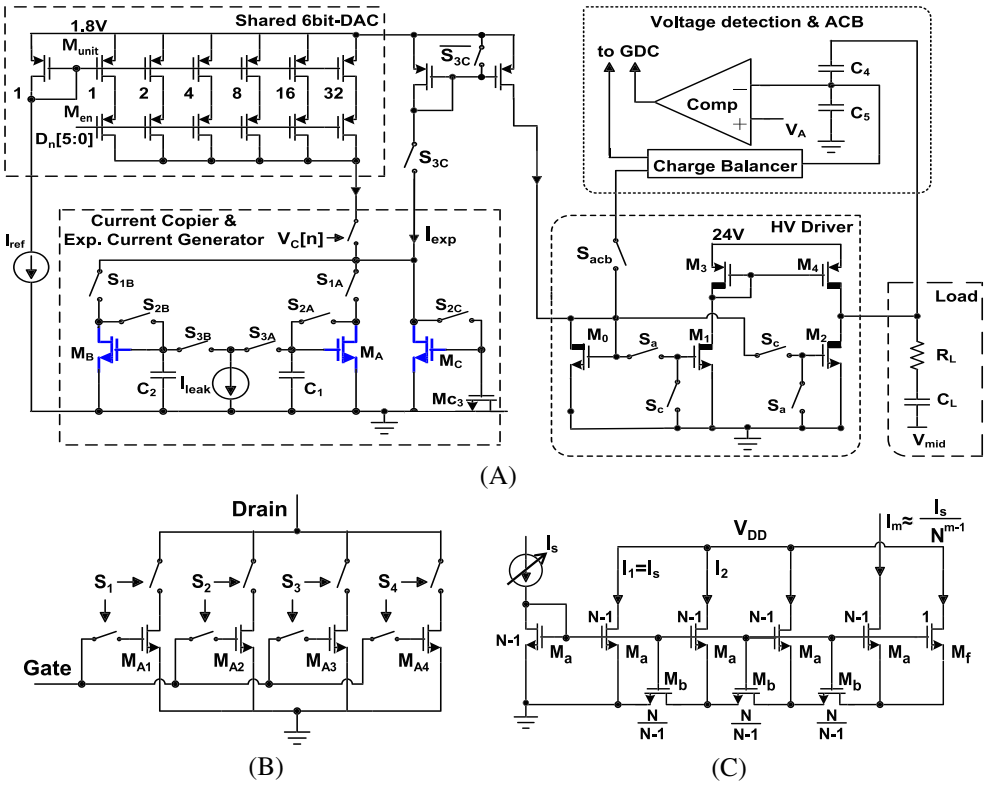


FIGURE 6 (A) Schematic of the shared 6-bit DAC and single-channel circuits, (B) switched transistor array M_A used in the current copier, and (C) ultra small current generator [Colour figure can be viewed at wileyonlinelibrary.com]

constant current term in 7, and 2 identical transistor arrays M_A and M_B are used to generate the time-dependent current term in 7. The schematic diagram of M_A is shown in Figure 6B.

Comparing 6 and 7, to obtain the exponential current waveform, the following condition has to be satisfied:

$$\frac{I_{\text{leak}}}{C\left(V_{\text{gs}(0)}-V_{\text{thn}}\right)}=\frac{1}{R_L C_L}. \tag{8}$$

Consequently, assuming a constant initial overdrive voltage $V_{\text{gs}(0)} - V_{\text{thn}} = 400$ mV, the values of I_{leak} and C (C_1 and C_2 in Figure 6) can be derived from the values of R_L and C_L. The transistor M_{C3} is used as a MOS capacitor of around 2 pF. Because the M_{C3} is used to keep the gate-source voltage of M_C constant, the MOS capacitor that has large capacitance density is used to save the chip area. For C_1 and C_2, MIM capacitors ($C = 2$ pF) are used to provide constant capacitance for the varying voltage across the capacitors. Practically, R_L and C_L have a wide range based on the electrode shape and implantation environment.[13,28,29] Thus, I_{leak} is required to be designed tunable to cover the wide range of R_L and C_L. In our system, a nanocurrent generator shown in Figure 6C by using the current splitter structure[30] provides I_{leak}. Controlled by the external current source I_s, the current splitter generates an output current ranging from 140pA to 3.5 nA, which can cover a wide range of electrode impedance from $R_L C_L = 2.3 \times 10^{-4}$ Ω F to $R_L C_L = 5.7 \times 10^{-3}$ Ω F. For the default value of I_{leak} using $R_L = 10$ kΩ and $C_L = 100$ nF as the load,[13] the calculated value of I_{leak} is 800 pA.

Practically, R_L and C_L have a wide range based on the electrode shape and implantation environment.[28,29] Besides, the initial overdrive voltage (Vgs(0) − Vthn) also changes due to process variation. Therefore, I_{leak} needs to be tunable to satisfy 8. A nanocurrent generator shown in Figure 6C is used to provide I_{leak}. In the circuit design, the gate nodes of all transistors are connected together. In the first-order cell, the current I_1 is equal to the reference current I_s, and the current flowing through M_b is approximately N times smaller than I_1. In this design, N is set to 10 and a fourth-order current splitting is used to generate I_{leak}. The default value of current source I_s is set to 1.2 μA to generate the current of about 800 pA for $R_L = 10$ kΩ and $C_L = 100$ nF. By tuning I_{leak} through the external current source I_S, 8 can be satisfied for the desired time constant ($R_L'C_L'$). This adjustable I_{leak} can also be used to calibrate the capacitor (C_1 and C_2) and threshold voltage (Vthn) variation-induced nonideality in 8.

The current copier and exponential current generator circuit operates in 3 phases as shown in Figure 7. First, in the current-replication phase, the control signal from the GDC connects the circuit to the DAC output. The switches S_{1A}, S_{2A}, S_{1B}, S_{2B}, and S_{2C} in Figure 6A are closed so that the DAC output current I_{DAC} can flow into transistor arrays MA, MB, and MC, as shown in Figure 7A. Because these 3 transistor arrays have the same size, they conduct the same amount of current ($I_{\text{DAC}}/3$) through each and the corresponding same gate-source voltages are stored in the capacitors C_1, C_2, and M_{C3}. As the cathodic stimulation phase starts, the circuit is disconnected from the DAC output and operates with the gate-source voltages stored in the capacitors. Because the current flowing through M_A and M_C forms the exponential current sink I_{exp} in the cathodic stimulation phase, the switches S_{1A} and S_{3A} are closed while all the other switches are open, as shown in Figure 7B. Similarly, during the anodic stimulation phase shown in Figure 7C, the circuit remains disconnected from the DAC output, and I_{exp} is generated from M_B and M_C by using the gate-source voltages stored in C_2 and M_{C3} with S_{1B} and S_{3B} closed.

In previous calculation of I_{leak}, the initial overdrive voltage V_{gs0}-V_{thn} is fixed as 400 mV; however, to support variable strengths of stimulation, the DAC generates I_{DAC}, which varies over the range from 4 μA to 252 μA. Therefore, the initial overdrive voltage ($V_{\text{gs}(0)}$-V_{thn}) of the transistors in current copier cells varies with the current, which will then affect the

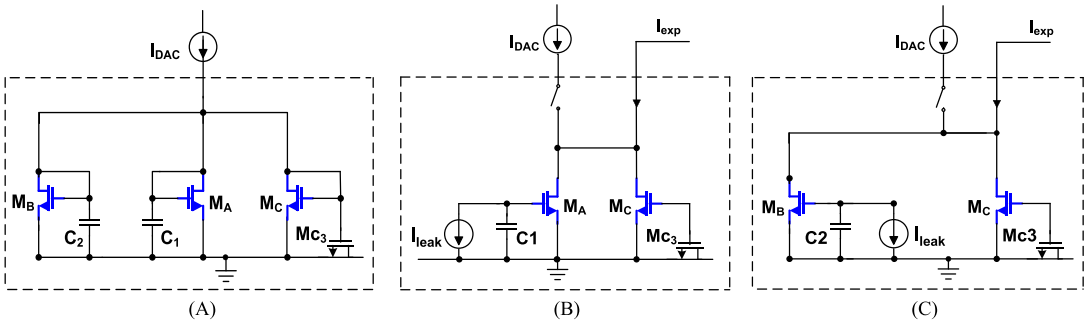


FIGURE 7 Operation of the current copier and exponential current generator circuit: (A) current-replication phase, (B) cathodic stimulation phase, and (C) anodic stimulation phase [Colour figure can be viewed at wileyonlinelibrary.com]

exponential current waveform. To solve this problem, the switched transistor arrays M_A, M_B, and M_C are implemented as shown in Figure 6B to maintain the initial overdrive voltage relatively constant over the range of I_{DAC}. The switches S_1, S_2, S_3, and S_4 in Figure 6B are controlled by using the logic shown in Table 1. For the nth stimulation channel, as the 6-bit DAC input code D_n[5:0] becomes larger, the DAC output current I_{DAC} increases and the larger transistor in the array is chosen. To minimize the circuit area overhead while maintaining the acceptable waveform accuracy, only 4 transistors (M_{A1}-M_{A4}) are used in each array by dividing the entire I_{DAC} range into 4 regions. For different regions, different transistors are activated. The transistors are sized proportional to the average I_{DAC} values in the corresponding regions. By doing so, the initial overdrive voltage (V_{gs0}-V_{thn}) of the transistors can be kept within the range from 300 mV to 400 mV, preventing significant degradation of the exponential current waveform generated.

4.2 | High-voltage current driver and active charge-balancing circuit

To provide sufficient stimulation strength even when the load impedance is high, 24-V output stages are designed by using a 0.18-μm high-voltage CMOS process. The output driver transforms the monophasic current to the biphasic current by switching between 2 paths—one for cathodic stimulation and the other for anodic stimulation. As shown in Figure 6A, the current mirror composed of M_0 and M_2 forms the anodic stimulation path, and the cathodic stimulation path consists of 2 pairs of current mirrors (M_0-M_1 pair and M_3-M_4 pair). Because M_0-M_2 and M_3-M_4 pairs mirror the current with the ratio of 1:10, nearly 90% of current is consumed in the final load-driving branch (namely output stage of the stimulator), reducing the current wasted in the branches added to form the current steering structure. In this multichannel stimulator, considering the large transistor size needed in the output driver, simple current mirror structure is adopted in the design instead of the cascode structure as cascode structure simply doubles the HVCD circuit area. The current mismatch can be compensated by setting different current amplitude in cathodic and anodic phases by programming the digital controller.

To secure the charge balancing, an ACB circuit shown in Figure 6A is implemented to remove the residual charge by using the pulse insertion technique.[31] First, before each stimulation cycle, the electrode voltage (V_e) equals the reference voltage (V_{mid}), and the node voltage (V_n) between capacitor *C4* and *C5* is initially set equal to V_A. After each stimulation, the electrode potential (V_e) is sampled by a capacitive voltage divider and compared with V_A by a comparator. If $V_n > V_A$ ($V_e > V_{mid}$), the GDC will send a short pulse to close switches S_{acb} and S_c, delivering a sink current to absorb the excessive residual charge on the electrode. Active charge-balancing keeps inserting pulses until V_n is slightly smaller than V_A. If $V_n < V_A$ ($V_e < V_{mid}$), in the similar way, the stimulator will deliver an anodic current pulse, until finally, the voltage on the electrode is kept within a safety level ($V_{mid} \pm 50$ mV). The detail sizes of the transistors in the key circuits shown in Figure 6 are summarized in Table 2.

TABLE 1 Switched transistor array control logic

D_n[5:0]	I_{DAC}	S_1	S_2	S_3	S_4
$0 \le D_n \le 4$	$0 \le I_{DAC} \le 16$ μA	1	0	0	0
$5 \le D_n \le 16$	20 μA $\le I_{DAC} \le$ 64 μA	0	1	0	0
$17 \le D_n \le 36$	68 μA $\le I_{DAC} \le$ 144 μA	0	0	1	0
$37 \le D_n \le 63$	148 μA $\le I_{DAC} \le$ 252 μA	0	0	0	1

TABLE 2 Summary of transistor sizes in key circuits (in Figure 6)

	M_{unit}	M_{en}	M_0, M_1	M_2	M_3	M_4	M_{A1}	M_{A2}	M_{A3}	M_{A4}	M_a	M_b, M_f
W (μm)	0.22	3	20	20	20	20	0.54	1.46	1.9	3.7	1	1
L (μm)	1.21	0.18	2	2	1.2	1.2	3	2	1	1	1	1
Multiplier	1	1	1	10	2	20	1	1	1	1	9	1

4.3 | Global digital controller and system operation

The GDC in the stimulator IC provides the signals to control the switches between the shared DAC and 16 stimulation channels as well as the switches in the current copier, exponential current generator, and high-voltage output driver for each channel. The timing diagram of control signals used for system operation is shown in Figure 8A. First, the stimulation parameters such as stimulation pulse width ($T[n]$), residue charge balancing duration ($T_{\text{dis}}[n]$), and stimulation current amplitude ($D_n[5:0]$) for all 16 channels are set by decoding the incoming commands to configure the stimulation duration and amplitude of each channel. The command frame format is shown in Figure 8B. When the nth channel is triggered, the digital code presenting the current amplitude of the selected channel goes to the DAC input through a multiplexer. $V_C[n]$ is set to logic 1 to connect the channel with the DAC output, and the switches are configured to operate the channel in the current-replication phase for 4 μs. The cathodic stimulation phase then begins 1 μs after $V_C[n]$ goes back to logic 0. By using the initial gate-source voltages stored during the current-replication phase, the transistor arrays M_A and M_C generate the exponential stimulation current during $T[n]$. After delivering the cathodic stimulation current, there is an interphasic delay of 30 μs before the anodic phase starts. In the anodic stimulation phase, the exponential current generated by M_B and M_C is steered into the high-voltage driver. The active charge balancing operation is initiated after the anodic stimulation phase and sustained for $T_{\text{dis}}[n]$. For multichannel operation, as it takes 4 μs for the selected channel to copy its current from the DAC output, the multichannel triggering signals should come in with a minimum interval of 4 μs.

5 | MEASUREMENT RESULTS

5.1 | Bench-top test

The 16-channel stimulator IC is implemented in a 0.18-μm CMOS technology with 24-V high-voltage laterally diffused metal oxide semiconductor option. The core area is 1.65 mm × 1.65 mm, and the total die area including pads is 2.5 mm × 2.5 mm. The microphotograph of the fabricated stimulator IC and measured performance summary are shown in Figure 9.

Figure 10A to C compare the constant-current stimulation and exponential-current stimulation in measured stimulation current and electrode voltage waveforms. In the measurement, 3 dummy loads with different R_L and C_L are used: 10-kΩ resistor and 100-nF capacitor for general high electrode impedance,[13] 3.7-kΩ resistor and 240-nF capacitor electrode,[28] and 8-kΩ resistor and 300-nF capacitor electrode.[29] The constant-current stimulation is carried out as a

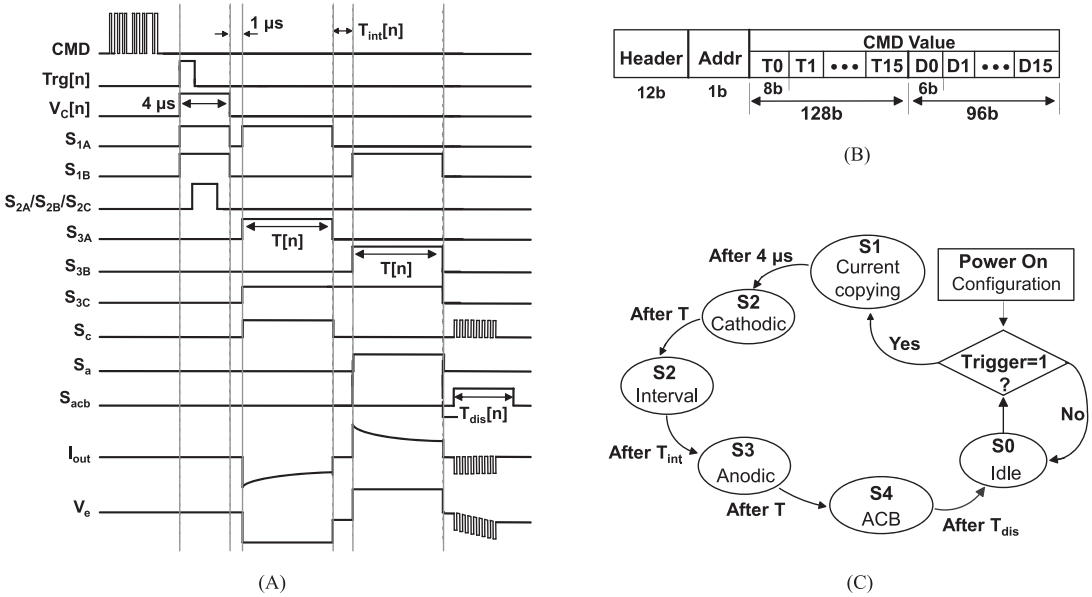
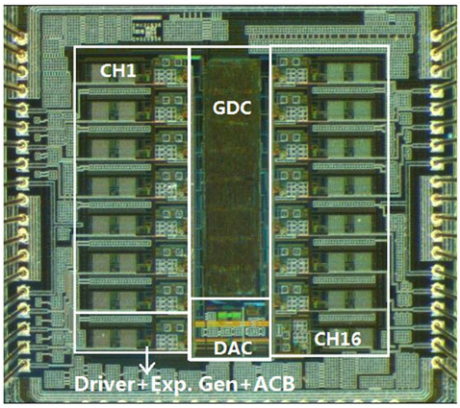


FIGURE 8 System operation: (A) digital control timing diagram: cathodic and anodic stimulation pulse width are determined by S_{3A} and S_{3B}, respectively; $Vc[n]$ controls the current copying phase; I_{out} and V_{e} represent the waveform of output current and electrode voltage; the duration of active charge balancing is controlled by S_{acb}; (B) command frame format and (C) control state diagram



Parameter	Value
Number of channels	16
Core area	1.65 mm × 1.65 mm
Stimulation method	Biphasic current mode
Current waveform	exponential waveform
Max. current amplitude	~1.8 mA
Current amplitude control step	~30 μA
Pulse duration	1 μs – 255 μs
Interphasic delay	30 μs
Resting potential (with charge balancing)	V_{ref} ± 50 mV
Quiescent power consumption (per channel)	45 μW
Max. stimulation PE of output stage (Eq. 2)	95.6%
Max. overall PE of the stimulator	87.8%

FIGURE 9 Die micrograph of the implemented 16-channel stimulator IC and its measured performances [Colour figure can be viewed at wileyonlinelibrary.com]

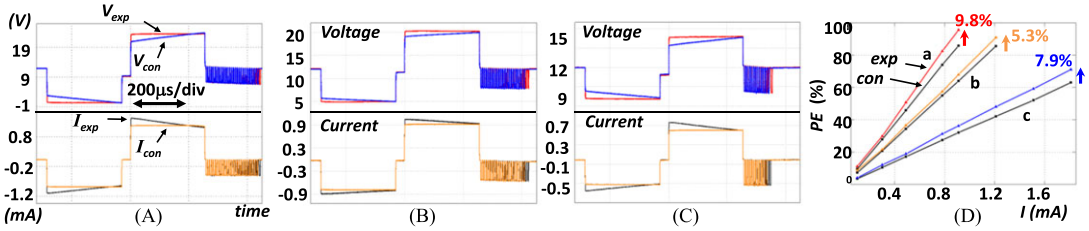
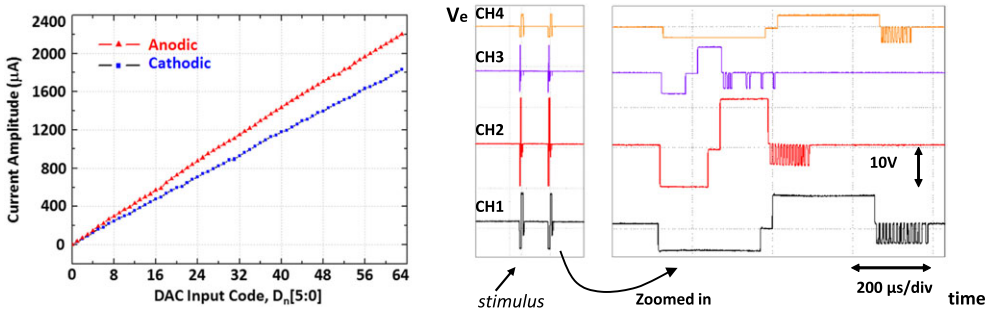


FIGURE 10 Measured waveforms of the stimulation currents and electrode voltages: (A) $R_L = 10$ kΩ and $C_L = 100$ nF load impedance, (B) $R_L = 3.7$ kΩ and $C_L = 240$ nF load impedance, (C) $R_L = 8$ kΩ and $C_L = 300$ nF load impedance, and (D) power efficiency versus stimulation current [Colour figure can be viewed at wileyonlinelibrary.com]

comparison with disabling the exponential current generator by setting a 0 local biasing (I_s and I_{leak} in Figure 6). In Figure 10A, the constant current is set at 910 μA, while the current source I_s is tuned to 1.3 μA. It is verified that the electrode voltage is kept almost constant when the exponential current is well tuned for stimulation. Figure 10D shows the measured PE versus the constant stimulation current. For plots *a* and *c*, the current stops at 1.21 mA and 910 μA, respectively, because of the limitation of the output voltage range. For plot b, the PE reaches at 71.2% at the maximum output current 1.8 mA. The PE of output stage is calculated by integrating 3 over the cathodic and anodic pulse duration, respectively, and taking the average value, using the measured electrode voltage waveforms. For default electrode impedance, as shown in Figure 10D, using exponential current, the maximum PE of 95.9% is achieved at 910 μA stimulation current, which is 10% improvement from 85.9% efficiency under constant-current stimulation. The maximum PE is only limited by the headroom voltage of PMOS and NMOS on the output stage. Considering the power consumption of the entire system (including GDC, DAC, etc), the overall stimulation PE is 87.8%, using default electrode model. In the future design, by adding transistor switches to the biasing circuits and using power gating technique[32] in digital blocks, the quiescent power consumption would be greatly reduced at sleep mode and the overall PE can be further improved.

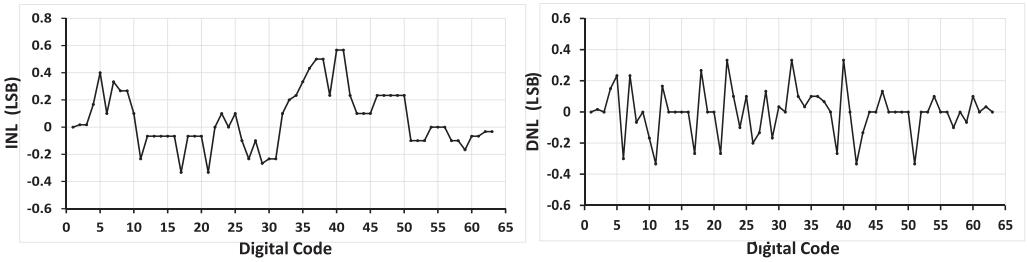
Figure 11A and B shows the curve of stimulation current versus digit code and the electrode voltage waveforms measured in multichannel stimulation, respectively. And the INL and DNL of the DAC are shown in Figure 12. As shown in Figure 11A, when the DAC input code increases from 1 to 63, the measured cathodic stimulation current varies from 30 μA to 1.8 mA while the anodic current changes from 34 μA to 2.2 mA. The unequal cathodic and anodic current is attributed to the channel length modulation effect on transistors in the HVCD circuit. The cascode structure is not used for current sources in the HVCD to save chip area and avoid excessive voltage headroom at the output stage, which leads to PE degradation. The residual charge caused by the unbalanced cathodic and anodic current is eliminated by active charge balancing circuit.

In Figure 11B, channels 1 and 2 are connected with a 10-kΩ resistor and a 100-nF capacitor in series as the load impedance, while channels 3 and 4 are connected with an 8-kΩ resistor and a 300-nF in series as the load impedance. The waveforms have been captured from 4 channels configured with different stimulation parameter values. The zoomed-in electrode voltage waveforms are shown on the right side of Figure 11B. I_s is tuned as 1.2 μA for channel 1, 1.3 μA for



(A) (B)

FIGURE 11 (A) Cathodic and anodic stimulation current measured with varying the DAC input code. (B) Measured multichannel stimulation waveforms: electrode voltage waveforms captured from the first 4 channels. Amplitude (D[5:0]) and pulse width (T[7:0]) of channel 1, channel 2, channel 3, and channel 4 are 20 and 255, 35 and 120, 20 and 60, and 10 and 255, respectively [Colour figure can be viewed at wileyonlinelibrary.com]



(A) (B)

FIGURE 12 Measurement results of (A) INL and (B) DNL of the 6-bit DAC in the stimulator

channel 2, and 0.5 μA for both channels 3 and 4. I_s is slightly different for the same R_L and C_L due to the different V_{gs}-V_{thn} caused by different stimulation currents. The measured result demonstrates that the DAC can be shared among multiple channels with the current-replication technique while facing different load impedance and stimulation parameters. The results also show that the proposed exponential current generator can be integrated and applied to multichannel stimulators for high PE.

5.2 | In vitro test

To verify the proposed method with real electrodes, in vitro experiments have been conducted by using the prototype 16-channel neural/muscular stimulator. In the in vitro experiment, phosphate buffered saline solution is used to emulate the tissue environment. Cuff electrodes (MicroProbes Inc) and concentric bipolar electrodes (SNE-100, 10 mm) are connected with the stimulator IC to deliver the stimulation current into phosphate buffered saline. Five different stimulation current levels are randomly selected, ranging from 100 μA to 1.6 mA. The voltage waveforms on the cuff electrode and concentric bipolar electrode are captured for further analysis and calculation. Figure 13A shows the measured voltage waveforms on the cuff electrode with the constant stimulation current as a comparison and exponential stimulation current for PE optimization. In Figure 13A, the peak current is set at $D = 9$ ($I_{stim} = 278$ μA) and I_s is manually tuned to 4.6 μA for exponential stimulation current to optimize PE. The same experiment is done with the concentric bipolar electrode and the results are shown in Figure 13B ($I_{stim} = 418$ μA, $I_s = 1.8$ μA). For both experiments using cuff and bipolar electrodes, the power efficiencies are calculated by integrating Equation 2 with a supply adapted VDD and the results show that the PE improves by 18.5% for the cuff electrode and 13% for the concentric bipolar electrode, respectively, using exponential stimulation current at different stimulation strength. The PE improvement also depends on the stimulation current amplitude and capacitance of the tissue-electrode load. The in vitro experiments with 2 commercial electrodes prove that using exponential stimulation current is an additional way to further improve the PE in those power efficient stimulators by using power adaptation techniques.[10,23]

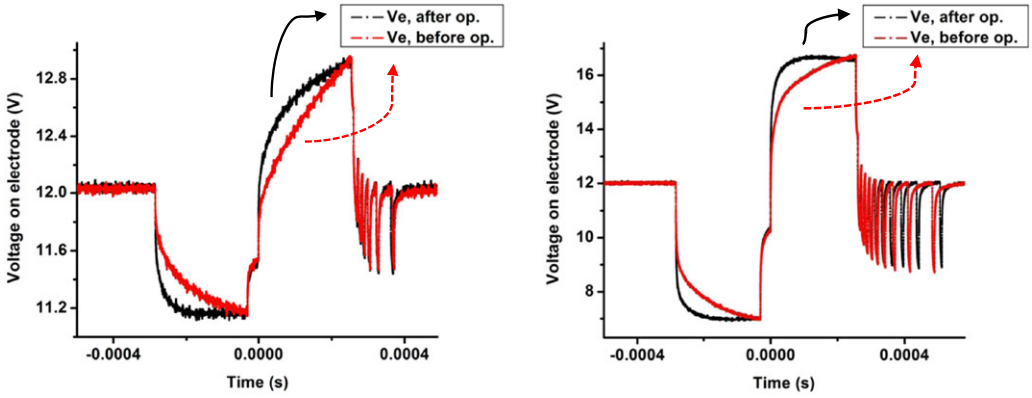


FIGURE 13 (A) Comparison of voltage waveforms measured with the cuff electrode when the constant current stimulation and proposed exponential current stimulation are applied. (B) Comparison of voltage waveforms measured with the concentric bipolar electrode when the constant current stimulation and proposed exponential current stimulation are applied [Colour figure can be viewed at wileyonlinelibrary.com]

5.3 | In vivo test

To further test the proposed method in practical use with tissue environment, an animal experiment has been conducted by using the prototype power-efficient 16-channel neural/muscular stimulator. Figure 14A shows the in vivo experiment setup. An external power supply provides 1.8-V and 24-V voltage to the IC. The laptop and field-programmable gate array are used to program stimulation parameters by sending the commands to the IC. Concentric bipolar needle electrodes (25 mm) are inserted into the gastrocnemius muscle on the right side of the anesthetized rat. When the stimulation is triggered, muscle contraction is observed and the voltage waveforms on the electrodes are plotted and captured by an oscilloscope.

Figure 14B and C shows the measured voltage waveforms on the electrode with and without the PE optimization, respectively. The constant current is set around 900 μA in Figure 14B, while the I_s is tuned to 4.5 μA for the exponential current waveform in Figure 14C. The PE at the output stage during cathodic phase is calculated to be 72.5% for the constant-current stimulation and 80.5% for the exponential-current stimulation. The PE improvement of 8% is achieved at the output stage, which agrees well with the bench-top testing results. The lower PE compared with the bench top measurement is due to a headroom voltage of about 2 V (equivalent to the rectangular area in Figure 2B) observed in the in vivo experiment, which degrades the PE. This can be avoided by either lower the supply voltage or employ the supply adaptation technique, mentioned in section 1, to remove the headroom. In anodic phase, it is observed that the electrode voltage is not ideally flat. It is probably due to the polarization of the electrode-tissue interface, resulting in different load impedance

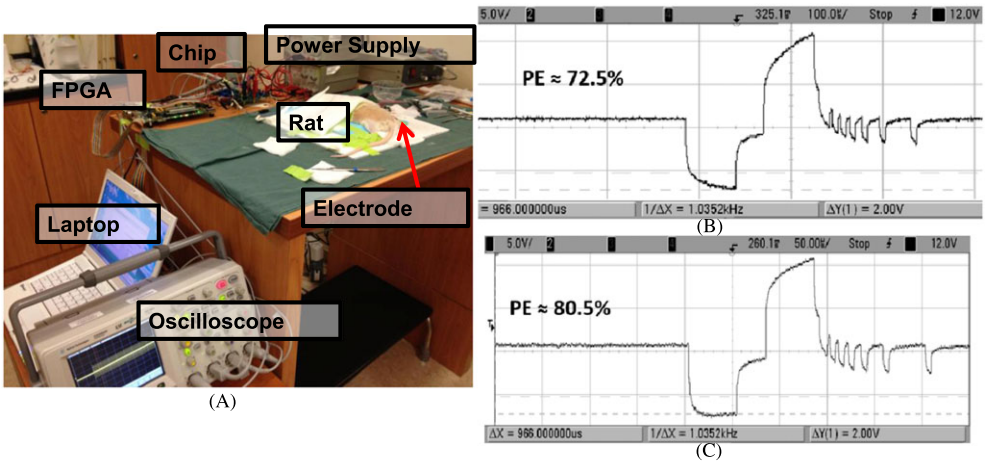


FIGURE 14 (A) In vivo experiment setup. (B) Electrode voltage waveforms measured when the constant current is used for stimulation, and (C) waveform when the exponential current is used for stimulation [Colour figure can be viewed at wileyonlinelibrary.com]

TABLE 3 Performance comparison of current-mode stimulators

Parameter	[19]	[33]	[34]	[22]	[35]	This Work
Process	0.18 μm CMOS	0.5 μm CMOS	0.18 μm CMOS	0.5 μm CMOS	0.18 μm CMOS	0.18 μm CMOS
Number of channels	8	1	1	4	8	16
Core area	5.4 mm^2	2.25 mm^2*	NA	2.25 mm^2*	2.25 mm^2*	2.72 mm^2
Stimulation current waveform	Constant	Constant	Constant	Constant	Constant	Exp
Max stimulation duration	NA	NA	200 μs	512 μs	200 μs	255 μs
Max current amplitude	500 μA	1.3 mA	1 mA	2.5 mA	250 μA	1.8 mA
Max voltage compliance	11.5 V	3.3 V	3 V	4.6 V	3.3 V	11.5 V
Quiescent power consumption (per channel)	23 μW	NA	53 μW	NA	NA	45 μW
Max PE of output stage (Equation 2)	83.3%**	60%**	***	68%	NA	95.9%

*Including pads.

**Calculated on simulation result in the ideal case.

***PE depends on the ripple amplitude.

(R_LC_L) for different stimulation phases. This problem could be solved by setting different I_{leak} values according to Equation 8 in the cathodic and anodic phases in the future design. In this animal experiment, when the stimulation current amplitude of the stimulator is set larger than 267 μA with pulse width of 50 μs, the desired muscle contraction is obviously observed. Muscle contraction becomes stronger with higher stimulation strength in both cases by using constant and exponential current. Although the neural stimulator has high-voltage output stage that can provide stimulation current up to 1.8 mA, a lower current amplitude (<500 μA) is recommended[14] in practical use in case tissue damage during long-term stimulation. The stimulation pulse width needs to be shortened if a large stimulation current is used.

The proposed power-efficiency improved stimulator IC is designed based on the electrode-tissue interface model shown in Figure 2A. With a more accurate model similar to work[33] in the future, the PE optimization would be maximized, but the stimulation current in that case needs to be produced by an extremely complicated circuit. Actually, the bench-top and experiment results have shown that the proposed method based on the simplified model[11,13] is still much effective to improve the PE as most electrode models show considerable capacitive feature. For the application with various electrodes, the precalibration with adjustable I_{leak} illustrated in section 4.1 helps to optimize the PE. The performance comparison of neural stimulators is shown in Table 3.

6 | CONCLUSION

In this work, a 16-channel 1.8-mA power-efficient neural/muscular stimulator IC with exponentially decaying stimulation current and a DAC-sharing scheme has been implemented. A time-continuous exponential current generator based on Taylor series approximation is proposed and demonstrated to improve the stimulation PE. The implemented stimulator improves the PE of the output stage by 10% when compared with the conventional constant-current stimulator[14,31] and the stimulation PE of the stimulator at the output stage reaches 95.9% at maximum. Moreover, by sharing the single DAC among 16 stimulation channels, the die area of the stimulator chip is saved by about 25%, which is desirable for implanted biomedical applications. This power-efficient stimulator also features high voltage compliance and active charge balancing, making the stimulation effective and safe. The measurement results from in vitro test and in vivo experiment show that the developed stimulator IC is suitable for peripheral nerve prosthesis with high PE.

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