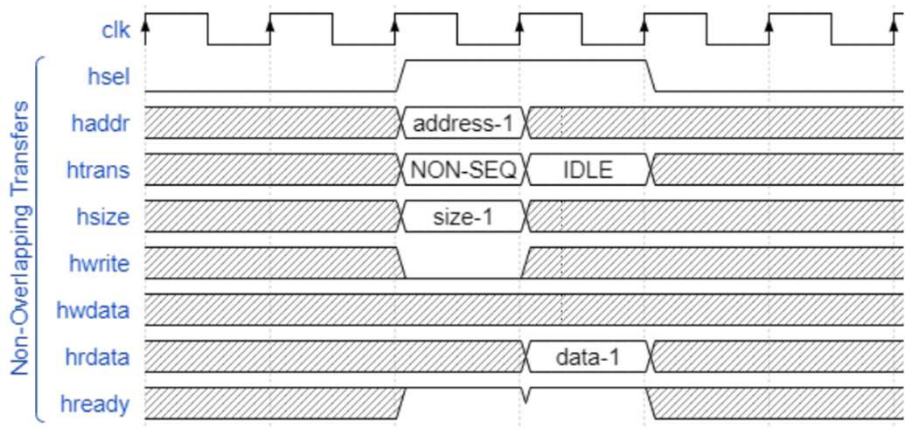
SoC Architecture – part 3

- More detail on AHB interface
  - More bus signals
  - Transaction types
  - Variable size data transfers

Updated 10/15/2020

HTRANS, HSIZE



HTRANS: **IDLE**, BUSY, **NON-SEQUENTIAL**, SEQUENTIAL

HSIZE: size in bytes = 2^(HSIZE-1)

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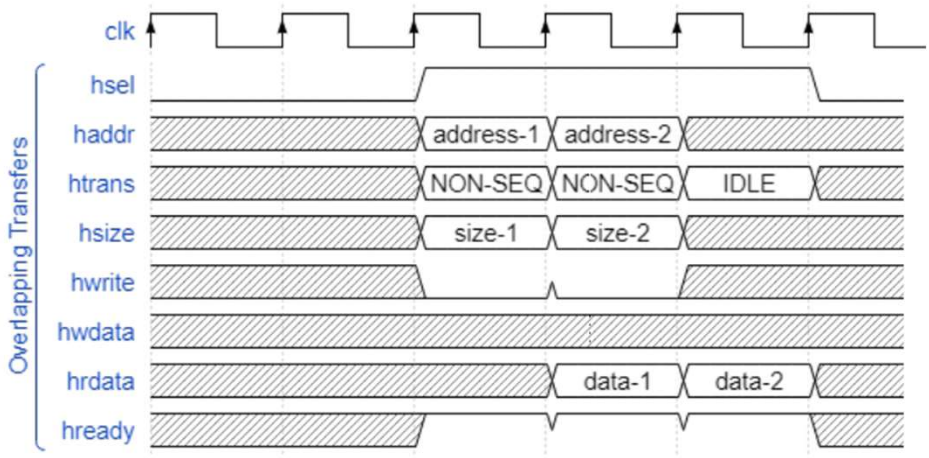
HTRANS, HSIZE



Two consecutive overlapping write transactions.
Like earlier examples, just more signals.

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Handling different transfer sizes (HSIZE) and bus width (PRDATA, PWDATA)

Basic principles

1. Think of it like memory accesses

   Addresses are for bytes not words

   Reads/write must be aligned to 2^n address boundaries

   E.g., for 32 bit words, a 32 bit read from addresses 7,8,9,10 is not possible. It splits 4,5,6,7 and 8,9,10,11

2. Don't change alignment of data

   E.g., given 32 bit words and Q[31:0] = AABBCCDD

   DD must also stay in right most position

   CC in 2nd from right position, etc.

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HSIZE for 32 bit data bus

(a very common case in practice)

- word size is 32 bits
- HSIZE = 0, one byte transfer
- HSIZE = 1, two byte transfer
- HSIZE = 2, 4 byte transfer
- HRDATA, HWDATA contents always word aligned
- HSIZE = 0, HADDR % 4 gives byte index in word
- HSIZE = 1, HADDR % 4, ignore LSB, gives ½ word
- HSIZE = 2, ignore bit0, bit1 of HADDR, gives word

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HSIZE examples

Given: 32 bit data bus, r3, r2, r1, r0 are registers at address 3, 2, 1, 0 respectively.

Treat {r3,r2,r1,r0} as 32 bit register

HSIZE	HWRITE	HADDR	HRDATA
0	0	2	{--,r2,--,--}
1	0	2	{r3,r2,--,--}
1	0	1	A = {--,--,r1,--} B = {--,r2,r1,--} C = {--,--,r1,r0} D = {r3,r2,r1,r0}

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HSIZE examples

Given: 32 bit data bus, same as last slide

HSIZE	HWRITE	HADDR		HWDATA	{r3,r2,r1,r0}
0	1	2		-- BB -- --	{r3,BB,r1,r0}
1	1	2		AA BB -- --	{AA,BB,r1,r0}
0	1	1		AA BB CC DD	{r3,r2,CC,r0}
2	1	0,1,2 or 3		AA BB CC DD	{AA,BB,CC,DD}
1	1	1	A B C D	-- -- CC DD -- BB CC -- -- -- CC DD -- -- -- DD	{r3,r2,CC,DD} {r3,BB,CC,r0} {r3,r2,CC,r0} {r3,r2,r1,DD}

HSIZE, for Lab 9

- Lab 9: word size is 16 bits
- HSIZE = 0, one byte transfer
- HSIZE = 1, two byte transfer
- HRDATA, HWDATA always word aligned
- HADDR even refers to lower byte
- HADDR odd refers to upper byte
- When HSIZE = 1, bit 0 of HADDR ignored

HSIZE examples

Given: 16 bit words. 8 bit register r3 at address 3 and 8 bit register r2 at address 2. (or 16 bit reg {r3,r2})

HSIZE	HWRITE	HADDR		HWDATA	{r3,r2}
0	1	2		-- BB	{r3,BB}
1	1	2		AA BB	{AA,BB}
0	1	3		AA BB	{AA,r2}
1	1	3	A B C D	AA -- AA BB -- CC -- --	{AA,r2} {AA,BB} {r3,CC} {r3,r2}

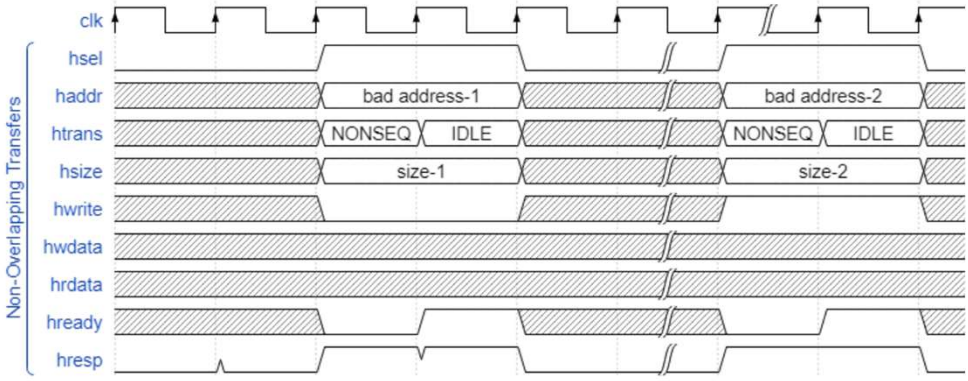
HSIZE examples

Given: 16 bit data bus, same as last slide.

{r3,r2} represents contents of r3,r2 registers

HSIZE	HWRITE	HADDR	HRDATA
0	0	2	{--,r2}
1	0	1	{r1,r0}
0	0	3	{r3,--}
1	0	2	A = {--,--} B = {r2,r1} C = {r2,--} D = {r3,r2}

HREADY, HRESP



HRESP: 1 indicates error

Your only use of HREADY: stall bus long enough for master to recognize error

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HPROT, HMASTERLOCK

- **HPROT** needed in systems that implement different protection levels for different addresses and transfer types. Not used in ECE337.
- HMASTERLOCK needed in multiple master systems. Not used in ECE337.

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