ASIC Design Laboratory
Lab 11
Evaluation Sheet

Fall 2020

Mg Account: _____
Section: _____

Lab Setup	TA Initials	Date	Score
Lab 11 folder and provided files in Git	_____	_____	____/1

Layout Process Analysis	TA Initials	Date	Score
What layers are used for supply ring bars: Horizontal? _____ Vertical? _____	_____	_____	____/1
What are the widths of the supply ring bars and their spacing: Bar Width? _____ Bar Spacing? _____	_____	_____	____/1
What is the spacing between the inner supply ring and the core area, and which prior command controls this?	_____	_____	____/1
How did the design change after running 'place_cells.tcl'?	_____	_____	____/1
What is a rough estimate for the core utilization?	_____	_____	____/1

What changed after running 'sroute'?			/1
In what ways are the three metal layers typically used in the routing?			/1
What percentage of the core appears to be filled with cells after running 'final_route.tcl'?			/1
And which command do you think primarily resulted in the change?			/1

Performing Layout Timing Analysis	TA Initials	Date	Score
What are the starting and ending gate-level components of the critical path?			/1
How many combinational logic cells are in between?			/1
What are the starting and ending blocks (design modules) of the critical path?			/1
Is the synthesis critical path similar to the layout one? What are their respective delays?			/1

Pad/Pin Placement based Timing Adjustment	TA Initials	Date	Score
Reduced negative slack after IO-frame adjustment			/4
What change(s) were made and why do you think they resulted in the reduction?			/2

Total points for lab /20