# SoC Module Design - Part 2

Basic SoC Bus protocols

Concepts:

- Multicycle bus
- Pipelined

Bus protocols

- APB (a multicycle protocol)
- AHB-lite (a pipelined protocol)

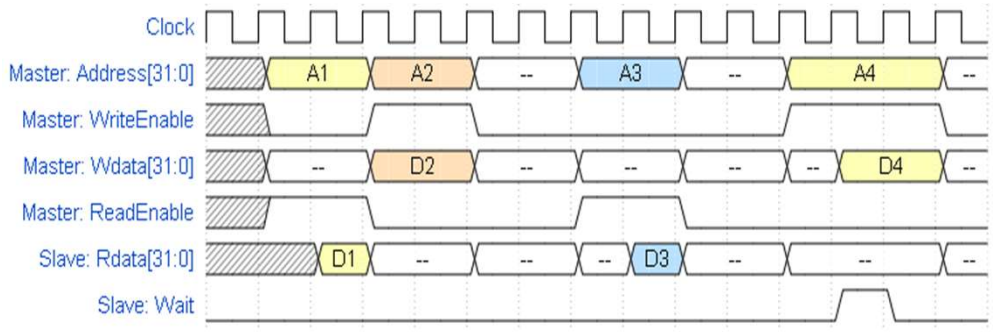


Updated 10/12/2020



# Multicycle SOC bus

Simple, slow, similar to APB, 2+ cycles/transfer



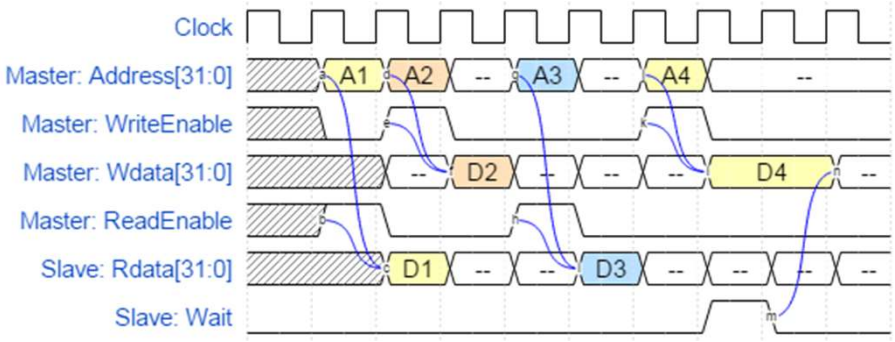

"Master:" indicates lines driven by bus master.
"Slave:" indicates lines driven by slave device.
Read, Write, Idle, Read, Idle, Write forced to wait



Updated 10/12/2020

# Pipelined SOC bus

similar to AHB or AHB-lite

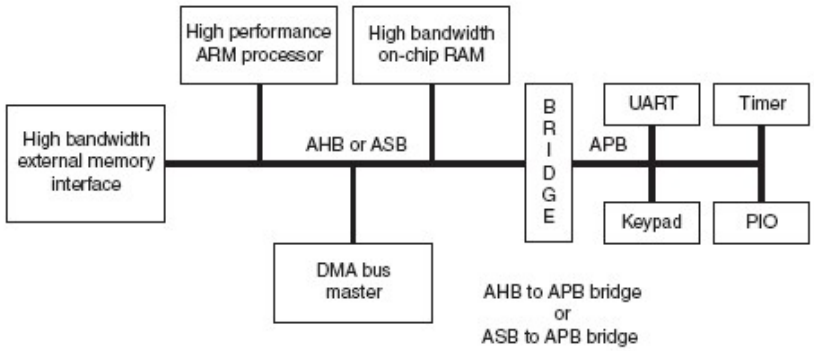



High performance busses work this way for the simple read and write transactions, but they usually support more complex transaction types as well.

3 Updated 10/12/2020

3

# AMBA 2.0




**AMBA AHB**

* High performance
* Pipelined operation
* Multiple bus masters
* Burst transfers
* Split transactions

**AMBA ASB**

* High performance
* Pipelined operation
* Multiple bus masters

**AMBA APB**

* Low power
* Latched address and control
* Simple interface
* Suitable for many peripherals

ECE 695R: System-on-Chip Design, Fall 2017 4

4

https://www.eecs.umich.edu/courses/eecs373/labs/lab3/IHI0024C_amba_apb_protocol_spec.pdf

# APB signals & timing

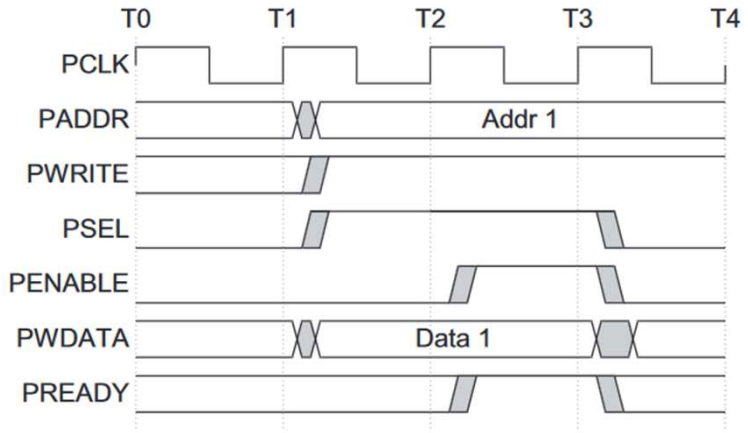



**Figure 2-1 Write transfer with no wait states**



5

Updated 10/12/2020

5

# APB

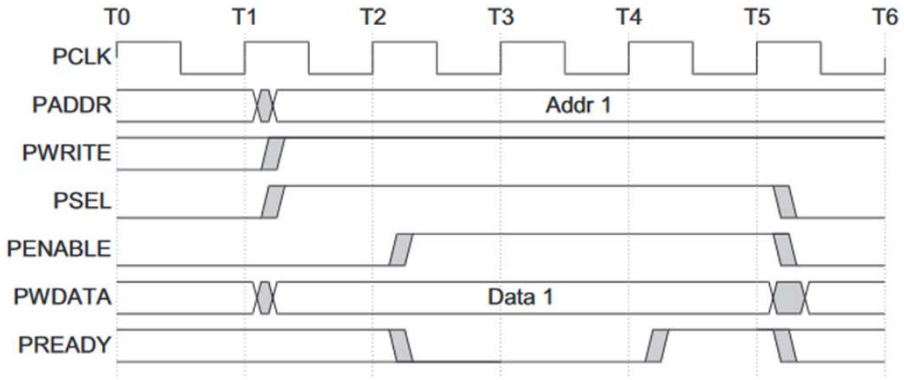



**Figure 2-2 Write transfer with wait states**



6

Updated 10/12/2020

6

# APB

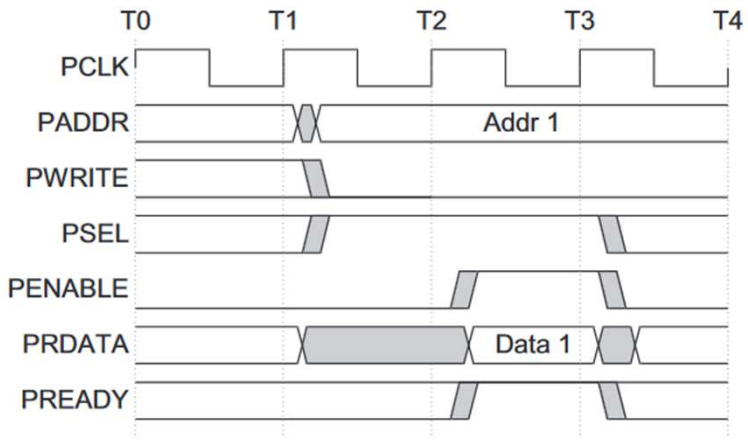



**Figure 2-3 Read transfer with no wait states**





# APB

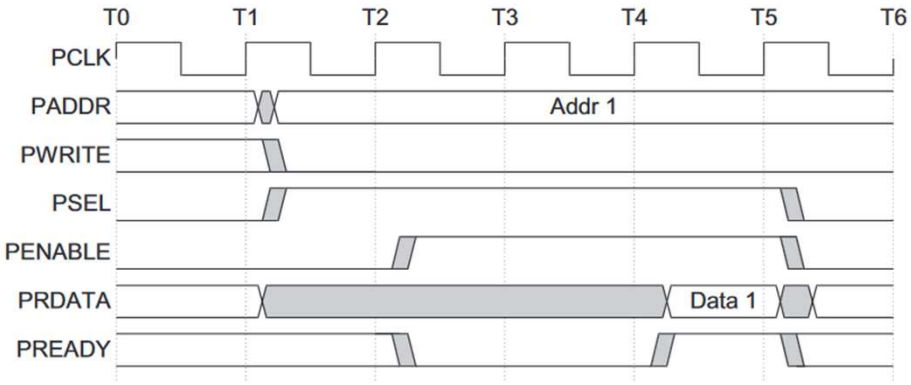
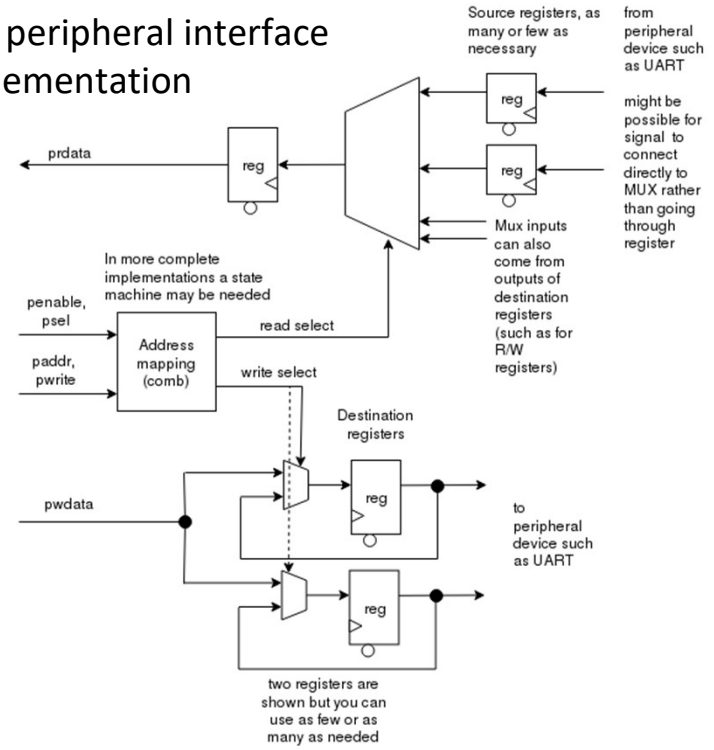



**Figure 2-4 Read transfer with wait states**

## APB peripheral interface implementation




9

Updated 10/12/2020

9

## AHB-lite timing

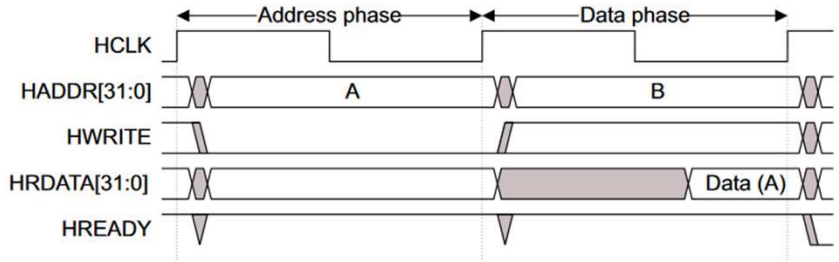



**Figure 3-1 Read transfer**

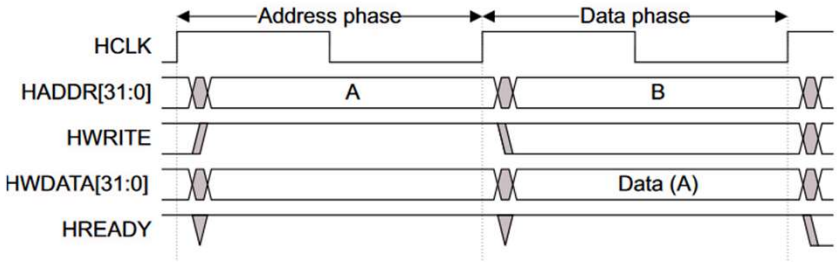



**Figure 3-2 Write transfer**



10

Updated 10/12/2020

10

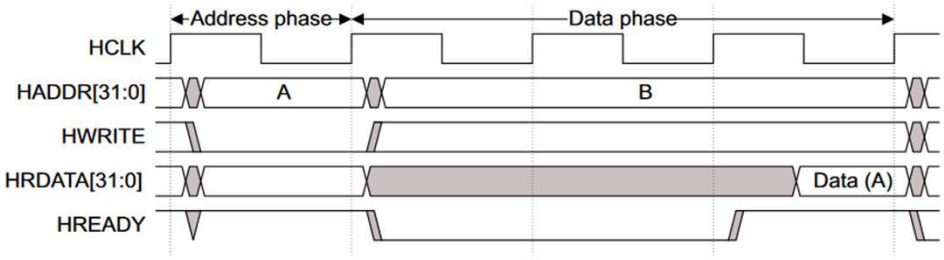



**Figure 3-3 Read transfer with wait states**

Figure 3-4 shows a write transfer with one wait state.

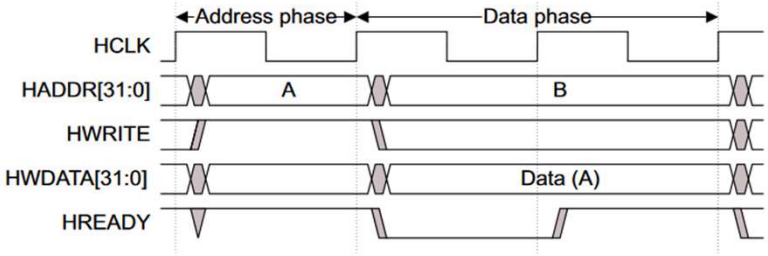
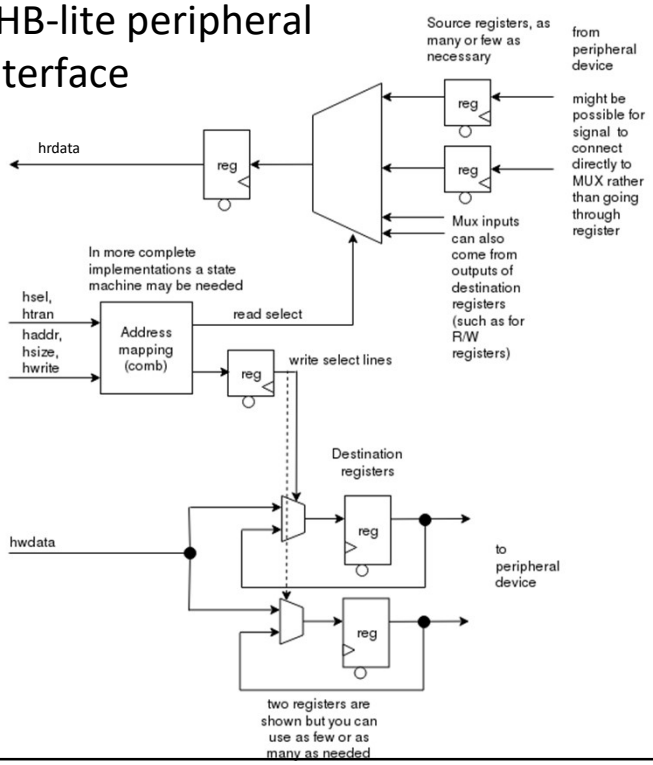



**Figure 3-4 Write transfer with wait state**

11 

11

## AHB-lite peripheral interface




partial picture of an AHB-lite slave design

very similar to APB, but register on write selects enable pipelining

12 Updated 10/12/2020

12