ASIC Design Laboratory
Lab 8
Evaluation Sheet

Fall 2020

Mg Account: _____
Section: _____

Preparation Phase (Submit together via Lab8prep)	TA Initials	Date	Score
Completed Detailed RTL Diagram for APB Slave			/4
Completed RTL diagram for the APB Slave's Controller			/1
Completed State Diagram for APB Slave's Controller			/1

Required Verification	TA Initials	Date	Score
APB Slave Module Test Bench w/ required test cases			/2
Full Design Test Bench w/ verification tasks, correct usage of APB bus model, and required minimum test cases			/4

Full Design Implementation Grading	TA Initials	Date	Score
Mapped Version Score **(submit via Lab8)**			/30

Total points for lab /42

NOTE: If a FSM-based controller is not used in the design, then the overall RTL diagram is out of 6 points