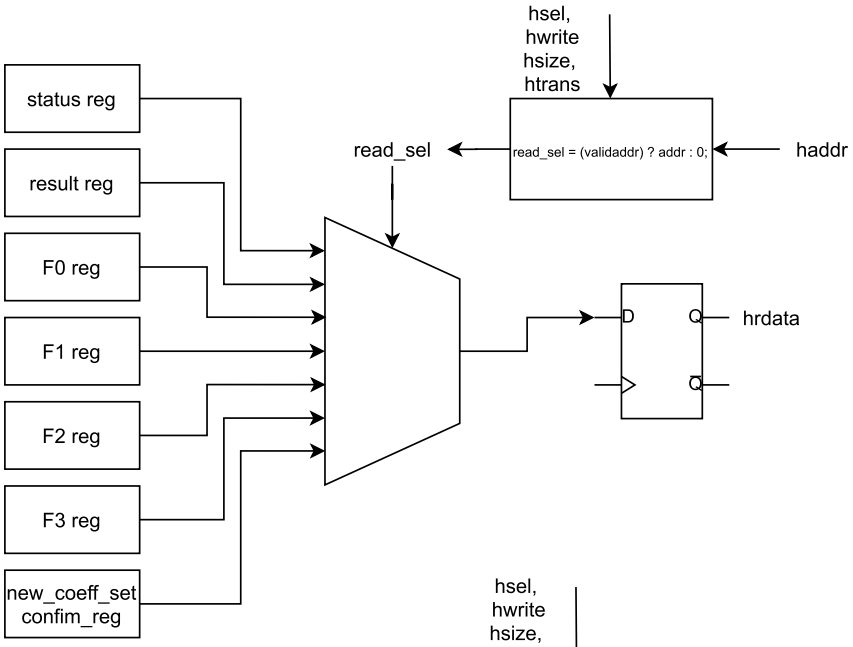
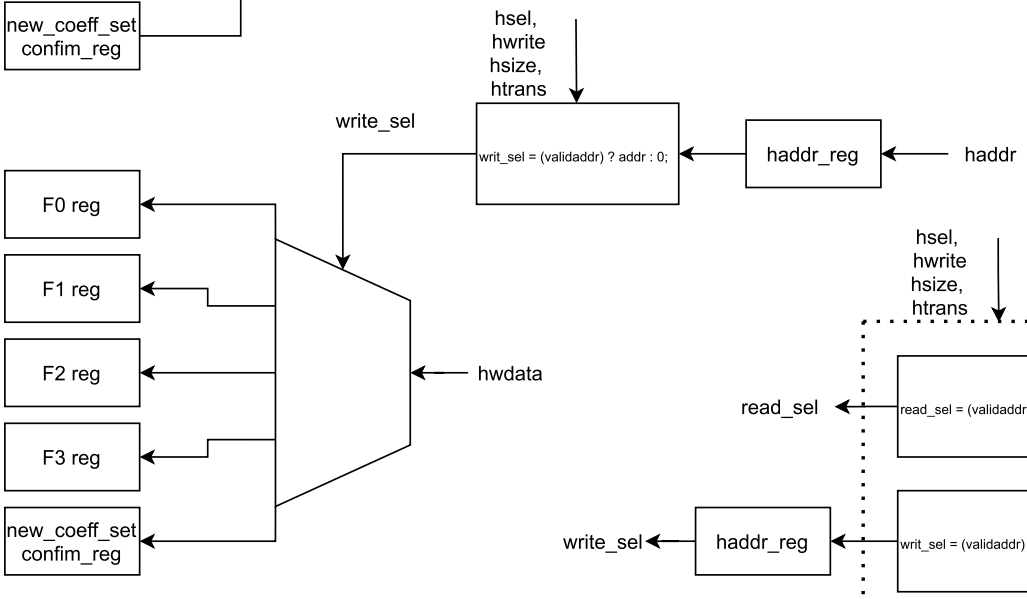


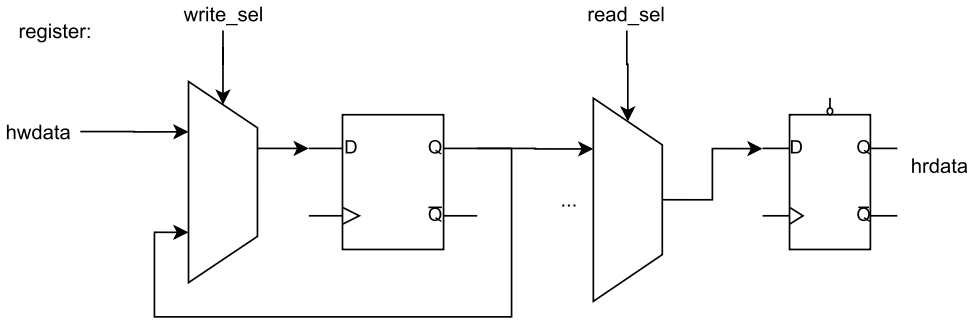
note: for the purpose of reserving space, use rectangle to express some of the registers inside the module.

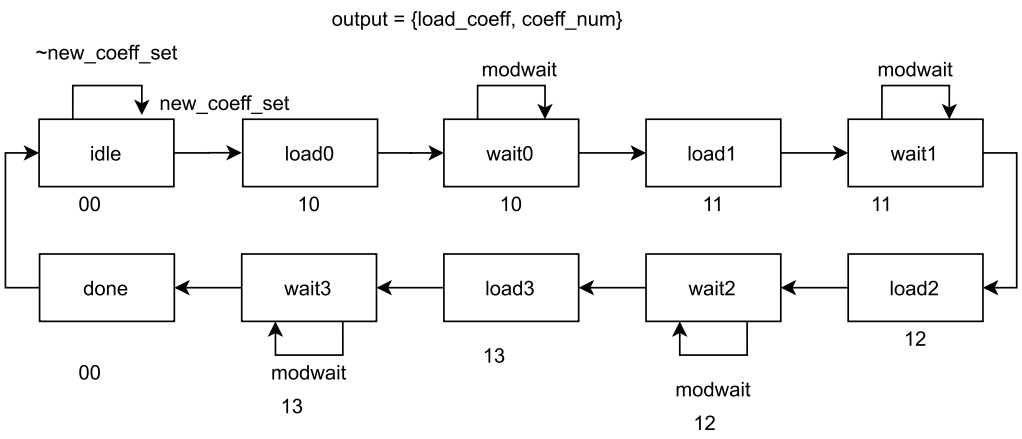
since the slave interface is conbinational, no need to plot state diagram.

error logic:
when err is true, assert hresp



always_comb: address_mapping
if hsel && hwrite write data to reg.
if hsel && ~hwrite read data from reg
else data_read = 0;




output = {load_coeff, coeff_num}
~new_coeff_set
new_coeff_set
idle
00
load0
10
modwait
wait0
10
load1
11
modwait
wait1
11
load2
12
wait2
modwait
12
load3
13
wait3
modwait
13
done
00