ACTIVITY 6A: Finite State Machine (Simple Washing Machine)

Jason Harvey Lorenzo, April 8, 2024
ENGG 125.03, Department of Electronics, Computer, and Communications Engineering
School of Science and Engineering, Ateneo de Manila University
Quezon City, 1108, Philippines
jason.lorenzo@obf.ateneo.edu

***Abstract*—The paper presents the development of a finite state machine (FSM) in Verilog HDL to simulate the operation of a simple washing machine. The FSM follows a predefined wash cycle, progressing through stages such as Idle, Soak, Wash, Rinse, and Spin. Additionally, it incorporates an optional ”Double Wash (DW)” feature, activated by a switch, which initiates a second wash and rinse cycle. The washing machine commences its operation upon coin insertion (C=1) and advances through the stages controlled primarily by a timer signal (T). Lid status (L) affects the machine only during the Spin stage. The FSM design utilizes state registers and bit registers to visualize the current stage of the washing process. The simulation results confirm the expected behavior of the FSM under different scenarios, validating the correctness of the design and implementation.**

***Index Terms*—Verilog HDL, finite state machine (FSM), simple washing machine**

I. Introduction

This task involves developing a finite state machine (FSM) using Verilog HDL to simulate the operation of a simple washing machine. The FSM is designed to follow a predefined wash cycle: Idle → Soak → Wash → Rinse → Spin. Additionally, an optional ”Double Wash (DW)” switch is available, which, when activated, triggers a second wash and rinse cycle. The washing machine initiates its operation upon the deposit of a coin (C) and progresses through the cycle stages. A single timer (T) governs the duration of each stage, generating a signal (T) upon completion of the time period before resetting and restarting for the next stage. If the lid (L) is lifted during the spin stage, the spinning action halts until the lid is closed again. The state processes are represented by virtual LEDs, depicted as bits in Table I.

TABLE I
LEDs and State Represented

LEDs	State
L0	Idle
L1	Soak
L2	Wash 1
L3	Rinse 1
L4	Wash 2
L5	Rinse 2
L6	Spin
L7	Stop

Here are the variables for reference:

- C = coint variable/sensor/switch (C = 1 means coin is inserted)
- T = 1 means the timer has elapsed
- L = lid variable/sensor/switch (L = 1 means lid is open)

II. FSM Design

Table I illustrates the finite state machine (FSM), comprising eight distinct states, each represented by its own bit, resulting in a total of 8 bits of output. The transition between these states is governed by the timer signal (T) and input variables, namely C (coin deposit) and DW (Double Wash switch). The FSM diagram depicted in Figure 1 provides a concise summary of these state transitions. Notably, due to the absence of direct influence from the input on the output, a Moore implementation approach was adopted.

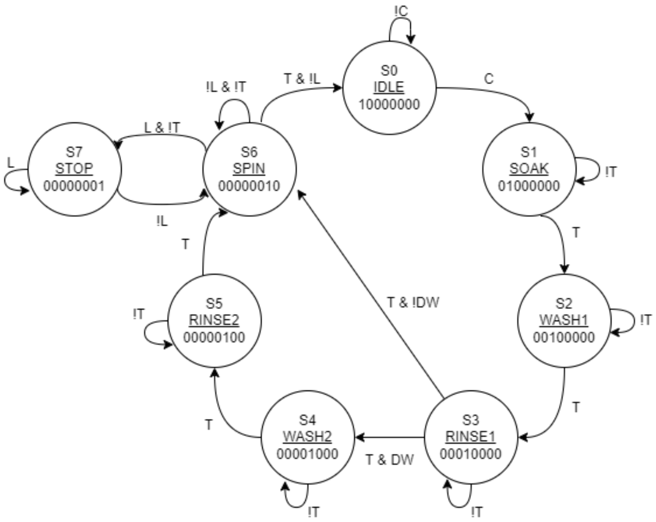

Fig. 1. Simple Washing Machine FSM Diagram

The 8-bit outputs represent the concatenation of output bits corresponding to each state.

III. HDL Code

Listing 1 shows an HDL code implementation of the FSM defined above.

Listing 1. Simple Washing Machine FSM HDL Code

```
module washingmachine (
  input CLK, C, L, DW,
  output reg T,L0,L1,L2,L3,L4,L5,L6,L7
);
parameter IDLE=3'd0,SOAK=3'd1,WASH1=3'd2,
  RINSE1=3'd3,WASH2=3'd4,RINSE2=3'd5,
  SPIN=3'd6,STOP=3'd7;
parameter stage_time = 3'd1; // +4 from
  state transitions for a total of 5
  clock pulse per stage
  // adjust accordingly

reg [2:0] state, next_state, counter;

initial
begin
  state <= IDLE;
  next_state <= IDLE;
  L0 <= 1'b1;
  L1 <= 1'b0;
  L2 <= 1'b0;
  L3 <= 1'b0;
  L4 <= 1'b0;
  L5 <= 1'b0;
  L6 <= 1'b0;
  L7 <= 1'b0;
  counter <= 3'd0;
end

always @(posedge CLK)
begin
  T <= (counter > stage_time);
  state <= next_state;

  L0 <= 1'b0;
  L1 <= 1'b0;
  L2 <= 1'b0;
  L3 <= 1'b0;
  L4 <= 1'b0;
  L5 <= 1'b0;
  L6 <= 1'b0;
  L7 <= 1'b0;
  case (state)
    IDLE: begin
      next_state <= (C) ? SOAK : IDLE;
      L0 <= 1'b1;
    end
    SOAK: begin
      counter <= (T)?3'd0:(counter+1'd1);
      next_state <= (T) ? WASH1 : SOAK;
      L1 <= 1'b1;
    end
    WASH1: begin
      counter <= (T)?3'd0:(counter+1'd1);
      next_state <= (T) ? RINSE1 : WASH1;
      L2 <= 1'b1;
    end
    RINSE1: begin
      counter <= (T)?3'd0:(counter+1'd1);
      if (T) next_state <=(DW)?WASH2:SPIN;
      else next_state <= RINSE1;
      L3 <= 1'b1;
    end
    WASH2: begin
      counter <= (T)?3'd0:(counter+1'd1);
      next_state <= (T) ? RINSE2 : WASH2;
      L4 <= 1'b1;
    end
    RINSE2: begin
      counter <= (T)?3'd0:(counter+1'd1);
      next_state <= (T) ? SPIN : RINSE2;
      L5 <= 1'b1;
    end
    SPIN: begin
      if (L) next_state <= STOP;
      else begin
        if (T) begin
             next_state<= IDLE;
             counter <= 3'd0;
           end
           else counter <= counter+1'd1;
         end
      L6 <= 1'b1;
      end
    STOP: begin
      next_state <= (L) ? STOP : SPIN;
      counter <= counter;
      L7 <= 1'b1;
    end
  endcase
end

endmodule
```

As mentioned, this Verilog module implements a finite state machine (FSM) to simulate the operation of a washing machine. The inputs are CLK (clock signal), C (coin deposit signal), L (lid status signal), and DW (double wash option signal). The outputs are T (timer signal) and LEDs L0-L7, representing different stages of the washing process. The FSM has seven states: IDLE, SOAK, WASH1, RINSE1, WASH2, RINSE2, SPIN, and STOP. The state transitions and LED outputs are determined based on the current state, input signals, and timer counter.

At the start, the state is initialized to IDLE, and the timer counter is set to 0. The LEDs are also initialized accordingly. On each clock cycle, the FSM evaluates the current state and updates the next state based on the inputs and timer signal. The timer counter increments until it reaches the stage_time value, indicating the completion of a stage. The LEDs corresponding to the current stage are turned on, and the FSM transitions to the next stage.

The FSM progresses through the default wash cycle from IDLE to SOAK, WASH1, RINSE1, WASH2, RINSE2, and SPIN stages. If the DW signal is active during RINSE1, an additional wash (WASH2) and rinse (RINSE2) stages are added before entering the SPIN stage. If the lid is lifted during the SPIN stage, the machine stops spinning and transitions to the STOP state until the lid is closed again. The FSM then either resumes spinning or remains in the STOP state based on the lid status signal.

IV. Output Circuit

Fig. 2 shows the output circuit of the code above.

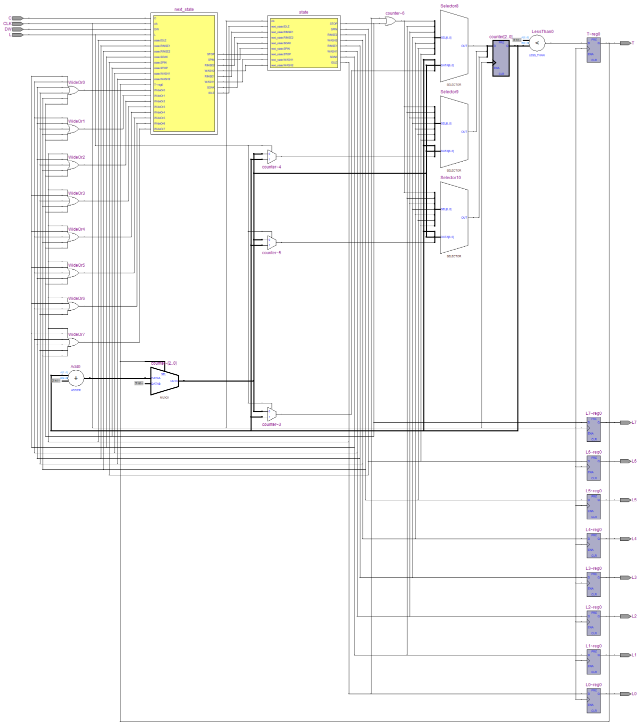

Fig. 2. Simple Washing Machine Implementation RTL Netlist

The diagram highlights the state registers (yellow blocks), which play a crucial role in determining the current and next states of the system. These registers are managed by the Quartus software, abstracting away the complexity of state management. Depending on the inputs and the states stored in other registers, the state registers produce specific outputs corresponding to the current state of the system. Note that the current state is determined by the value stored in the next state register.

V. Simulation

Fig. 3 and 4 shows respective output waveforms of the simple washing machine given test inputs, DW on for fig. 3 and DW off for fig. 4.

In Fig. 3, the washing machine begins its operation in the IDLE state, indicated by the illuminated L0. Upon the insertion of a coin (C=1), triggering the start of the cycle, the system transitions to the SOAK state, denoted by the activation of L1. Subsequent state transitions are primarily controlled by the timer signal (T). In this scenario, with the Double Wash (DW) option disabled, the FSM bypasses the WASH2 (L4) and RINSE2 (L5) states, proceeding directly to the SPIN state (L6=1). When the lid is opened (L=1) during the SPIN cycle, the system enters the STOP state (L7=1). Upon lid closure (L=0), the machine resumes spinning without resetting the timer count. Once the spinning cycle is complete, the system returns to the IDLE state, ready for another operation.

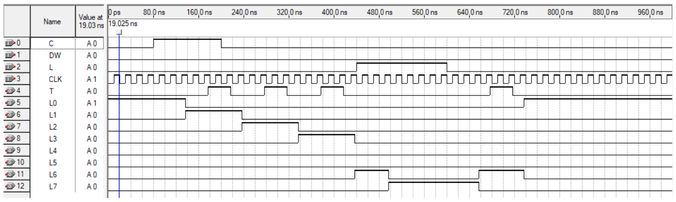

Fig. 3. Simple Washing Machine (DW off) Implementation Simulation Waveforms

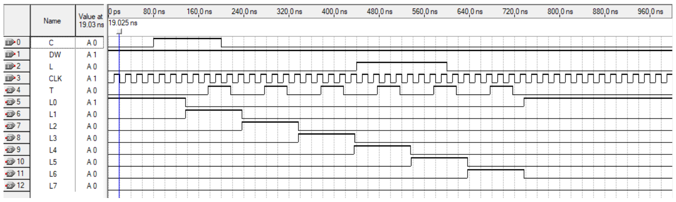

Fig. 4. Simple Washing Machine (DW on) Implementation Simulation Waveforms

In Fig. 4, the simulation closely mirrors the behavior depicted in Fig. 3, with the exception that the Double Wash (DW) feature is enabled. Consequently, the FSM progresses through the WASH2 (L4) and RINSE2 (L5) states as indicated by the respective illuminated LEDs. Notably, the lid status (L) only impacts the machine operation during the SPIN stage. Therefore, during the interval from approximately 440 ns to 600 ns, where L=1, no visible change occurs in the machine's state.

All these behaviors align precisely with the defined state transitions and functionality outlined in the FSM diagram depicted in Fig. 1, reaffirming the consistency and correctness of the designed finite state machine.