ACTIVITY 4A: COUNTER

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***Abstract*—This paper details the construction of a decade counter, aiming to replicate the functionality of a 74190 IC. The 74190's operation involves counting up when U/D' is 0 and down when set to 1, synchronized with positive clock edges. MAX/MIN output transitions to 1 at count boundaries (0 for down, 9 for up), with RCO' being its inverse. Additionally, LOAD' allows loading the 4-bit input. The CTEN' input either enables normal counting or pauses it. The Verilog HDL implementation comprises sequential operations controlled by the clock, with MAX_MIN and RCOn outputs determined by multiplexers dependent on U_Dn and count Q. Simulation results validate the counter's functionality, affirming its successful integration.**

***Index Terms*—Verilog HDL, decade counter**

I. Introduction

This activity involves the construction of a decade counter, specifically the task is to imitate the function of a 74190 IC as outlined in Fig. 1.

Inputs					Present State	Next State	Outputs	
LD input	CLK	LOAD'	CTEN'	U/D'	Q	Q'	MAX/MIN	RCO'
XXXX	0	X	X	X	XXXX	Q	0	1
XXXX	1	0	X	X	XXXX	LD input	0	1
XXXX	1	1	0	0	if Q<1001	Q = Q+1	0	1
					else if Q==1001	Q = 0000	1	0
					else if Q > 1001		0	1
XXXX	1	1	0	1	if Q==0000	Q = 1001	1	0
					else if Q >1001		0	1
					else if Q >0000	Q = Q-1	0	1
XXXX	1	1	1	X	XXXX	Q	0	1

Fig. 1. 74190 Simplified State Table

In the 74190's simplified state table depicted in Fig. 1, its primary operation involves counting up when the U/D' signal is 0, and down when set to 1, occurring on each positive clock pulse edge. During counting up, reaching the maximum digit (9) triggers a transition to 0, and conversely when counting down. At the count boundaries (0 for down, 9 for up), the MAX/MIN output becomes 1, and 0 otherwise, with RCO' being its inverse. Additionally, a LOAD' command allows loading the 4-bit LD (load) input into the counter's state for the subsequent clock edge. This accommodates inputs exceeding 9 but below 15 (10-15 or A-F in hexadecimal), causing the counter to reset to 0 when counting up, or to 9 when counting down, on the next clock edge. The CTEN' input enables normal counter operation when low and holds the current state when high, effectively pausing it.

Listing 1 shows the HDL code implementation of the function defined above.

Listing 1. 74XX138 Decoder HDL Code

```
module dec_counter(CLK, LOADn, CTENn,
   U_Dn, LD_INPUT, MAX_MIN, RCOn, Q);
parameter N=4;
input CLK, LOADn, CTENn, U_Dn;
input [N-1:0] LD_INPUT;
output MAX_MIN, RCOn;
output [N-1:0] Q;

wire [N-1:0] Q;
reg [N-1:0] next_Q;
wire MAX_MIN;

assign MAX_MIN = (U_Dn) ?
  (Q === 4'b0000) : (Q === 4'b1001);
assign RCOn = !MAX_MIN;
assign Q = (LOADn) ? (next_Q)
  : (LD_INPUT);

always @(posedge CLK)
  if (!CTENn)
    if (U_Dn)
      begin
        if (Q===4'b0000|Q>4'b1001)
            next_Q <= 4'b1001;
        else next_Q <= Q-1;
      end
    else
      begin
        if (Q<4'b1001) next_Q <= Q+1;
        else next_Q <= 4'b0000;
      end
endmodule
```

Counters, particularly the 74190, exhibit a blend of asynchronous and sequential behaviors. While the primary sequential aspect involves the counting operation, much of its functionality, including output generation, is asynchronous. MAX_MIN and RCOn, derived through continuous assignments, rely solely on the state Q and the direction input U_DN. Specifically, when U_DN is 1 (indicating counting down), MAX_MIN becomes 1 only if Q reaches 4'b0000, otherwise remaining at 0. Conversely, with U_DN at 0 (signifying counting up), MAX_MIN transitions to 1 solely upon Q reaching 4'b1001, otherwise maintaining a 0 state. This logic

is encapsulated within MAX_MIN's continuous assignment. RCOn, conversely, is the inversion of MAX_MIN. As for Q, its value is asynchronously determined by LOADn; when active (LOADn=0), Q takes the value of LD_INPUT, otherwise, it gets its current state from a register (as further explained below).

To address the synchronous aspect, a 4-bit register named next_Q was introduced. This register serves as the intermediary variable for incrementing (when U_DN=0) or decrementing (when U_DN=1) through an if-else statement within the procedural block. These conditions are already designed to accommodate the possibility of loading a number within the range of 10-15 (A-F). Additionally, the procedural statement exclusively executes the counting process when CTENn equals 0, indicating the device is enabled; otherwise, it just passes through, maintaining the current values and effectively pausing the system's state/count.

II. Output Circuit

Fig. 2 shows the output circuit of the code above.

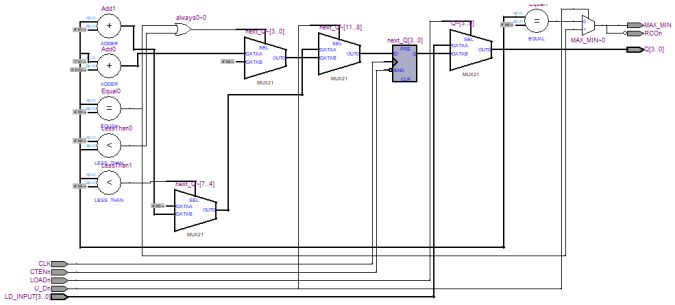

Fig. 2. 74190 Decade Counter Circuit Implementation RTL Netlist

On the far left of the diagram, we find the comparators (<, =) and adders. These comparators play a crucial role in establishing the conditions within our if statements and serve as the selectors for the multiplexers, which are generated from the if-else statements. Adders, on the other hand, facilitate the increment and decrement operations of the register next_Q for counting purposes. In the center of Fig. 2 is the gray D flip-flop, important for the procedural aspect of the circuit. Its input D is linked to the nested if statements (multiplexers) within our procedural block. Essentially, how this input is incremented/decremented depends on the CLK input and is enabled by CTENn. The resultant output from this process is then directed to the combinational part of the circuit, where it can be switched to LD_INPUT via the next multiplexer. Another multiplexer is tasked with implementing MAX_MIN and RCOn, contingent on U_Dn and Q.

III. Simulation

Fig. 3 shows respective output waveforms of the device given test inputs.

As observed, with an LD_input of D (hexadecimal 13) and LOADn set to 0 asynchronously, Q accurately loaded with 13. Subsequently, as this value exceeds the counter's limits

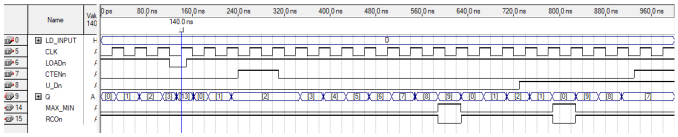

Fig. 3. 74190 Decade Counter Implementation Simulation Waveforms

and U_Dn signals counting up (0), Q reset to 0 on the next positive clock edge. When CTENn was toggled to 1 while Q counted from 1, the counting paused until CTENn reverted to 0, allowing the process to resume. Progressing through counts until 9, the counter looped back to 0 for further incrementation. Conversely, with U_Dn at 1 (indicating counting down), decrementing commenced until 0, followed by Q switching to 9 and decrementing until CTENn's reactivation, locking at 7. This simulation conforms precisely to the functionalities outlined in Fig. 1, validating the successful integration of a 74190 decade counter in Verilog HDL.