Simulation Lab #3

EECS 170LC

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1 Introduction

A differential amplifier is designed for a particular bias current and maximum output swing. Its differential and common mode gains are then analyzed, both with theoretical and simulation results. A sinusoid is then used to test the maximum input voltage before the output waveform clamps.

2 Part 1

Two resistor values need to be determined in order to properly design the differential amplifier. R_{REF} needs to be determined to design the current source. The two transistors M_{2A} and M_{2B} are matched and conduct a total current of I_{SS}. Thus, each conducts a current of $\frac{I_{SS}}{2}$. Because M_D is diode connected, $V_{DS} = V_{GS}$. Therefore, R_{REF} can be determined using Ohm's Law:

$$R_{REF} = \frac{V_{DD} - V_{GS}}{\frac{I_{SS}}{2}} \tag{1}$$

Ignoring channel-length modulation effects, the current through M_D can be acquired using $\frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_{tn})^2 = \frac{I_{SS}}{2}$. Therefore, V_{GS} can acquired using:

$$V_{GS} = V_{tn} + \sqrt{\frac{I_{SS}}{k'_n \frac{W}{L}}} \tag{2}$$

Using equations (2) and (1), $R_{REF} = 15.14\text{k}\Omega$. This ensures that the I_{SS} =450.0µA specification is met. To achieve maximum output swing, one must know the midpoint of V_{out}^+ and V_{out}^-, referred to as $V_{midpoint}$. From this information, R_D can be acquired:

$$R_D = \frac{V_{DD} - V_{midpoint}}{\frac{I_{SS}}{2}} \tag{3}$$

$V_{midpoint}$ is the only unknown for this circuit. At either V_{out}^+ or V_{out}^-, the highest value is the supply voltage V_{DD} when the transistors are cutoff. The lowest value is approximately the output voltage during the transition from triode to saturation. This occurs when $V_{DS} = V_{GS} - V_{tn}$ or equivalently when $V_D = V_{out}^{+,-} = V_G - V_{tn}$. The transistor is biased at $V_G = 2.5\text{V}$and V_{tn} is known. Therefore, the midpoint of the output voltage at either side of the amplifier occurs at:

$$V_{midpoint} = \frac{V_{High} + V_{Low}}{2} = \frac{V_{DD} + (V_G - V_{tn})}{2} \tag{4}$$

Using equations (3) and (4), $V_{midpoint}$ =3.05Vand R_D =8.67kΩ. Figure (1) depicts the amplifier design with the DC operating point results.

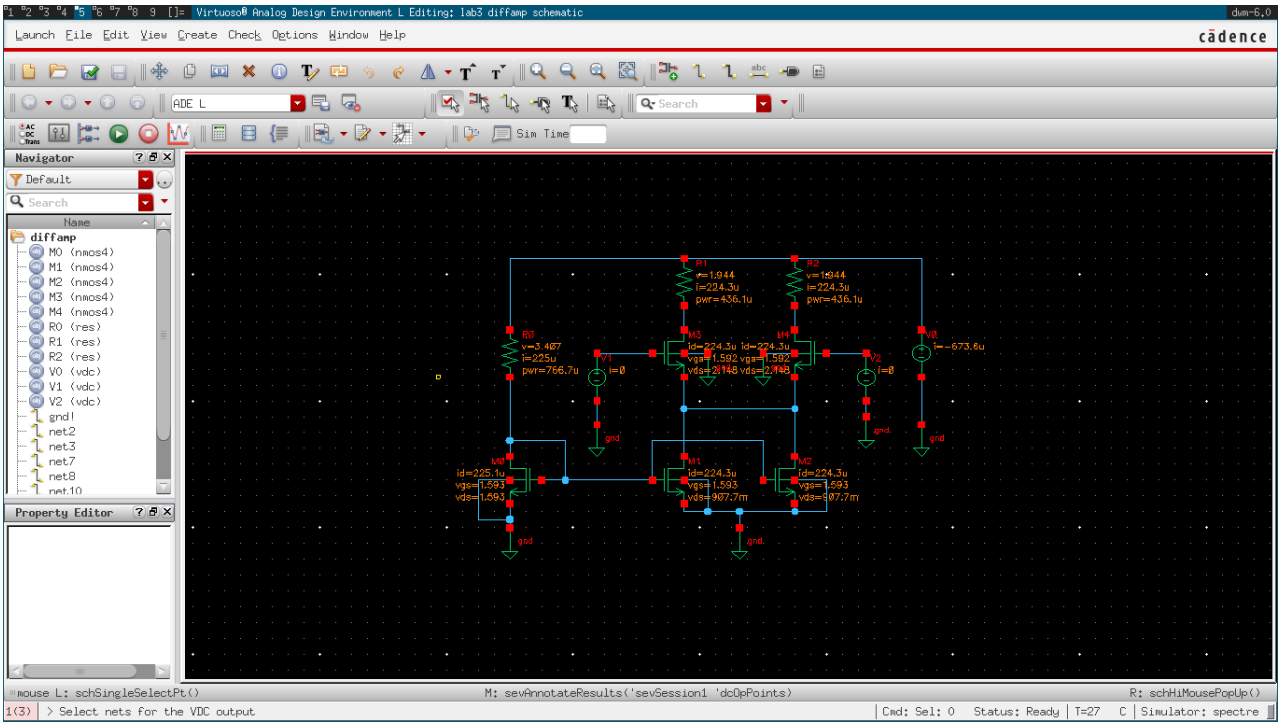

Figure 1: Differential Amplifier with DC Operating Point Results

All of the transistors are in saturation as expected. I_{SS} is about 448.6µA, which is slightly below the desired 450µA. This is a result of channel-length modulation effects causing the currents in the current source to depend on V_{DS}. Let $V_{DS,D}$ be V_{DS} for M_D and $V_{DS,AB}$ be V_{DS} for either M_{2A} or M_{2B}. To a first order approximation, the ratio of the current in M_{2A} or M_{2B} to the current in M_D is:

$$\frac{1 + \lambda_n V_{DS,AB}}{1 + \lambda_n V_{DS,D}} \tag{5}$$

If the current through M_D as well as other relevant parameters from figure (1) and the MOSFET model are used, then the expected current through M_{2A} or M_{2B} is about 224.3µA, which is precisely what is observed in the simulation. If R_{REF} is decreased slightly to 15.09kΩ, I_{SS} becomes exactly 450µA, determined from the sum of the currents through each current source. Figure (2) depicts the results for this second design iteration. It should be noted that this does not affect the output voltage swing since that is determined by R_D. Furthermore, all of the transistors remain in saturation.

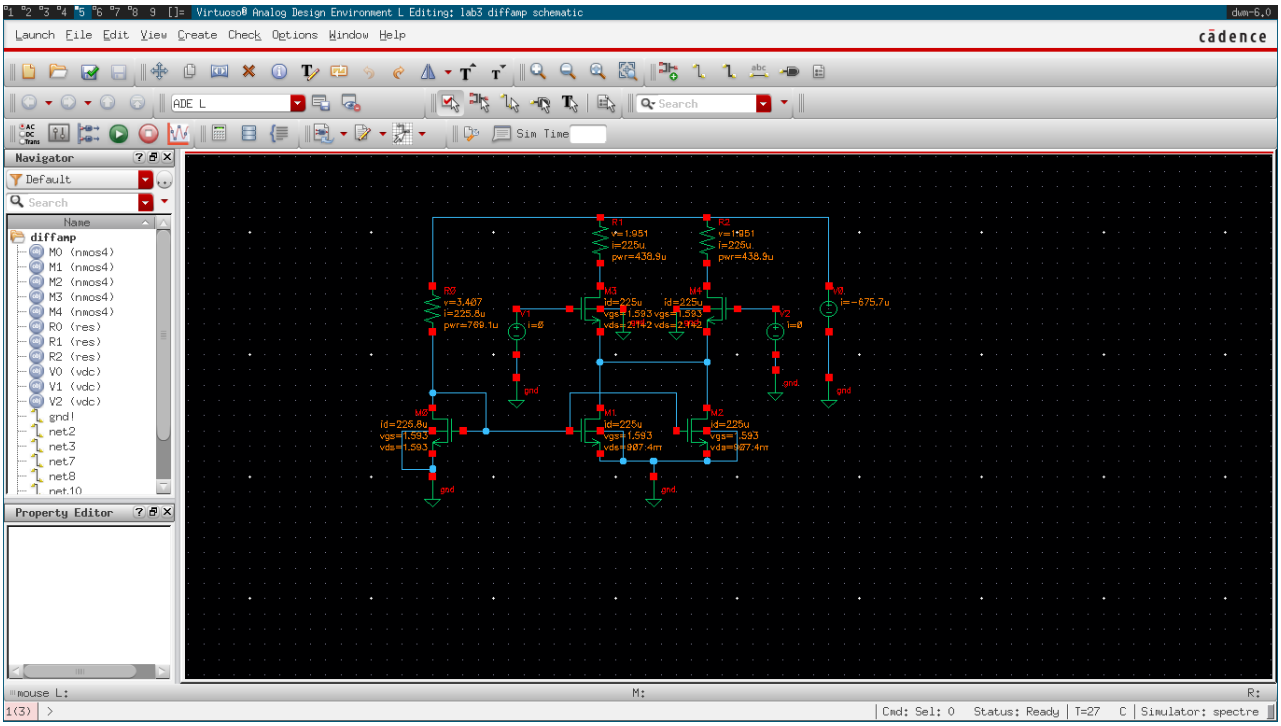

Figure 2: Second Differential Amplifier Design Iteration

Assume the small-signal parameters of the circuit are known. For only differential mode signals, the source of M_{1A} and M_{1B} becomes an AC ground. Therefore, the half-circuit is simply a common-source amplifier with drain resistor R_D. The negative sign disappears since the negative and positive differential inputs are flipped in the circuit. $g_{m1A,B}$ is g_m for both M_{1A} and M_{1B} which turns out to be the same. $r_{o1A,B}$ is the output resistance of M_{1A} and M_{1B}.

$$A_{dm} = g_{m1A,B}(R_D||r_{o1A,B}) \tag{6}$$

The common-mode gain can be acquired by recognizing that the current sources act as MOSFETs with the gate and source grounded since only DC signals exist in the reference part of the circuit. So, the small-signal model of these transistors reduces to the output resistance of each of the MOSFETs, which turn out to be identical. $r_{o2A,B}$ is the output resistance of M_{2A} and M_{2B}. Note that $r_{o1A,B} = r_{o2A,B}$. By analyzing the half-circuit with Kirchhoff's Laws, the following expression is acquired for the common-mode gain:

$$A_{cm} = -\frac{g_{m1A,B}R_D r_{o1A,B}}{R_D + g_{m1A,B}r_{o1A,B}^2} \tag{7}$$

g_m can be calculated using $\frac{2I'_D}{V_{GS}-V_{tn}}$, where I'_D is the drain current excluding channel-length modulation effects. Here, assume $I_D \approx I'_D$ since channel-length modulation effects are negligible. r_o can be calculated using $\frac{1}{\lambda_n I'_D}$. It should be noted that these gain calculations use the values in figure (2).

Table 1: Gains for Part 1 Second Iteration Amplifier

Differential Mode Gain [V/V]	Common Mode Gain [V/V]	Common-Mode Rejection Ratio
20.01	-0.0097	2052.54

3 Part 2

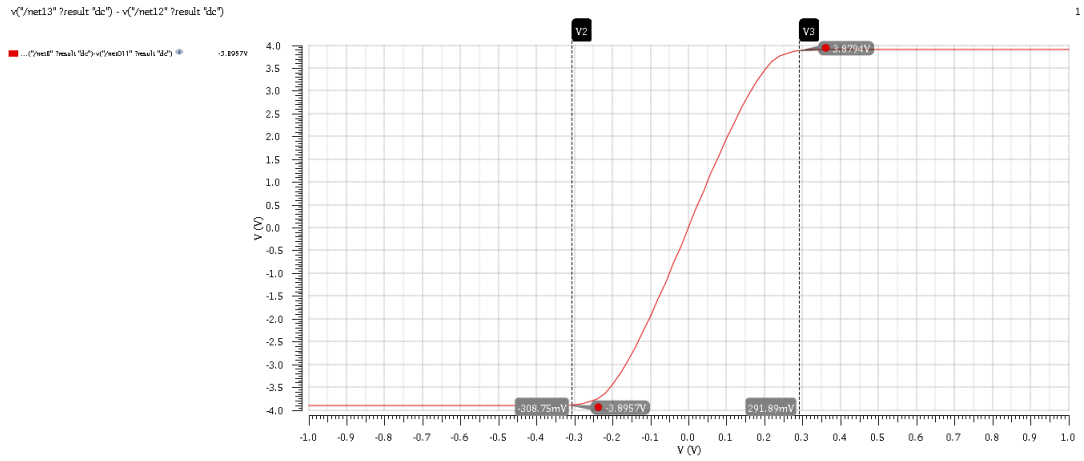

Figure 3: Simulation 2 Sweep - $V_{out,dm}$ versus $V_{in,dm}$

Table (2) contains the ranges of input and output differential-mode values for which the transistors are biased in saturation.

Table 2: Conditions for All Transistors to be in Saturation

	Maximum [V]	Minimum [V]
DM Output Voltage	3.8794	-3.8957
DM Input Voltage	0.29189	-0.30875

The differential-mode gain can be acquired by computing the slope near $V_{in,dm} = 0$V. Table (3) contains these values. The theoretical prediction is very close to the simulation result.

Table 3: Simulation versus Theoretical Differential-Mode Gain

Theoretical Calculation [V/V]	Simulation Result [V/V]	Error
20.01	20.03	0.09%

4 Part 3

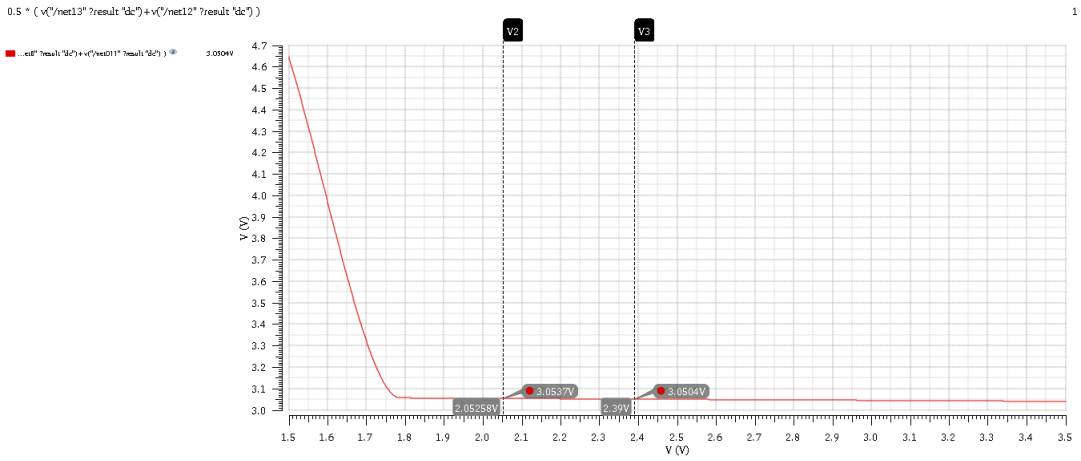

Figure 4: $V_{out,cm}$ versus $V_{in,cm}$

In order to determine where saturation begins or ends, a wider DC sweep must be taken.

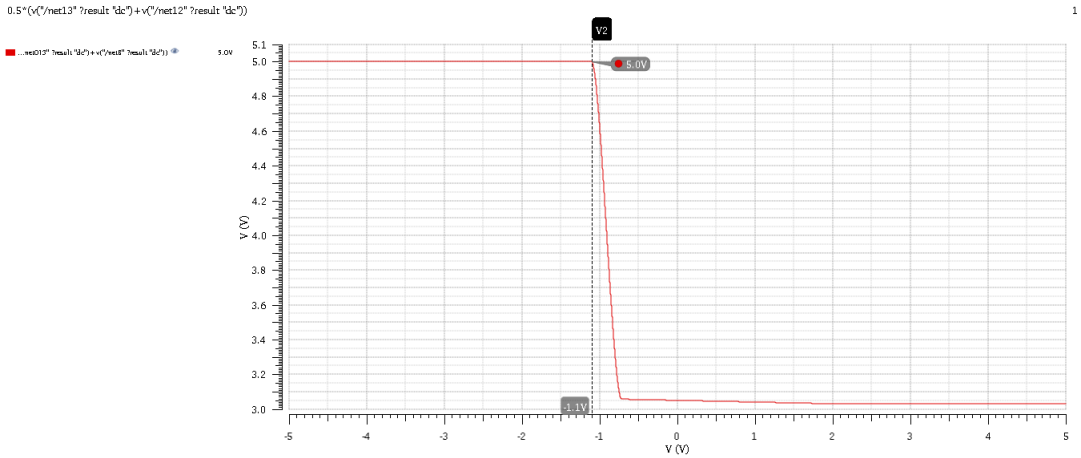

Figure 5: CM Input Voltage Sweep from -5V to 5V

The transistors are observed to enter cutoff around $V_{in,cm} = -1.1$V. The linear region should also have both transistors in saturation since dropping the gate voltage from saturation should not cause them to enter triode. It is not clear that the transistor enters triode since the large-signal common-mode voltages hover about the midpoint of the saturation region's output voltage as the input voltage becomes increased.

Table 4: Conditions for All Transistors to be in Saturation

	Maximum [V]	Minimum [V]
CM Output Voltage	1.95	-0.0216
CM Input Voltage	-1.1	N/A

Common-mode output voltage is acquired by taking the large-signal common-mode output voltage in the simulation and subtracting the midpoint of the saturation region's output voltage since the transistors are biased at this point anyway.

The simulation result for the common-mode gain is tabulated in table (5). The simulation result and theoretical calculation are essentially the same.

Table 5: Common-Mode Gain Results from Simulation

Theoretical Calculation [V/V]	Simulation Result [V/V]	Error
-0.0097	-0.01	2.56%

5 Part 4

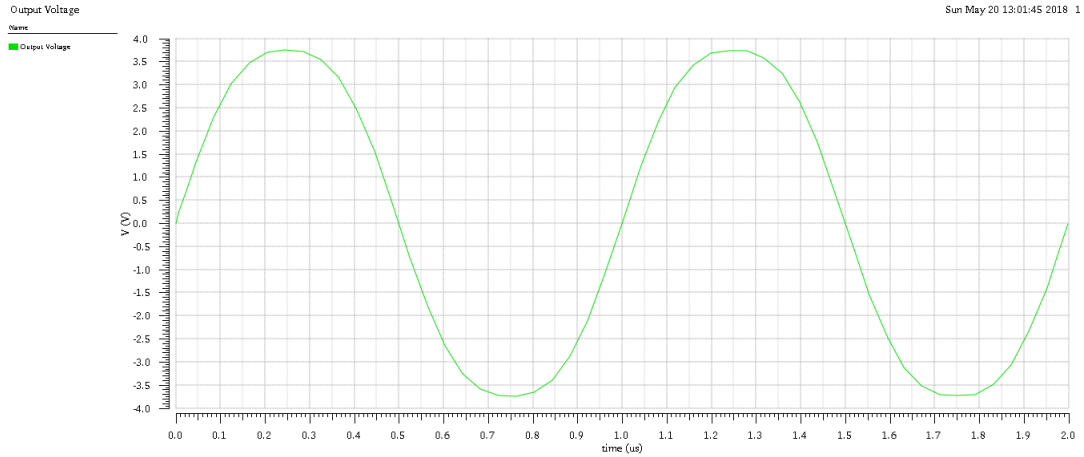

Figure 6: Differential-Mode Output Waveform when 117.5mV Differential-Mode Input Signal is Applied

The maximum amplitude of the applied signal is about 117.5mV. The corresponding maximum output amplitude is about 3.7V. The true value is likely even less because before the transistors enter triode or cutoff mode, distortions at the edge of the saturation region occur. Past this point the amplifier begins to distort the output waveform and cause it to clamp.

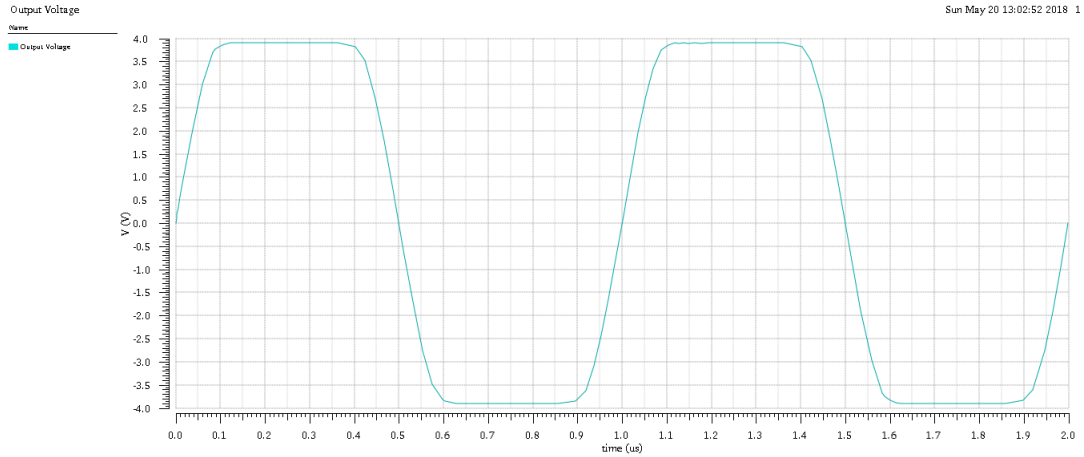

Figure 7: Significant Clamping of the Ouput Signal at 225mV

6 Conclusion

The bias currents in the differential amplifier turn out to be slightly less in practice due to channel-length modulation effects. Dropping R_{REF} increases the bias current to the level at which it needs to be. The differential and common-mode gain results align with the theoretical predictions. The amplifier has a very

low common-mode gain and a very high differential-mode gain, leading to a very high common-mode rejection ratio. The output swing of the amplifier is limited by the transistors entering cutoff or saturation. At either point, the output waveform clamps and distorts.