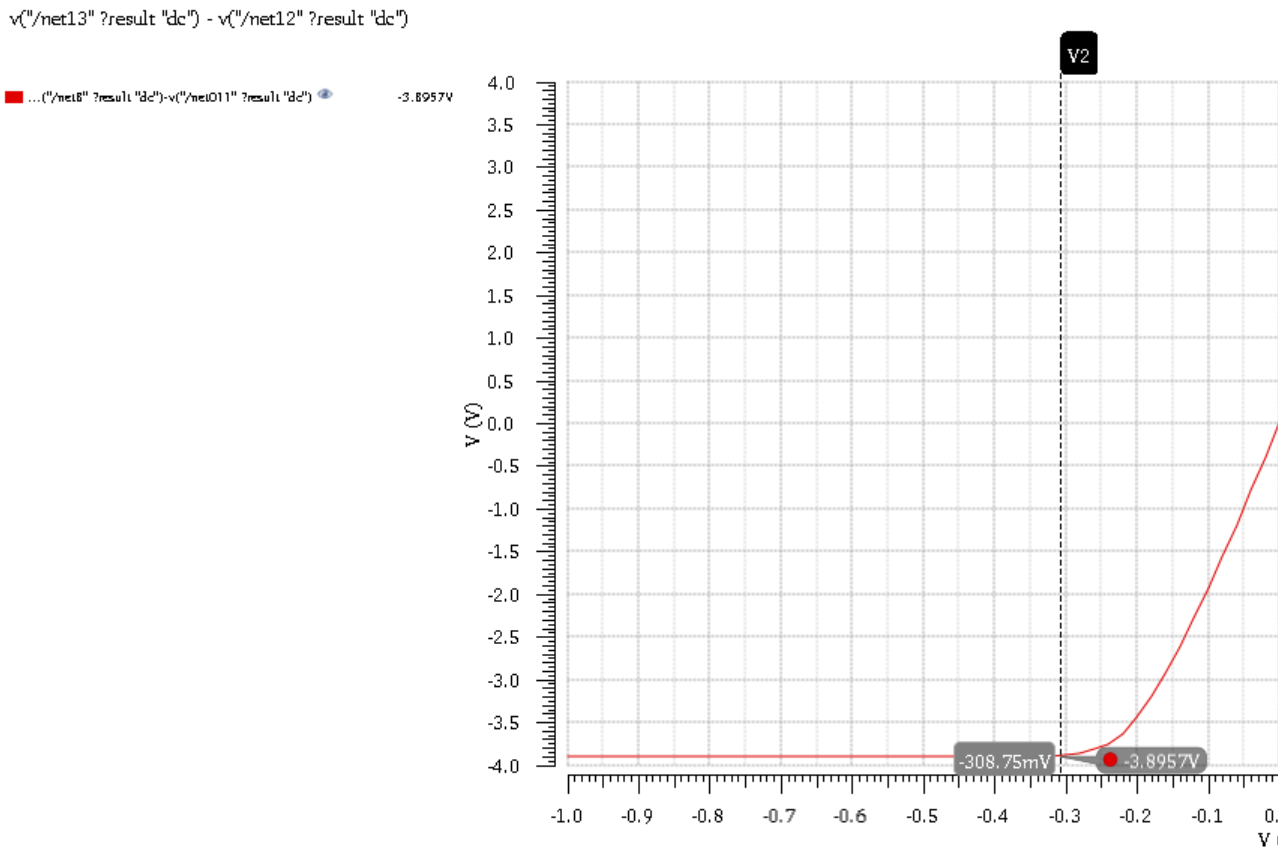

Figure 1: Simulation 2 Sweep - $V_{out,dm}$ versus $V_{in,dm}$

Table (1) contains the ranges of input and output differential-mode values for which the transistors are biased in saturation.

Table 1: Conditions for All Transistors to be in Saturation

	Maximum [V]	Minimum [V]
DM Output Voltage	3.8794	-3.8957
DM Input Voltage	291.89	-308.75

The differential-mode gain can be acquired by computing the slope near $V_{in,dm} = 0$V. Table (2) contains these values. The theoretical prediction is very close to the simulation result.

Table 2: Simulation versus Theoretical Differential-Mode Gain

Theoretical Calculation [V/V]	Simulation Result [V/V]	Error
20.01	20.03	0.09%