Measurement Lab #2

EECS 170LC

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1 Introduction

1.1 Introduction

In this lab we analyze the common-source and common-drain amplifiers using the CD4007 MOSFET package as an NMOS. Each amplifier's VTC and small-signal gain is determined, and the effects of the gain under a small load resistance is investigated. In particular, we investigate how cascading the two configurations can produce a larger gain on a small load.

2 Part 1

2.1 Part 1

The common-drain amplifier shown in Figure 1 is constructed, using two $10k\ \Omega$ resistors in parallel for the $5k\ \Omega$ resistor. These resistors are measured to have a parallel resistance of $4.924k\Omega$.

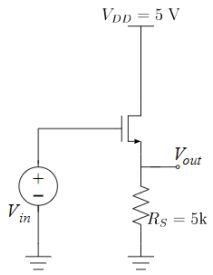

Figure 1: Common-Drain Amplifier

With V_{DS} constant at 5V, V_{GS} is swept from 0 to 5V to obtain the voltage transfer characteristic shown in Figure (2) and Table (1).

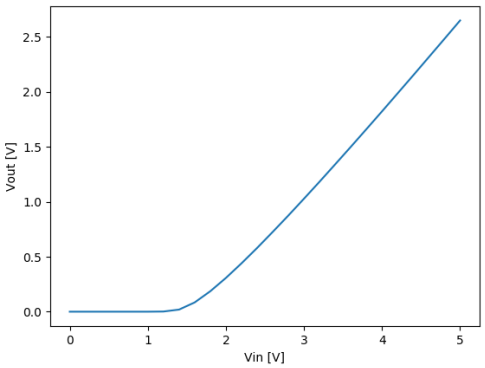

Figure 2: V_{out} vs V_{in} for the Common-Drain Amplifier

Table 1: Figure (2) Data

Vin [V]	Vout [V]
0.0	0.00
0.2	0.00
0.4	0.00
0.6	0.00
0.8	0.00
1.0	0.00
1.2	0.0014
1.4	0.0191
1.6	0.0842
1.8	0.186
2.0	0.307
2.2	0.440
2.4	0.580
2.6	0.726
2.8	0.875
3.0	1.028
3.2	1.183
3.4	1.341
3.6	1.500
3.8	1.661
4.0	1.823
4.2	1.987
4.4	2.151
4.6	2.317
4.8	2.483
5.0	2.650

For this circuit, $V_{out} = I_D R_S$, so $V_{out} = 0$V while the transistor is in cutoff. Afterward, even when Vin = 5V, V_{DS} is more than $V_{in} - V_t$ so that the transistor is in saturation any time it is on. The threshold voltage appears to be around 1.4V. For maximum possible input swing, the circuit is biased at the middle of the saturation region where $V_{in} = V_{in(eq1)} = 3.3$V. 3.3V is acquired by finding the midpoint of V_{out} and then determining the V_{in} for which that V_{out} occurs. Here, the midpoint of V_{out} occurs at $\frac{2.65+0.00}{2} \approx 1.33$V. This occurs when $V_{in} \approx 3.3$V. Thus, $V_{in(eq1)} \approx 3.3$V.

Next, a 10mV signal is applied to V_{in}, starting off at 1kHz under the assumption that the amplifier performs better when at lower frequencies. The amplifier should have a higher low-frequency gain because of the transistor's parasitics, such as the junction capacitances between the doped regions. At higher frequencies, these parasitic capacitances dominate, causing the BJT to act like a low-pass filter, thereby decreasing the high-frequency gain. The frequency is subsequently increased to 100kHz and then 1MHz. Oscilloscope screenshots are shown for each frequency in Figures (3), (4), and (5), respectively. The gains at each frequency are tabulated in Table (2).

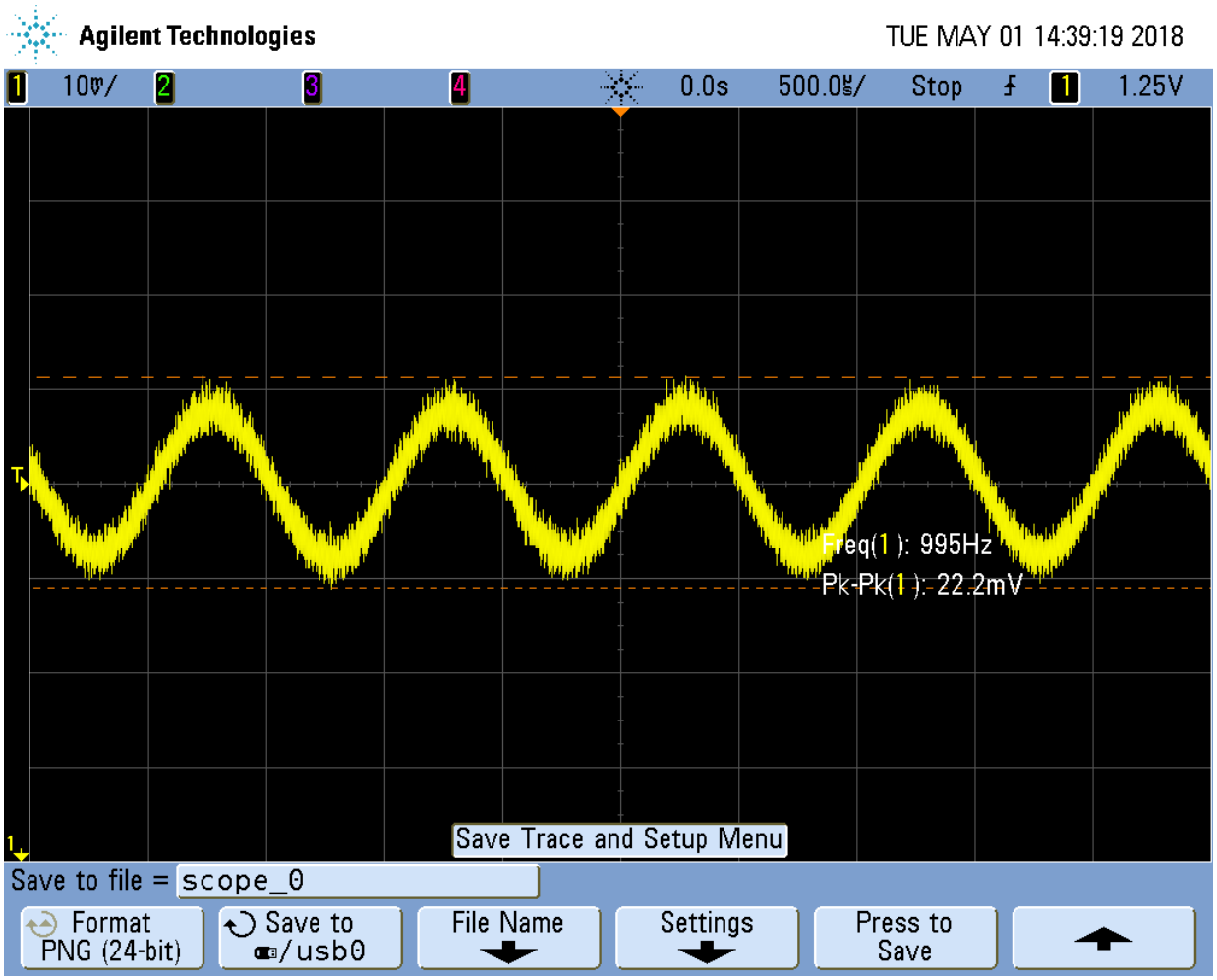

Figure 3: Amplified Waveform of a 1kHz Signal of Peak-to-Peak Amplitude of 20mV

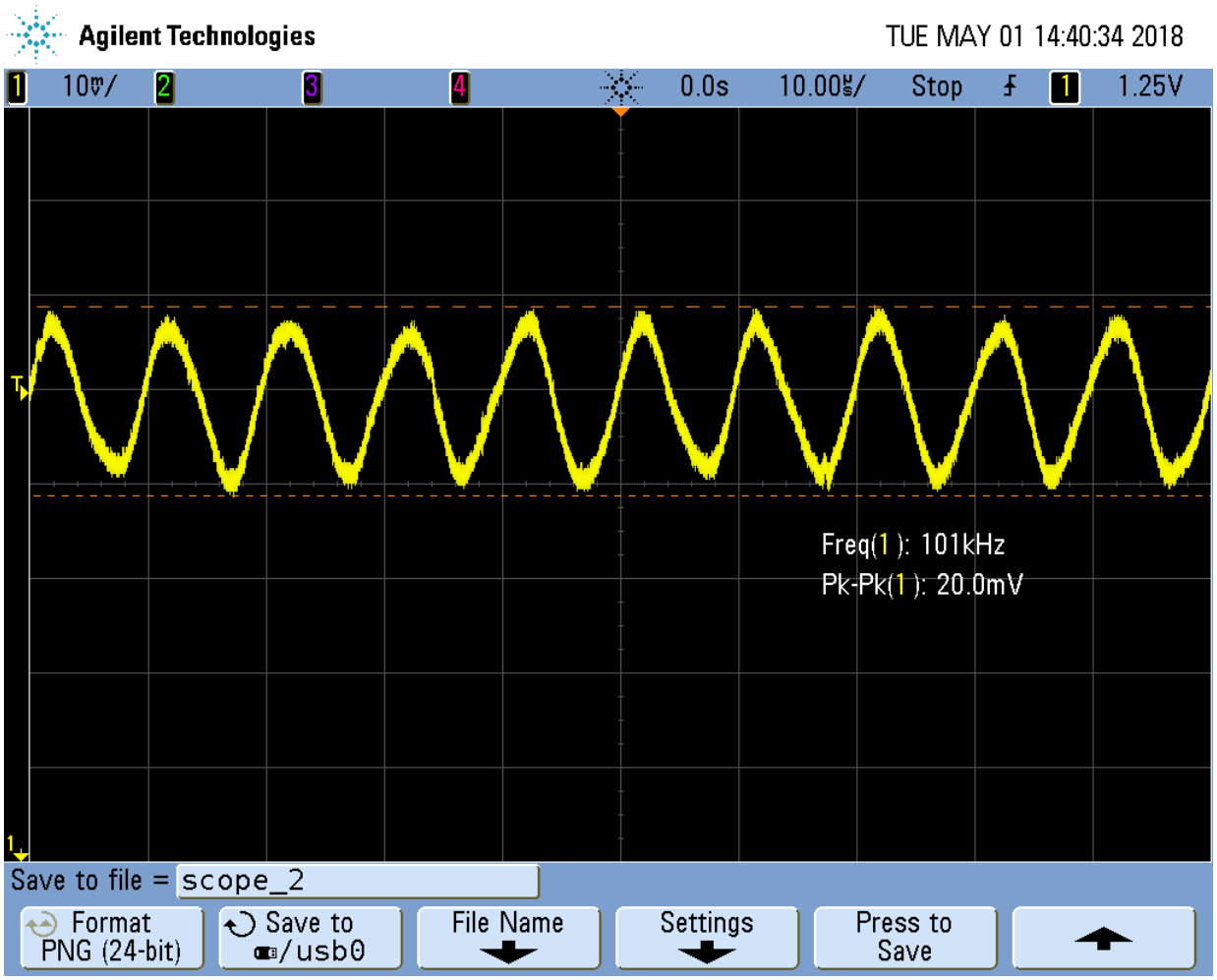

Figure 4: Amplified Waveform of a 100kHz Signal of Peak-to-Peak Amplitude of 20mV

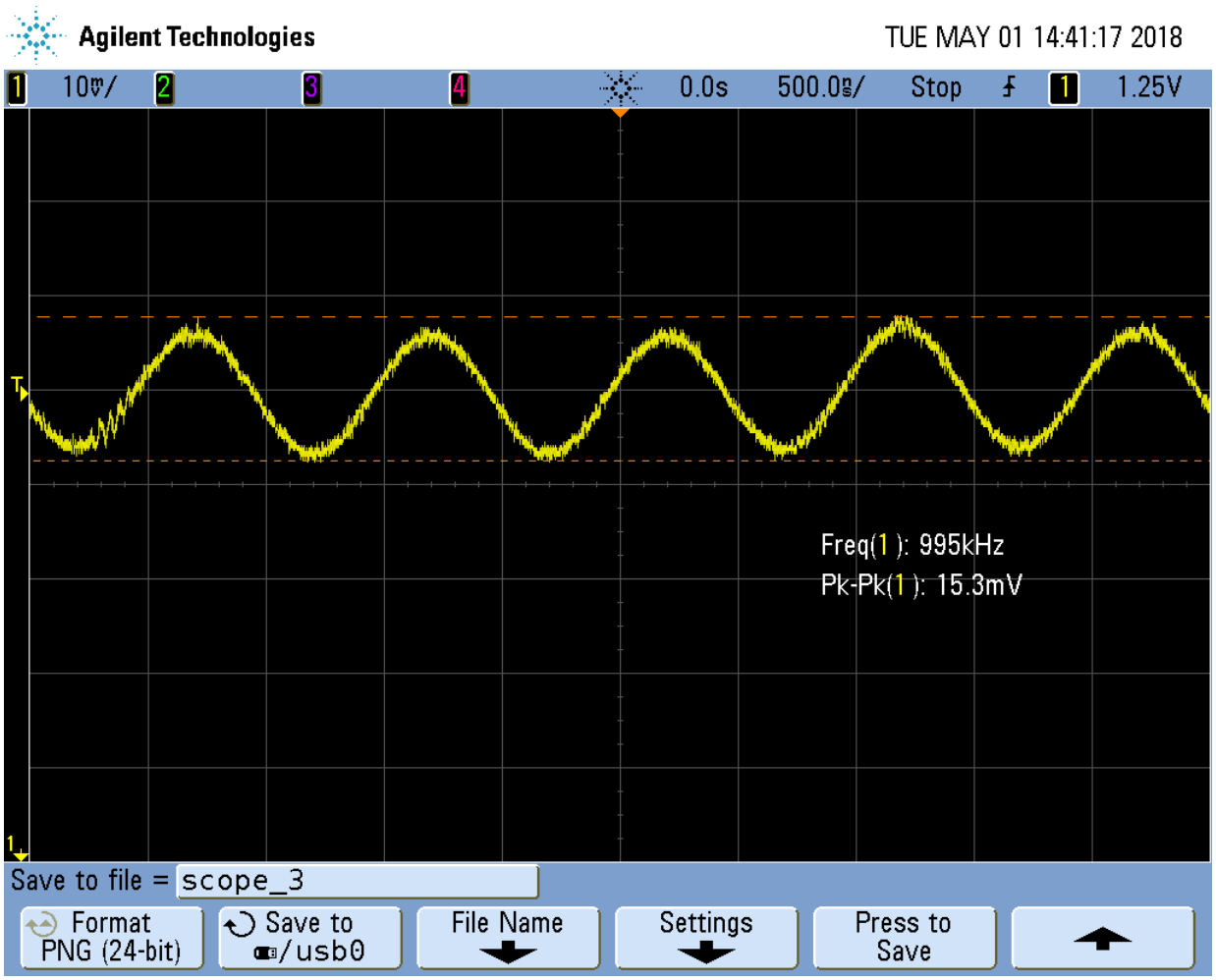

Figure 5: Amplified Waveform of a 1MHz Signal of Peak-to-Peak Amplitude of 20mV

Table 2: Figure (5) Data

Frequency [kHz]	Gain [V/V]
1	1.11
100	1.00
1000	0.77

The varying gains as a function of frequency shows that the amplifier is not as effective at higher frequencies. In order for this circuit to function as a voltage follower or buffer as it is intended, the signal frequency should stay near 100kHz.

This procedure is repeated when biasing the transistor 10mV higher. Results are shown in Figures (6), (7), and (8), respectively, and gains are tabulated in Table (3).

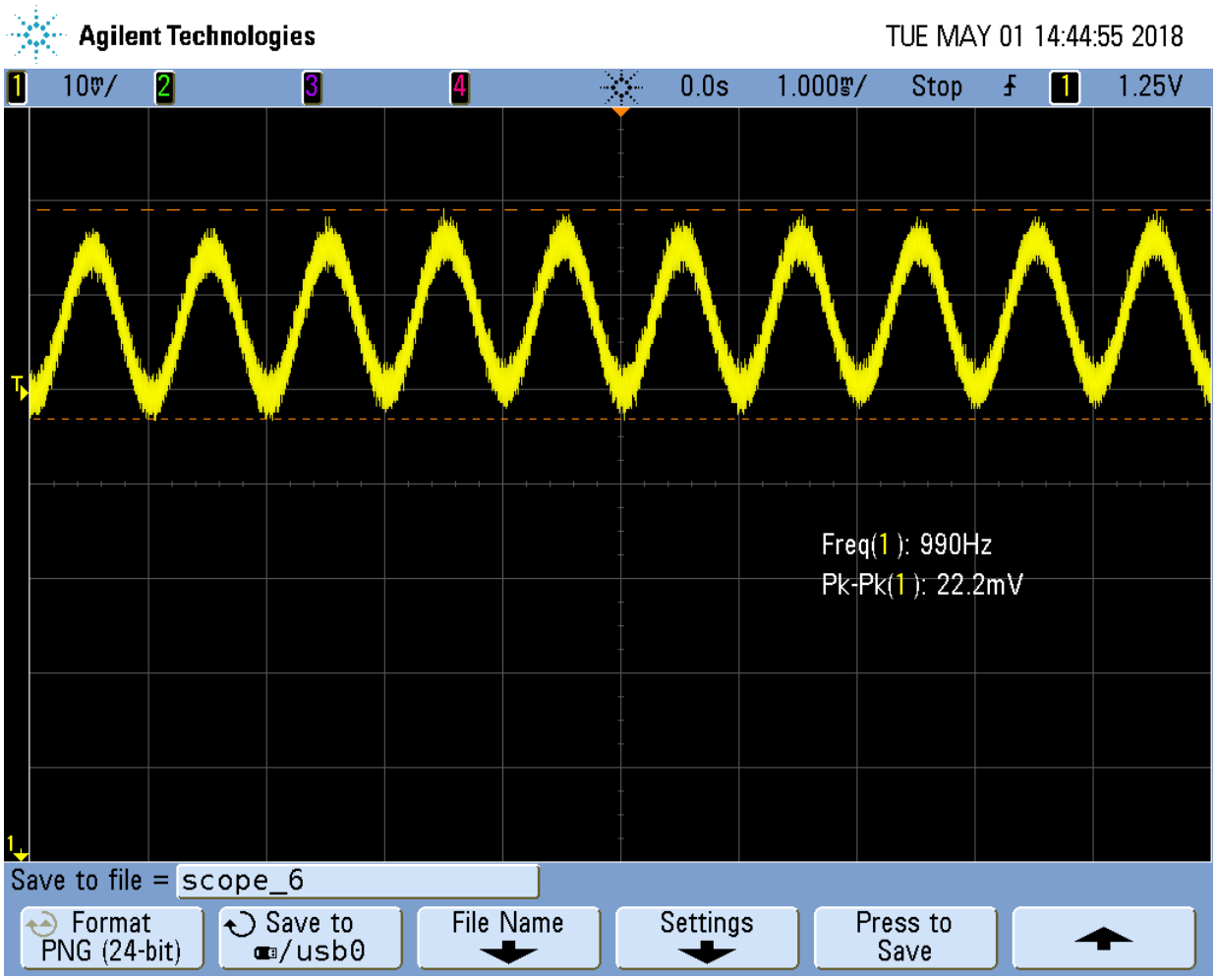

Figure 6: Amplified Waveform of a 1kHz Signal of Peak-to-Peak Amplitude of 20mV

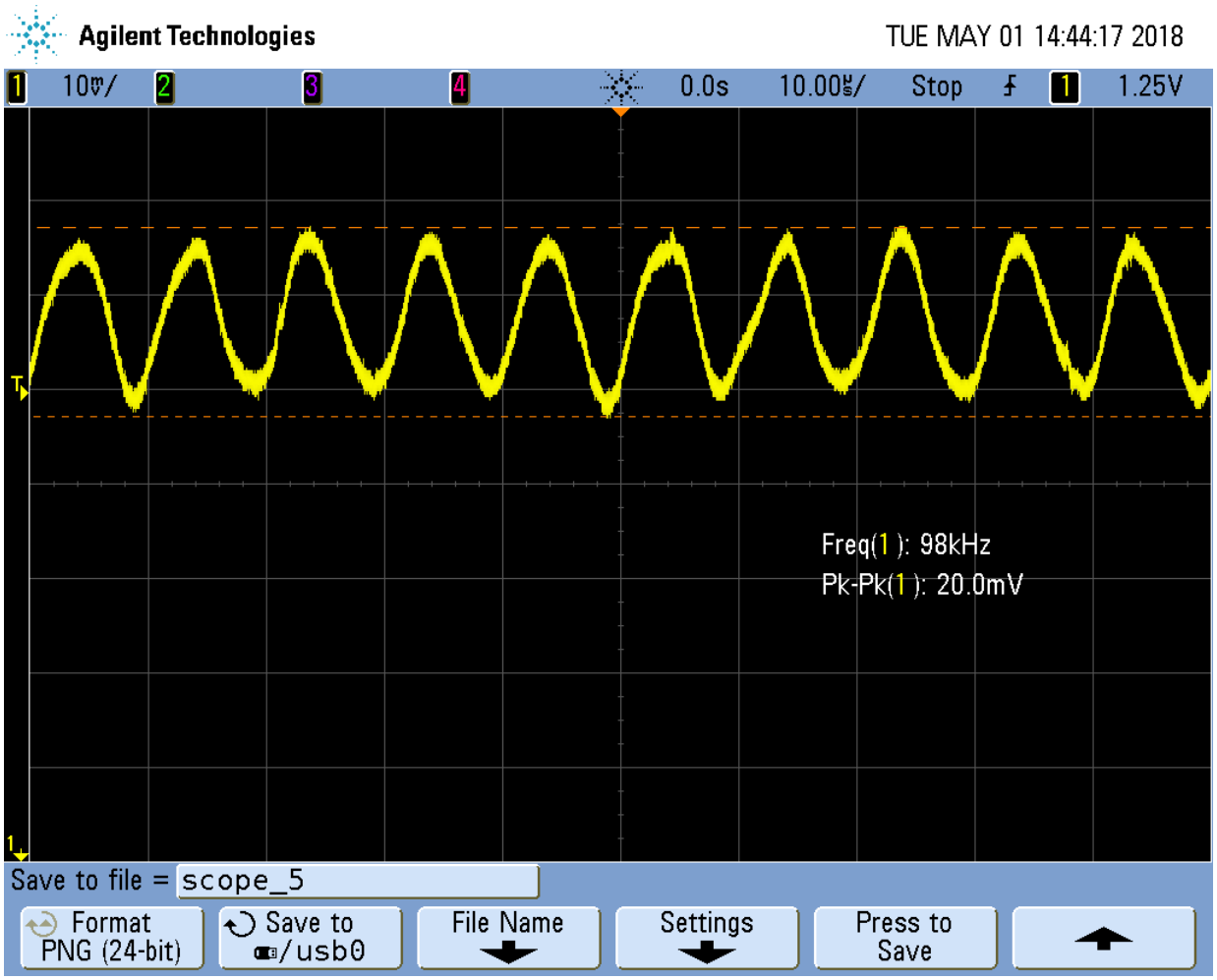

Figure 7: Amplified Waveform of a 100kHz Signal of Peak-to-Peak Amplitude of 20mV

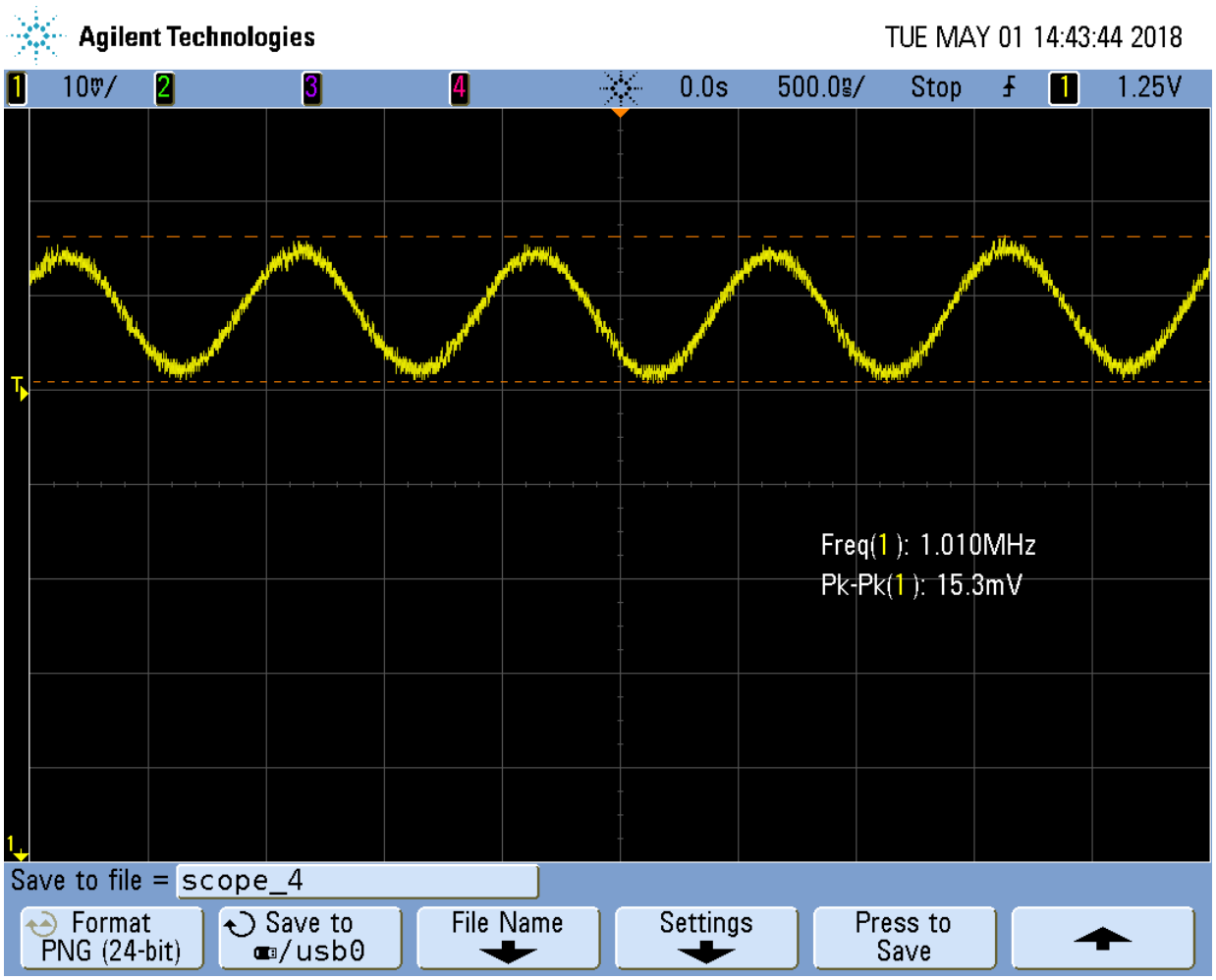

Figure 8: Amplified Waveform of a 1MHz Signal of Peak-to-Peak Amplitude of 20mV

Table 3: Figure (8) Data

Frequency [kHz]	Gain [V/V]
1	1.11
100	1.00
1000	0.765

Due to the nearly uniform slope of the VTC in the saturation region, the gain as a function of the bias voltage is nearly constant. Thus, these waveforms and gains are practically identical to what is observed earlier.

3 Part 2

A common source NMOS amplifier is constructed for dc and small signal analysis.

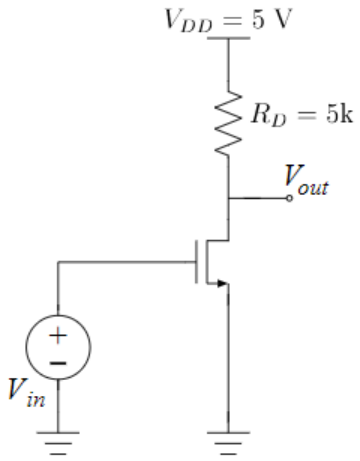

Figure 9: Common-Source Amplifier

V_{in} or V_{GS} is swept from 0 V to 3 V in increments of 0.1 V and V_{out} or V_{DS} is measured at each point. This range is chosen in order to capture the full range of the saturation operating mode and the transition from saturation to triode mode of the NMOS in the VTC. The results are plotted and tabulated below.

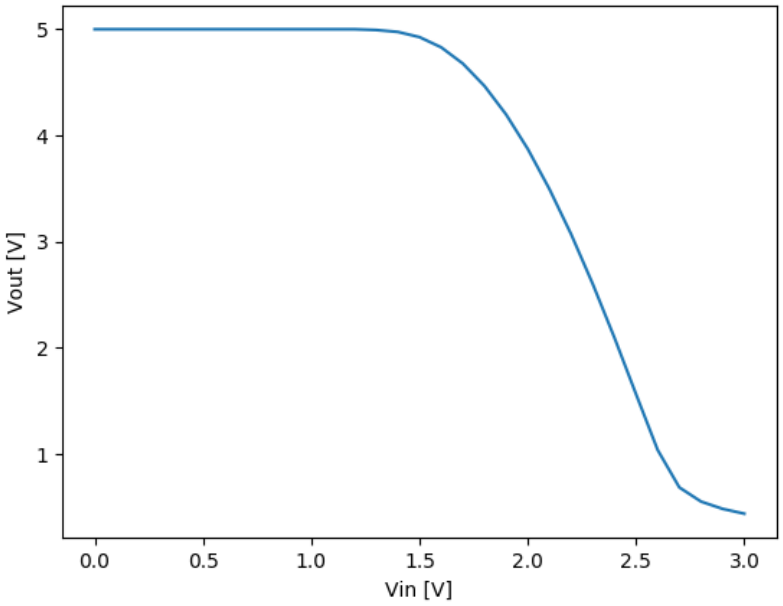

Figure 10: VTC of Common Source NMOS Amplifier

Table 4: Figure (10) Data

Vin [V]	Vout [V]
0.0	5.000
0.1	5.000
0.2	5.000
0.3	5.000
0.4	5.000
0.5	5.000
0.6	5.000
0.7	5.000
0.8	5.000
0.9	5.000
1.0	5.000
1.1	5.000
1.2	5.000
1.3	4.993
1.4	4.975
1.5	4.926
1.6	4.830
1.7	4.677
1.8	4.466
1.9	4.197
2.0	3.873
2.1	3.495
2.2	3.071
2.3	2.602
2.4	2.097
2.5	1.564
2.6	1.038
2.7	0.686
2.8	0.553
2.9	0.484
3.0	0.439

From the VTC in Figure (10), the NMOS begins and remains in cutoff until $V_{in} = 1.3$ V where V_{out} begins to dip below V_{DD}. The NMOS then enters the saturation region and remains there until the slope of the curve begins to decrease at around $V_{in} = 2.6$ V. Beyond that point, the NMOS operates in triode mode.

To find the DC voltage at the middle of saturation region $V_{in(eq2)}$, the average from the highest and lowest V_{out} value in the VTC is calculated. Then, and the closest value of V_{in} that corresponds to the the calculated average is the value taken for $V_{in(eq2)}$.

$$\frac{5V + 0.439V}{2} = 2.720V \approx V_{out} = 2.602V \Rightarrow V_{in(eq2)} = 2.3V \tag{1}$$

Then circuit is then biased at the $V_{in(eq2)}$ found above and a sine wave with 10 mV amplitude and 1 MHz is applied at the input. Note, for the measurement taken at 1 MHz, a 30 mV amplitude is used for the input sine wave because the original 10 mV amplitude is too weak and yielded a heavily distorted output signal that is immeasureable with the oscilloscope.

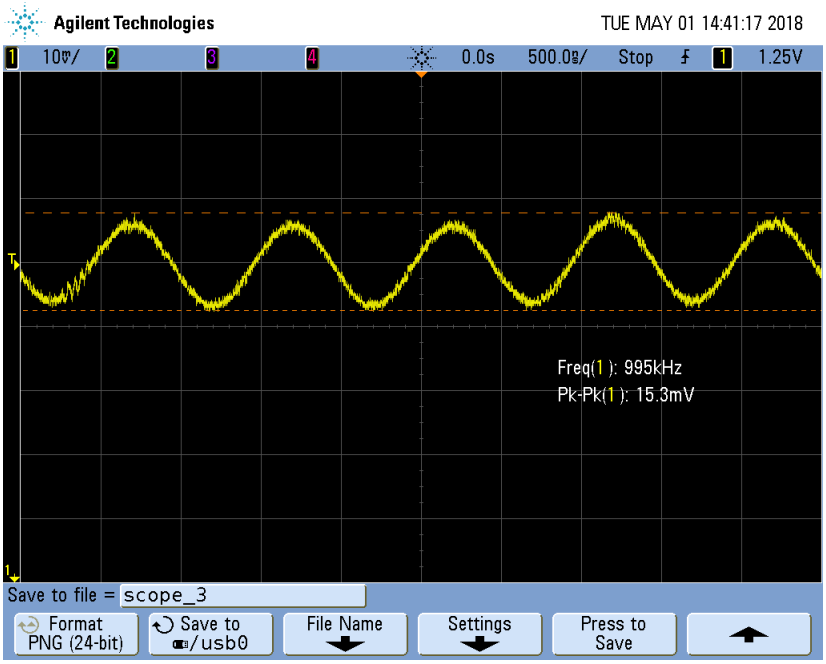

Figure 11: Output Voltage Sine Wave, 1 MHz

This experiment is repeated with sine waves with varying frequencies.

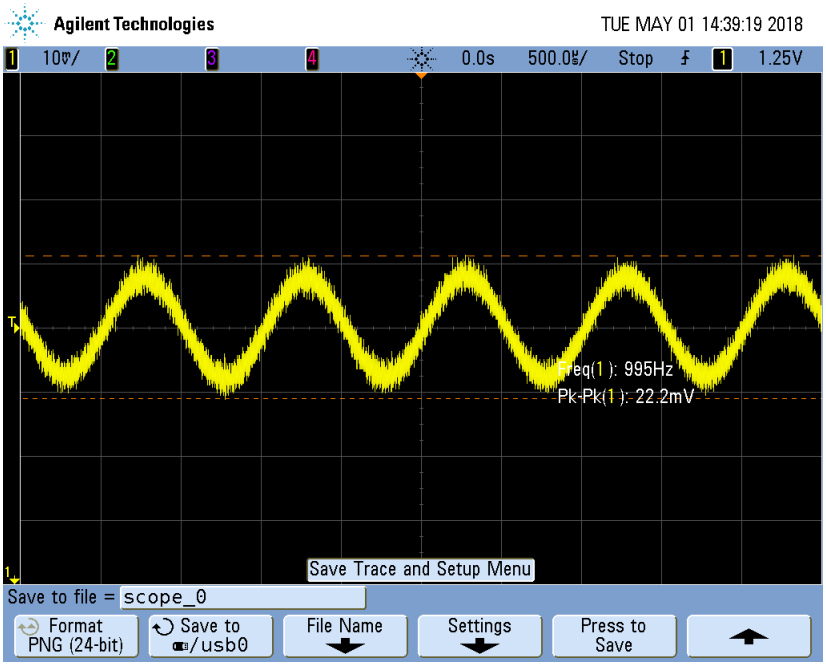

Figure 12: Output Voltage Sine Wave, 1 kHz

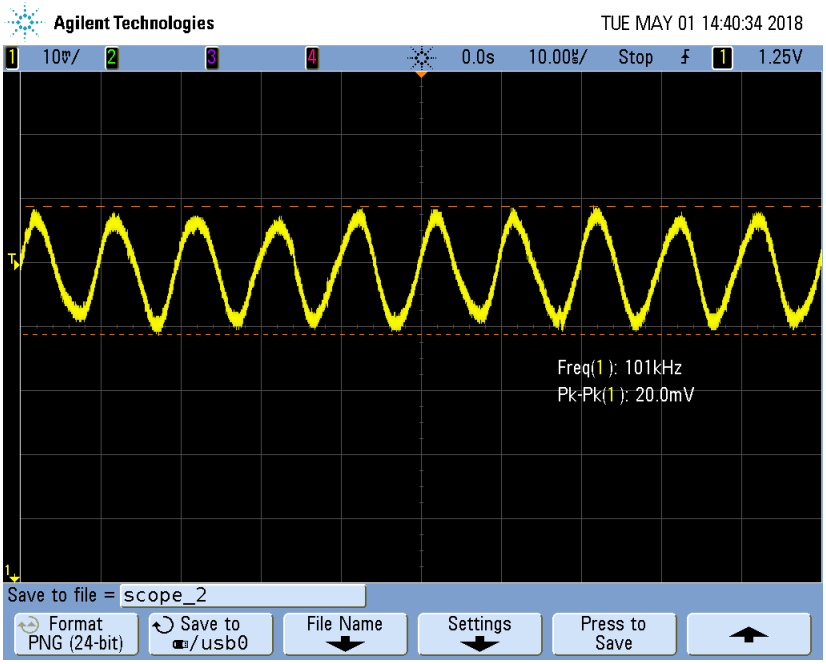

Figure 13: Output Voltage Sine Wave, 100 kHz

The amplitude of the output sine wave is measured for each input sine wave. From the output amplitudes, the small signal gain in $\frac{V}{V}$ is found for each frequency.

Table 5: Gain of Common Source Amplifier

Frequency [kHz]	Gain [V/V]
1	-6.5
100	-5.0
1000	-1.2

The small signal gain is observed to decrease as the frequency increases. This is expected because parasitic capacitances in the NMOS cause the circuit to effectively behave like a low-pass filter.

The DC bias of the circuit is then increased by 10 mV, and the experiment is repeated.

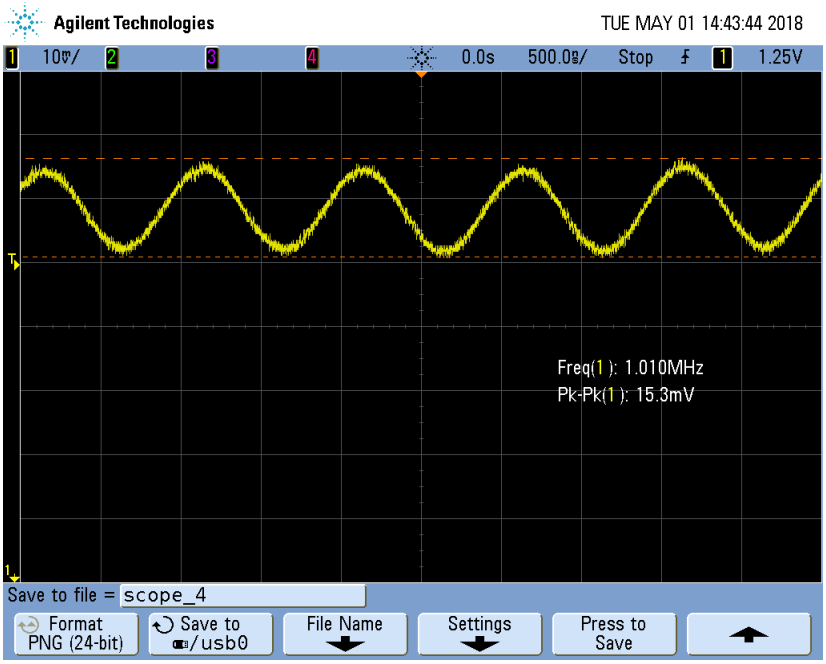

Figure 14: Output Voltage Sine Wave, 1 MHz, Increased dc Bias

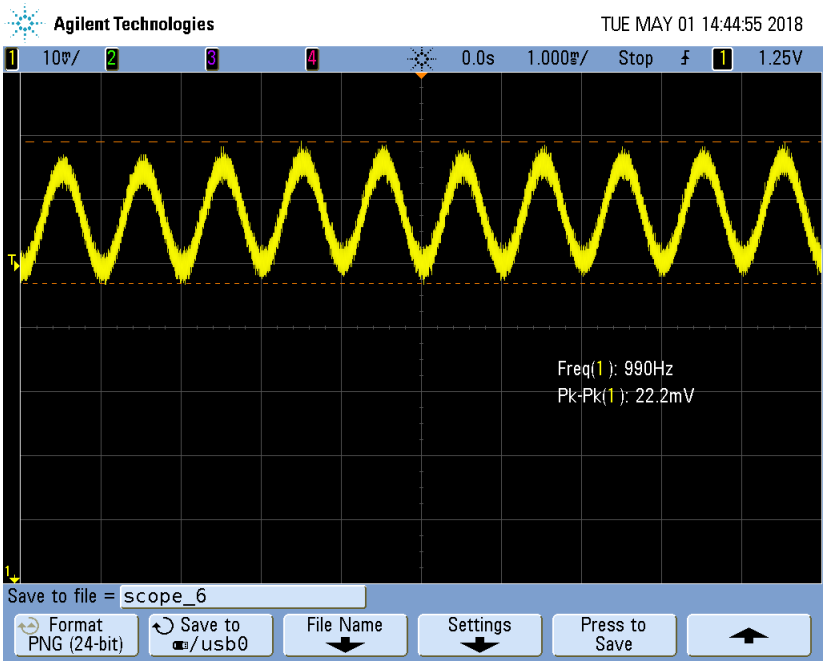

Figure 15: Output Voltage Sine Wave, 1 kHz, Increased dc Bias

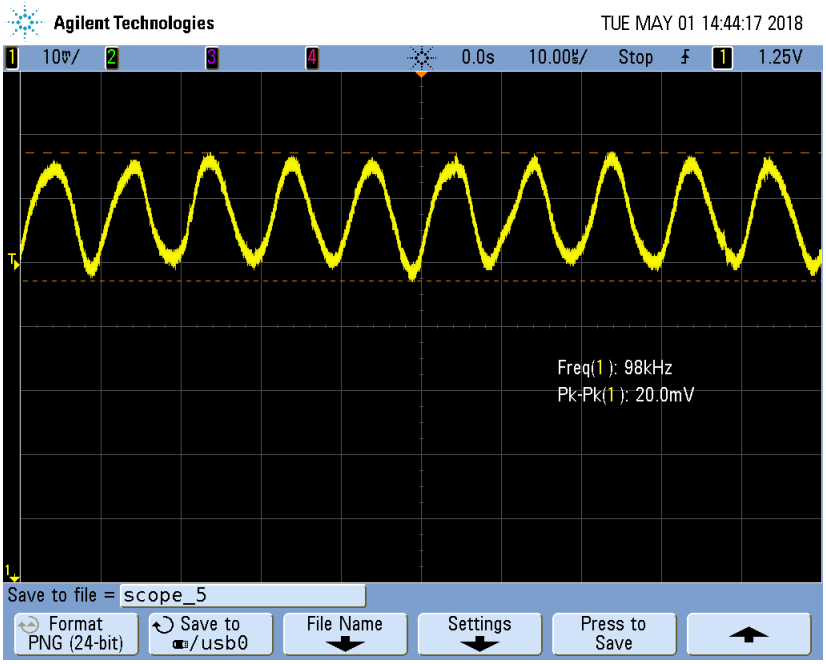

Figure 16: Output Voltage Sine Wave, 100 kHz, Increased dc Bias

The small-signal gain values found are tabulated below.

Table 6: Gain of Common Source Amplifier with 10 mV Higher Bias

Frequency [kHz]	Gain [V/V]
1	-6.5
100	-5.0
1000	-1.2

As expected, the new gain values are slightly higher than the values found for the original DC bias. This is because in saturation mode, V_{out} is directly proportional to the drain current, which is directly proportional to the square of V_{in}. This means that as V_{in} increases in the saturation region, the slope of the VTC $\frac{dV_{out}}{dV_{in}}$, another definition for the small-signal gain, increases as well.

4 Part 3

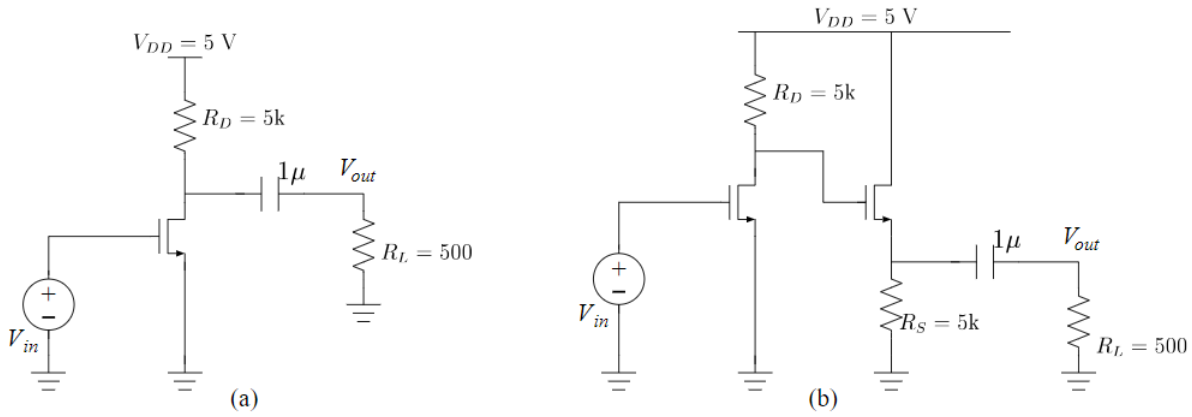

Figure 17: Amplifiers with Loads and Decoupling Capacitors

The common-source amplifier is constructed with a 1µF decoupling capacitor and 500Ω load at the output. The decoupling capacitor ensures that the output has a DC bias of 0V since any DC voltage simply charges the capacitor and does not make it to the resistor. The gain is determined at different frequencies. Again, the gain degrades at higher frequencies due to the parasitic capacitances of the MOSFET acting as a low-pass filter, which cuts down on the signal's amplitude. Because of the attached load, only $\frac{R_L}{r_{out}+R_L}V_{in}$ ends up appearing at the output, where r_{out} is the amplifier's output resistance. Since R_L is comaparable in magnitude to r_{out}, the voltage division effect causes the gain to be much lower than an ideal open circuit gain, measured in part 2.

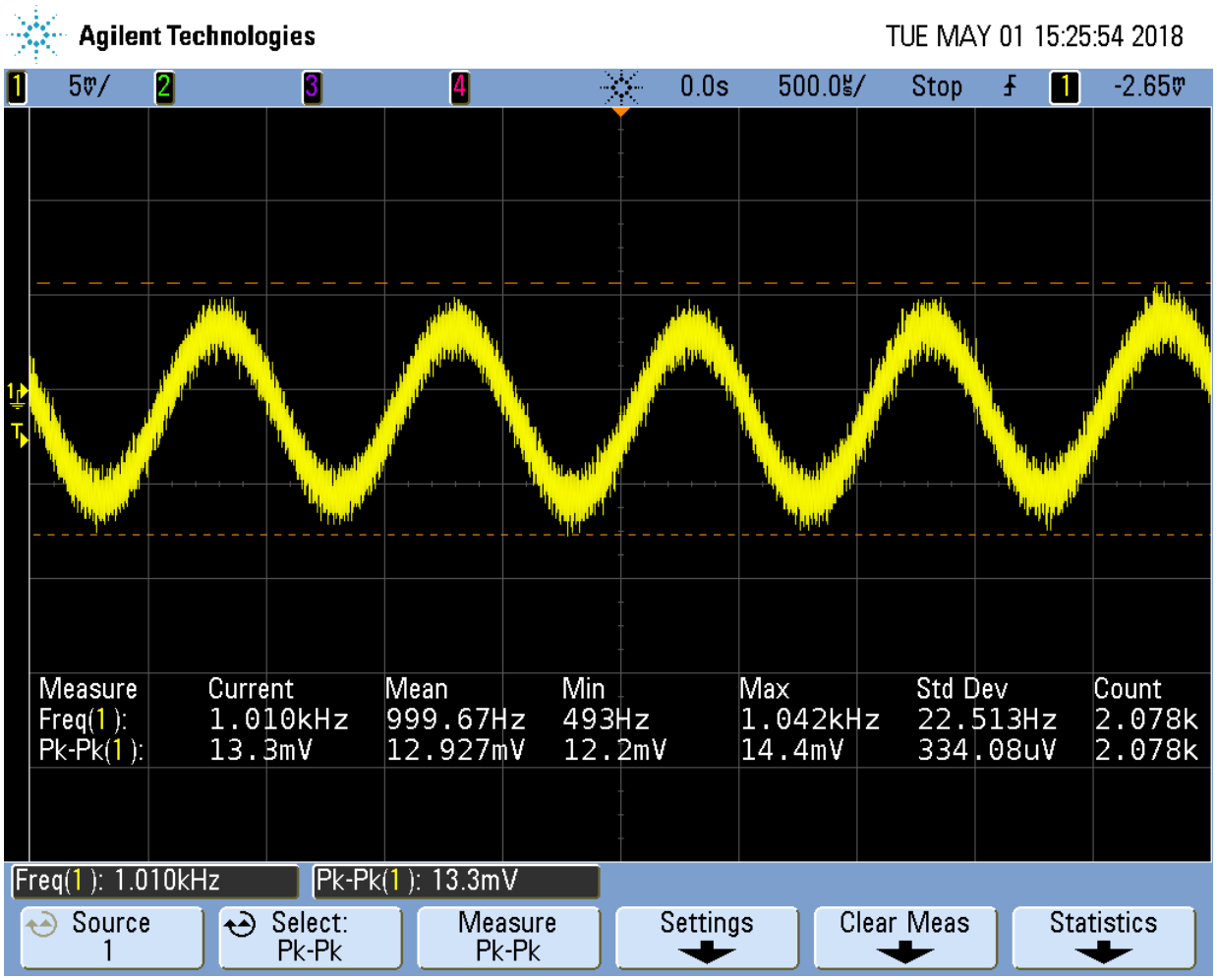

Figure 18: Common-Source Amplifier with Load and Decoupling Capacitors, 1kHz Input

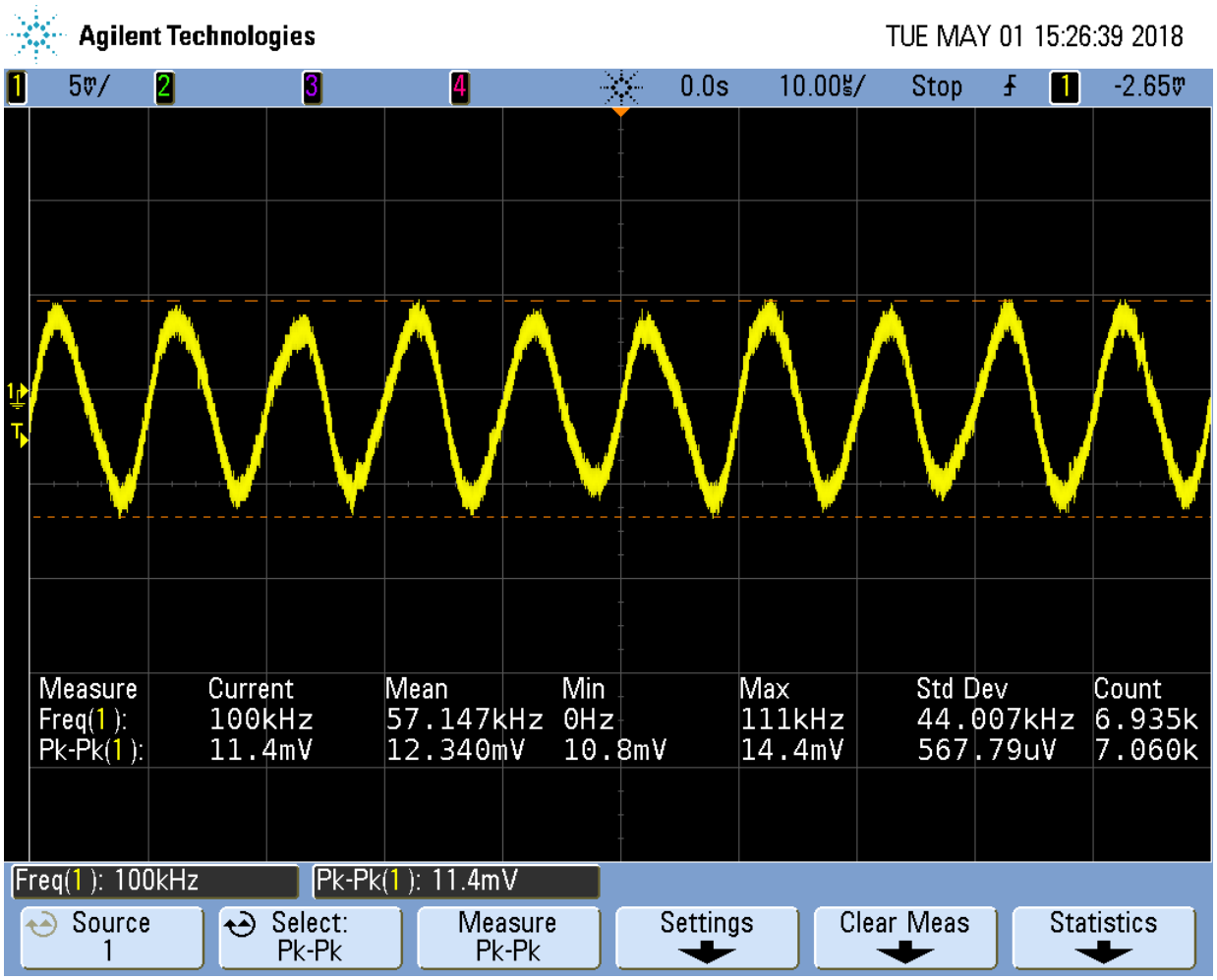

Figure 19: Common-Source Amplifier with Load and Decoupling Capacitors, 100kHz Input

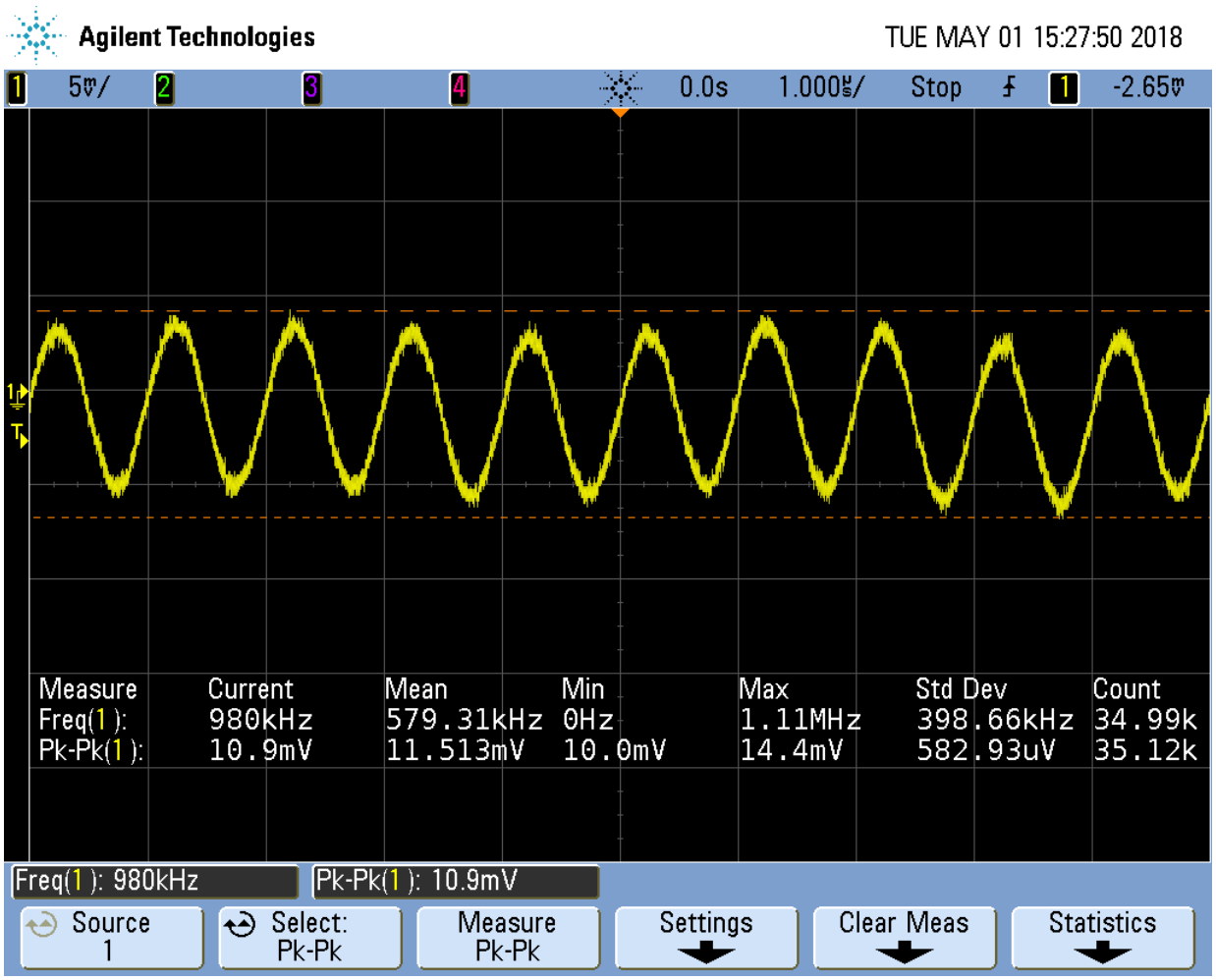

Figure 20: Common-Source Amplifier with Load and Decoupling Capacitors, 1MHz Input

Table 7: Common-Source Amplifier with Decoupling Capacitor and Load Gain

Frequency [kHz]	Gain [V/V]
1	-0.665
100	-0.570
1000	-0.545

A common-drain amplifier is then connected to the output of the common-source amplifier. The common-drain amplifier's output resistance is given by $r_{out,CDA} = R_S||r_o||\frac{1}{g_m}$. Assuming r_o is very large, $r_{out,CDA} \approx R_S||\frac{1}{g_m}$. The common-source amplifier's output resistance is given by $r_{out,CSA} = R_D||r_o$. Making the same assumption about r_o, $r_{out,CSA} \approx R_D$.

In this specific case, $R_S = R_D = R$. Expanding $r_{out,CDA}$, the equation can be rewritten as:

$$r_{out,CDA} = \frac{R}{1 + g_m R} \tag{2}$$

Likewise, $r_{out,CSA}$ can be written as:

$$r_{out,CSA} = R \tag{3}$$

Assume $R > 0\Omega$ and $g_m > 0\frac{mA}{V}$. $g_m R > 0$ must then be true. This further implies that $1 + g_m R > 1$ and that $\frac{1}{1+g_m R} < 1$. Because $R > 0\Omega$, $\frac{R}{1+g_m R} < R$. Invoking equations (2) and (3), $r_{out,CDA} < r_{out,CSA}$.

Therefore, in this configuration, the cascaded amplifier should have a lower output resistance since the output is presented with $r_{out,CDA}$ and not $r_{out,CSA}$. As a result, for the same load, the gain should be higher since R_L is now relatively larger in the voltage divider. This claim is corroborated by the data at various frequencies. The gain magnitude increases.

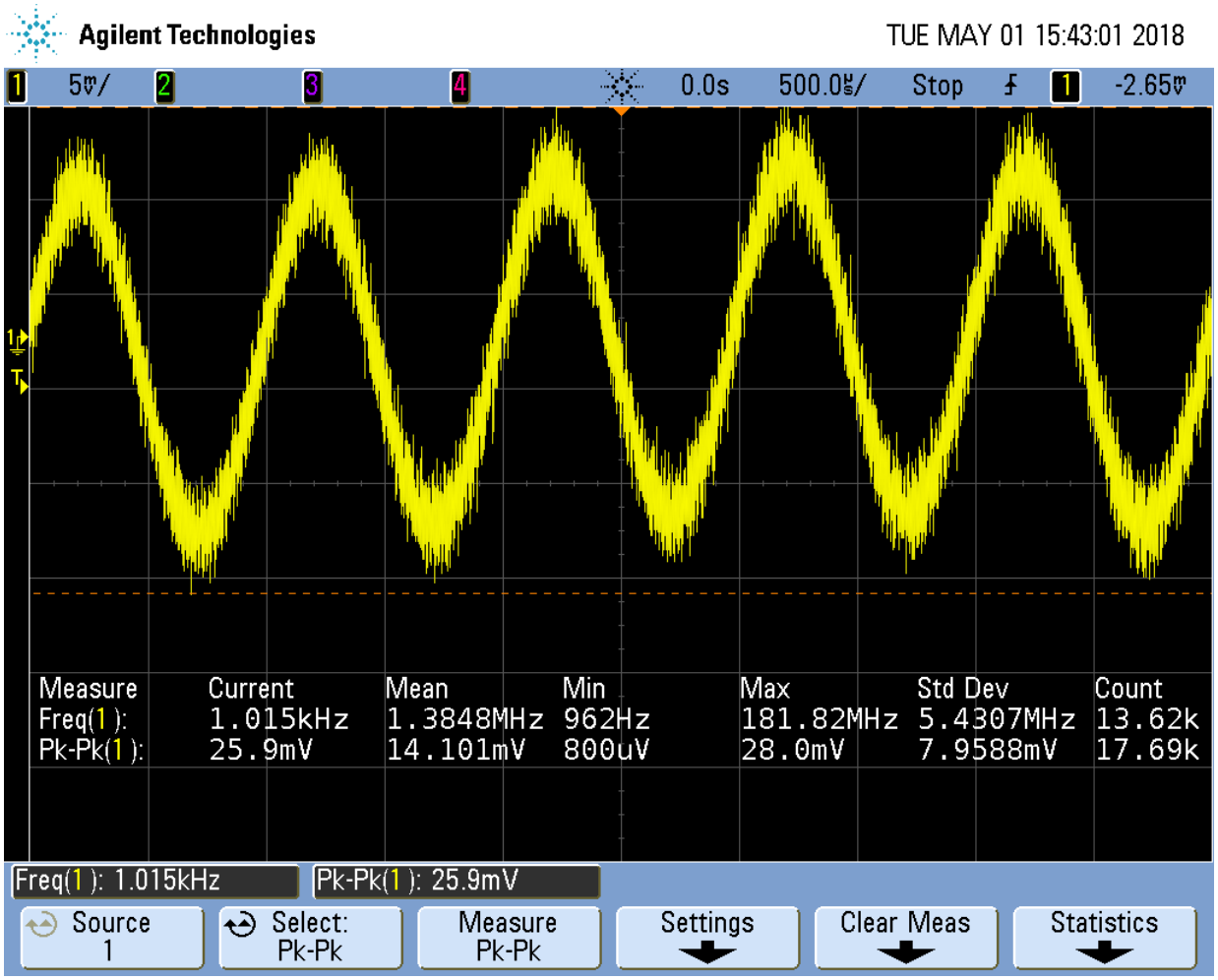

Figure 21: Two-Stage Amplifier with Load and Decoupling Capacitors, 1kHz

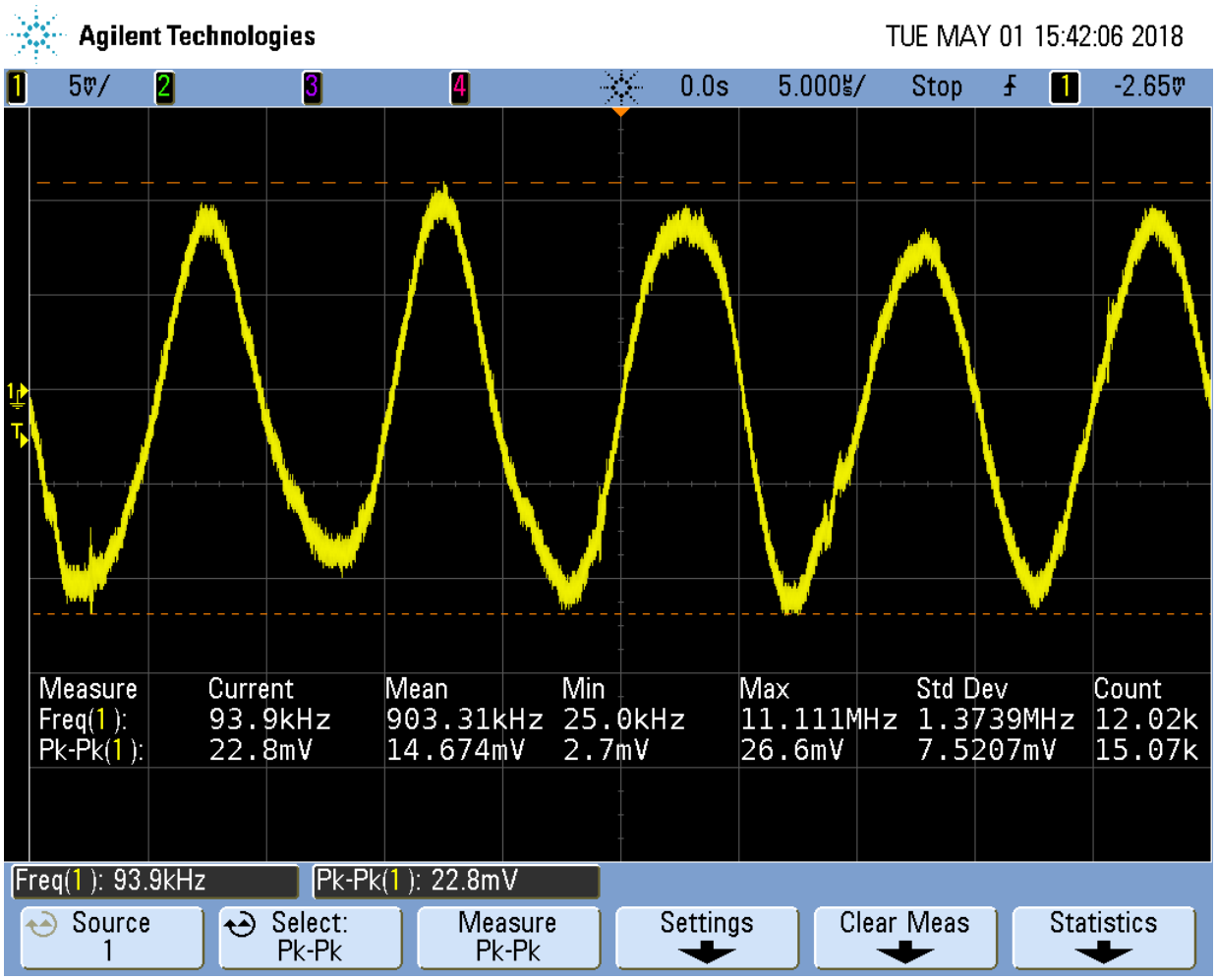

Figure 22: Two-Stage Amplifier with Load and Decoupling Capacitors, 100kHz

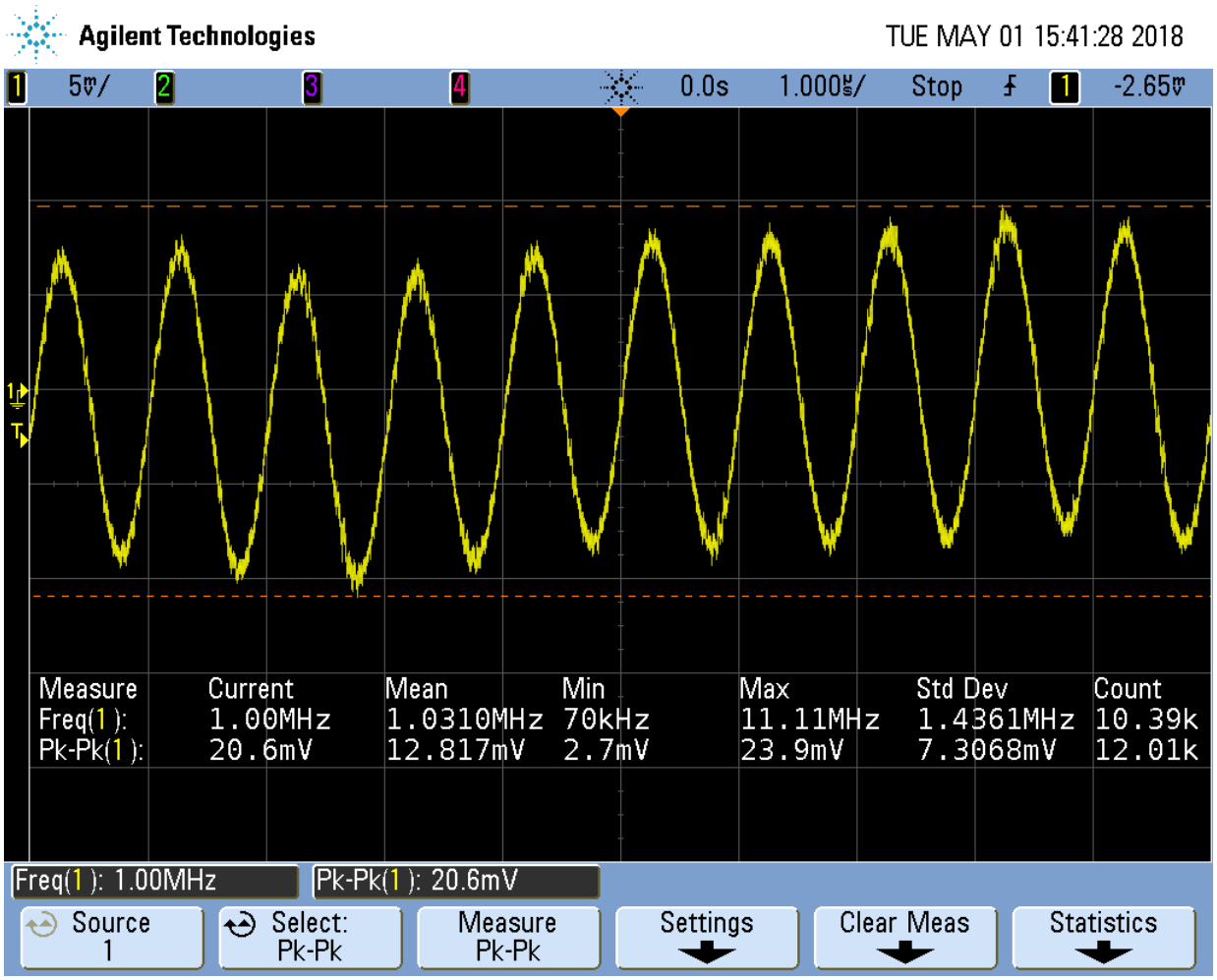

Figure 23: Two-Stage Amplifier with Load and Decoupling Capacitors, 1MHz

Table 8: Two-Stage Amplifier with Decoupling Capacitor and Load Gain

Frequency [kHz]	Gain [V/V]
1	-1.30
100	-1.14
1000	-1.03

5 Conclusion

5.1 Part 1

The common-drain configuration behaves as expected in both DC and AC tests. The circuit's near-unity gain makes it an excellent voltage follower if operated at the right frequency. There is a noticable decrease in gain at higher frequencies due to the unavoidable parasitic capacitances in the package and the transistor.

5.2 Part 2

The common source amplifier exhibited expected behavior within reasonable tolerances. The VTC of the circuit shows distinct cutoff, saturation, and triode regions. However, sweeping V_{in} from 0 to 2 V does not provide a sufficient range for the entire saturation region to be observed, which is why V_{in} is swept from 0 to 3 V instead. For the small-signal analysis, input sine waves at 1 MHz produced distorted output sine waves, especially at low amplitudes. This provided motivation for lower frequencies and higher amplitudes to be used in the experiment. Because 1 mV amplitude input signal is much too weak for this application, 30 mV amplitude is used for the 1 MHz input signal, and 10 mV amplitude is used for the other frequencies. Because no clamping of the output signal is observed, the gain values calculated should not be adversely affected despite the different amplitudes applied for different frequencies.

5.3 Part 3

Decoupling capacitors should be used in practice for amplifier designs to prevent the output signal from having a DC bias that may affect later circuit stages. When a small load resistance is added to the output, the gain is going to drop significantly due to the formation of a voltage divider with the amplifier's output resistance. One way to remedy this with common-source amplifiers is to add a common-drain amplifier stage to its output because common-drain amplifiers typically have lower output resistances. The data and oscilloscope plots confirm these claims.