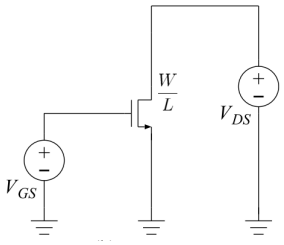

Figure 1: Circuit 2

Using the same circuit as before, i_D was measured while sweeping V_{DS} for $V_{GS} = 2.5$V and then 5.0V and keeping $V_{SB} = 0$V. Results are shown in Figure 2a and 2b.

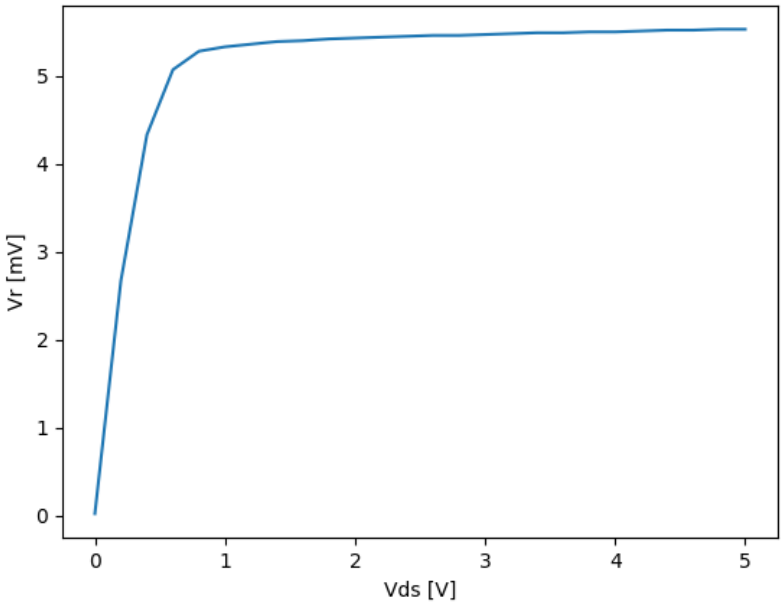

Figure 2: i_D versus V_{DS} of NMOS where $V_{GS} = 2.5$V

Table 1: Figure (**??**) Data

Vds [V]	Id [mA]
0.0	0.00
0.2	0.28
0.4	0.45
0.6	0.52
0.8	0.55
1.0	0.55
1.2	0.55
1.4	0.56
1.6	0.56
1.8	0.56
2.0	0.56
2.2	0.56
2.4	0.56
2.6	0.56
2.8	0.56
3.0	0.57
3.2	0.57
3.4	0.57
3.6	0.57
3.8	0.57
4.0	0.57
4.2	0.57
4.4	0.57
4.6	0.57
4.8	0.57
5.0	0.57

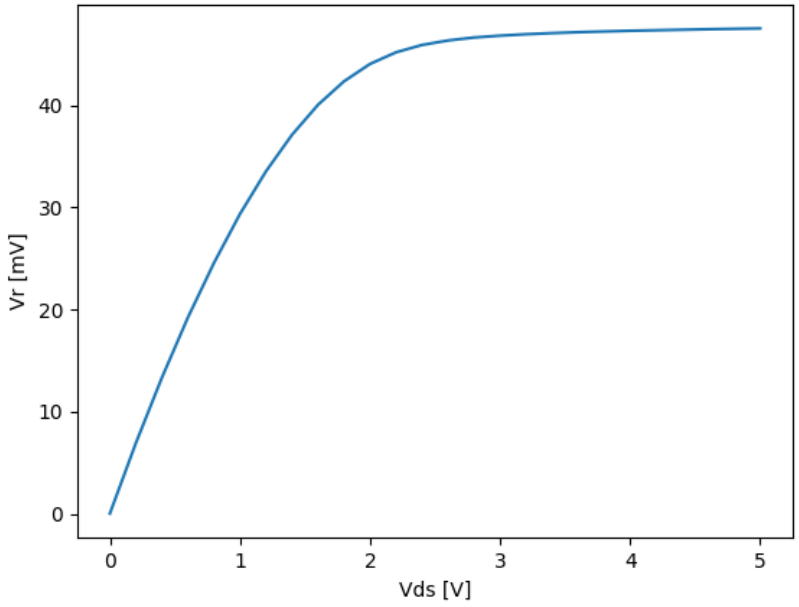

Figure 3: i_D versus V_{DS} of NMOS where $V_{GS} = 5$V

Table 2: Figure (3) Data

Vds [V]	Id [mA]
0.0	0.00
0.2	0.72
0.4	1.38
0.6	1.99
0.8	2.54
1.0	3.04
1.2	3.47
1.4	3.84
1.6	4.14
1.8	4.38
2.0	4.55
2.2	4.67
2.4	4.75
2.6	4.79
2.8	4.82
3.0	4.84
3.2	4.86
3.4	4.87
3.6	4.88
3.8	4.88
4.0	4.89
4.2	4.90
4.4	4.90
4.6	4.91
4.8	4.91
5.0	4.91

In both cases of V_{GS}, the transistor saturates near the value of $V_{GS} - V_{tn}$. For $V_{GS} = 2.5$V, this value is about 0.8V, and for $V_{GS} = 5.0$V, saturation occurs at around 3V This suggests that V_{tn} is around 1.8V, consistent with what was found in part 1.