

The following circuit is constructed for dc analysis.

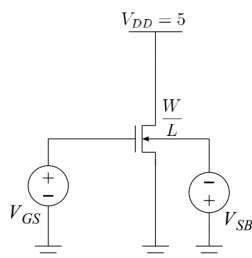


Figure 1: Circuit 1

V_{GS} is swept from 0 V to 5 V in increments of 0.2 V and i_D is measured at each value of V_{GS} . The results are plotted and tabulated below.

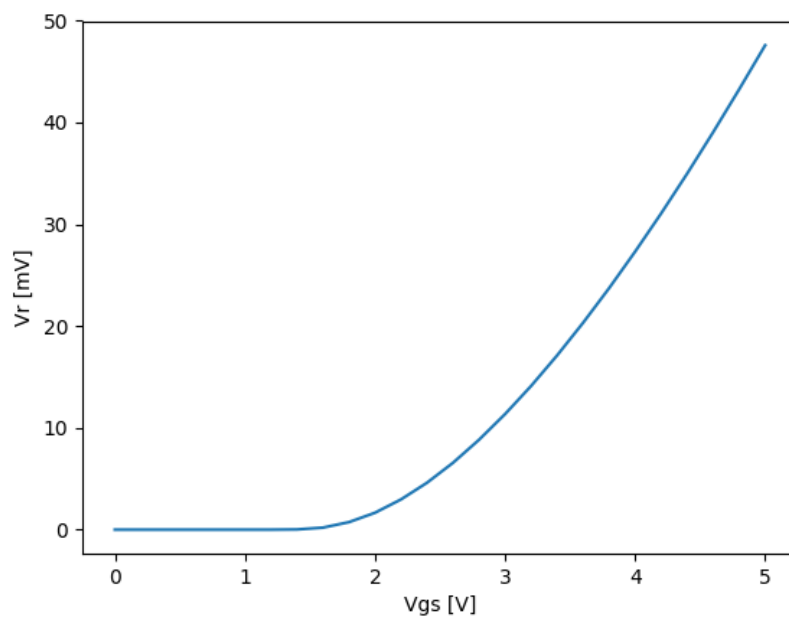


Figure 2: i_D versus V_{GS} of NMOS where $V_{SB} = 0$ V

Table 1: Figure (2) Data

Vgs [V]	Id [mA]
0.0	0.00
0.2	0.00
0.4	0.00
0.6	0.00
0.8	0.00
1.0	0.00
1.2	0.00
1.4	0.00
1.6	0.02
1.8	0.08
2.0	0.17
2.2	0.31
2.4	0.48
2.6	0.68
2.8	0.91
3.0	1.17
3.2	1.46
3.4	1.77
3.6	2.10
3.8	2.45
4.0	2.82
4.2	3.21
4.4	3.62
4.6	4.04
4.8	4.47
5.0	4.92

When a gate voltage V_{GS} is applied to the NMOS, an electric field is generated across the metal gate and p-type substrate. This electric field repels majority holes from the surface of the substrate, creating a depletion region. The NMOS operates in cutoff region for V_{GS} between 0 V to about 1.5 V.

When V_{GS} exceeds 1.5 V, donor electrons move to the surface of the substrate to form an n-type channel between the drain and source of the NMOS. This voltage is the threshold voltage V_{tn} . At this point, the NMOS is operating in saturation region because the saturation condition, $V_{DS} > V_{GS} - V_{tn}$ is met. This is clear, as $V_{DS} = V_D - V_S = V_{DD} - 0 = 5$ V and V_{GS} never exceeds 5 V. In saturation mode, the drain current is observed to quadratically increase as the gate voltage increases. This is consistent with the drain current equation for NMOS in saturation, $i_D = \frac{1}{2}k'_n \frac{W}{L}(V_{GS} - V_{tn})^2$.

Then, V_{SB} is set to 5 V so a negative voltage is applied to the bulk of the

NMOS, and the experiment is repeated. The results are plotted and tabulated below.

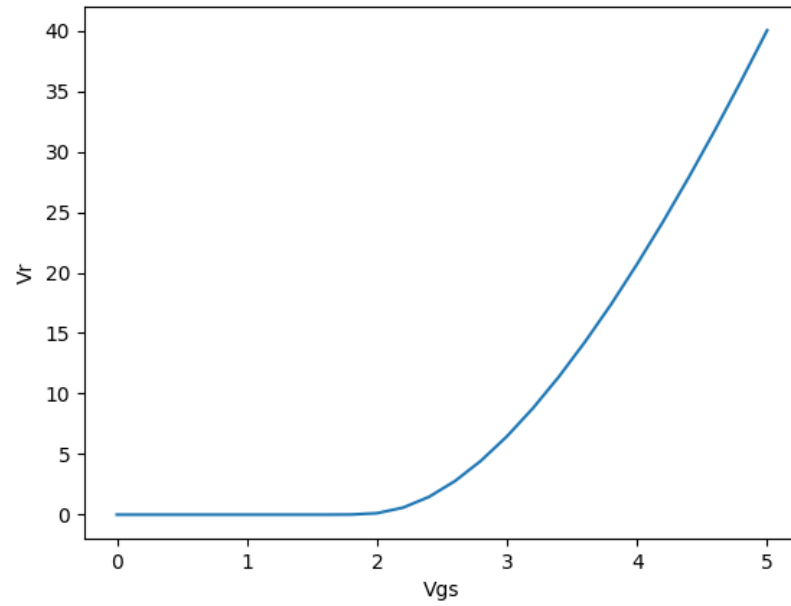


Figure 3: i_D versus V_{GS} of NMOS where $V_{SB} = 0.5V$

Table 2: Figure (3) Data

Vgs [V]	Id [mA]
0.0	0.00
0.2	0.00
0.4	0.00
0.6	0.00
0.8	0.00
1.0	0.00
1.2	0.00
1.4	0.00
1.6	0.00
1.8	0.00
2.0	0.01
2.2	0.06
2.4	0.15
2.6	0.29
2.8	0.46
3.0	0.67
3.2	0.91
3.4	1.18
3.6	1.48
3.8	1.80
4.0	2.14
4.2	2.50
4.4	2.89
4.6	3.29
4.8	3.71
5.0	4.14

The negative voltage applied to the bulk of the NMOS causes the depletion region between the heavily doped n-type drain/source and the p-type substrate to widen. The wider depletion region impedes the formation of the n-type channel and the gate voltage must be increased to compensate. This effectively increases the threshold voltage of the NMOS. This also agrees with the Shichman-Hodges model for the body effect of MOSFETs, $V_{tn} = V_{to} + \gamma(\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f})$ where V_{to} is the threshold voltage when no voltage is applied to the body, γ is the body effect parameter and ϕ_f is the bulk potential of the MOSFET. In this experiment, the threshold voltage V_{tn} increased from 1.5 V to about 1.9 V.

Refer to Part 3 for $\frac{W}{L}$ ratio of the NMOS.