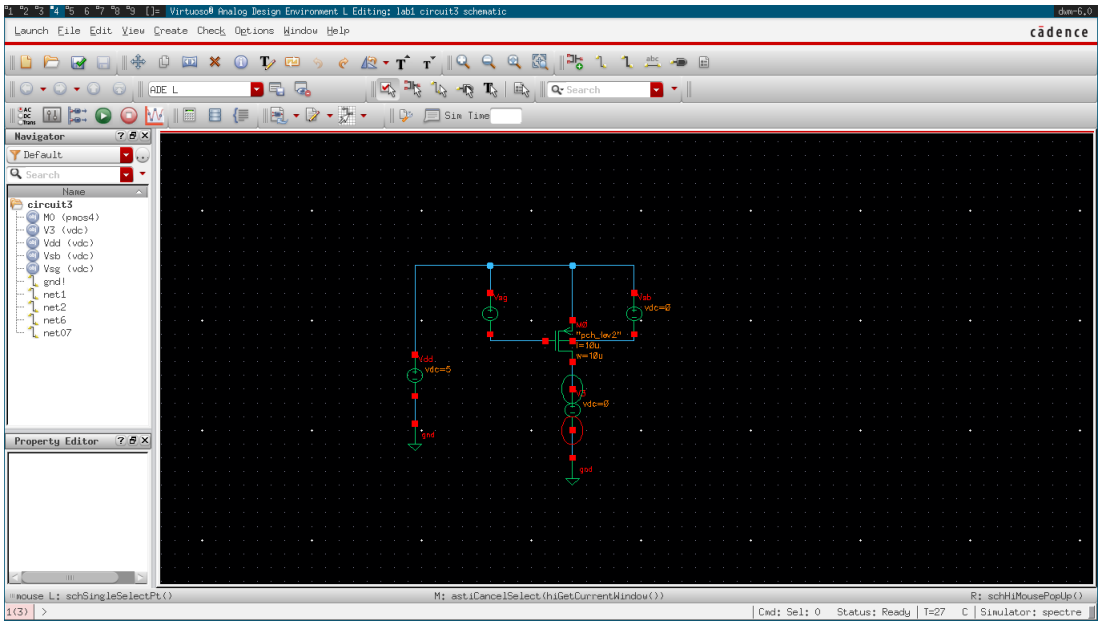

Figure 1: Circuit for Simulation 3

Simulation 3 is similar to Simulation 1 except that a PMOS is used instead of an NMOS.

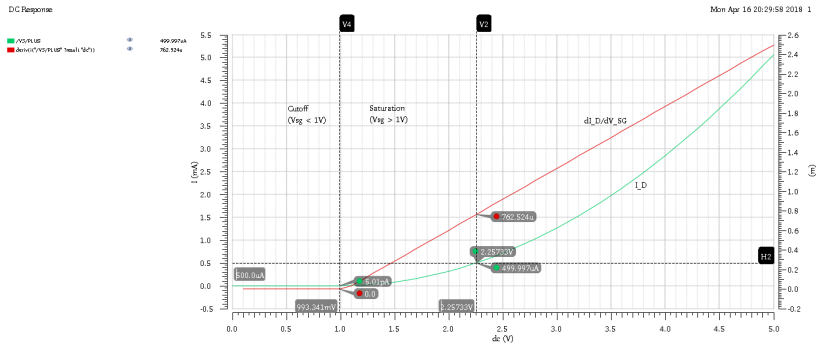

Figure 2: I_D and $\frac{\partial I_D}{\partial V_{SG}}$ versus V_{SG} for PMOS

Again, the transistor is in saturation when it exits cutoff because $V_{SD} = 5$V and $V_{SG} < 5$V, meaning $V_{SG} - |V_t| < V_{SD}$V. For the PMOS, the definition $g_m = \frac{\partial I_D}{\partial V_{SG}}$ shall be used.

Table 1: Simulation 3 Results

Vsg [V]	gm from DC operating point simulation [uA / V]	gm from Graph [uA / V]	Percentage E
2.25733	794.1	762.52	4.1%