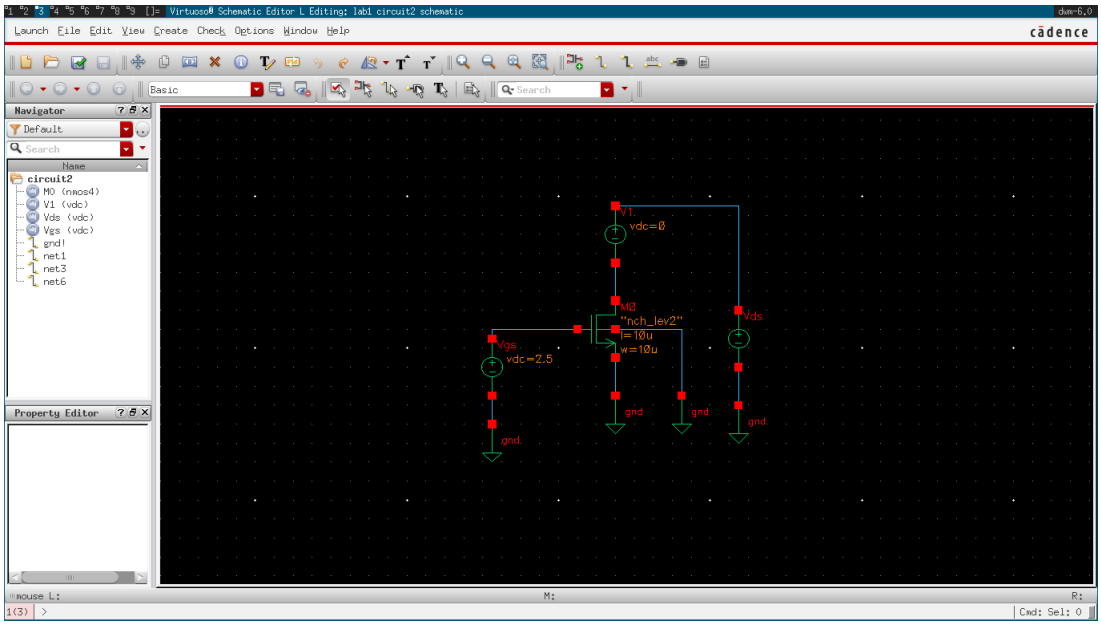

Figure 1: Circuit for Simulation 2

The I_D versus V_{DS} characteristics of the n-channel MOSFET are analyzed. For MOSFETs with channel-length modulation, $r_o = \frac{1}{\lambda I'_D}$ by definition, where $I'_D = \frac{k_n}{2} V_{ov}^2$ is the saturation current without channel-length modulation effects. Here, V_{ov} is the transistor's overdrive voltage, and k_n is the MOSFET's transconductance parameter. The small-signal drain-to-source conductance g_{ds} is to be defined as $g_{ds} = \frac{1}{r_o} = \lambda I'_D$. However, I'_D is difficult to acquire from realistic simulations.

To a first-order approximation, $I_D = \frac{k_n}{2} V_{ov}^2 (1 + \lambda V_{DS}) = I'_D (1 + \lambda V_{DS})$ in saturation mode. So, $\frac{\partial I_D}{\partial V_{DS}} = \lambda I'_D = g_{ds}$. Thus, by analyzing the derivative of I_D with respect to V_{DS} at a particular value of V_{DS}, g_{ds} can be determined from simulation.

First, a simulation is run with $V_{GS} = 0$V.

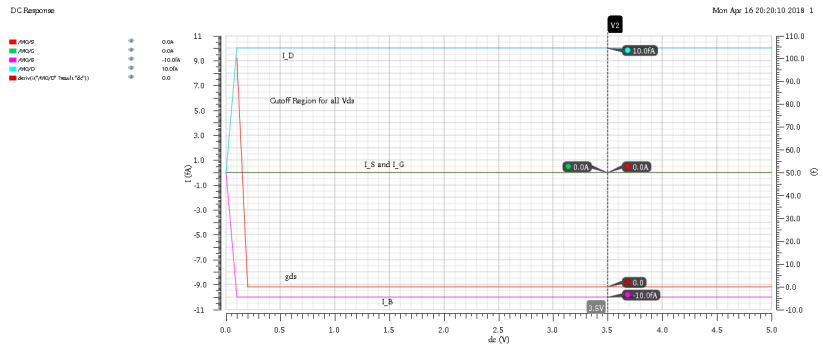

Figure 2: NMOS I_D versus V_{DS} when $V_{GS} = 0$V

Here, $I_S = 0$ and $I_D = -I_B \neq 0$. Because the transistor is in cutoff mode, no channel between the source and drain forms. However, the drain's doped n-region forms a pn-junction with the p-type body of the NMOS. Thermally-generated carriers in the depletion layer become accelerated by the potential difference of the junction's depletion layer. Thus, a "leakage" current occurs from the drain to the body. As the drain voltage increases, thermally-generated carriers become accelerated by a larger potential difference, thereby increasing the current. This relationship can be somewhat accurately modeled by the ideal (or Shockley) diode equation:

$$I_{DB} = I_S(e^{\frac{V_{DB}}{V_T}} - 1) \tag{1}$$

Here, I_{DB} is the current that flows from the drain to the body of the MOSFET. I_S is the reverse saturation current, which is approximately 10fA. V_{DB} is the voltage between the drain and the body. $V_T = \frac{k_B T}{q}$ is the diode's thermal voltage. For $V_{DB} << -V_T$, $I_{DB} \approx -I_S$, which explains why the curve is constant for large V_{DS}. Note that $V_{DS} = V_D - V_S = V_D - V_B = V_{DB}$.

The definition of g_{ds} requires that the transistor be in saturation. However, if a small signal is to be applied at the MOSFET's gate, one would expect $g_{ds} = 0$ since the channel cannot conduct any current. Plotting $\frac{\partial I_D}{\partial V_{DS}}$, labeled g_{ds} in figure (2), $g_{ds} = 0$ at $V_{DS} = 3.5$V, the particular voltage of interest, consistent with intuition.

V_{GS} is now increased to 2.5V. In the triode region, I_D depends on $-V_{DS}^2$ because $I_D = k_n(V_{ov} - 0.5V_{DS})V_{DS}$. So, $\frac{\partial I_D}{\partial V_{DS}}$ depends linearly on $-V_{DS}$. In the saturation region, $\frac{\partial I_D}{\partial V_{DS}}$ is constant with V_{DS}. Therefore, the transition point between a linear curve and a constant curve marks the transition from saturation to triode, whose intervals are labeled in figure (3).

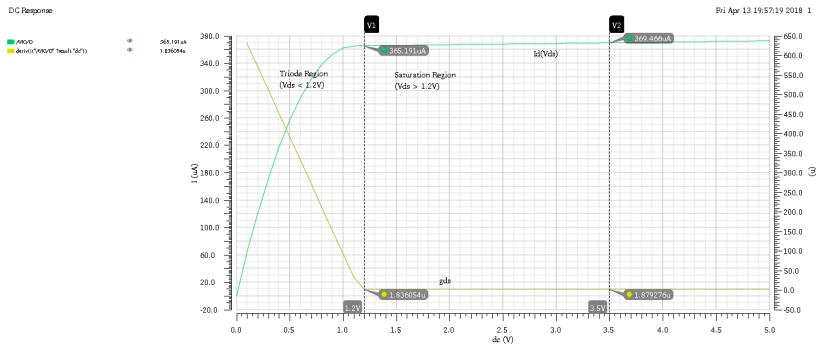

Figure 3: NMOS I_D versus V_{DS} when $V_{GS} = 2.5$V

Here, g_{ds} can be properly evaluated since the transistor is analyzed at $V_{DS} = 3.5$V, which occurs in the saturation region.

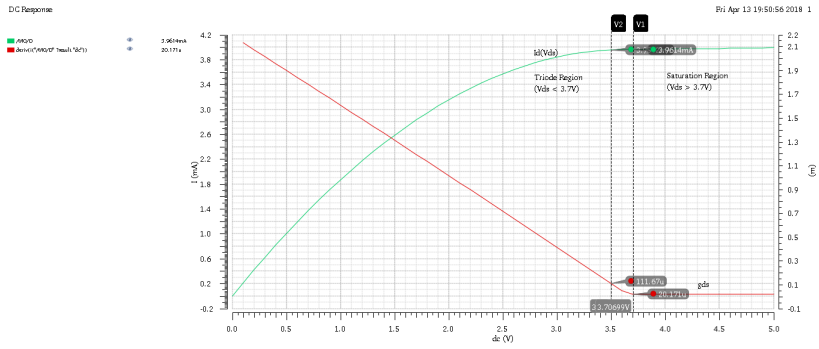

Figure 4: NMOS I_D versus V_{DS} when $V_{GS} = 5.0$V

The simulation results for $V_{GS} = 5.0$V are shown in figure (4). The transistor operates in the triode region at $V_{DS} = 3.5$V, but the same definition is applied nonetheless. The final results are tabulated in table (1).

Table 1: Simulation 2 Results

Vgs [V]	gds from Simulation Curves [uA / V]	gds from DC Operating Point Simulation [mA / V]
0	0	0
2.5	1.88	1.88
5.0	111.67	81.19