A common source NMOS amplifier is constructed for dc and small signal analysis.

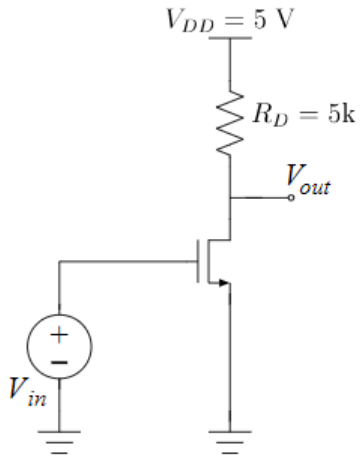

Figure 1: Circuit 2

V_{in} or V_{GS} is swept from 0 V to 3 V in increments of 0.1 V and V_{out} or V_{DS} is measured at each point. This range was chosen in order to capture the full range of the saturation operating mode and the transition from saturation to triode mode of the NMOS in the VTC. The results are plotted and tabulated below.

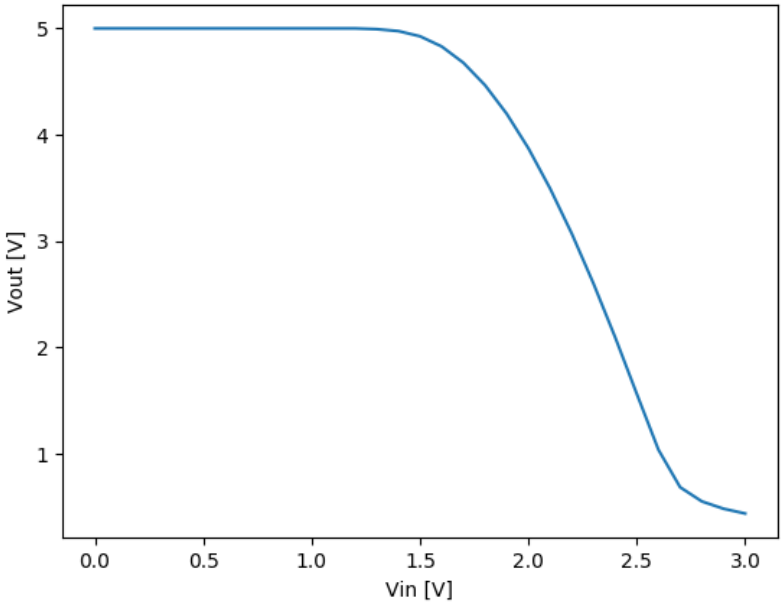

Figure 2: VTC of Common Source NMOS Amplifier

Table 1: Figure (2) Data

Vin [V]	Vout [V]
0.0	5.000
0.1	5.000
0.2	5.000
0.3	5.000
0.4	5.000
0.5	5.000
0.6	5.000
0.7	5.000
0.8	5.000
0.9	5.000
1.0	5.000
1.1	5.000
1.2	5.000
1.3	4.993
1.4	4.975
1.5	4.926
1.6	4.830
1.7	4.677
1.8	4.466
1.9	4.197
2.0	3.873
2.1	3.495
2.2	3.071
2.3	2.602
2.4	2.097
2.5	1.564
2.6	1.038
2.7	0.686
2.8	0.553
2.9	0.484
3.0	0.439

From the VTC in Figure (2), the NMOS begins and remains in cutoff until $V_{in} = 1.3$ V where V_{out} begins to dip below V_{DD}. The NMOS then enters the saturation region and remains there until the slope of the curve begins to decrease at around $V_{in} = 2.6$ V. Beyond that point, the NMOS operates in triode mode.

To find the dc voltage at the middle of saturation region $V_{in(eq2)}$, the average from the highest and lowest V_{out} value in the VTC is calculated. Then, and the closest value of V_{in} that corresponds to the the calculated average is the value taken for $V_{in(eq2)}$.

$$\frac{5V + 0.439V}{2} = 2.720V \approx V_{out} = 2.602V \Rightarrow Vin(eq2) = 2.3V \tag{1}$$

Then circuit is then biased at the $Vin(eq2)$ found above and a sine wave with 10 mV amplitude and 1 MHz is applied at the input. Note, for the measurement taken at 1 MHz, a 30 mV amplitude is used for the input sine wave because the original 10 mV amplitude is too weak and yielded a heavily distorted output signal that is immeasureable with the oscilloscope.

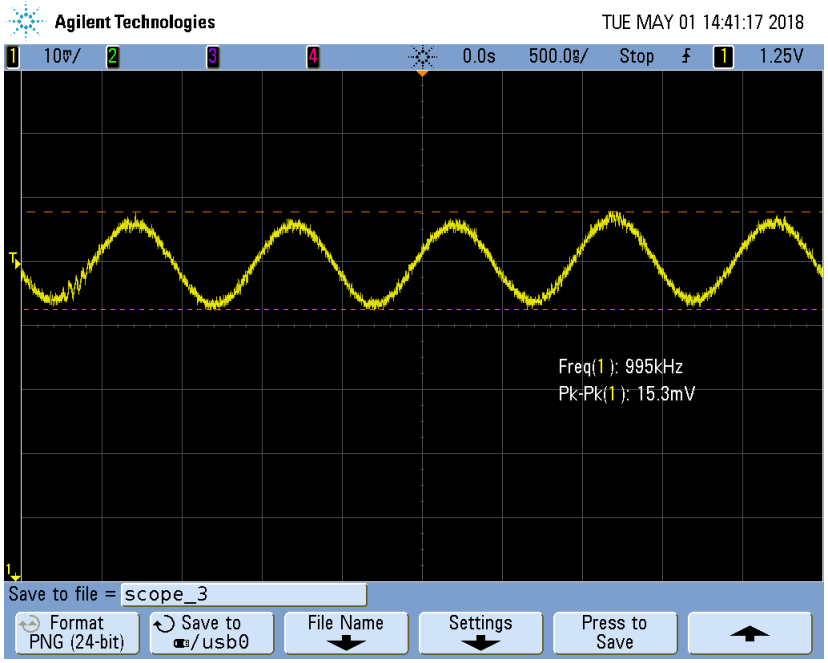

Figure 3: Output Voltage Sine Wave, 1 MHz

This experiment is repeated with sine waves with varying frequencies.

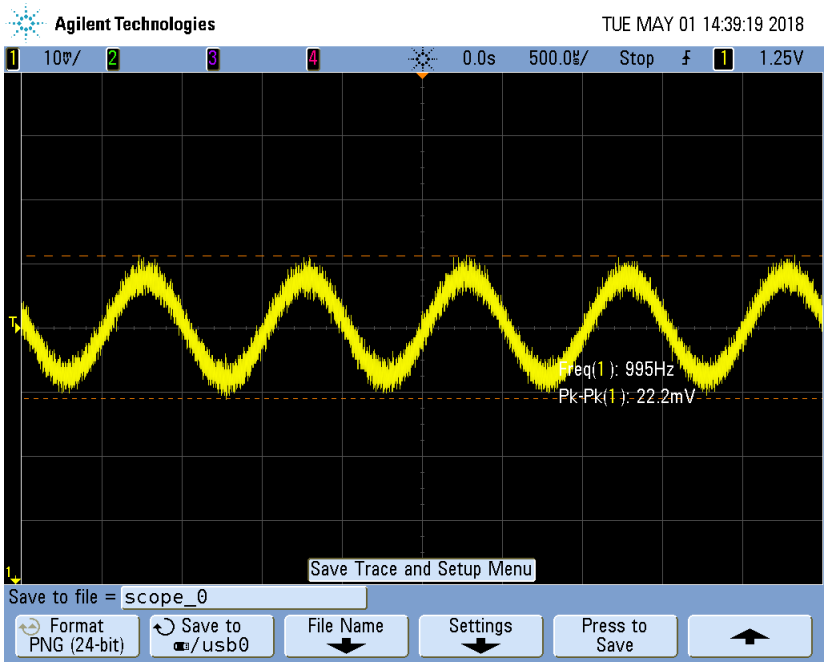

Figure 4: Output Voltage Sine Wave, 1 kHz

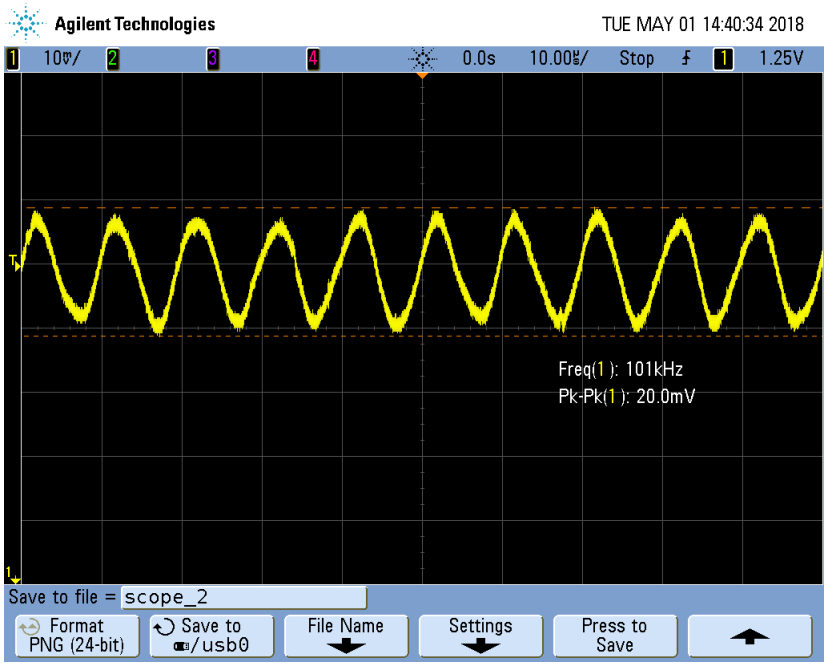

Figure 5: Output Voltage Sine Wave, 100 kHz

The amplitude of the output sine wave is measured for each input sine wave. From the output amplitudes, the small signal gain in dB is found for each frequency.

Table 2: Gain of Common Source Amplifier

Frequency [kHz]	Gain [V/V]
1	-6.5
100	-5.0
1000	-1.2

The small signal gain is observed to decrease as the frequency increases. This is expected because capacitances in the NMOS cause the circuit to effectively behave like a highpass filter.

The dc bias of the circuit is then increased by 10 mV and the experiment is repeated.

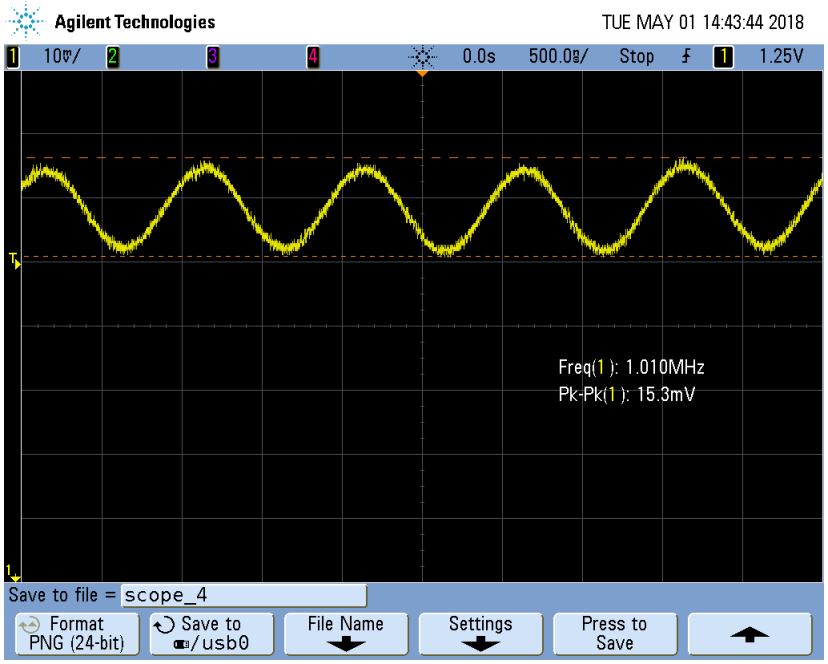

Figure 6: Output Voltage Sine Wave, 1 MHz, Increased dc Bias

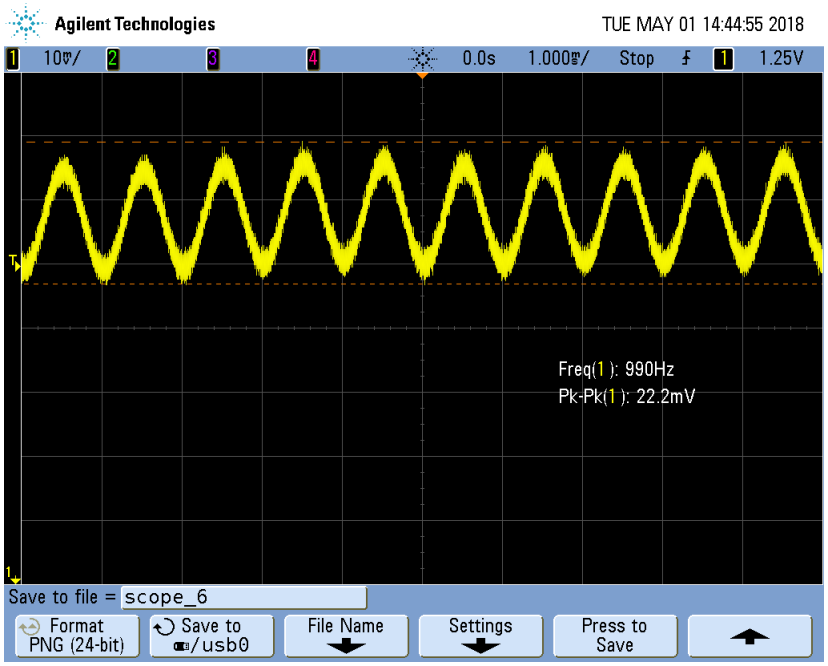

Figure 7: Output Voltage Sine Wave, 1 kHz, Increased dc Bias

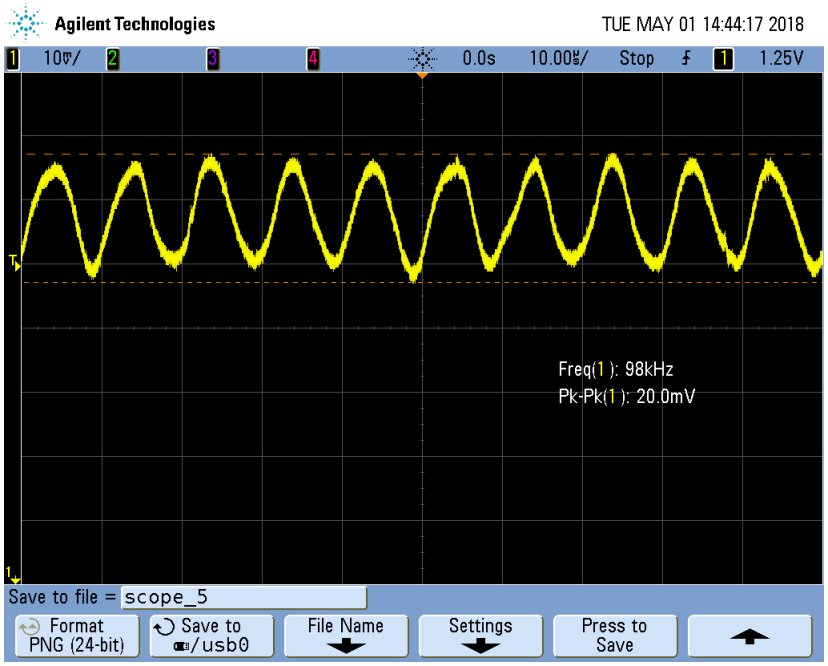

Figure 8: Output Voltage Sine Wave, 100 kHz, Increased dc Bias

The small signal gain values found are tabulated below.

Table 3: Gain of Common Source Amplifier with 10 mV Higher Bias

Frequency [kHz]	Gain [V/V]
1	-6.5
100	-5.0
1000	-1.2

As expected, the new gain values are slightly higher than the values found for the original dc bias. This is because in saturation mode, V_{out} is directly proportional to the drain current, which is directly proportional to the square of V_{in}. This means that as V_{in} increases in the saturation region, the slope of the VTC, another definition for the small signal gain, will increase as well.