Measurement Lab #1

EECS 170LC

April 23, 2018

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1 Introduction

1.1 Introduction

In this lab we use the CD4007 MOSFET transistor set to test NMOS and PMOS current-voltage relationships as seen in our previous simulations. With these I-V characteristics we can estimate transistor parameters such as W/L and Vt.

2 Part 1

The following circuit is contructed for dc analysis.

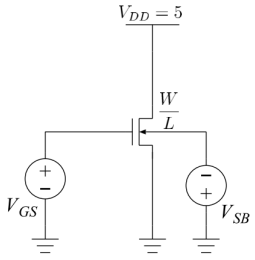

Figure 1: Circuit 1

V_{GS} is swept from 0 V to 5 V in increments of 0.2 V and i_D is measured at each value of V_{GS}. The results are plotted and tabulated below.

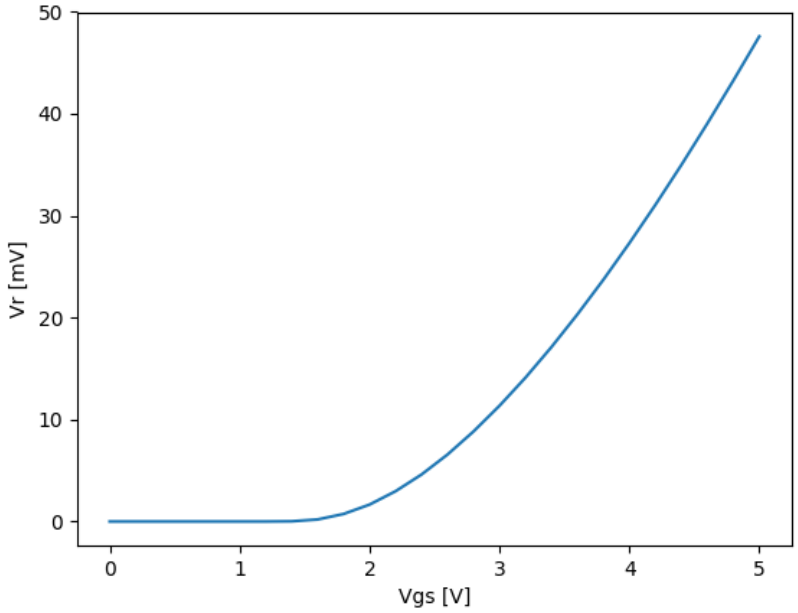

Figure 2: i_D versus V_{GS} of NMOS where $V_{SB} = 0$V

Table 1: Figure (2) Data

Vgs [V]	Id [mA]
0.0	0.00
0.2	0.00
0.4	0.00
0.6	0.00
0.8	0.00
1.0	0.00
1.2	0.00
1.4	0.00
1.6	0.02
1.8	0.08
2.0	0.17
2.2	0.31
2.4	0.48
2.6	0.68
2.8	0.91
3.0	1.17
3.2	1.46
3.4	1.77
3.6	2.10
3.8	2.45
4.0	2.82
4.2	3.21
4.4	3.62
4.6	4.04
4.8	4.47
5.0	4.92

When a gate voltage V_{GS} is applied to the NMOS, an electric field is generated across the metal gate and p-type substrate. This electric field repels majority holes from the surface of the substrate, creating a depletion region. The NMOS operates in cutoff region for V_{GS} between 0 V to about 1.5 V.

When V_{GS} exceeds 1.5 V, donor electrons move to the surface of the substrate to form an n-type channel between the drain and source of the NMOS. This voltage is the threshold voltage V_{tn}. At this point, the NMOS is operating in saturation region because the saturation condition, $V_{DS} > V_{GS} - V_{tn}$ is met. This is clear, as $V_{DS} = V_D - V_S = V_{DD} - 0 = 5$ V and V_{GS} never exceeds 5 V. In saturation mode, the drain current is observed to quadratically increase as the gate voltage increases. This is consistant with the drain current equation for NMOS in saturation, $i_D = \frac{1}{2}k'_n\frac{W}{L}(V_{GS} - V_{tn})^2$.

Then, V_{SB} is set to 5 V so a negative voltage is applied to the bulk of the NMOS, and the experiment is repeated. The results are plotted and tabulated below.

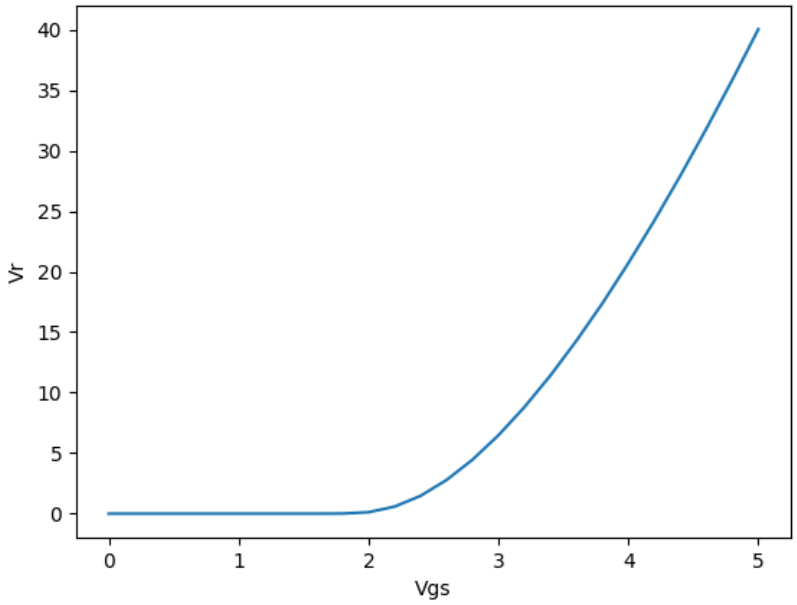

Figure 3: i_D versus V_{GS} of NMOS where $V_{SB} = 0.5$V

Table 2: Figure (3) Data

Vgs [V]	Id [mA]
0.0	0.00
0.2	0.00
0.4	0.00
0.6	0.00
0.8	0.00
1.0	0.00
1.2	0.00
1.4	0.00
1.6	0.00
1.8	0.00
2.0	0.01
2.2	0.06
2.4	0.15
2.6	0.29
2.8	0.46
3.0	0.67
3.2	0.91
3.4	1.18
3.6	1.48
3.8	1.80
4.0	2.14
4.2	2.50
4.4	2.89
4.6	3.29
4.8	3.71
5.0	4.14

The negative voltage applied to the bulk of the NMOS causes the depletion region between the heavily doped n-type drain/source and the p-type substrate to widen. The wider depletion region impedes the formation of the n-type channel and the gate voltage must be increased to compensate. This effectively increases the threshold voltage of the NMOS. This also agrees with the Shichman-Hodges model for the body effect of MOSFETs, $V_{tn} = V_{to} + \gamma(\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f})$ where V_{to} is the threshold voltage when no voltage is applied to the body, γ is the body effect parameter and ϕ_f is the bulk potential of the MOSFET. In this experiment, the threshold voltage V_{tn} increased from 1.5 V to about 1.9 V.

Refer to Part 3 for $\frac{W}{L}$ ratio of the NMOS.

3 Part 2

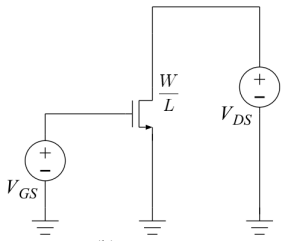

Figure 4: Circuit 2

Using the same circuit as before, i_D was measured while sweeping V_{DS} for $V_{GS} = 2.5$V and then 5.0V and keeping $V_{SB} = 0$V. Results are shown in Figure 2a and 2b.

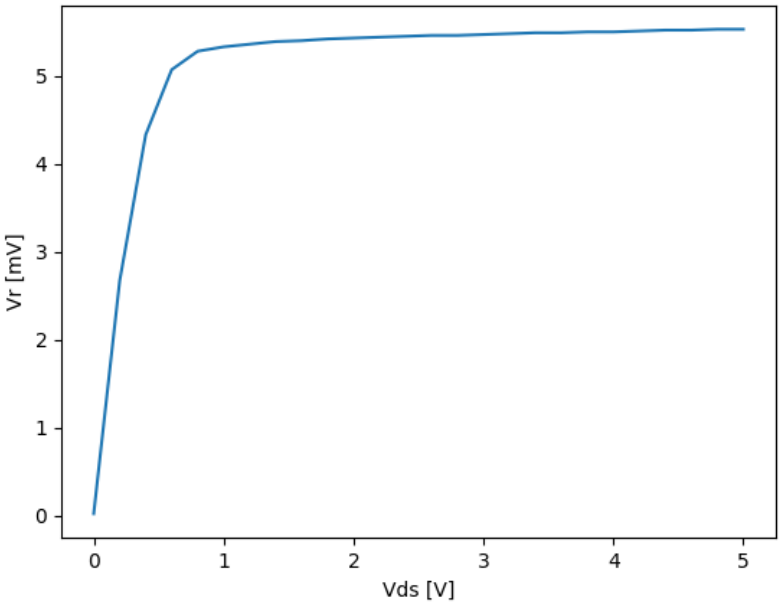

Figure 5: i_D versus V_{DS} of NMOS where $V_{GS} = 2.5$V

Table 3: Figure (**??**) Data

Vds [V]	Id [mA]
0.0	0.00
0.2	0.28
0.4	0.45
0.6	0.52
0.8	0.55
1.0	0.55
1.2	0.55
1.4	0.56
1.6	0.56
1.8	0.56
2.0	0.56
2.2	0.56
2.4	0.56
2.6	0.56
2.8	0.56
3.0	0.57
3.2	0.57
3.4	0.57
3.6	0.57
3.8	0.57
4.0	0.57
4.2	0.57
4.4	0.57
4.6	0.57
4.8	0.57
5.0	0.57

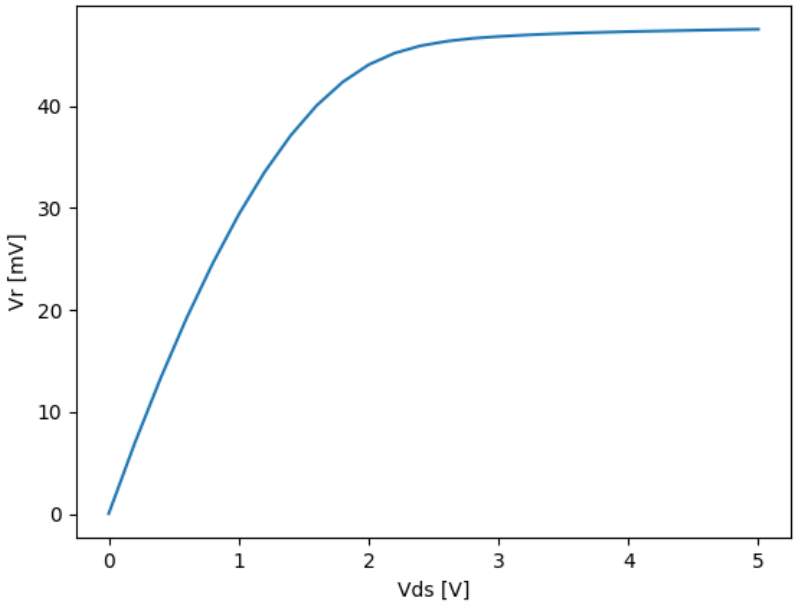

Figure 6: i_D versus V_{DS} of NMOS where $V_{GS} = 5$V

Table 4: Figure (6) Data

Vds [V]	Id [mA]
0.0	0.00
0.2	0.72
0.4	1.38
0.6	1.99
0.8	2.54
1.0	3.04
1.2	3.47
1.4	3.84
1.6	4.14
1.8	4.38
2.0	4.55
2.2	4.67
2.4	4.75
2.6	4.79
2.8	4.82
3.0	4.84
3.2	4.86
3.4	4.87
3.6	4.88
3.8	4.88
4.0	4.89
4.2	4.90
4.4	4.90
4.6	4.91
4.8	4.91
5.0	4.91

In both cases of V_{GS}, the transistor saturates near the value of $V_{GS} - V_{tn}$. For $V_{GS} = 2.5$V, this value is about 0.8V, and for $V_{GS} = 5.0$V, saturation occurs at around 3V This suggests that V_{tn} is around 1.8V, consistent with what was found in part 1.

4 Part 3

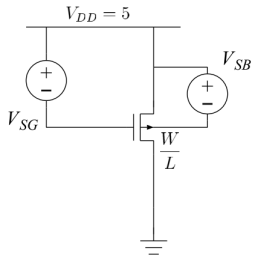

Figure 7: Circuit 3

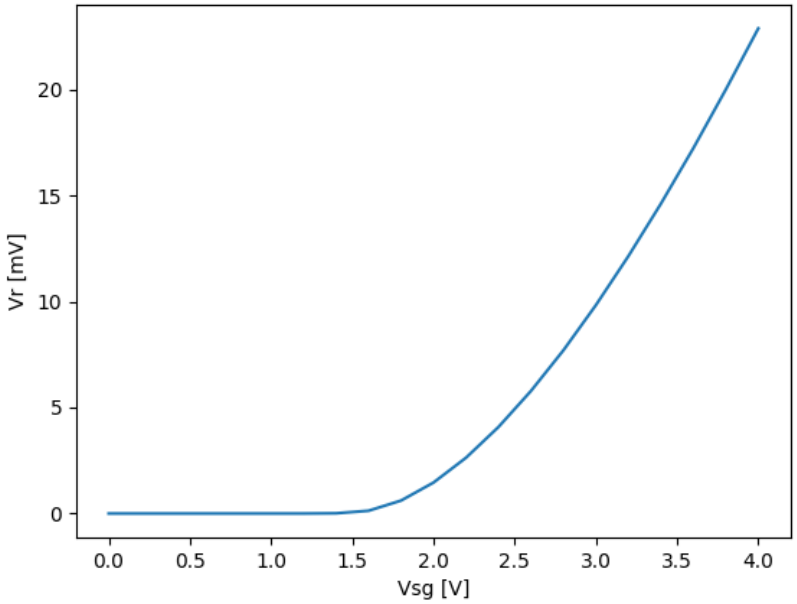

Figure 8: i_D versus V_{SG} of PMOS where $V_{SB} = 0$V

Table 5: Figure (8) Data

Vsg [V]	Id [mA]
0.0	0.00
0.2	0.00
0.4	0.00
0.6	0.00
0.8	0.00
1.0	0.00
1.2	0.00
1.4	0.00
1.6	0.01
1.8	0.06
2.0	0.15
2.2	0.27
2.4	0.42
2.6	0.60
2.8	0.80
3.0	1.02
3.2	1.26
3.4	1.51
3.6	1.78
3.8	2.07
4.0	2.36

As V_{SG} is increased, electrons are repelled from the channel beneath the gate of the PMOS. This exposes a depletion layer in the channel. Once V_{SG} hits the threshold voltage $|V_{tp}|$, for which $|V_{tp}| \approx 1.5$V in this case, holes are ripped from the positively-charged donor ions in n-type substrate, and a p-type channel is formed.

The transistor exits cutoff past $|V_{tp}|$. If $V_{SD} > V_{SG} - |V_{tp}|$, then the transistor operates in the saturation region. The drain in this circuit is grounded. The source is set to supply, which is $V_{DD} = 5\text{V}$. Therefore, $V_{SD} = 5\text{V}$. If $|V_{tp}| \geq 0$ by the definition of the absolute value of a real number. Therefore, so long as $V_{SG} < V_{SD} + |V_{tp}| \leq 5\text{V}$, the transistor stays in saturation. If V_{SG} is increased past about 4V, the current in the actual experiment becomes much too large to handle. As a result, the test cases are limited to $V_{SG} < 4\text{V}$. Thus, by design, the transistor exits cutoff and enters saturation, in which case the current grows with V_{SG}^2.

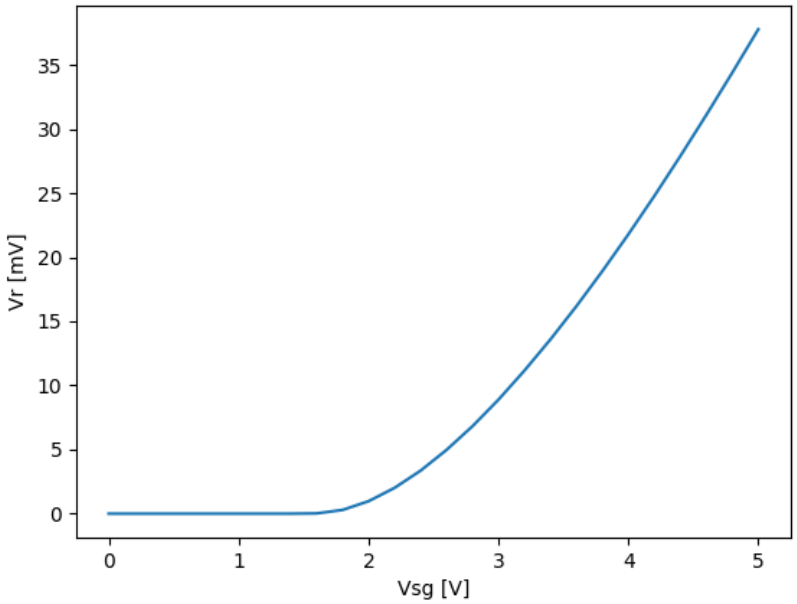

Figure 9: i_D versus V_{SG} of PMOS where $V_{SB} = 0.5\text{V}$

Table 6: Figure (9) Data

Vsg [V]	Id [mA]
0.0	0.00
0.2	0.00
0.4	0.00
0.6	0.00
0.8	0.00
1.0	0.00
1.2	0.00
1.4	0.00
1.6	0.00
1.8	0.03
2.0	0.10
2.2	0.21
2.4	0.35
2.6	0.51
2.8	0.71
3.0	0.92
3.2	1.15
3.4	1.41
3.6	1.67
3.8	1.96
4.0	2.25
4.2	2.56
4.4	2.88
4.6	3.22
4.8	3.56
5.0	3.91

When increasing the source-bulk voltage V_{SB}, the threshold voltage increases slightly to about 1.7V. In a very simplified model, two pn-junction diodes exist in a PMOS transistor. The first is between the source and the bulk. The other is between the drain and the bulk. Initially, the source and bulk voltages are both 5V relative to ground. In this situation, because the drain is grounded, a slight reverse saturation current occurs from the bulk to the drain, but no current flows from the source to the bulk. Now, drop the bulk voltage to 4.5V, so that $V_{SB} = 0.5$V, while still keeping the source at the supply voltage. The reverse saturation current in the drain-bulk diode drops slightly, meaning less current flows into the drain. Moreover, the current from the source to the bulk increases dramatically. As a result, current is drawn from the source, and less current flows into the drain. Therefore, less current flows through the channel. So, a higher V_{SG} is required to achieve the same current. Thus, the threshold voltage $|V_{tp}|$ must increase. The transistor exits cutoff around 1.6V this time. Therefore, in line with theory, the threshold voltage increased slightly with the increased V_{SB}, namely from about 1.5V to 1.7V.

The current in the saturation region for an NMOS transistor is approximately given by:

$$i_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_{tn})^2 \tag{1}$$

Rearranging the equation, the NMOS's $\frac{W}{L}$ ratio can be determined:

$$\frac{W}{L} = \frac{2i_D}{k'_n(V_{GS} - V_{tn})^2} \tag{2}$$

A similar result is obtained for the PMOS:

$$\frac{W}{L} = \frac{2i_D}{k'_p(V_{SG} - |V_{tp}|)^2} \tag{3}$$

So, if the various parameters on the right-side of either equation are known for different test cases, then $\frac{W}{L}$ can be calculated for different points, and the average can be taken for a good estimate of the true value. i_D and V_{SG} are trivial since those are essentially directly measured in the experiment. V_{tn} and $|V_{tp}|$ are given in the SPICE model of the CD4007 transistors, but they do not reflect what is observed in the actual transistors. However, from analyzing the measured data points, the threshold voltages can be easily obtained for the transistors in lab, and those are to be used. The threshold voltages are given in table (7):

Table 7: Measured Threshold Voltages for NMOS and PMOS

NMOS Threshold Voltage [V]	PMOS Threshold Voltage [V]
1.5	-1.5

The only unknown values are the process transconductance parameters k'_n and k'_p. It is difficult to decouple k'_n from $\frac{W}{L}$. The same applies to the PMOS values. So, the k'_n and k'_p values from the SPICE model are to be used.

Table 8: SPICE Model Process Transconductance Parameters for NMOS and PMOS

NMOS kn [mA / V2]	PMOS kp [mA / V2]
0.6	0.6

Using the data in tables (7) and (8) as well as equations (2) and (3), the $\frac{W}{L}$ ratios for each transistor can be approximated.

Table 9: $\frac{W}{L}$ Ratios for NMOS and PMOS

W over L - NMOS	W over L - PMOS
2.019	1.740

5 Part 4

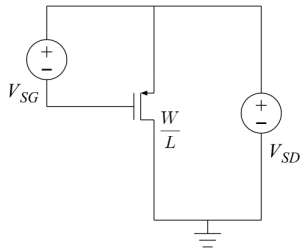

Figure 10: Circuit 4

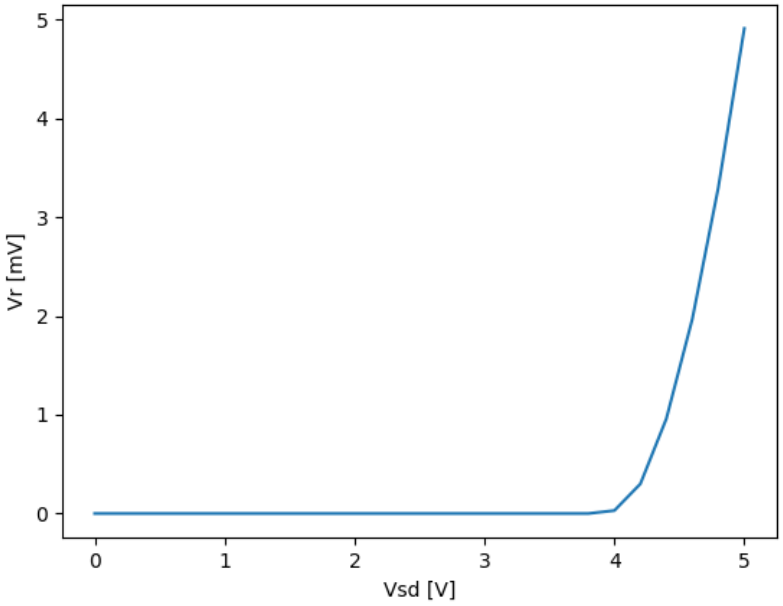

Figure 11: i_D versus V_{SD} for PMOS with $V_{SG} = 2.5$V

One would hope to acquire similar results in figure (11) for the PMOS as are obtained for the NMOS. However, the results are drastically different. Reliable data for the $V_{GS} = 5$V case could not be acquired.

6 Conclusion

6.1 Part 1

The NMOS exhibited normal i_D versus V_{GS} characteristics and applying a negative voltage to the bulk ($V_{SB} = 0.5$ V) effectively increased the threshold voltage V_{tn}, which is also the expected result. Overall, the NMOS performed well in this experiment and did not deviate from expected behavior.

6.2 Part 2

The i_D versus V_{DS} curves suggest that the transistor saturates near $V_{GS} - V_{tn}$ in each case. This is consistent with both theory and simulation results.

6.3 Part 3

The i_D versus V_{SG} characteristics of the PMOS are as expected. Furthermore, increasing V_{SB} increases $|V_{tp}|$, which is in line with theory. Enough informaton is available to determine the $\frac{W}{L}$ ratios for the transistors, which turn out to be 2.019 for the NMOS and 1.740 for the PMOS. However, this is probably not terribly accurate since k_n' and k_p' are taken from the SPICE model. The threshold voltage is considerably different from the SPICE model, so there is reason to believe that the k parameters are as well. These parameters should be determined through further experimentation before making a definitive statement about the $\frac{W}{L}$ ratio of the transistor.

6.4 Part 4

The i_D versus V_{SD} characteristics for the PMOS are not at all consistent with intuition nor theory. One possibility is that the CD4007 chips have been damaged due to short circuits or other practical considerations, leading to the bizarre characteristics that make it act as a diode with a very high forward voltage. However, this is a difficult argument to make since the i_D versus V_{SG} characteristics are in tact. The measurement equipment or the circuit used to perform this analysis are likely the culprit.