Lab 8 Final Project: Design of a D-Latch

EECS 170LB

March 19, 2018

Roman Parise (59611417)
Johnathan Fritsche (11106947)
Jason Wang (42873192)

Thursday 8:00am - 10:50am Section 18365

Lab TA: Dmitry Oshmarin

1 Introduction

A D-latch, a common component in digital logic used for storing bits for fast access later, is designed using a 90nm CMOS technology. The circuit is first prototyped at a transistor level and tested in a SPICE simulator. Once its behavior in this higher-level simulation is verified, the layout is designed in a layout editor. The circuit is then simulated in the layout editor for more realistic information on its performance after fabrication.

2 Procedure and Results

2.1 SPICE Simulation

An inverter with input A and output Q follows the following truth table:

Table 1: Inverter Truth Table

Input A	Output Q
0	1
1	0

The inverter can then be realized in CMOS technology. The width-to-length ratio of the inverter's NMOS shall be referred to as n and p for the PMOS.

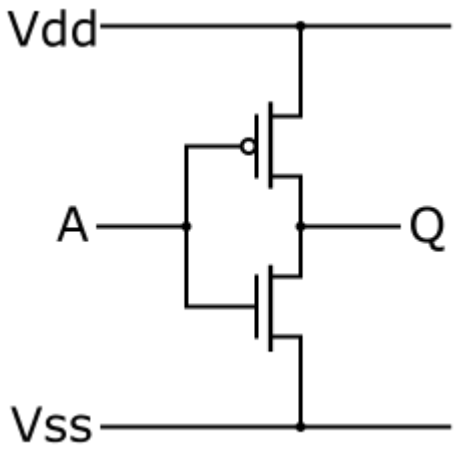

Figure 1: CMOS Inverter

Taken from link `https://en.wikipedia.org/wiki/CMOS#/media/File:CMOS_Inverter.svg`

A NAND gate with inputs A and B and output C has a truth table given by:

Table 2: NAND Truth Table

Input A	Input B	Output C
0	0	1
0	1	1
1	0	1
1	1	0

The NAND gate can be implemented in CMOS like so:

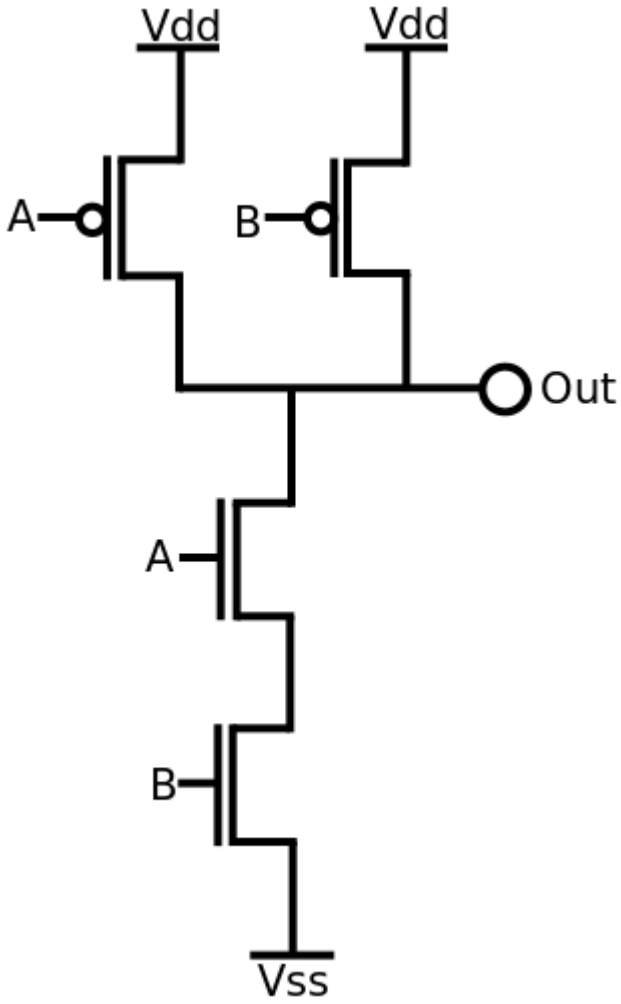

Figure 2: CMOS NAND Gate

Taken from link `https://upload.wikimedia.org/wikipedia/commons/e/e2/CMOS_NAND.`

svg

Here, the width-to-length ratio of the NMOSs is $2n$ to compensate for the fact that the current driven from ground is halved in this series configuration. The width-to-length ratio of the PMOSs is still p since this issue does not occur with the parallel PMOSs.

The D-latch circuit is built using a CMOS inverter and four NAND gates, using two PMOS and two NMOS transistors each. The gate-level design is given in the figure below:

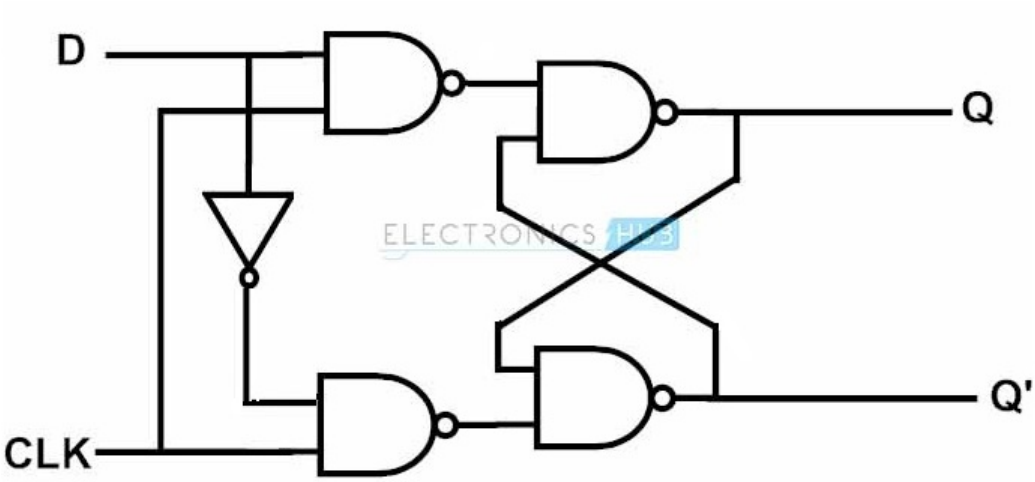

Figure 3: D-Latch Gate Level Schematic

Taken from link `https://www.electronicshub.org/d-flip-flop/`

The circuit is shown in figure (4).

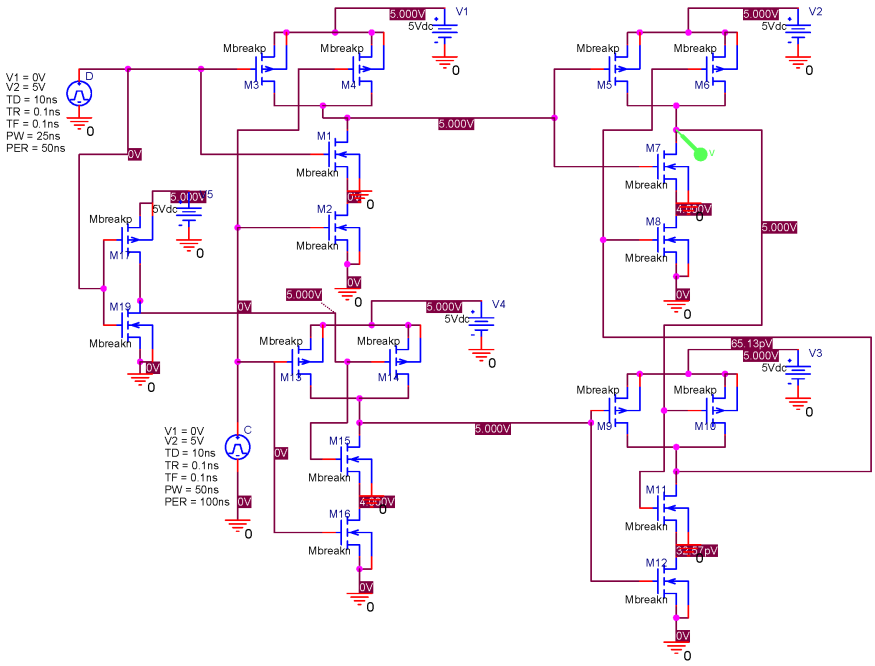

Figure 4: The D-Latch Circuit Model for PSpice Simulation

When the control input, C, is high, the value of the input, D, is stored as the output value. However, when the control input is low, the value of the output cannot be changed. For example, if D is high and C high, the output Q is high, but if C is set to low, then the value of D before the change is stored as the output value Q until C is brought high again. The behavior of the D-Latch is shown in the FSM in figure (13).

The results of all the simulations are consistent with the assumed behavior of the D-Latch circuit. In figure (6), it is shown that when the control input C is high the value of input D is stored at the output Q, and when the control input C is low the value of D is not passed to the output Q. For this simulation, the settings in figure (5) are used for the inputs. These values are supplied in the lab specification document.

There is a small spike that occurs when D is becoming high while C is becoming low. When this switch occurs, the bottom NAND gate of the SR latch portion of the design has one of its inputs change from 0 to 1. The NAND gate includes two NMOSs in series. When both inputs are 0, the NMOSs act as open circuits, which are similar to two capacitors in series at DC. When one of the inputs goes to 1, one of the NMOSs turns on. For a brief period of time, only one of the NMOSs is now an open circuit, whereas the other allows current to flow. Assuming both NMOSs have the same effective "capacitance" when they

are both off, the effective "capacitance" of the open circuit in the pull-down network doubles. So, for a brief instant, current is drawn from supply and from the load capacitance connected to the output of the NAND gate. This briefly pulls down the NAND gate's output, which is enough to send a brief 0 pulse to the top latch, briefly setting Q to 1. These effects quickly die out as the other NMOS becomes fully charged and acts as a pure open circuit again. The values then return to the expected behavior. However, this hypothesis is difficult to determine without further experimentation.

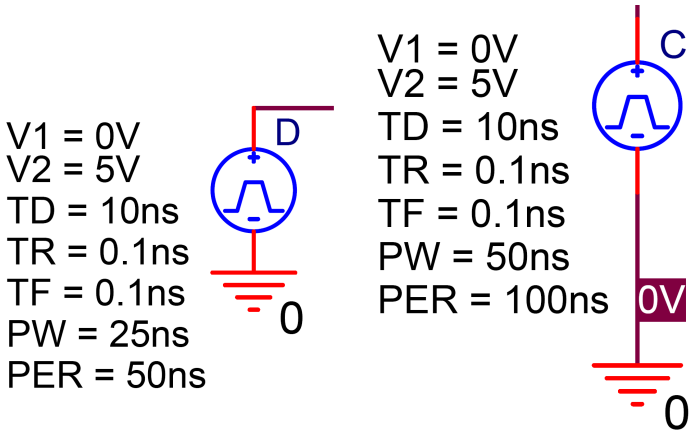

Figure 5: The Simulated Input (Left) and the Simulated Control Input

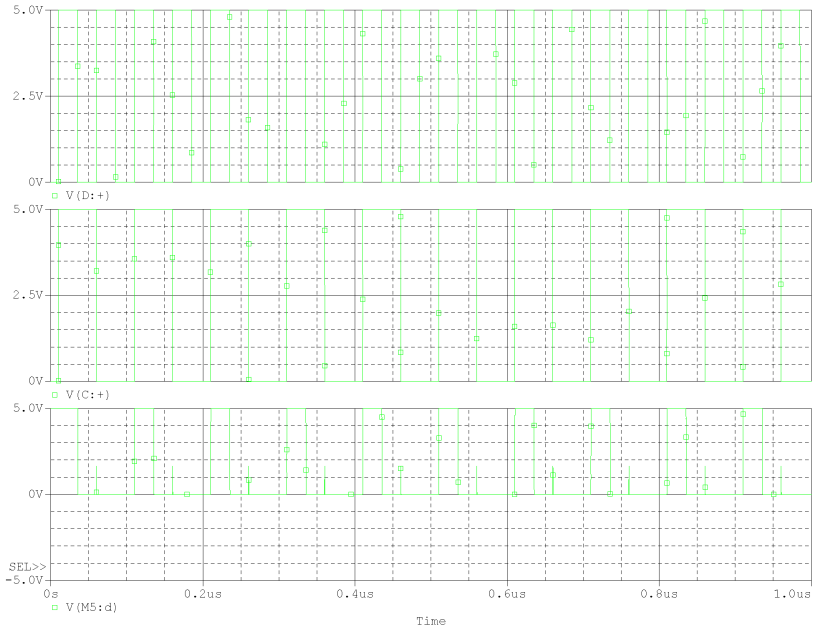

Figure 6: Simulation Results of D-Latch Using Inputs from Figure (5)

2.2 Microwind Layout

A CMOS inverter and CMOS logic NAND gate is constructed to be used in the D Latch layout design.

The width and length of the NMOS to be used in the inverter is given to be 0.5 µm and 0.1 µm, respectively. The PMOS to be used in the inverter is then designed so that the inverter is matched (steepest slope of the VTC curve occurs when $V_{out} = V_{in} = \frac{V_{DD}}{2}$). The CMOS inverter is matched using a PMOS with a width $W = 1.2$ µm and a length $L = 0.1$ µm. This results in the following layout for the CMOS inverter.

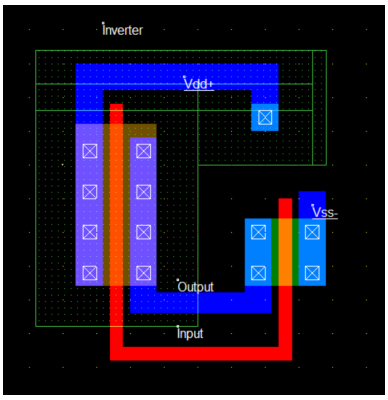

Figure 7: CMOS Inverter Layout

The VTC of the CMOS inverter shown below verifies that it is matched.

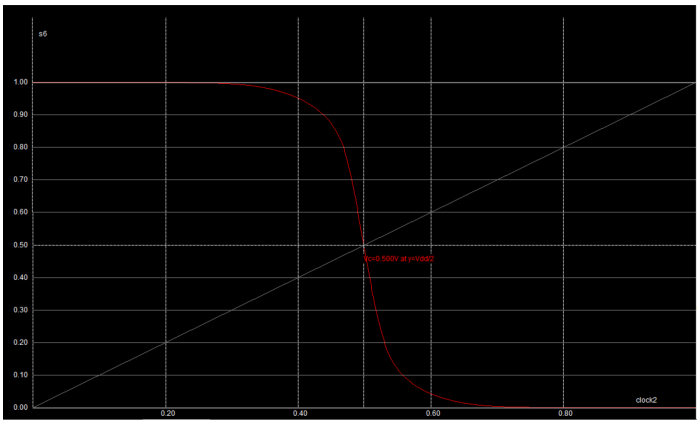

Figure 8: VTC of CMOS Inverter Layout

The logic of the CMOS inverter is verified using a 250 MHz clock input with a rise and fall time of 0.050 ns.

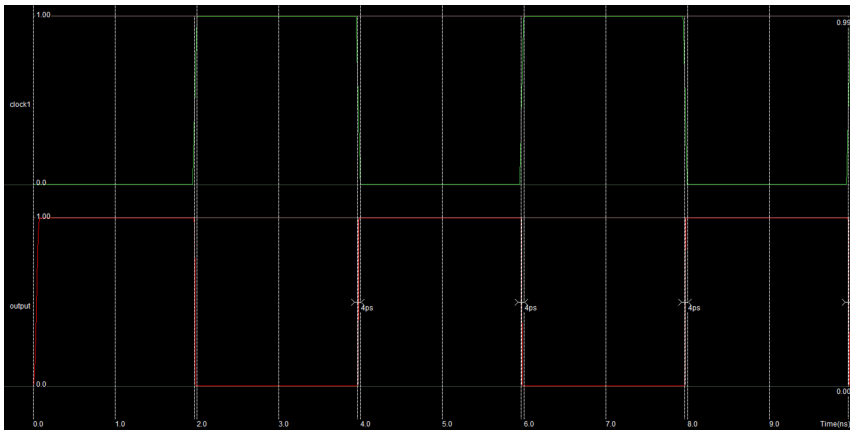

Figure 9: CMOS Inverter Logic Test

Next, a CMOS logic NAND gate is constructed with two PMOS in parallel and two NMOS in series. The NAND gate is designed so that it operates with the same speed of the CMOS inverter. To achieve this design goal, the width of both NMOS are doubled to $W = 1.0$ µm so that it operates twice as fast to compensate for the speed lost due to having two NMOS connected in series. This results in the following layout for the NAND gate.

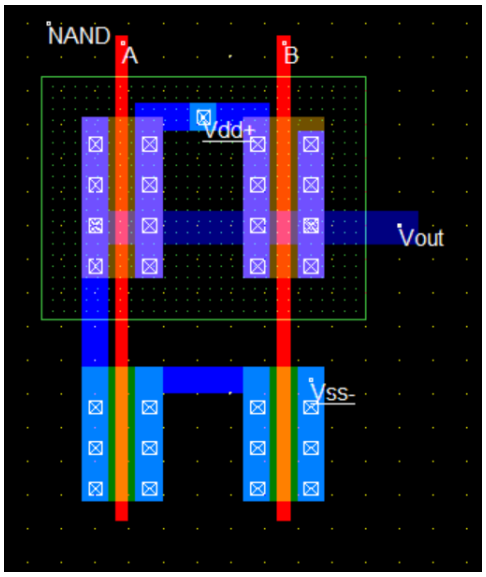

Figure 10: NAND Gate Layout

The logic of the NAND gate verified using a 250 MHz clock input and a 125

MHz clock input with rise and fall times of 0.050 ns.

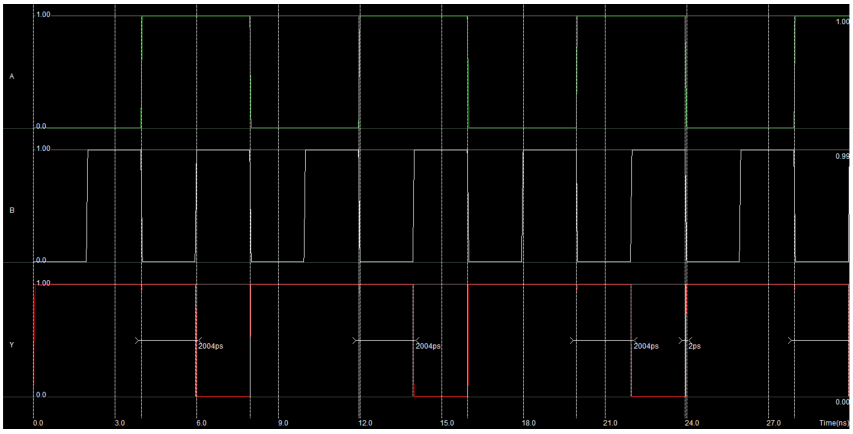

Figure 11: NAND Gate Logic Test

Using the CMOS inverter and NAND gate designed above, the following D Latch layout is constructed.

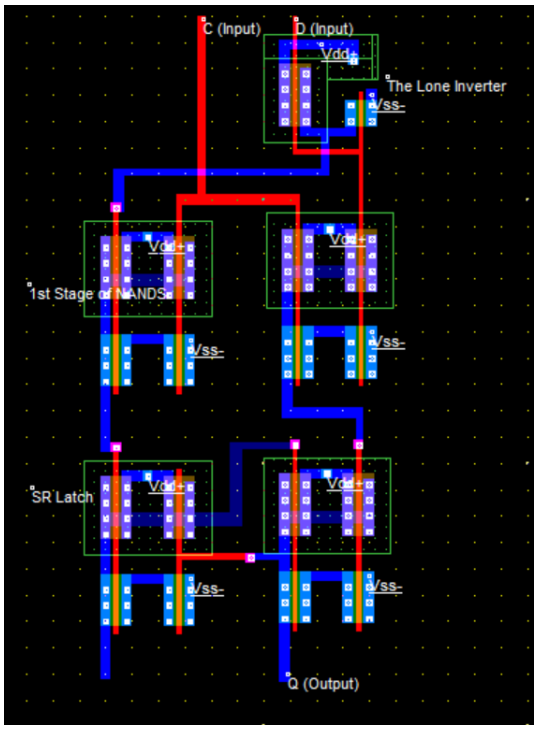

Figure 12: D Latch Layout

The expected behavior of the D Latch can be expressed in the following truth table.

Table 3: Logic Chart of D Latch Circuit

C	D	Q_{prev}	Q
0	0	0	0
0	1	0	0
1	0	0	0
1	1	0	1
0	0	1	1
0	1	1	1
1	0	1	0
1	1	1	1

The truth table above translates to the the following finite state machine (FSM).

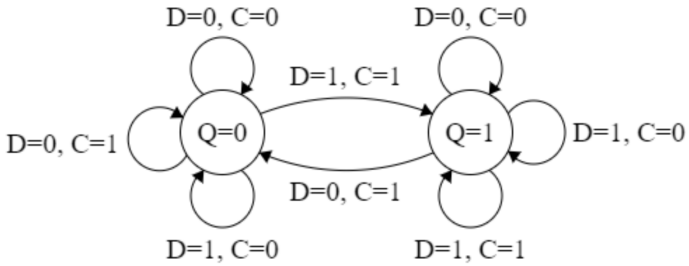

Figure 13: D Latch FSM

The delays for the transitions between Q high and Q low (τ_{PHL}) and vice versa (τ_{PLH}) can be used to determine the maximum operating frequency of the D Latch.

The D Latch is tested with input clock C at 250 MHz, 1 GHz, and 4 GHz with clock D always set to half the frequency of C. Rise and fall times of 0.050 ns and 0.001 ns are tested for each clock frequency.

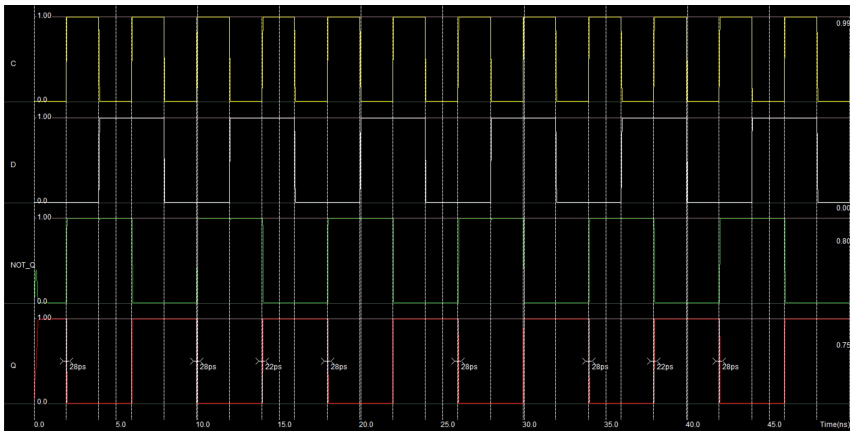

Figure 14: Test Case 1 - $f_C = 250$ MHz, Rise/Fall Time = 0.050 ns

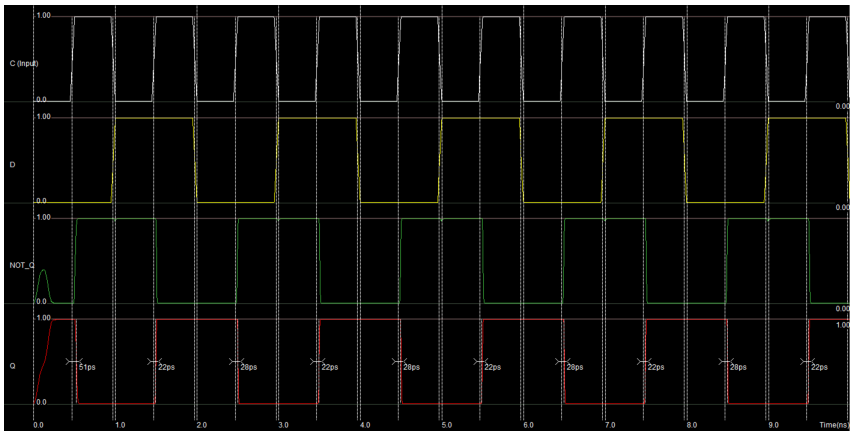

Figure 15: Test Case 2 - $f_C = 1$ GHz, Rise/Fall Time = 0.050 ns

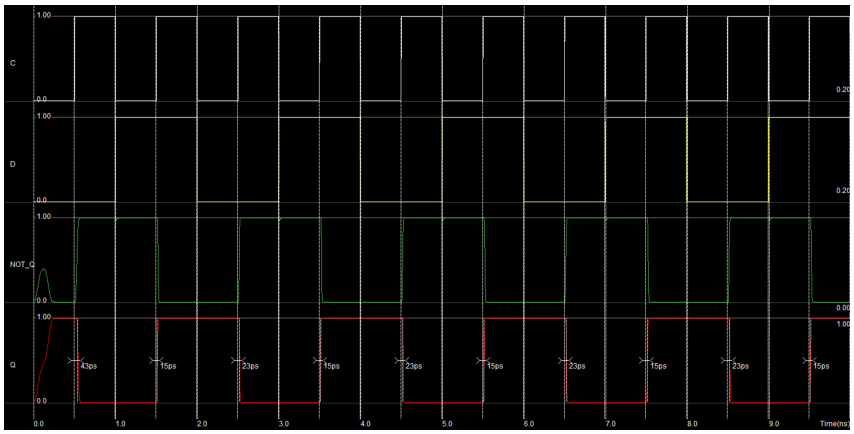

Figure 16: Test Case 3 - $f_C = 1$ GHz, Rise/Fall Time = 0.001 ns

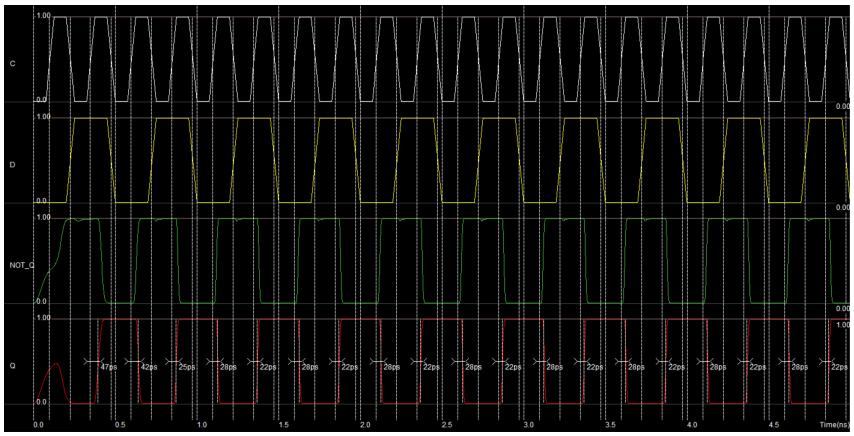

Figure 17: Test Case 4 - $f_C = 4$ GHz, Rise/Fall Time = 0.050 ns

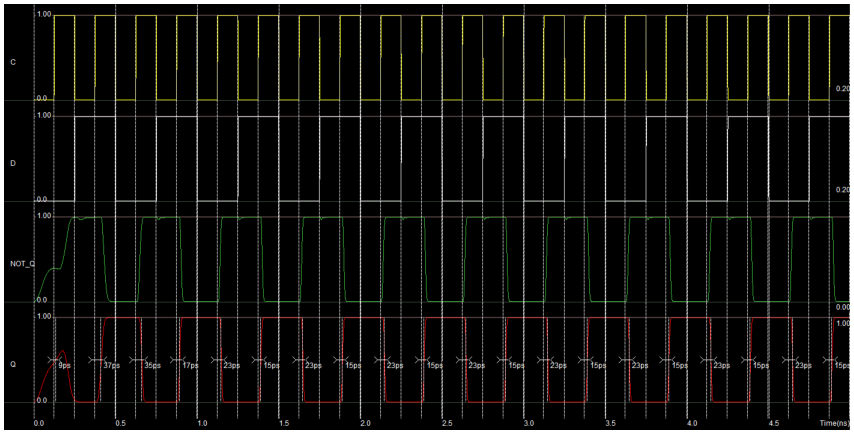

Figure 18: Test Case 5 - $f_C = 4$ GHz, Rise/Fall Time = 0.001 ns

The following delays and average power dissipation values are found.

Table 4: D Latch Layout Test Results

fC [GHz]	fD	Rise/Fall Time [ns]	tPHL of Q [ps]	tPLH of Q [ps]	Average Power [uW]
0.25	0.125	0.050	28	22	4.340
1	0.5	0.050	28	22	16.218
1	0.5	0.001	23	15	14.240
4	2	0.050	28	22	58.177
4	2	0.001	23	15	52.991

It is observed that the delay of the D Latch is only dependent on the rise and fall times of the input clocks. This behavior is expected because the dynamic

portions of the inputs are kept constant, and the length of the static portions of the input should not affect the performance of the circuit as long as they are longer than the delays.

Rise and fall times of the input signals affect the propagation delays. So, in order to discuss critical path delays and other timing metrics, rise and fall times need to be fixed so that those figures are meaningful. Otherwise, one could simply change the rise and fall times of the input signals and argue that certain circuits operate differently from or better than other circuits. So, the standard used herein for measuring propagation delays is when the rise and fall times are smallest at 0.001 ns.

A propagation delay only technically matters when the output transitions from one state to another. When the rise and fall times of the input clocks are 0.001 ns, the output delays are given by $\tau_{PHL} = 23$ ps and $\tau_{PLH} = 15$ ps. The FSM for the latch contains only two transitions whose delays would be measurable, when $C = 1$, $D = 1$, and $Q = 0$ and when $C = 1$, $D = 0$, and $Q = 1$. The former corresponds to τ_{PLH} since Q transitions from 0 to 1 before the state change occurs, and the latter therefore corresponds to τ_{PHL}. The longer of the two delays is $\tau_{PHL} = 23$ ps. This makes sense since the critical path delay should run through the inverter, and the inverter switching states is what causes the output to change.

So, the propagation delay is given by $\tau_P = \frac{\tau_{PHL}+\tau_{PLH}}{2}$, which is 19 ps. So, the maximum switching frequency is given by $f_{max} = \frac{1}{2t_p} \approx 26.3$GHz.

The length of the D Latch layout is 12.650 µm and the width of the layout is 5.850 µm. The total area of the layout is $74\mu m^2$.

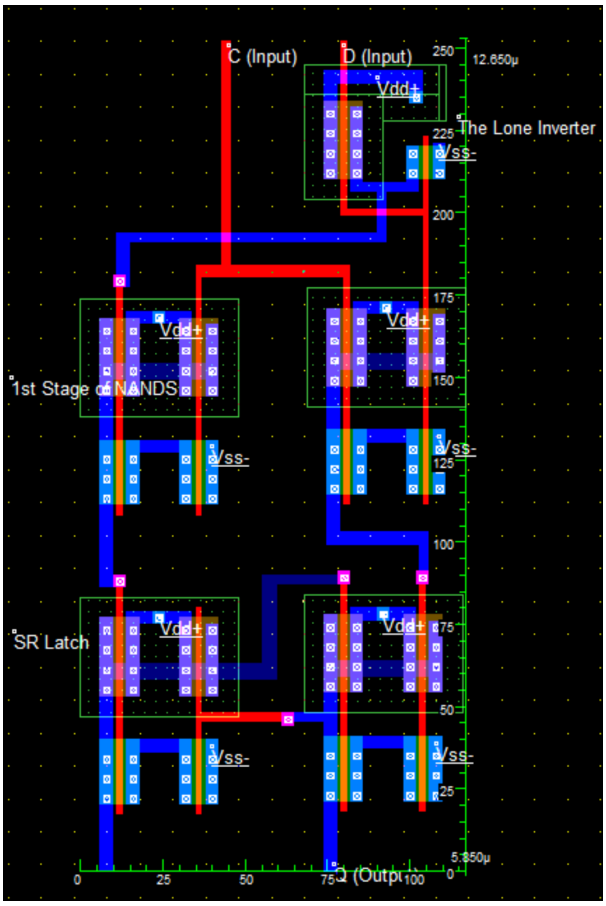

Figure 19: Total Area of D Latch Layout

Operating at 1 GHz, the average power consumption is determined to be 14.240 µW.

Table 5: Final Layout Characteristics

Maximum Switching Frequency [GHz]	26.3
Power Consumption at 1 GHz [uW]	14.240
Layout Area [um2]	74

The maximum switching frequency far exceeds the required 1GHz, the power consumption falls well below the required 100W, and the area is considerably smaller than the required $100m^2$. Therefore, the design satisfies the specification.

3 Conclusion

3.1 SPICE Simulation

The D-latch design satisfies its behavioral description. The only nonideality that occurs is the brief spiking behavior when D is switched to 1 and C is switched to 0. So long as a sufficient amount of time, likely on the order of picoseconds at most, is given to allow the circuit's values to stabilize, this should not be a major concern. The same transistor dimensions used in the SPICE simulation are used for the Microwind layout. In SPICE, no physical issues arise from the transistor dimensions, but a true layout provides a more realistic simulation of the circuit's behavior when fabricated.

3.2 Microwind Layout

The final D-latch design outperforms all aspects of the specification by a decent amount. However, the design can be made even better. The area can decreased substantially by consolidating many of the PMOS and NMOS transistors. For instance, the PMOSs in each NAND gate can be implemented using one p-diffusion region and two gates, sharing the same drain terminal, saving area on the chip. Furthermore, speed and area can be saved by using only inverters and transmission gates in the design. Signals would need to travel through fewer transistors, increasing speed and decreasing area.