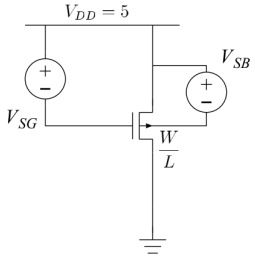

Figure 1: Circuit 3

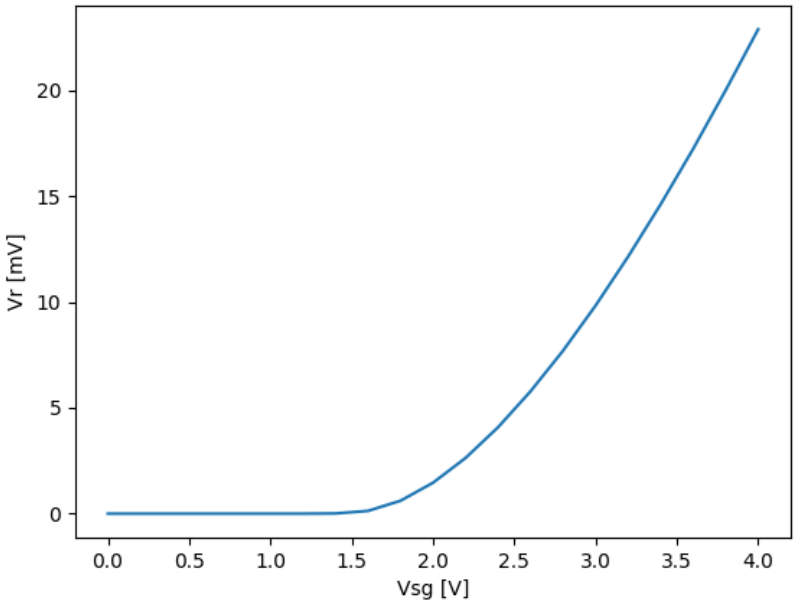

Figure 2: i_D versus V_{SG} of PMOS where $V_{SB} = 0$V

Table 1: Figure (2) Data

Vsg [V]	Id [mA]
0.0	0.00
0.2	0.00
0.4	0.00
0.6	0.00
0.8	0.00
1.0	0.00
1.2	0.00
1.4	0.00
1.6	0.01
1.8	0.06
2.0	0.15
2.2	0.27
2.4	0.42
2.6	0.60
2.8	0.80
3.0	1.02
3.2	1.26
3.4	1.51
3.6	1.78
3.8	2.07
4.0	2.36

As V_{SG} is increased, electrons are repelled from the channel beneath the gate of the PMOS. This exposes a depletion layer in the channel. Once V_{SG} hits the threshold voltage $|V_{tp}|$, for which $|V_{tp}| \approx 1.5$V in this case, holes are ripped from the positively-charged donor ions in n-type substrate, and a p-type channel is formed.

The transistor exits cutoff past $|V_{tp}|$. If $V_{SD} > V_{SG} - |V_{tp}|$, then the transistor operates in the saturation region. The drain in this circuit is grounded. The source is set to supply, which is $V_{DD} = 5$V. Therefore, $V_{SD} = 5$V. If $|V_{tp}| \geq 0$ by the definition of the absolute value of a real number. Therefore, so long as $V_{SG} < V_{SD} + |V_{tp}| \leq 5$V, the transistor stays in saturation. If V_{SG} is increased past about 4V, the current in the actual experiment becomes much too large to handle. As a result, the test cases are limited to $V_{SG} < 4$V. Thus, by design, the transistor exits cutoff and enters saturation, in which case the current grows with V_{SG}^2.

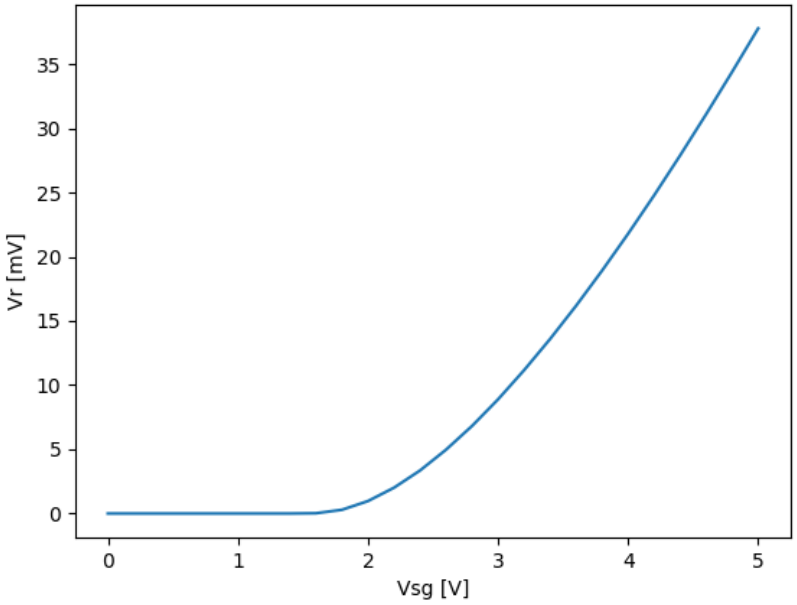

Figure 3: i_D versus V_{SG} of PMOS where $V_{SB} = 0.5$V

Table 2: Figure (3) Data

Vsg [V]	Id [mA]
0.0	0.00
0.2	0.00
0.4	0.00
0.6	0.00
0.8	0.00
1.0	0.00
1.2	0.00
1.4	0.00
1.6	0.00
1.8	0.03
2.0	0.10
2.2	0.21
2.4	0.35
2.6	0.51
2.8	0.71
3.0	0.92
3.2	1.15
3.4	1.41
3.6	1.67
3.8	1.96
4.0	2.25
4.2	2.56
4.4	2.88
4.6	3.22
4.8	3.56
5.0	3.91

When increasing the source-bulk voltage V_{SB}, the threshold voltage increases slightly to about 1.7V. In a very simplified model, two pn-junction diodes exist in a PMOS transistor. The first is between the source and the bulk. The other is between the drain and the bulk. Initially, the source and bulk voltages are both 5V relative to ground. In this situation, because the drain is grounded, a slight reverse saturation current occurs from the bulk to the drain, but no current flows from the source to the bulk. Now, drop the bulk voltage to 4.5V, so that $V_{SB} = 0.5$V, while still keeping the source at the supply voltage. The reverse saturation current in the drain-bulk diode drops slightly, meaning less current flows into the drain. Moreover, the current from the source to the bulk increases dramatically. As a result, current is drawn from the source, and less current flows into the drain. Therefore, less current flows through the channel. So, a higher V_{SG} is required to achieve the same current. Thus, the threshold voltage $|V_{tp}|$ must increase. The transistor exits cutoff around 1.6V this time. Therefore, in line with theory, the threshold voltage increased slightly with the increased V_{SB}, namely from about 1.5V to 1.7V.

The current in the saturation region for an NMOS transistor is approximately given by:

$$i_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_{tn})^2 \tag{1}$$

Rearranging the equation, the NMOS's $\frac{W}{L}$ ratio can be determined:

$$\frac{W}{L} = \frac{2i_D}{k'_n(V_{GS} - V_{tn})^2} \tag{2}$$

A similar result is obtained for the PMOS:

$$\frac{W}{L} = \frac{2i_D}{k'_p(V_{SG} - |V_{tp}|)^2} \tag{3}$$

So, if the various parameters on the right-side of either equation are known for different test cases, then $\frac{W}{L}$ can be calculated for different points, and the average can be taken for a good estimate of the true value. i_D and V_{SG} are trivial since those are essentially directly measured in the experiment. V_{tn} and $|V_{tp}|$ are given in the SPICE model of the CD4007 transistors, but they do not reflect what is observed in the actual transistors. However, from analyzing the measured data points, the threshold voltages can be easily obtained for the transistors in lab, and those are to be used. The threshold voltages are given in table (3):

Table 3: Measured Threshold Voltages for NMOS and PMOS

NMOS Threshold Voltage [V]	PMOS Threshold Voltage [V]
1.5	-1.5

The only unknown values are the process transconductance parameters k'_n and k'_p. It is difficult to decouple k'_n from $\frac{W}{L}$. The same applies to the PMOS values. So, the k'_n and k'_p values from the SPICE model are to be used.

Table 4: SPICE Model Process Transconductance Parameters for NMOS and PMOS

NMOS kn [mA / V2]	PMOS kp [mA / V2]
0.6	0.6

Using the data in tables (3) and (4) as well as equations (2) and (3), the $\frac{W}{L}$ ratios for each transistor can be approximated.

Table 5: $\frac{W}{L}$ Ratios for NMOS and PMOS

W over L - NMOS	W over L - PMOS
2.019	1.740