Measurement Lab #3

EECS 170LC

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1 Objective

A differential amplifier is constructed on a breadboard. The differential outputs are analyzed, and the common-mode and differential-mode gain are calculated. The limits of the output voltages before clamping distortions occur are then determined.

2 Descriptions

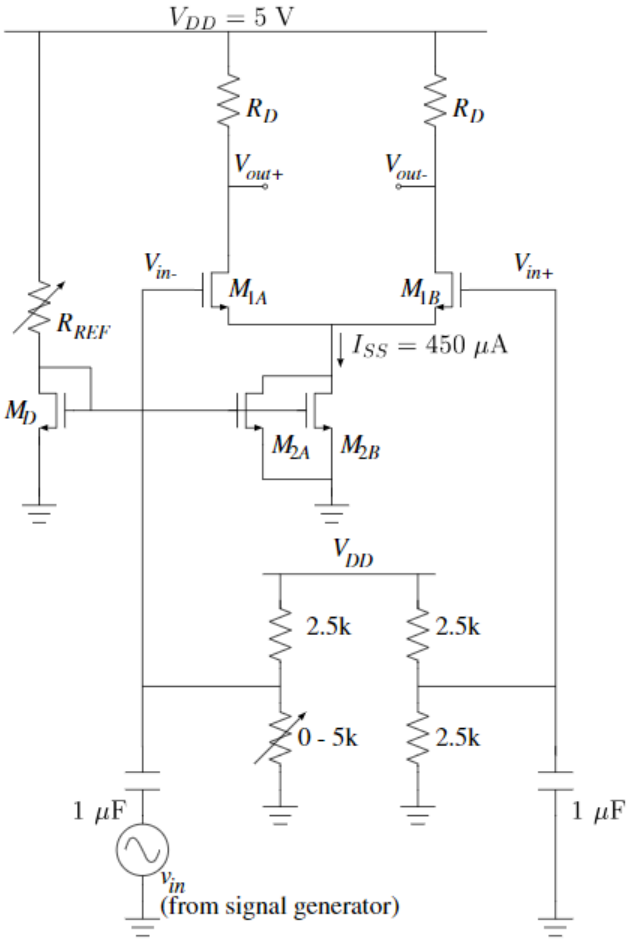

Figure 1: Differential Amplifier

First, the left hand portion of the current source is constructed. The resistor R_{REF} is tuned to get the proper 225µA current. A 10kΩ resistor is used, which yields a 213µA current. The two transistors for the current sources are then attached. Since each current source is expected to produce 225µA, the total current I_{SS} is expected to be 450µA. Their total current I_{SS} is measured to be about 480µA, which is quite close. They are tested by setting the drain voltage sufficiently high so that both of the transistors on the right-hand of the current source enter saturation.

The first voltage divider is then constructed and tested with two 5kΩ resistors in series. Common source amplifiers are constructed with M_{1A} and M_{1B}. 5kΩ and 10kΩ resistors in parallel (3.3kΩ equivalent resistance) for R_D turn out to be sufficient to ensure that both transistors at the voltage input are biased in the middle of the saturation region, which corresponds to an output voltage of about 3.0V.

The current sources and the two halves of the differential pair are then connected to form the final amplifier. The bias current on either half of the differential pair is expected to be about 225µA. On one side, 240µA is measured. On the other side, 246µA is measured. These values are astonishingly close to the design specification.

3 Calculations

3.1 Differential-Mode & Common-Mode Gain

A sine wave centered at 0V with amplitude 100mV and frequency 1MHz is applied to v_{in} as indicated by the differential amplifier circuit schematic. The oscilloscope displayed the following waveforms for V_{out+} and V_{out-}.

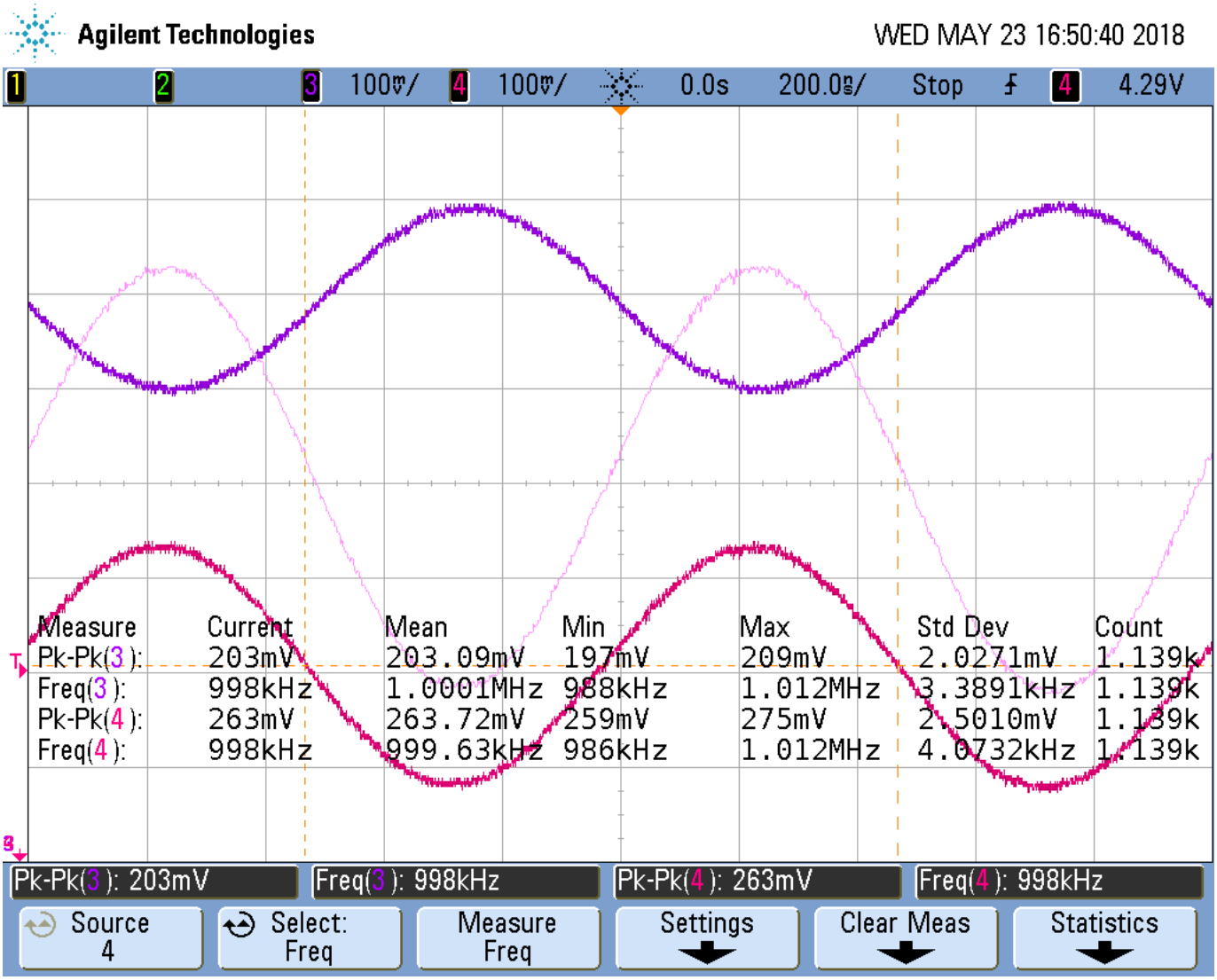

Figure 2: V_{out+} (4), V_{out-} (3), and $V_{out+} - V_{out-}$ for 100mV input at 1MHz

As expected, V_{out+} and V_{out-} are 180 degrees out of phase. The peak-to-peak amplitudes of V_{out+} and V_{out-} are 263 and 203mV, respectively. By taking the difference of the amplitudes, $V_{out+} - V_{out-} = 466$mV

peak-to-peak.

The voltage applied to V_{in-} has an ac amplitude of 100mV. The voltage applied to V_{in+} has no ac component. From these input signals, the differential-mode component of the input $v_{in(dm)} = v_{in+} - v_{in-} = -100\text{mV}$ amplitude or 200mV peak-to-peak. The common-mode component of the input $v_{in(cm)} = \frac{1}{2}(v_{in+} + v_{in-}) = 50\text{mV}$ amplitude or 100mV peak-to-peak.

3.2 Clamping & Distortion

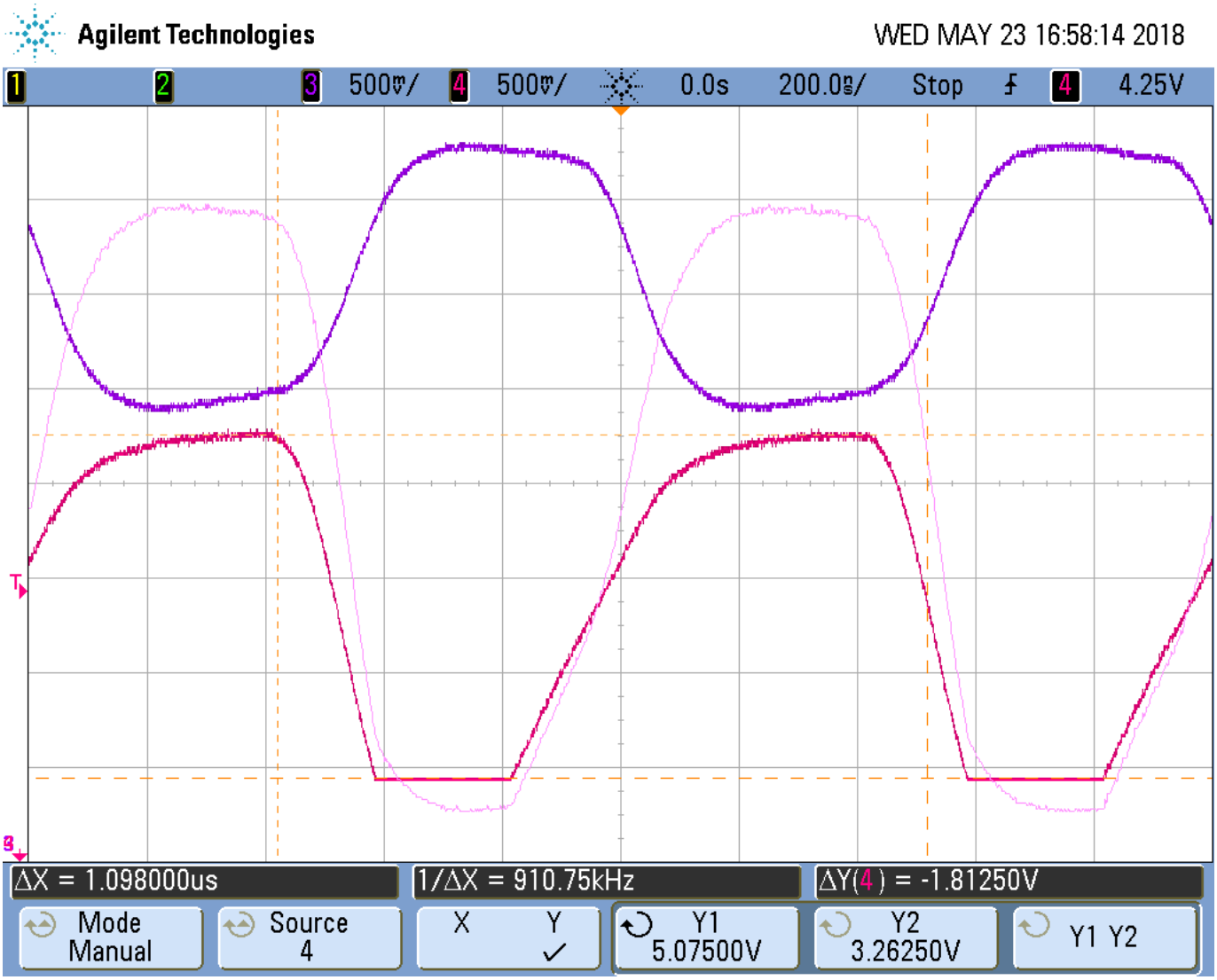

Figure 3: Measured maximum signal swing of V_{out+} from a 2V p/p input at 1MHz

Figure 4: Measured maximum signal swing of V_{out-} from a 2V p/p input at 1MHz

From the cursors in (3), V_{out+} ranges from 5.075 to 3.262 V, resulting in a swing of 1.81V. Similarly, the cursors in (4) reveal a range of 1.38V for V_{out-}. Thus, the voltage range for the signal $V_{out+} - V_{out-}$ is the sum of these two ranges, or 3.19V. From these parameters, an input signal that will avoid clipping should have an amplitude lower than 3.19V / $A_{dm} \approx 1.5$ V.

4 Analysis

4.1 Differential-Mode & Common-mode Gain

The differential-mode gain and common-mode gain from simulations performed prior to this lab are approximately 20 and 0.01 V/V. $v_{out(dm)}$ and $v_{out(cm)}$ can be found by evaluating the product of the corresponding gain values and input components. Thus, $v_{out(dm)} = A_{dm}v_{in(dm)} = 4$V peak-to-peak and $v_{out(cm)} = A_{cm}v_{in(cm)} = 1$mV peak-to-peak. However, the result for $v_{out(dm)}$ is much too large when compared to the amplitudes seen on the oscilloscope. The result for $v_{out(cm)}$ is reasonable since the common-mode component of the output is typically a negligible quantity.

Using the results from the oscilloscope, and assuming that the common-mode component of the output is negligible, $v_{out(dm)}$ can be approximated by $V_{out+} - V_{out-} = 466\text{mV}$ peak-to-peak. The differential-mode gain can then be found: $A_{dm} = \frac{v_{out(dm)}}{v_{in(dm)}} = 2.33$ V/V. This is significantly lower than the value from the simulation. Because the common-mode output is assumed to be negligible, the common-mode gain cannot be conclusively found so the common-mode rejection ratio cannot be found either by extension. However, if the common-mode gain from the simulation is assumed to be correct (this is a baseless assumption), then the CMRR would be 233.

4.2 Clamping & Distortion

Given the voltage ranges of which the amplifying transistors work from (3) and (4), V_{out+} seems to exhibit a larger swing. Although we biased these transistors as identically as we could with the current mirrors and DC voltage dividers, they still exhibit some differences. Notably, the transistor for V_{out+} clearly hits cutoff where the one for V_{out-} does not. The voltage variation in $V_{out+} - V_{out-}$ was earlier found to be 3.19V Interestingly, this is approximately equal to $V_{DD} - V_t$, which is the normal limit in voltage output swing for a common-source amplifier.

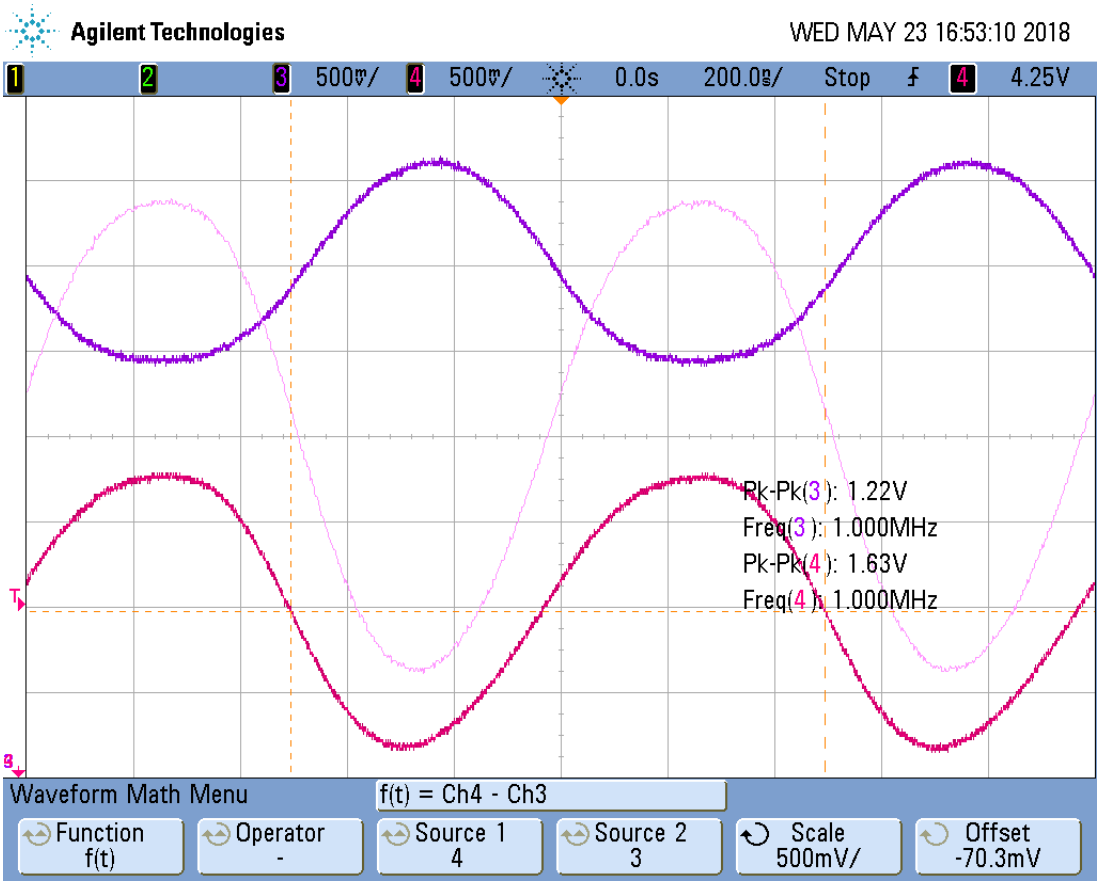

Figure 5: Measured maximum signal swing of V_{out+} and V_{out-} from a 1.5V p/p input at 1MHz

Therefore, for this differential amplifier, the input signal magnitude should be no greater than 1.5V p/p to avoid significant distortion in signal. This quantity is similar to the output voltage swing divided by A_{dm}.

5 Conclusion

5.1 Differential-Mode & Common-mode Gain

The differential amplifier produced results that are clear and easily measurable. However, the differential-mode gain of the amplifier is observed to be a whole order of magnitude lower than the results from simulation. This may be partly due to high frequency attentuation since the circuit is operating at a relatively fast 1MHz frequency. When the frequency of v_{in} is changed to 1kHz, the output amplitudes increase.

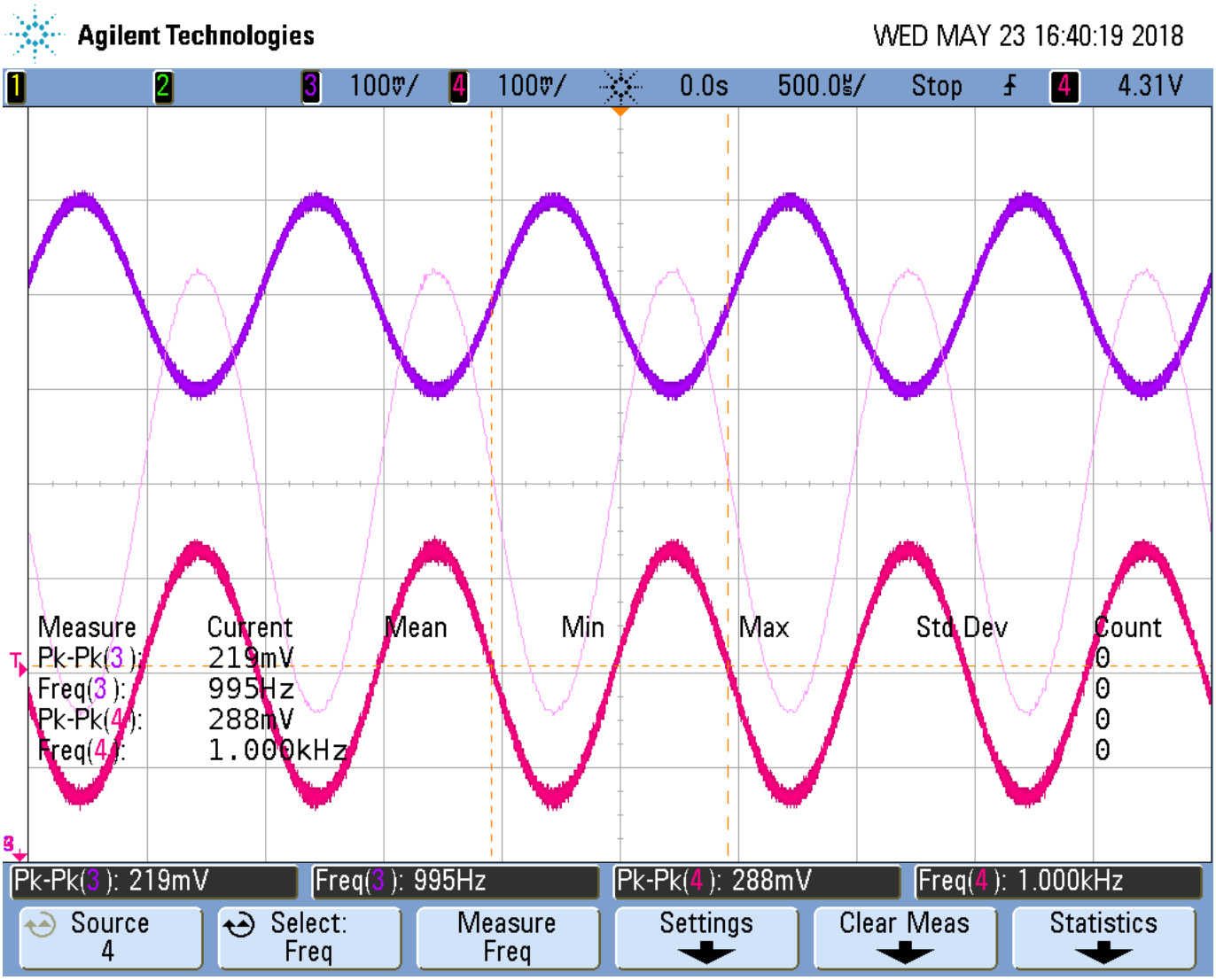

Figure 6: V_{out+} (4), V_{out-} (3), and $V_{out+} - V_{out-}$ for 100mV input at 1kHz

Also, it is observed that transistors M1A and M1B have a slight mismatch as V_{out+} and V_{out-} vary by 60mV and the drain currents on each side of the differential amplifier vary by 6µA. Other inconsistancies may be due to slight variations in resistor values as well. Overall, the differential amplifier exhibited behavior within the realm of expectation.

5.2 Clamping & Distortion

The output voltage swing of V_{in+}, V_{in-}, and of $V_{in+} - V_{in-}$ is overall consistent with the simulated differential amplifier. When one transistor is near cutoff, the other is near triode, and vice-versa so that the differential mode output is large. The value of the differential mode output swing is near the expected value of $V_{DD} - V_t$, which when divided by A_{dm} is consistent with the maximum input amplitude that we found to incur only slight distortion.