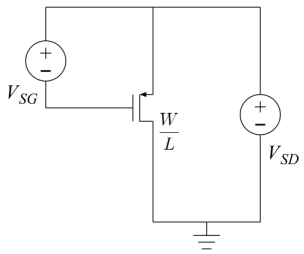

Figure 1: Circuit 4

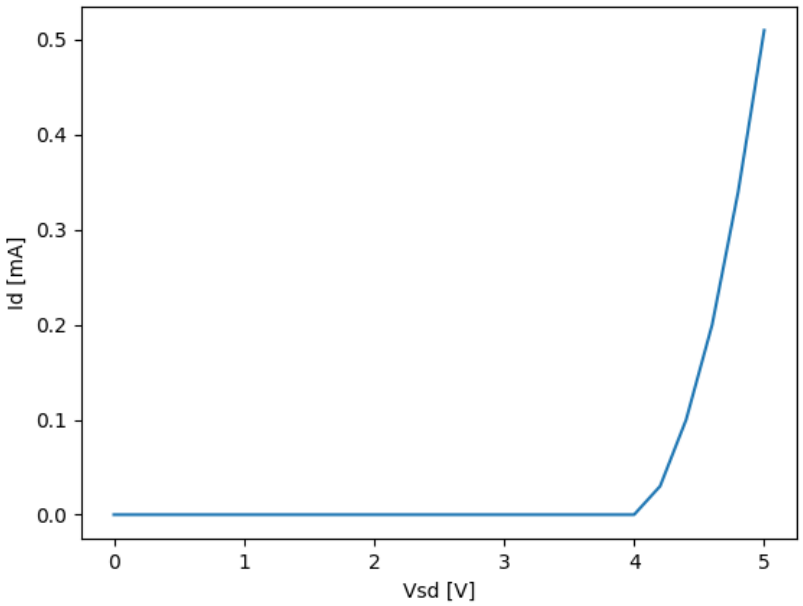

Figure 2: i_D versus V_{SD} for PMOS with $V_{SG} = 2.5$V

One would hope to acquire similar results in figure (2) for the PMOS as are obtained for the NMOS. However, the results are drastically different. Reliable data for the $V_{GS} = 5$V case could not be acquired.