

Simulation Assignment #1  
EECS 170LC  
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# 1 Introduction

p- and n-channel transistors are characterized using Cadence Virtuoso. The  $I_D$  versus  $V_{GS}$  and  $I_D$  versus  $V_{DS}$  curves of the n-channel MOSFET are analyzed. Then the  $I_S$  versus  $V_{SG}$  and  $I_S$  versus  $V_{SD}$  curves of the p-channel MOSFET are analyzed. Other properties such as body leakage current are considered.

## 2 Simulation 1

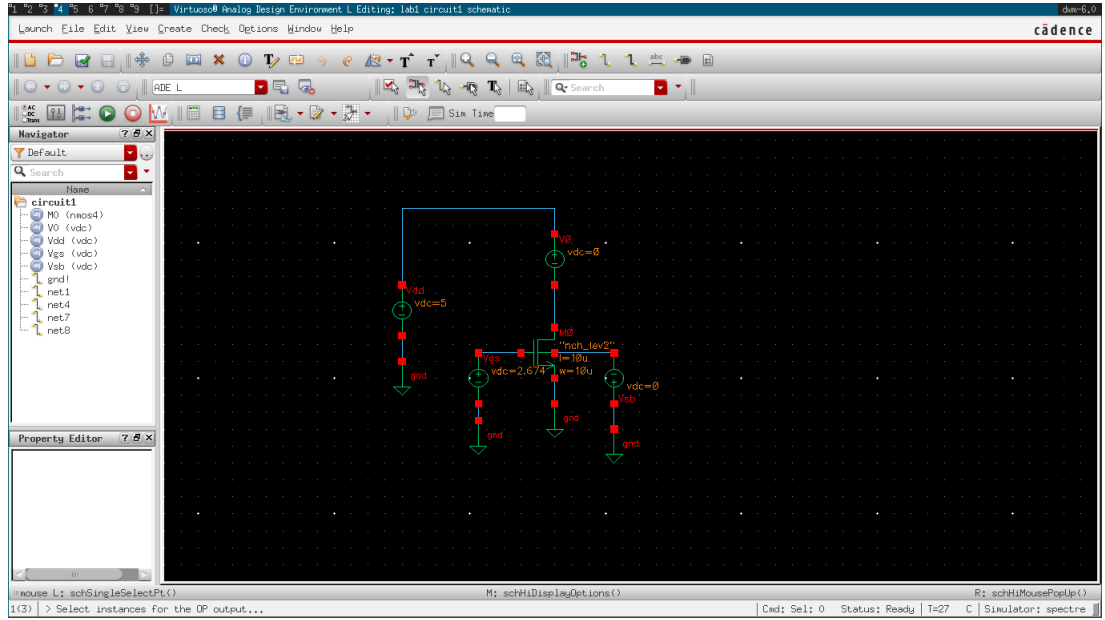


Figure 1: Circuit for Simulation 1

The value of  $V_{GS}$  for which  $I_D = 500\mu A$  is listed in table (1).  $g_m$  is determined from a DC operating point analysis in Virtuoso as well as from the plot in figure (2).



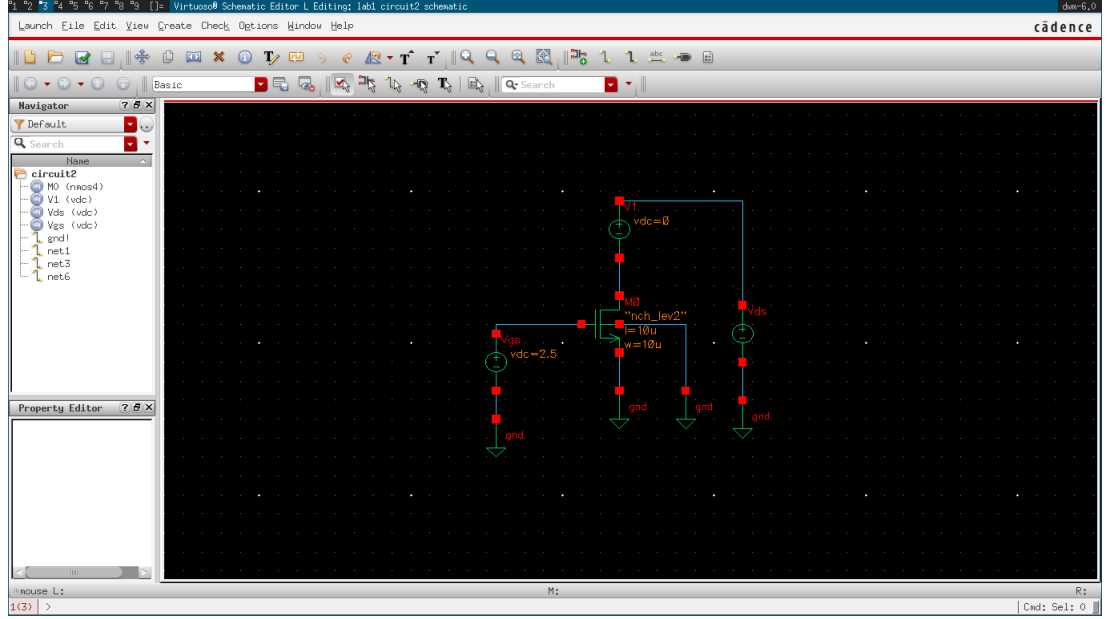
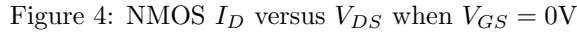


Figure 3: Circuit for Simulation 2

The  $I_D$  versus  $V_{DS}$  characteristics of the n-channel MOSFET are analyzed. For MOSFETs with channel-length modulation,  $r_o = \frac{1}{\lambda I'_D}$  by definition, where  $I'_D = \frac{k_n}{2} V_{ov}^2$  is the saturation current without channel-length modulation effects. Here,  $V_{ov}$  is the transistor's overdrive voltage, and  $k_n$  is the MOSFET's transconductance parameter. The small-signal drain-to-source conductance  $g_{ds}$  is to be defined as  $g_{ds} = \frac{1}{r_o} = \lambda I'_D$ . However,  $I'_D$  is difficult to acquire from realistic simulations.

To a first-order approximation,  $I_D = \frac{k_n}{2} V_{ov}^2 (1 + \lambda V_{DS}) = I'_D (1 + \lambda V_{DS})$  in saturation mode. So,  $\frac{\partial I_D}{\partial V_{DS}} = \lambda I'_D = g_{ds}$ . Thus, by analyzing the derivative of  $I_D$  with respect to  $V_{DS}$  at a particular value of  $V_{DS}$ ,  $g_{ds}$  can be determined from simulation.

First, a simulation is run with  $V_{GS} = 0V$ .


$$I_{DB} = I_S(e^{\frac{V_{DB}}{V_T}} - 1) \quad (1)$$

$V_{GS}$  is now increased to 2.5V. In the triode region,  $I_D$  depends on  $-V_{DS}^2$  because  $I_D = k_n(V_{ov} - 0.5V_{DS})V_{DS}$ . So,  $\frac{\partial I_D}{\partial V_{DS}}$  depends linearly on  $-V_{DS}$ . In

the saturation region,  $\frac{\partial I_D}{\partial V_{DS}}$  is constant with  $V_{DS}$ . Therefore, the transition point between a linear curve and a constant curve marks the transition from saturation to triode, whose intervals are labeled in figure (5).

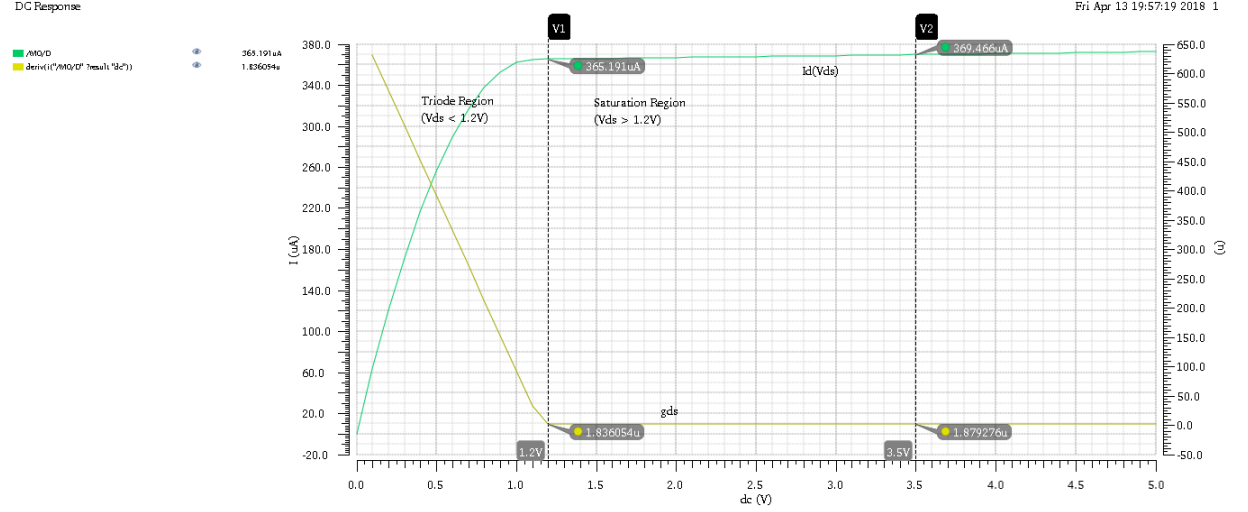


Figure 5: NMOS  $I_D$  versus  $V_{DS}$  when  $V_{GS} = 2.5V$

Here,  $g_{ds}$  can be properly evaluated since the transistor is analyzed at  $V_{DS} = 3.5V$ , which occurs in the saturation region.

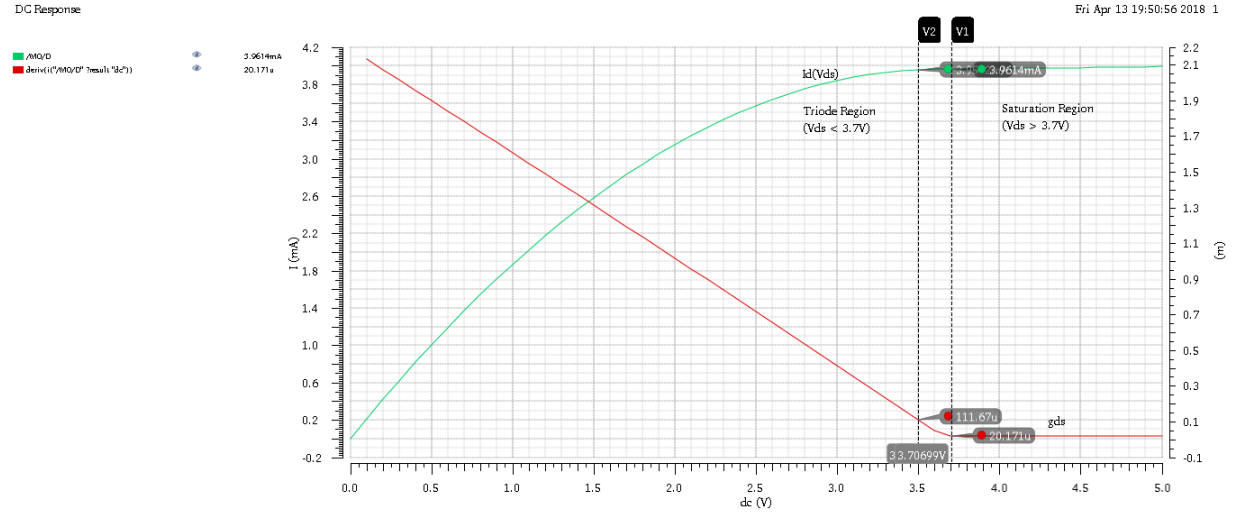


Figure 6: NMOS  $I_D$  versus  $V_{DS}$  when  $V_{GS} = 5.0V$

The simulation results for  $V_{GS} = 5.0V$  are shown in figure (6). The transistor

operates in the triode region at  $V_{DS} = 3.5\text{V}$ , but the same definition is applied nonetheless. The final results are tabulated in table (2).

Table 2: Simulation 2 Results

Vgs [ V ]	gds from Simulation Curves [ uA / V ]	gds from DC Operating Point Simulation [ mA / V ]
0	0	0
2.5	1.88	1.88
5.0	111.67	81.19

## 4 Simulation 3

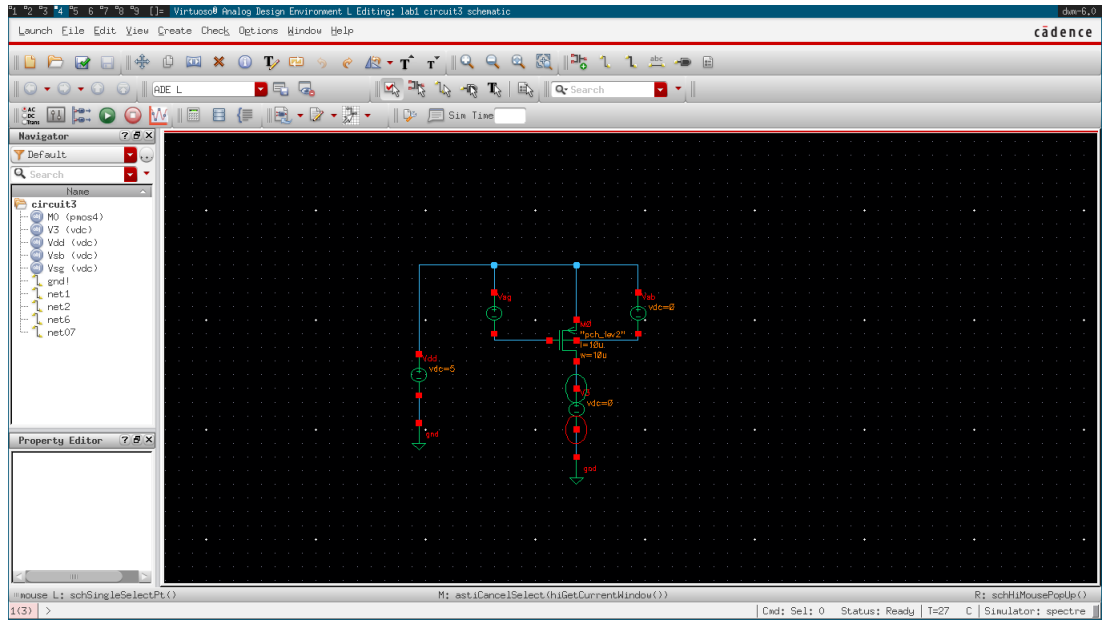


Figure 7: Circuit for Simulation 3

Simulation 3 is similar to Simulation 1 except that a PMOS is used instead of an NMOS.

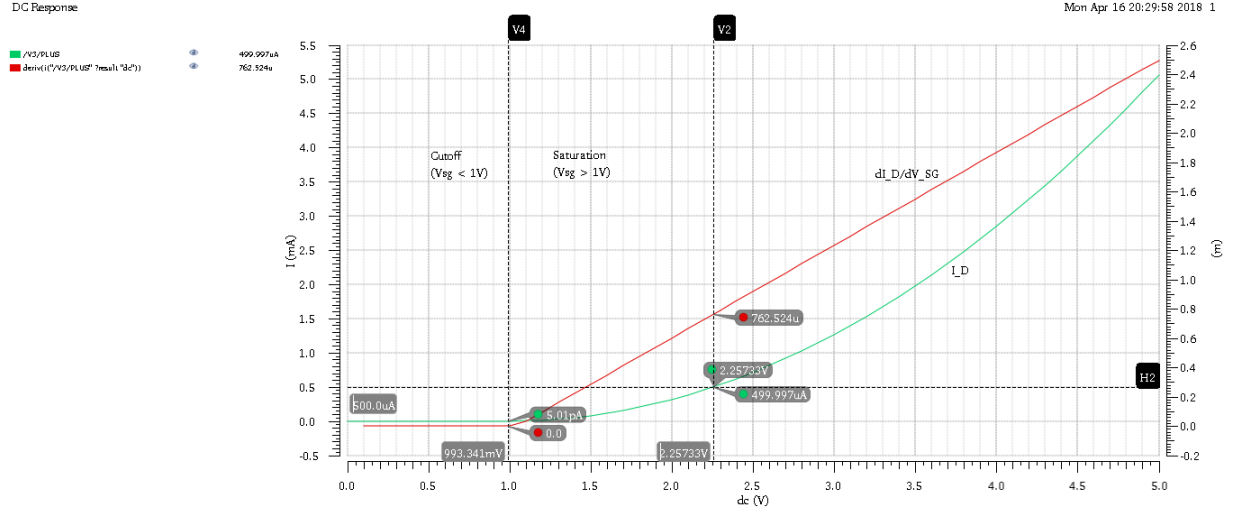


Figure 8:  $I_D$  and  $\frac{\partial I_D}{\partial V_{SG}}$  versus  $V_{SG}$  for PMOS

Again, the transistor is in saturation when it exits cutoff because  $V_{SD} = 5V$  and  $V_{SG} < 5V$ , meaning  $V_{SG} - |V_t| < V_{SD}$ . For the PMOS, the definition  $g_m = \frac{\partial I_D}{\partial V_{SG}}$  shall be used.

Table 3: Simulation 3 Results

Vsg [ V ]	gm from DC op point [ uA / V ]	gm from Graph [ uA / V ]	Error
2.25733	794.1	762.52	4.1%

## 5 Simulation 4



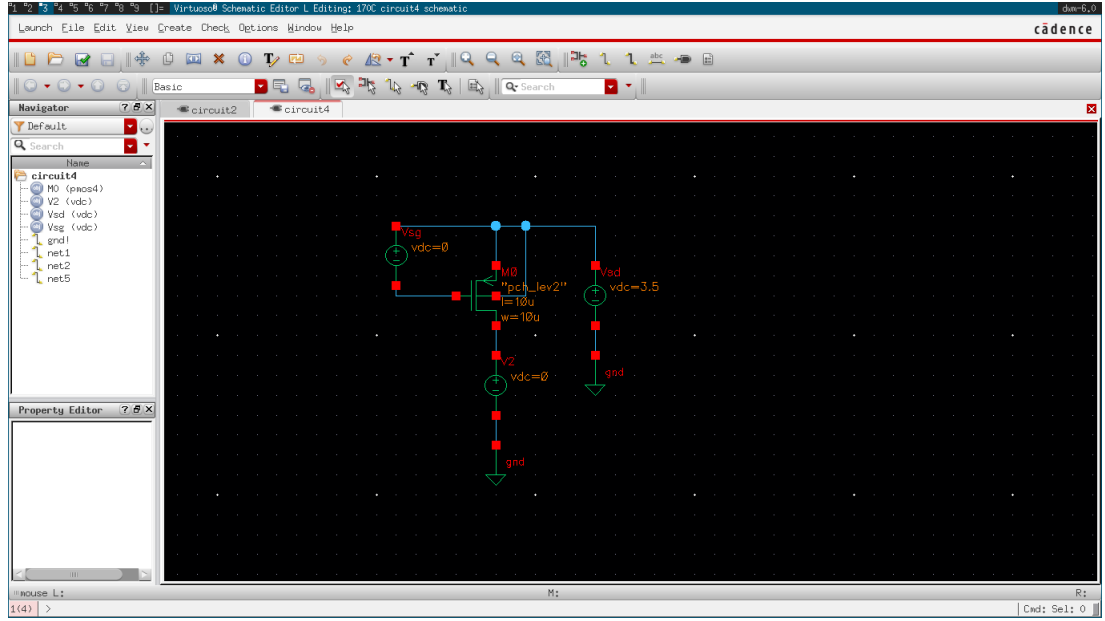


Figure 9: Circuit for Simulation 4

The results for Simulation 4 are similar to Simulation 2, except a PMOS is used instead of an NMOS. The definition  $g_{sd} = \frac{\partial I_D}{\partial V_{SD}}$  is used instead.

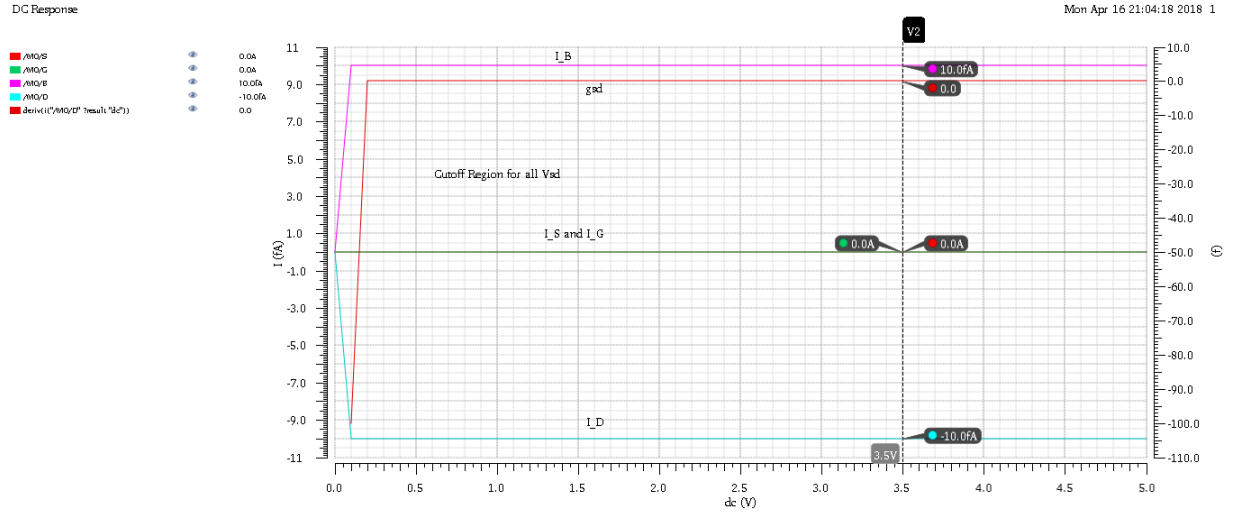


Figure 10: PMOS  $I_D$  versus  $V_{SD}$  when  $V_{SG} = 0V$

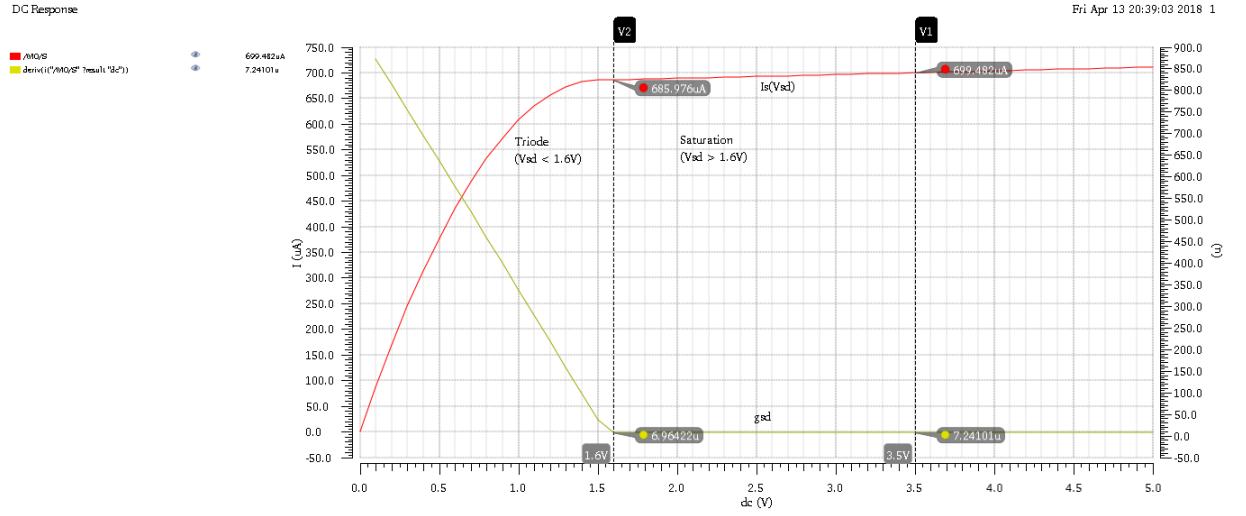


Figure 11: PMOS  $I_D$  versus  $V_{SD}$  when  $V_{SG} = 2.5V$

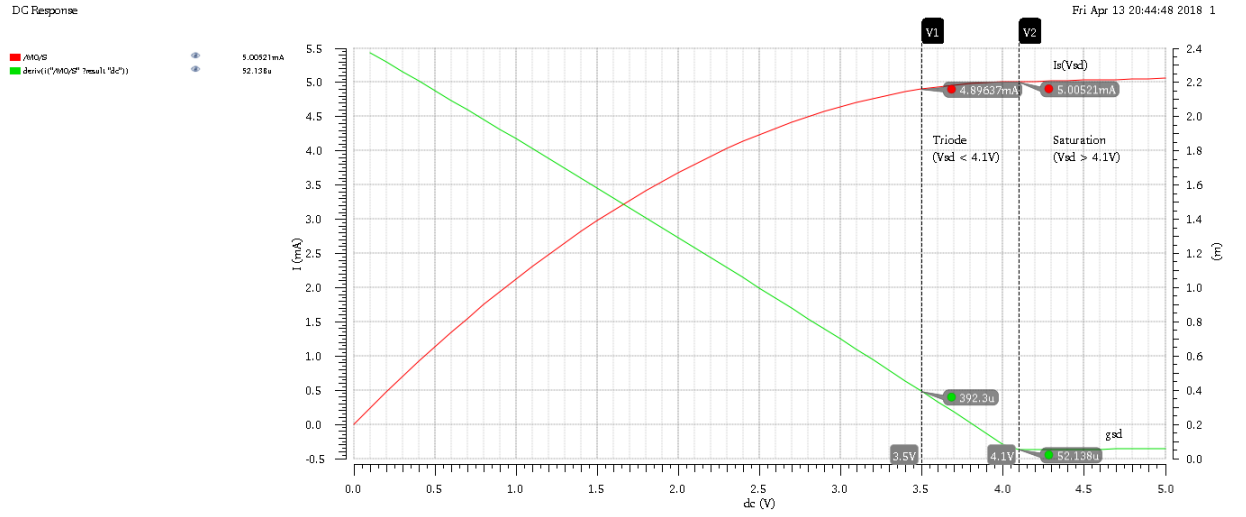


Figure 12: PMOS  $I_D$  versus  $V_{SD}$  when  $V_{SG} = 5.0V$

Table 4: Simulation 4 Results

Vsg [ V ]	gsd from Graph [ uA / V ]	gsd from DC Op Point [ mA / V ]	Error
0	0	0	0%
2.5	7.24	7.249	0.12%
5.0	392.3	361.6	8.5%

$\lambda$  for the NMOS and PMOS can be calculated from the given data. Two samples are already taken for each transistor: the current at the edge of saturation and triode  $I_{D1}$  and the current at  $V_{DS} = 3.5V$  (or  $V_{SD}$  in the case of a PMOS). Consider the transistor at  $V_{GS} = 2.5V$  (or  $V_{SG}$  in the case of a PMOS). It operates in saturation at this  $V_{DS}$  (or  $V_{SD}$  value). Therefore, its current is given by  $I_D = I'_D(1 + \lambda V_{DS})$  (or  $V_{SD}$  in the case of a PMOS). So,  $\lambda$  can be determined from a system of equations. The equations are written for the NMOS, but extrapolating to the PMOS is trivial by simply replacing  $V_{DS}$  with  $V_{SD}$ :

$$I_{D1} = I'_D(1 + \lambda V_{DS1}) \quad (2)$$

$$I_{D2} = I'_D(1 + \lambda V_{DS2}) \quad (3)$$

Solving equations (2) and (3) for  $\lambda$  yields:

$$\lambda = \frac{I_{D2} - I_{D1}}{I_{D1}V_{DS2} - I_{D2}V_{DS1}} \quad (4)$$

$\lambda$  for each transistor is presented in table(5). The results are compared with the simulation models.

Table 5: Lambda Calculations for Transistors

	Calculated Lambda	Model-Specified Lambda	Percentage Error
NMOS	0.00512	0.00500	2.41860%
PMOS	0.01054	0.01000	5.37199%

A simpler approach can also be taken to determine  $\lambda$ . For processes with relatively long transistors,  $\lambda$  should not be very large. Because  $\lambda = \frac{1}{V_A}$ , where  $V_A$  is the Early voltage, this implies that  $V_A$  is quite large. So, long as  $V_{DS}$  (or  $V_{SD}$  in the case of a PMOS) is not very large relative to  $V_A$  ( $V_{DS} \ll V_A$ ), the following approximation can be made:

$$I_D = I'_D(1 + \lambda V_{DS}) = I'_D(1 + \frac{V_{DS}}{V_A}) \approx I'_D \quad (5)$$

Therefore,  $g_{ds} = \lambda I'_D \approx \lambda I_D$  for  $V_A \gg V_{DS}$  (or  $V_A \gg V_{SD}$  for a PMOS). So,  $\lambda$  can also be approximated using  $\lambda \approx \frac{g_{ds}}{I_D}$  (or  $g_{sd}$  in the case of a PMOS) provided that these assumptions about the transistor hold.

## 6 Conclusion

The  $g_m$  values for all of the simulations are quite close (within 5%) of the value provided by Virtuoso's DC operating point analysis.  $g_{ds}$  is generally quite accurate as well. However, for the NMOS at  $V_{GS} = 5V$ , the simulation result from the graph is off from the DC operating point analysis by over 30%. The reasons for this are not quite clear, though it may be that Virtuoso's definition of  $g_{ds}$  in the triode region differs from  $\frac{\partial I_D}{\partial V_{DS}}$ . A deeper investigation is required to understand this discrepancy. Furthermore, the simulation model captures the leakage current through the body of the MOSFET and can thus be considered quite accurate compared to real transistors. Lastly, the calculated  $\lambda$  values are close to, but not exactly equal to, the  $\lambda$  value in the simulation model. The equations used for channel-length modulation are likely a first-order approximation, and Virtuoso may be using a higher-order model that considers  $\lambda^2$  or even  $\lambda^3$  terms.