1 PSpice Simulation

An inverter with input A and output B follows the following truth table:

Table 1: Inverter Truth Table

Input A	Output B
0	1
1	0

The inverter can then be realized in CMOS technology. The width-to-length ratio of the inverter's NMOS shall be referred to as n and p for the PMOS.

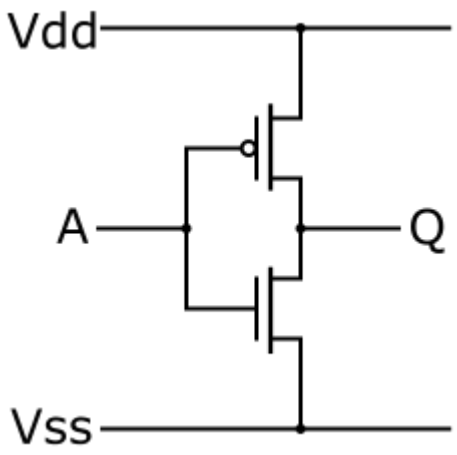

Figure 1: CMOS Inverter

Taken from link `https://en.wikipedia.org/wiki/CMOS#/media/File:CMOS_Inverter.svg`

A NAND gate with inputs A and B and output C has a truth table given by:

Table 2: NAND Truth Table

Input A	Input B	Output C
0	0	1
0	1	1
1	0	1
1	1	0

The NAND gate can be implemented in CMOS like so:

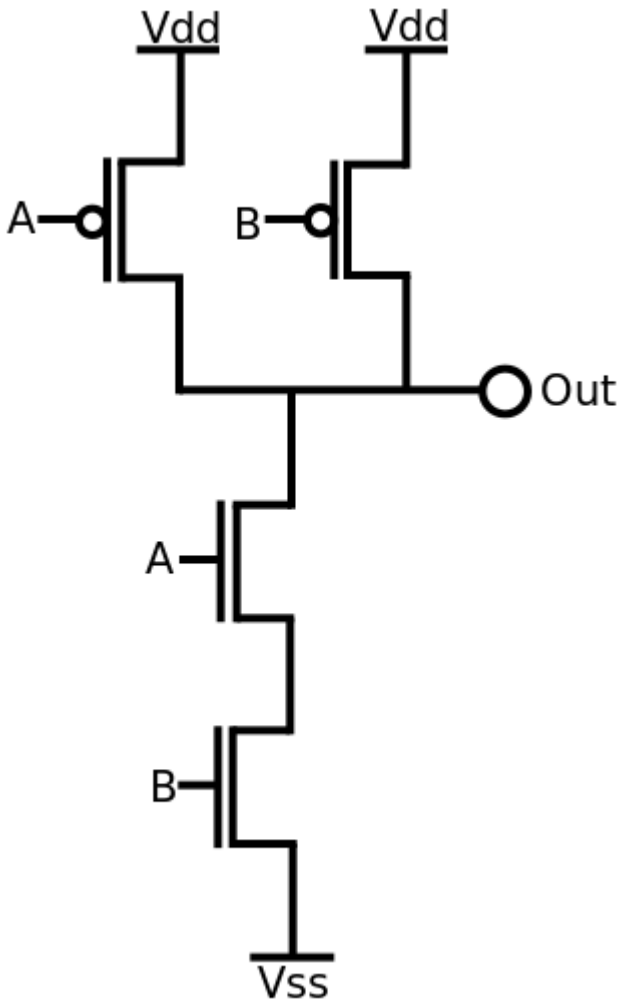

Figure 2: CMOS NAND Gate

Taken from link `https://upload.wikimedia.org/wikipedia/commons/e/e2/CMOS_NAND.svg`

Here, the width-to-length ratio of the NMOSs is $2n$ to compensate for the fact that the current driven from ground is halved in this series configuration. The width-to-length ratio of the PMOSs is still p since this issue does not occur with the parallel PMOSs.

The D-Latch circuit is built using a CMOS inverter and four NAND gates, using two PMOS and two NMOS transistors each. The gate-level design is given in the figure below:

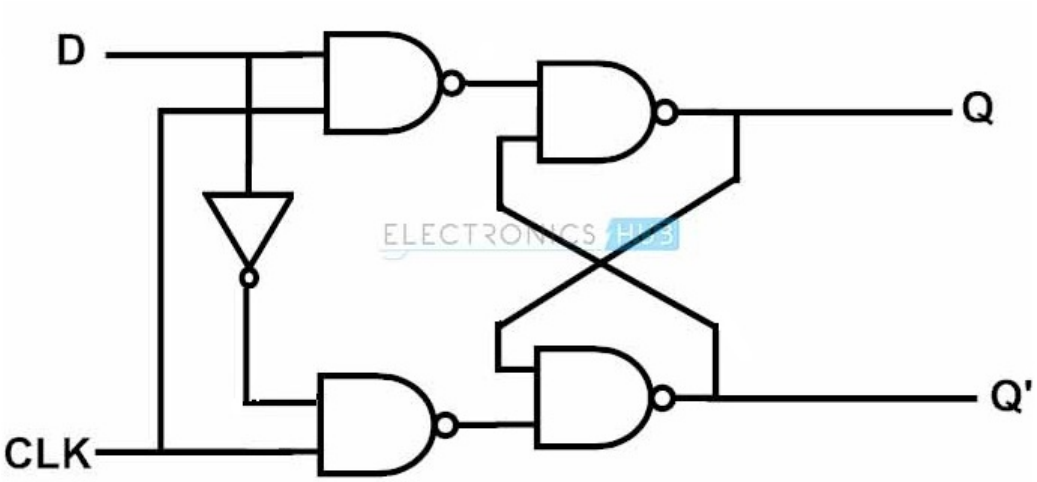

Figure 3: D-Latch Gate Level Schematic

Taken from link `https://www.electronicshub.org/d-flip-flop/`

The circuit is shown in figure (4).

When the control input, C, is high, the value of the input, D, is stored as the output value. However, when the control input is low, the value of the output cannot be changed. For example, if D is high and C high, the output Q is high, but if C is set to low, then the value of D before the change is stored as the output value D until C is brought high again. The behavior of the D-Latch is shown in the FSM in figure (5).

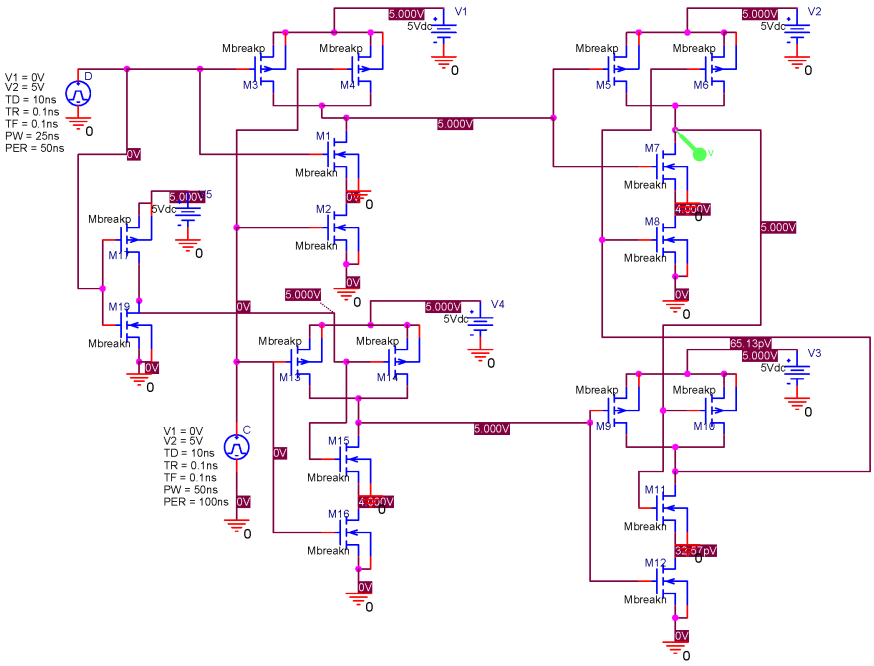

Figure 4: The D-Latch circuit model for PSpice simulation.

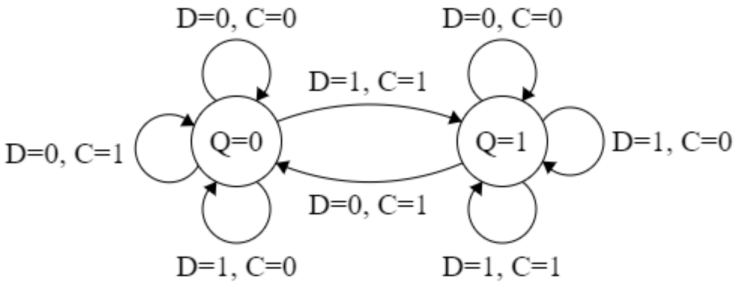

Figure 5: The behavior of a D-Latch.

The results of all the simulations are consistent with the assumed behavior of the D-Latch circuit. In figure (7), it is shown that when the control input C is high the value of input D is stored at the output Q, and when the control input C is low the value of D is not passed to the output Q. For this simulation, the settings in figure (6) are used for the inputs. These values are supplied in the lab specification document.

There is a small spike that occurs when D is becoming high while C is

becoming low. When this switch occurs, the bottom NAND gate of the SR latch portion of the design has one of its inputs change from 0 to 1. The NAND gate includes two NMOSs in series. When both inputs are 0, the NMOSs act as open circuits, which are similar to two capacitors in series at DC. When one of the inputs goes to 1, one of the NMOSs turns on. For a brief period of time, only one of the NMOSs is now an open circuit, whereas the other allows current to flow. Assuming both NMOSs have the same effective "capacitance" when they are both off, the effective "capacitance" of the open circuit in the pull-down network doubles. So, for a brief instant, current is drawn from supply and from the load capacitance connected to the output of the NAND gate. This briefly pulls down the NAND gate's output, which is enough to send a brief 0 pulse to the top latch, briefly setting Q to 1. These effects quickly die out as the other NMOS becomes fully charged and acts as a pure open circuit again. The values then return to the expected behavior. However, this hypothesis is difficult to determine without further experimentation.

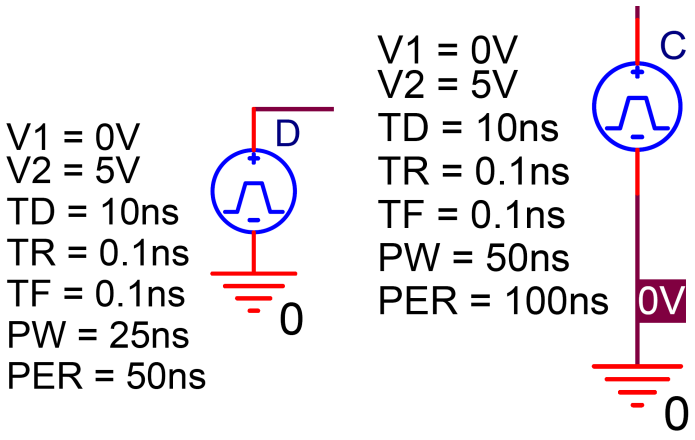

Figure 6: The simulated input (left) and the simulated control input.

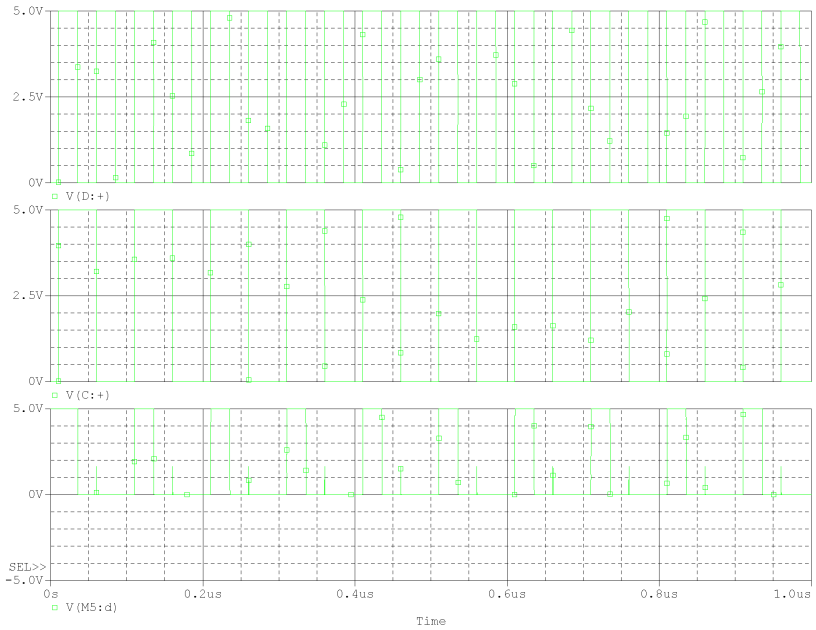

Figure 7: The simulation results of our D-Latch, using inputs from figure 6.