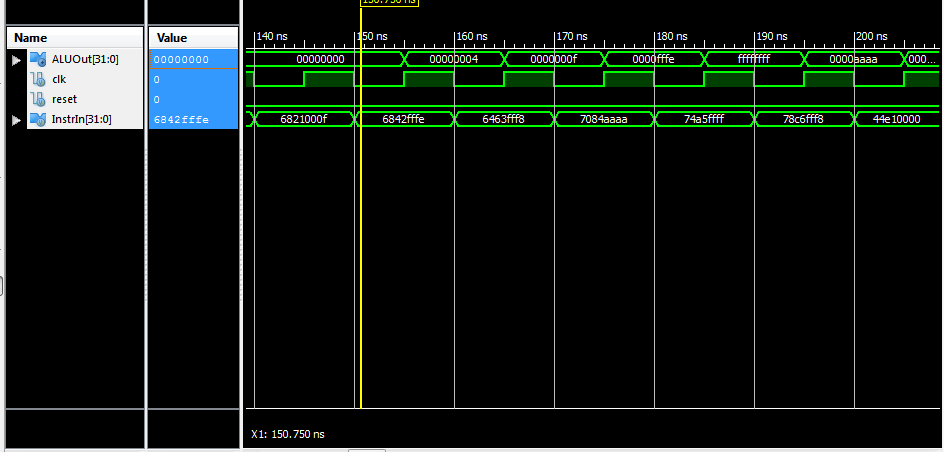
Jackson Hsu

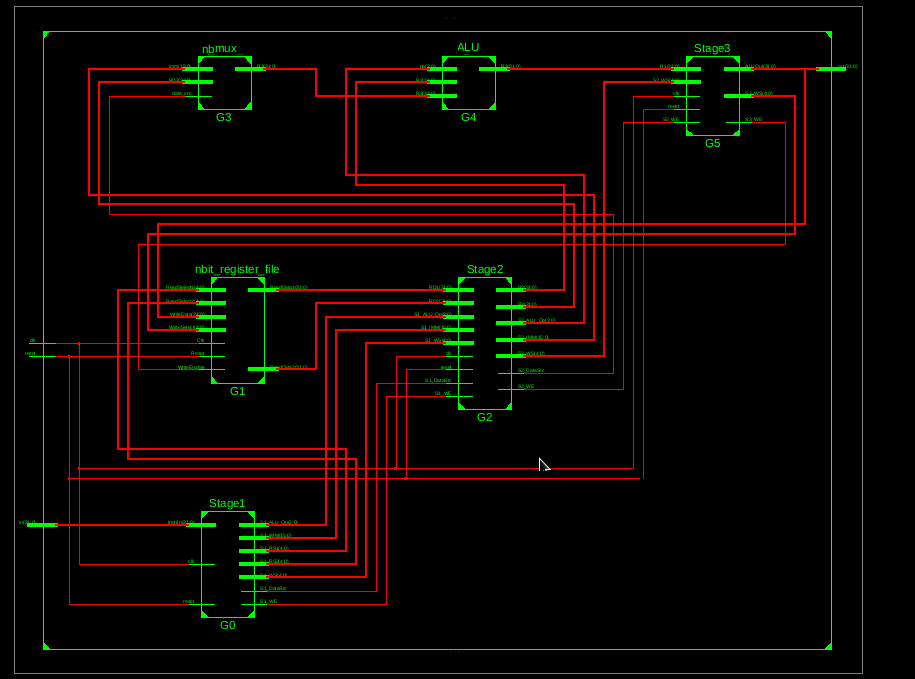
Lab 6

In lab 6 we had to make a 4-stage pipelined datapath. We made a stage1, stage2, and stage3 module that was hierarchal. We made a MUX (nbmux) module, ALU module, and the provided register module. The pipelined datapath takes an input and the opcode, determining whether it’s Immediate type or Register type, and decides the operation will be performed. In the top module I connected stage1 to the register and stage 2. Then I connected stage 2 to the MUX which would determine its type and pass it to the ALU. The ALU would then compute the data given and output to stage3 which would output to the register. I tested this by making sure the numbers outputted matched the correct values.

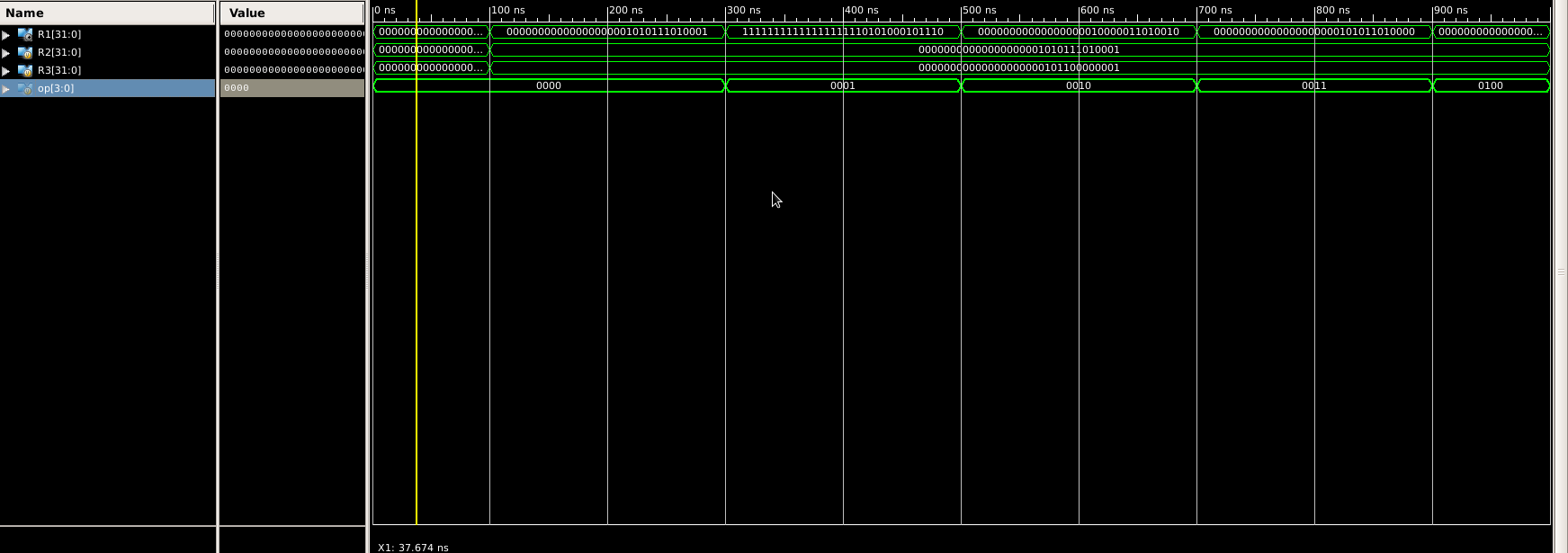
Below is the top module simulation:



Below is the Schematic of the Top Module



ALU:  
I tested the ALU using the given test bench. My ALU was almost the exact same one from Lab 5.



MUX:

The MUX was used to determine whether the input given to the Top Module was an immediate or a register. If it was 1 then it was the immediate type, if 0 then it was the register type.

Reg:

The register was a module given to us. To test the register I used the given testbench and confirmed the outputs given were the desired outputs

