Performance of pipeline with stalls

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Performance with Stalls

Stalls degrade performance of a pipeline:

- Result in deviation from 1 instruction executing/clock cycle.
- Let's examine by how much stalls can impact CPI…

Pipeline Performance

$$\text{PipelineSpeedup} = \frac{\text{ClockCycleTimeWithoutPipelining} \times \text{CPIWithoutPipelining}}{\text{ClockCycleTimeWithPipelining} \times \text{CPIWithPipelining}}$$

$$\text{A pipelined machine's idealCPI} = \frac{\text{CPIWithoutPipelining}}{\text{PipelineDepth}}$$

$$\text{PipelineSpeedup} = \frac{\text{ClockCycleTimeWithoutPipelining} \times \text{idealCPI} \times \text{PipelineDepth}}{\text{ClockCycleTimeWithPipelining} \times \text{CPIWithPipelining}}$$

$$\text{CPIWithPipelining} = \text{idealCPI} + \text{PipelineStallClockCyclesPerInstruction}$$

$$\text{PipelineSpeedup} = \frac{\text{ClockCycleTimeWithoutPipelining} \times \text{idealCPI} \times \text{PipelineDepth}}{\text{ClockCycleTimeWithPipelining} \times (\text{idealCPI} + \text{PipelineStallClockCyclesPerInstruction})}$$

If we ignore the pipeline overhead, then

$$\text{PipelineSpeedup} = \frac{\text{idealCPI} \times \text{PipelineDepth}}{\text{idealCPI} + \text{PipelineStallClockCyclesPerInstruction}}$$

if ideal CPI for pipeline machine =1 Cycle then

Speedup Due to Pipelining

$$= \frac{1}{1 + Pipeline\ stall\ cycles\ per\ instruction} \times Pipeline\ depth$$

Consider two processor p1 and p2 But both have ideal CPI of 1clock cycle. Both have different stall cycles for data and control hazard which is given below.

	P1	P2
Cycle time	400ns	500
Taken branch stalls	1	3
Not Taken branch stalls	1	3
Load use stalls	1	2
Store Stalls	1	2

A program consists of 30% branches, 20% loads,20% stores and 30% other instructions. Find out the CPI of both machines if 80% of branches are taken and 60% of loads are followed by a dependent instruction. Which machine is faster to execute the above program.