pipeline processor performance

Presented By

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parameters serve as criterion to estimate the performance of pipelined execution-

- SpeedUp
- Efficiency
- Throughput

speedup(S)

It gives an idea of "how much faster" the pipelined execution is as compared to non-pipelined execution.

It is calculated as-

$$\text{speedup (S)} = \frac{\text{Exetution time\_non-pipeline}}{\text{Execution time\_with pipeline}}$$

Ideal Pipeline Speedup

- *k-stage* pipeline processes *n* tasks in k + (n-1) clock cycles:
  - *k* cycles for the first task and *n-1* cycles for the remaining *n-1* tasks.
- Total time to process *n* tasks
- $[\,k + (n-1)]\,\tau$
- For the non-pipelined processor

$n\,k\,\tau$

Pipeline Speedup Expression

So, speedup (S) of the pipelined processor over non-pipelined processor, when 'n' tasks are executed on the same processor is:

S = (Performance of pipelined processor /Performance of Non-pipelined processor)

As the performance of a processor is inversely proportional to the execution time, we have,

$$\textbf{pipeline speedup} = \frac{\textbf{Exetution time\_non-pipeline}}{\textbf{Execution time\_with pipeline}}$$

$$S = \frac{n\,k\,\tau}{[\,k + (n-1)]\,\tau} = \frac{n\,k}{k + (n-1)}$$

$= (n \times k) / (k + n - 1)$

$= (n \times k) /\{ n + (k - 1)\}$

$= k / \{ 1 + (k - 1)/n \}$

- ***Maximum speedup = S_{max} =K ,for n >> K***

- For very large number of instructions, $n \rightarrow \infty$. Thus, speed up = k.
- Practically, total number of instructions never tend to infinity.
- Therefore, speed up is always less than number of stages in pipeline.

- Efficiency

speedup

Efficiency = **--**

Number of stages in pipeline archiceture

Efficiency of pipeline

The **efficiency** of K stages in a pipeline is defined as ratio of the actual speedup to the maximum speedup.

- n:- no. of task or instruction
- k:- no. of pipeline stages
- τ:- clock period of pipeline

- Hence pipeline efficiency can be defined by:-
- Efficiency = Given speed up / Max speed up = S / Smax
- We know that, Smax = k
- So, Efficiency = S / k

$$\eta = \frac{n * k * \tau}{K \, [\, k*\tau + (n-1)\, \tau \,]} = \frac{n}{k+(n-1)}$$

Throughput is defined as number of instructions executed per unit time.

It is calculated as-

$$\boxed{\text{Throughput} = \frac{\text{Number of instructions executed}}{\text{Total time taken}}}$$

Throughput of pipeline

- Number of result task that can be completed by a pipeline per unit time.

$$W = \frac{n}{k*\tau+(n-1)\tau} = \frac{n}{[k+(n-1)]\tau} = \frac{\eta}{\tau}$$

- Idle case $w = 1/\tau$ = **f when** η **=1.**
- Maximum throughput = frequency of linear pipeline

In instruction pipelining,Speed up, Efficiency and Throughput serve as performance measures of pipelined execution.

example:

Consider a pipeline having 5 phases with duration 60, 50, 90 and 80 ns, 65ns. Given latch delay is 10 ns.

Calculate-

Pipeline cycle time

Non-pipeline execution time

Pipeline time for 1000 tasks

Sequential time for 1000 tasks

speed up for 1000 task

efficiency

Throughput

example:

Consider a pipeline having 15 stages with a stage delay of 90ns. Given pipeline register delay is 5ns.

Calculate-

Pipeline cycle time

Non-pipeline cycle time

pipeline Speedup for executing 100 task

Pipeline execution time for executing 100 Task

Sequential execution time for 100 task

pipeline efficiency?

pipeline Throughput?

example

A four stage pipeline has the stage delays as 150, 120, 160 and 140 ns respectively. Registers are used between the stages and have a delay of 5 ns each. the total time taken to process 1000 data items on the pipeline will be-

120.4 μs
160.5 μs
165.5 μs
590.0 μs

Solution-

Given-

- Four stage pipeline is used
- Delay of stages = 150, 120, 160 and 140 ns
- Delay due to each register = 5 ns
- 1000 data items or instructions are processed

Cycle Time-

Cycle time= Maximum delay due to any stage + Delay due to its register

= Max { 150, 120, 160, 140 } + 5 ns

= 160 ns + 5 ns

= 165 ns

Pipeline Time To Process 1000 Data Items-

Pipeline time to process 1000 data items= Time taken for 1st data item + Time taken for remaining 999 data items

= 1 x 4 clock cycles + 999 x 1 clock cycle

= 4 x cycle time + 999 x cycle time

= 4 x 165 ns + 999 x 165 ns

= 660 ns + 164835 ns

= 165495 ns

= 165.5 μs

Example

We have 2 designs D1 and D2 for a pipeline processor. D1 has 5 stage pipeline with execution time of 3 ns, 2 ns, 4 ns, 2 ns and 3 ns. While the design D2 has 8 pipeline stages each with 2 ns execution time. How much time can be saved using design D2 over design D1 for executing 100 instructions?
(hints:assume latch delay time 10)

a.214 ns
b. 102 ns
c.86 ns
d.200 ns
e. None of the above

Cycle Time in Design D1-

Cycle time= Maximum delay due to any stage + Delay due to its register
= Max { 3, 2, 4, 2, 3 } + 10
= 14 ns

Execution Time For 100 Instructions in Design D1-

Execution time for 100 instructions= Time taken for 1st instruction + Time taken for remaining 99 instructions
= 1 x 5 clock cycles + 99 x 1 clock cycle
= 5 x cycle time + 99 x cycle time
= 5 x1 4 ns + 99 x 14 ns
= 70 ns + 1386 ns
= 1456 ns

Cycle Time in Design D2-

Cycle time= Delay due to a stage + Delay due to its register
= 2 ns + 10
= 12 ns

Execution Time For 100 Instructions in Design D2-

Execution time for 100 instructions= Time taken for 1st instruction + Time taken for remaining 99 instructions
= 1 x 8 clock cycles + 99 x 1 clock cycle
= 8 x cycle time + 99 x cycle time
= 8 x 12 ns + 99 x 12 ns
= 96 ns + 1188 ns
= 1284 ns **Time saved== 1486 ns-1284= 272ns**