Superscalar , superpipelined and VLIW processor archiceture

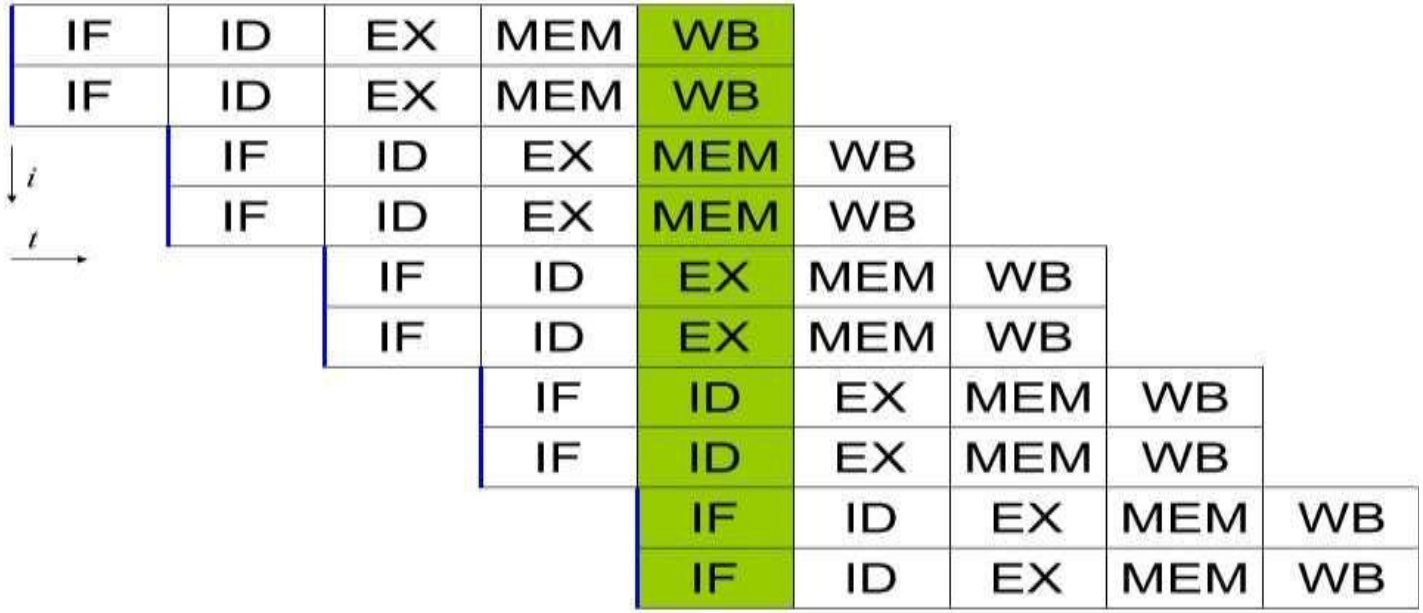
Presented By

Dr. Banchhanidhi Dash

School of Computer Engineering
KIIT University

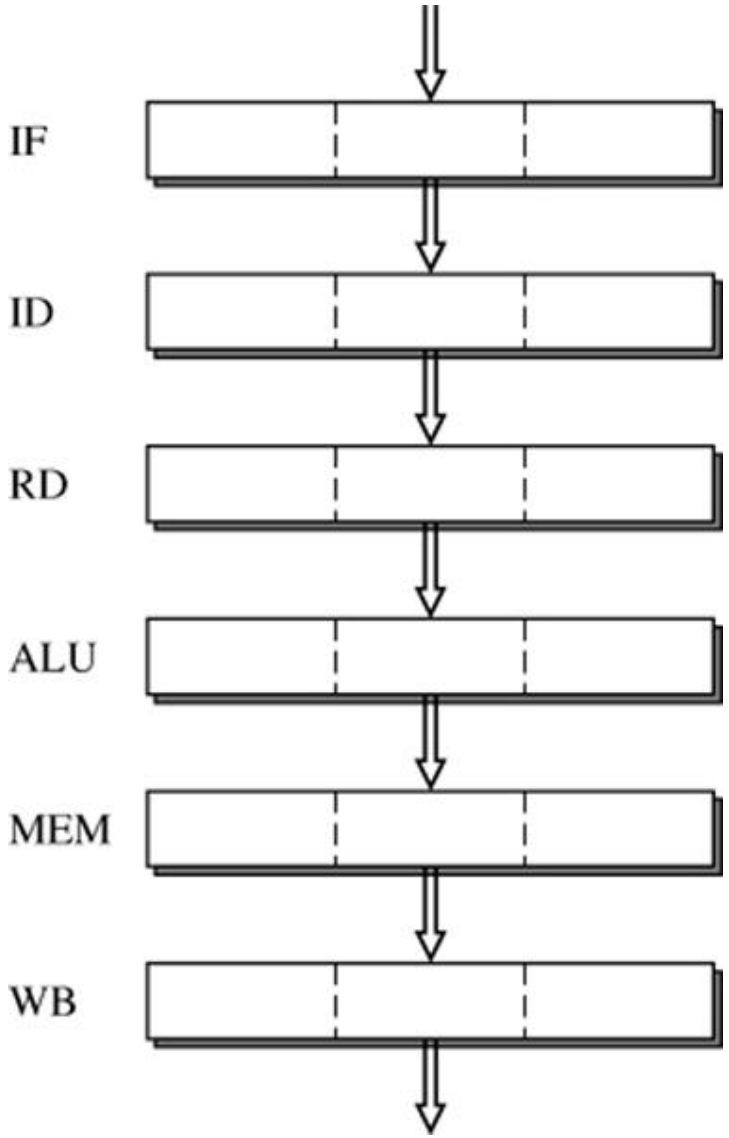
- **Scalar processors** represent a class of computer processors. A scalar processor processes only one data item at a time, with typical data items being integers or floating point numbers.
- A scalar processor is classified as a SISD processor (Single Instructions, Single Data) in Flynn's taxonomy.
- A **superscalar processor** is a CPU that implements a form of parallelism called instruction-level parallelism within a single processor
- In contrast to a **scalar processor** that can execute at most one single instruction per clock cycle, a **superscalar processor** can execute more than one instruction during a clock cycle by simultaneously dispatching multiple instructions to different execution units on the processor.
- Each execution unit is not a separate processor (or a core if the processor is a multi-core processor), but an execution resource within a single CPU such as an arithmetic logic unit.

Simple superscalar pipeline



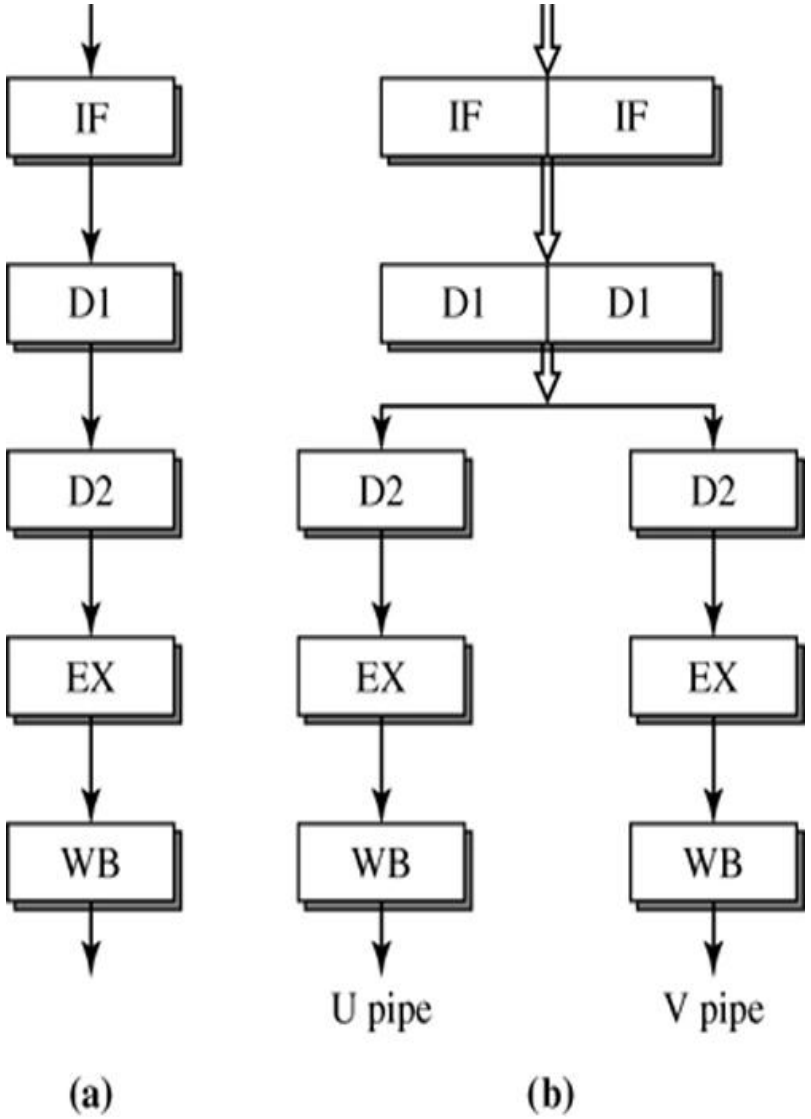
By fetching and dispatching two instructions at a time, a maximum of two instructions per cycle can be completed. (IF = Instruction Fetch, ID = Instruction Decode, EX = Execute, MEM = Memory access, WB = Register write back, i = Instruction number, t = Clock cycle [i.e., time])

A Parallel Pipeline



Width = 3

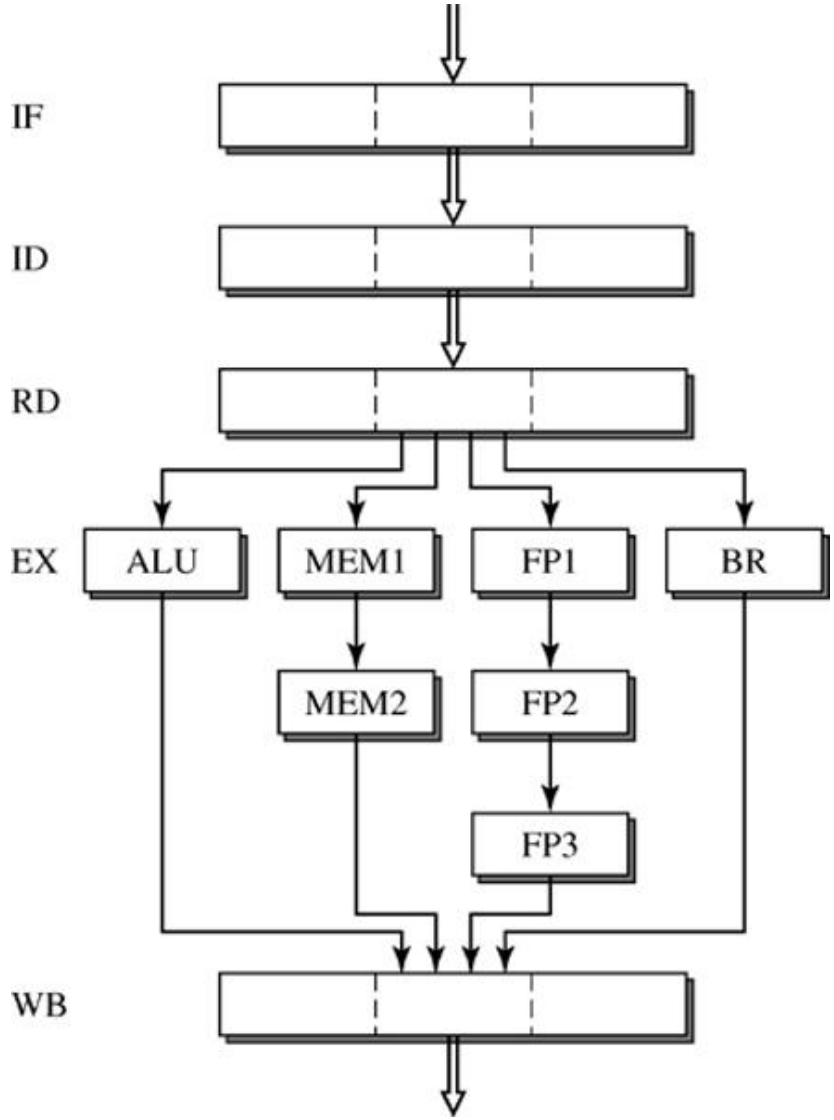
Scalar and Parallel Pipeline



(a) The five-stage i486 scalar pipeline

(b) The five-stage Pentium Parallel Pipeline of width=2

Diversified Parallel Pipeline

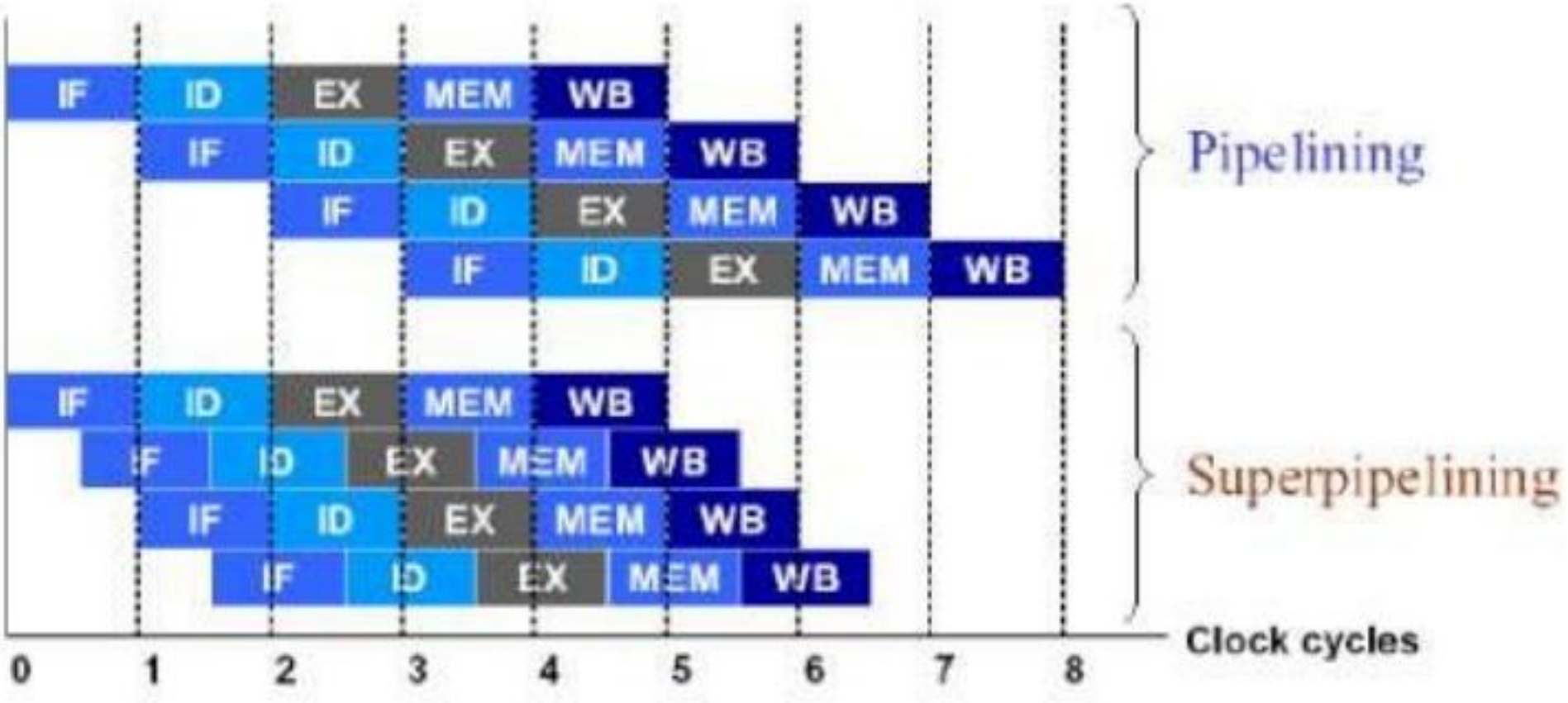


Super pipeline

- Super-pipelining is the breaking of stages of a given pipeline into smaller stages (thus making the pipeline deeper) in an attempt to shorten the clock period and thus enhancing the instruction throughput by keeping more and more instructions.

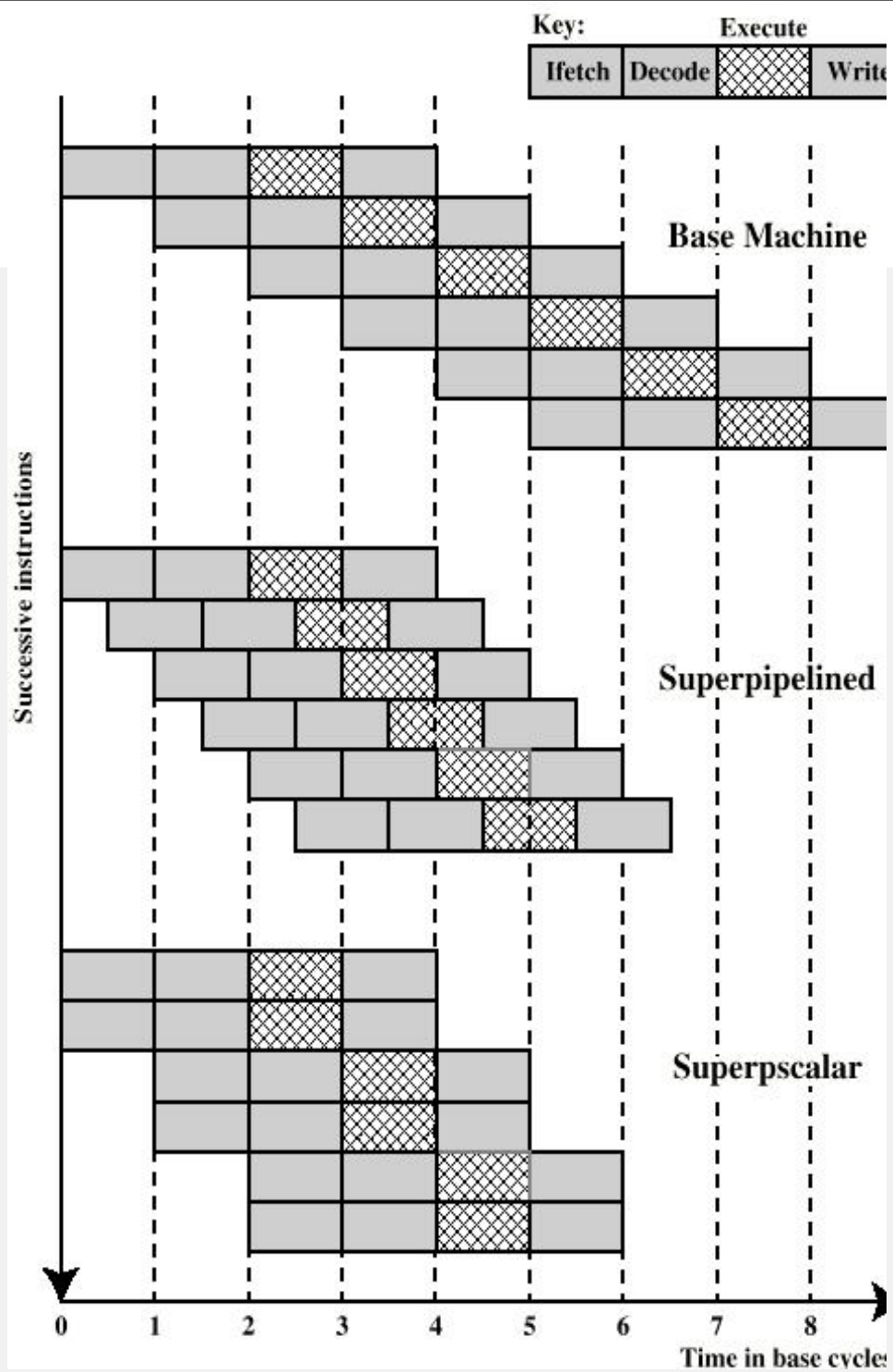
Super pipeline Performance

- The performance is shown below in the figure:



Superscalar versus super-pipeline

- Simple pipeline system performs only one pipeline stage per clock cycle
- Super-pipeline system is capable of performing two pipeline stages per clock cycle
- Superscalar performs only one pipeline stage per clock cycle in each parallel pipeline

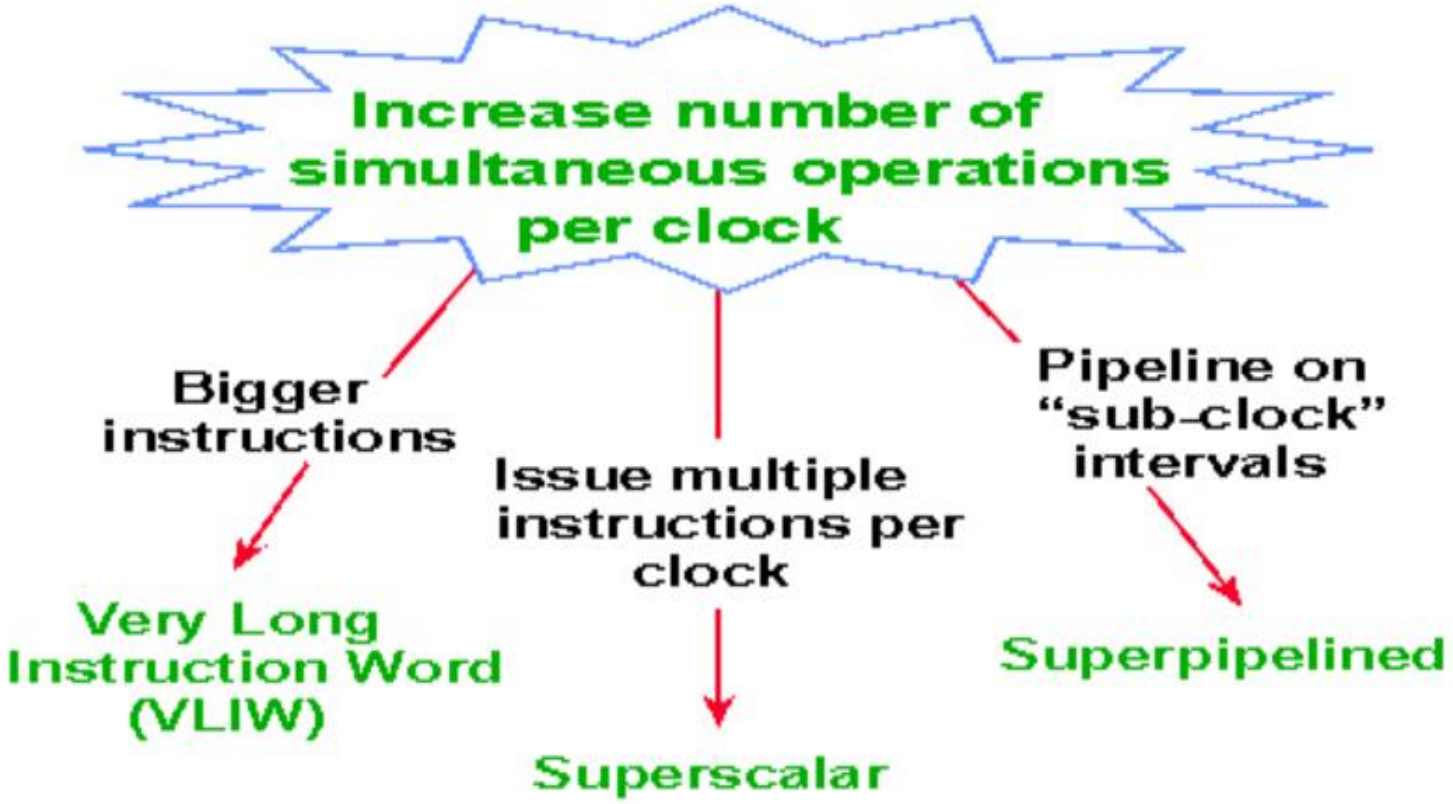


VLIW(very long Instruction word) Processor archiceture

Presented By
Dr. Banchhanidhi Dash

School of Computer Engineering
KIIT University

Realizing CPI < 1.0



All require instruction-level parallelism

VLIW vs Superscalar

- VLIW - Compiler finds parallelism:
  - Superscalar – hardware finds parallelism
- VLIW – Simpler hardware:
  - Superscalar – More complex hardware

Very Long Instruction Word (VLIW) Processors

- Hardware cost and complexity of superscalar schedulers is a major consideration in processor design.
  - VLIW processors rely on compile time analysis to identify and bundle together instructions that can be executed concurrently.
- These instructions are packed and dispatched together,
  - Thus the name very long instruction word.
  - This concept is employed in the **Intel IA64 processors**.
  - The Itanium architecture is based on explicit instruction-level parallelism, in which the compiler decides which instructions to execute in parallel. This contrasts with superscalar architectures, which depend on the processor to manage instruction dependencies at runtime.

VLIW Processors

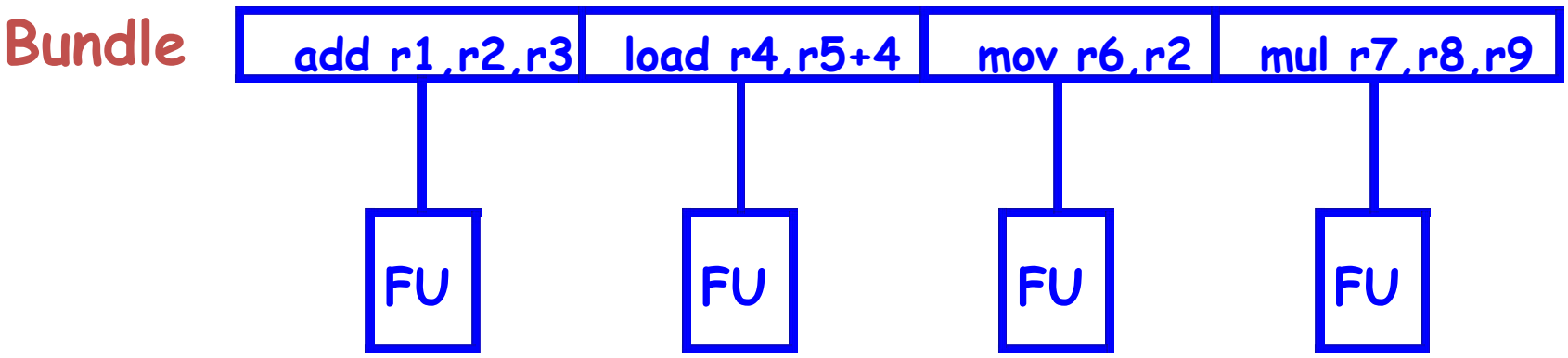
- The compiler has complete responsibility of selecting a set of instructions:
  - These can be concurrently be executed.
- VLIW processors have static instruction issue capability:
  - As compared, superscalar processors have dynamic issue capability.

VLIW Processors

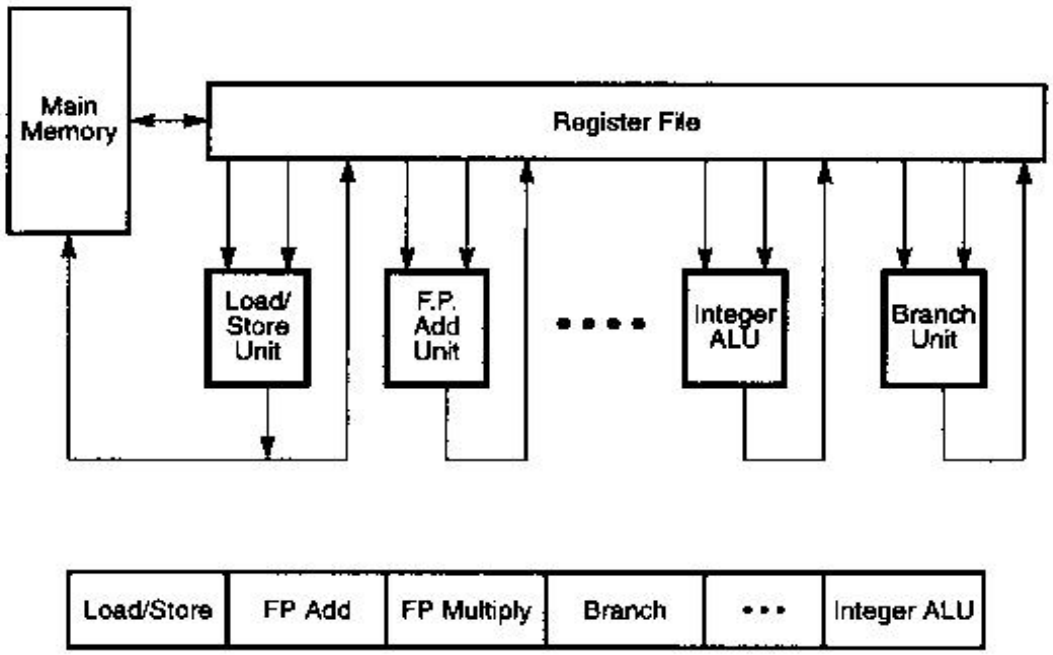
- Assume a 4-issue superscalar processor:
  - During fetch stage, 1 to 4 instructions would be fetched.
  - The group of instructions that could be issued in a single cycle are called:
    - An issue packet or a Bundle.
  - If an instruction could cause a structural or data hazard:
    - It is not issued.

VLIW (Very Long Instruction Word)

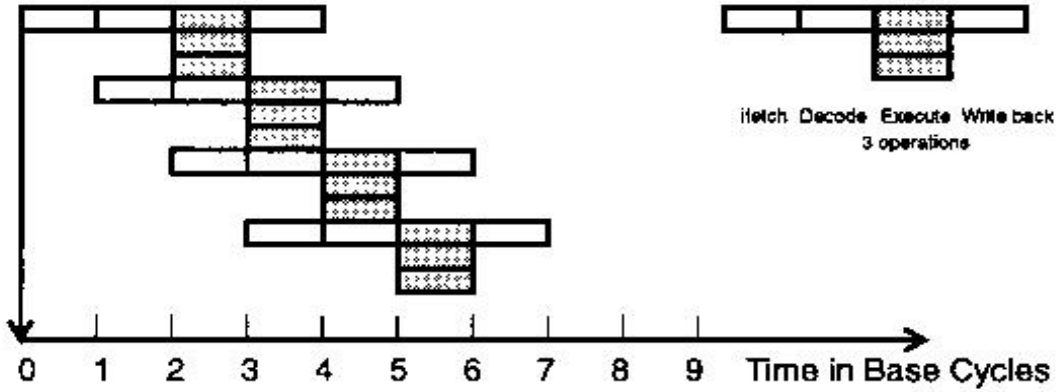
- One single VLIW instruction:
  - separately targets differently functional units.
- MultiFlow TRACE, TI C6X, IA-64



Schematic Explanation for a VLIW Instruction



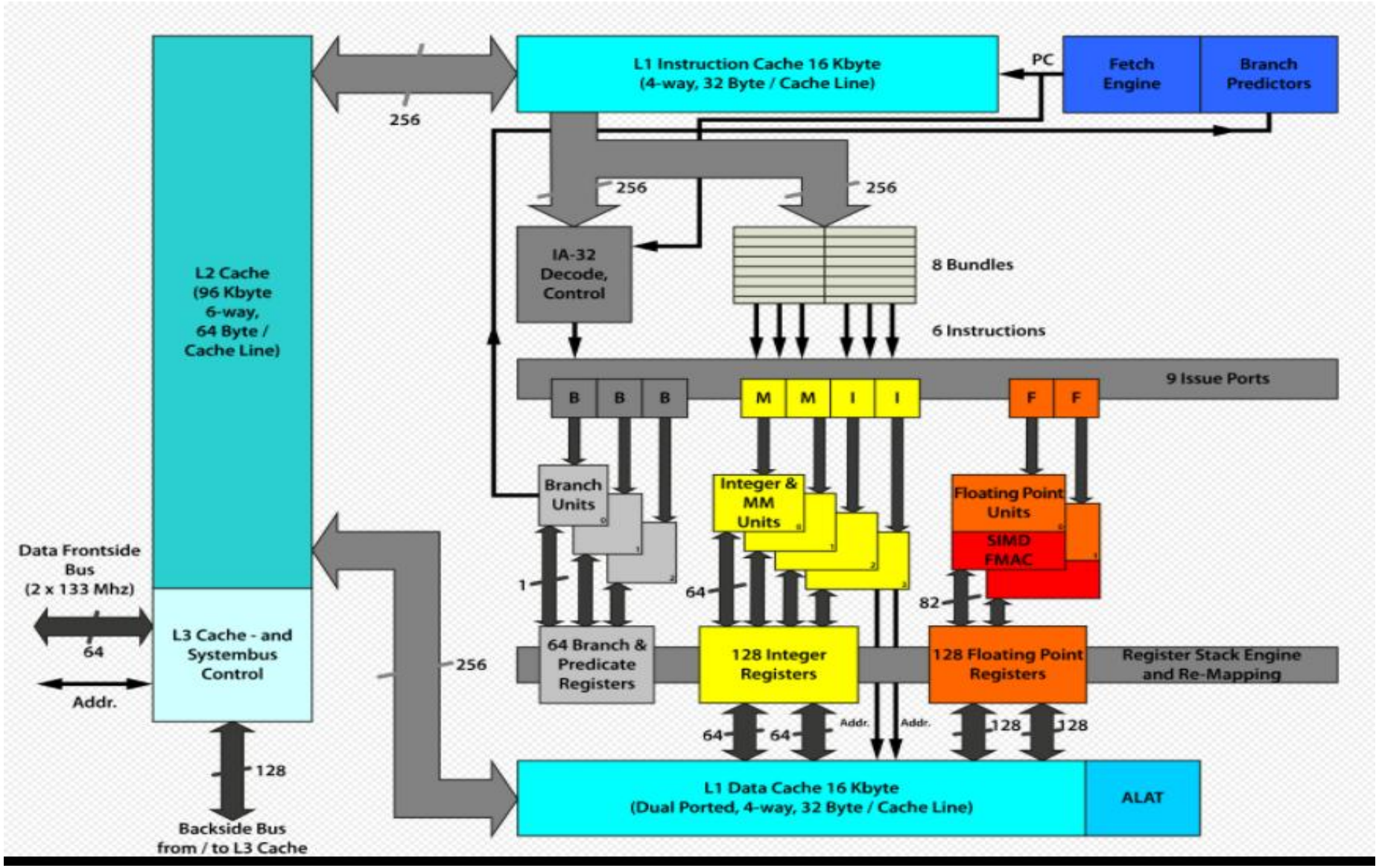
(a) A typical VLIW processor and instruction format



(b) VLIW execution with degree $m = 3$

Figure 4.14 The architecture of a very long instruction word (VLIW) processor and its pipeline operations. (Courtesy of Multiflow Computer, Inc., 1987)

Intel IA archiceture



VLIW Summary

- Each "instruction" is very large
  - Bundles multiple operations that are independent.
- Complier detects hazard, and determines scheduling.
- There is no (or only partial) hardware hazard detection:
  - No dependence check logic for instructions issued at the same cycle.
- Tradeoff instruction space for simple decoding
  - The long instruction word has room for many operations.
  - But have to fill with NOP if enough operations cannot be found.