

# Introduction to Cadence Virtuoso CAD Tool

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In this tutorial, you are going to explore the following:

- 1) Understand the software structure of Cadence Virtuoso.
- 2) Understand the process design kits (PDK) and standard cell library.
- 3) Design a simple circuit component, including:
  - a) Schematic design
  - b) Simulation
  - c) Layout design
  - d) Design rule check (DRC)
  - e) Layout versus schematic (LVS)
  - f) Parasitic extraction (PEX)

**CAD tools troubleshoot:** If you encounter any problems when using the CAD tools, we recommend you first check for any existing solutions on the Ed Discussion page of the Sakai course site. Contact the TA or CAD admins for further assistance if no existing solutions are available. You are highly encouraged to post your CAD tools issues and solutions (if available) on the Ed Discussion page to share information with other classmates.

## 1. Setup and Launch Cadence Virtuoso CAD Tool

### Windows Users

Mac users should skip to Page 5.

To access the CAD tools using the server, download the Home Edition of MobaXterm: <https://mobaxterm.mobatek.net/download.html>.

MobaXterm Home Edition

Download MobaXterm Home Edition (current version):

[!\[\]\(2638cc0dbaac7e439e77f3f17b90e9a7\_img.jpg\) MobaXterm Home Edition v23.2  
\(Portable edition\)](#)

[!\[\]\(0d311d25730ba240da04d497f85aaefa\_img.jpg\) MobaXterm Home Edition v23.2  
\(Installer edition\)](#)

Download previous stable version: [MobaXterm Portable v23.1](#) [MobaXterm Installer v23.1](#)

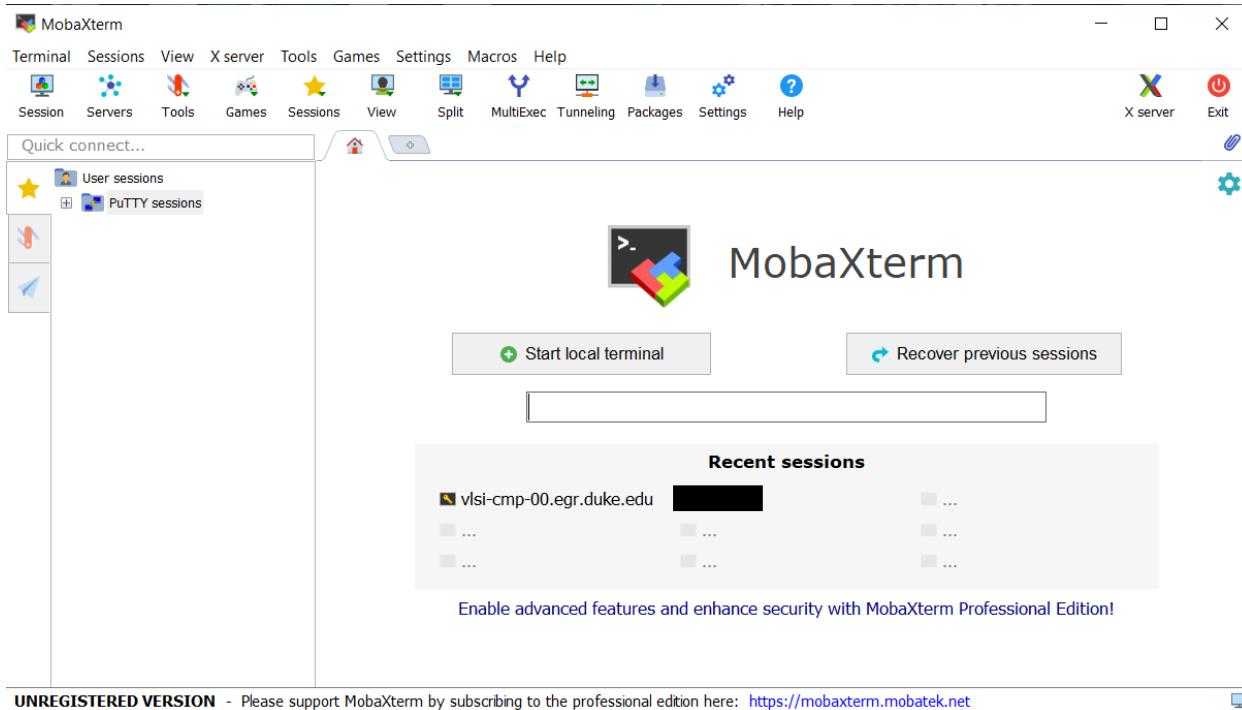
You can also get early access to the latest features and improvements by downloading MobaXterm Preview version:

[MobaXterm Preview Version](#)

By downloading MobaXterm software, you accept [MobaXterm terms and conditions](#)

You can download the third party plugins and components sources [here](#)

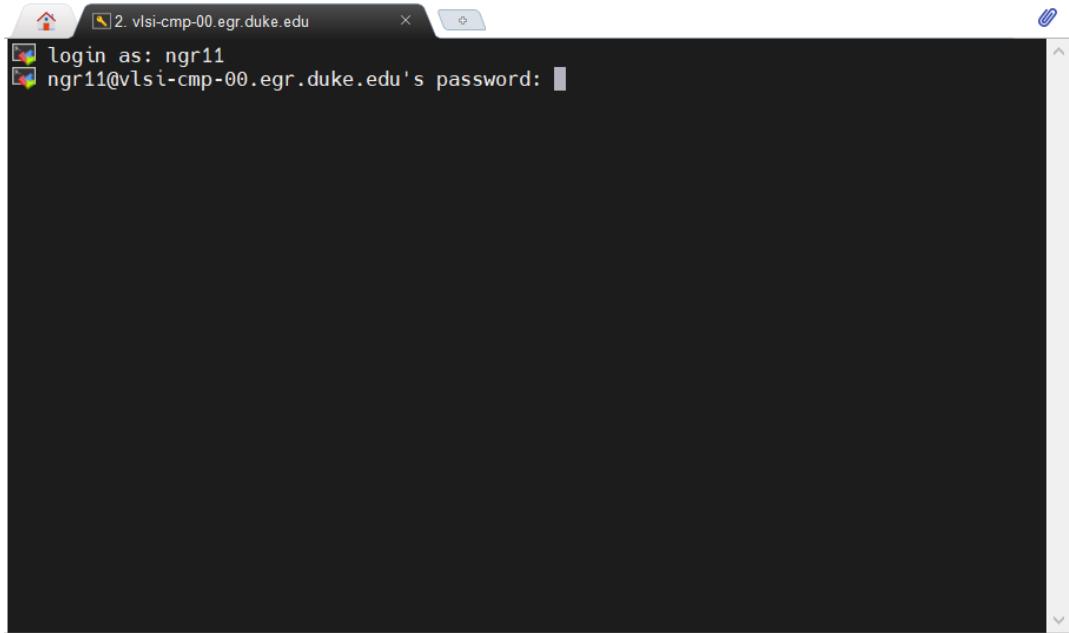
Click on the **MobaXterm\_installer\_23.2 Windows Installer Package** and follow the instructions to complete the setup. When you start MobaXterm, you should see the following home screen. Since this will be your first time using it, you will not see any recent sessions until you connect to the VLSI server.



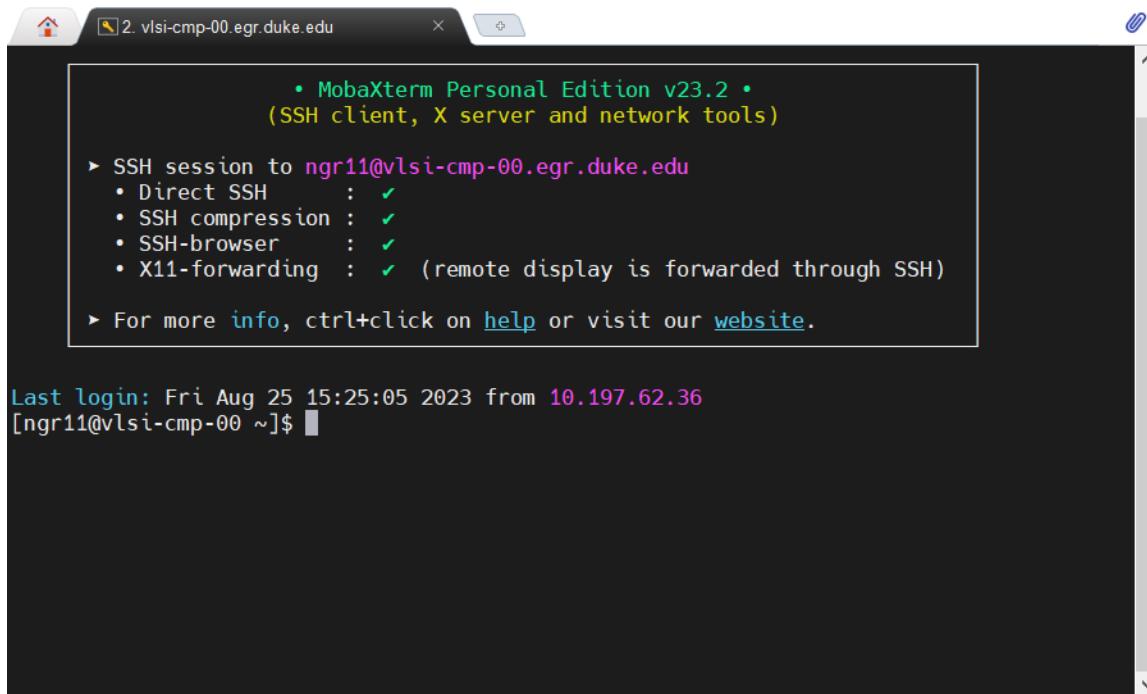
Copy the following address into the bar and then press enter:

**vlsi-cmp-00.egr.duke.edu**

The login following screen should appear. Enter your Duke net ID and press enter. You will then be prompted to enter your net ID password. Linux will automatically mask passwords, so it is normal if the terminal does not show what you type. If you are asked to save your password, click 'No'.



You will see the following screen after you log in. If **Direct SSH**, **SSH compression**, **SSH-browser** or **X11-forwarding** does not have a green check mark, end your session and log in again. If this problem persists, please alert the TA.



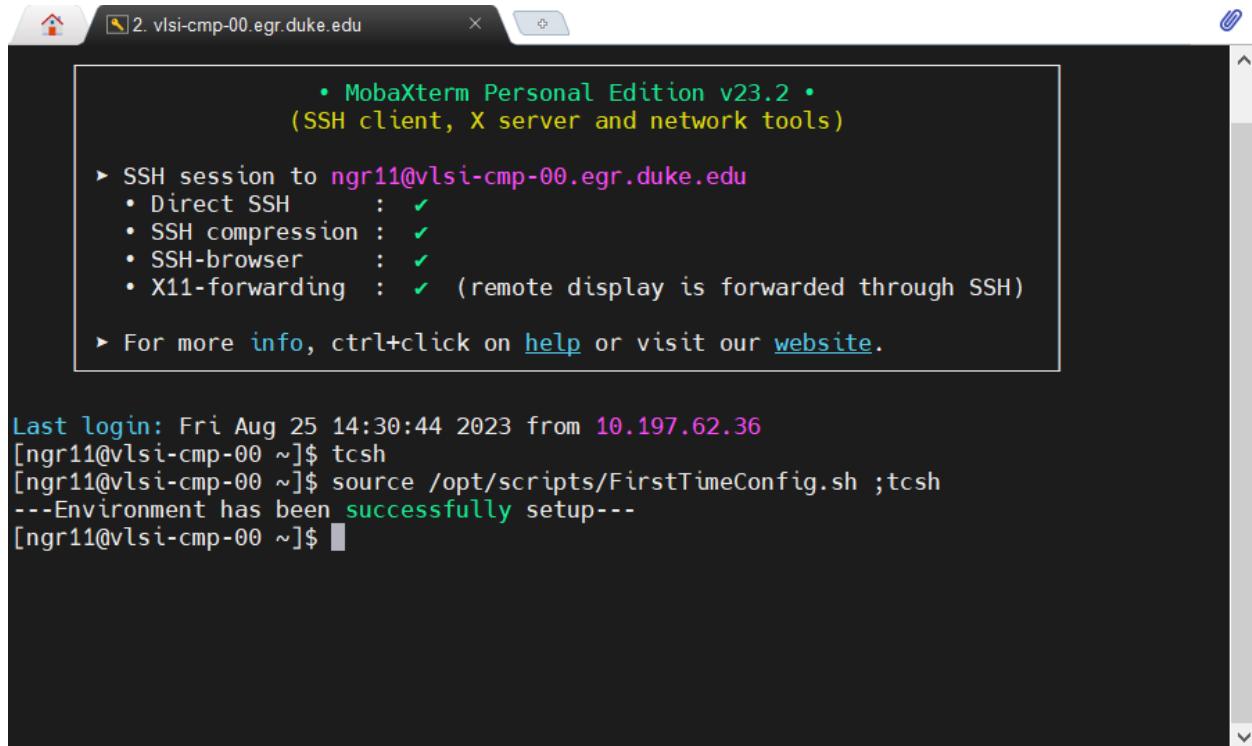
Since this is your first time starting up the server, we will need to setup the Cadence environment. Type the following in the terminal and press enter:

**tesh**

Then type the following command and press enter:

```
source /opt/scripts/FirstTimeConfig.sh ;tcsh
```

“---Environment has been successfully setup---” should appear, otherwise please alert the TA or CAD admins. Please note that you do not need to repeat this step every time you log in.



The screenshot shows a terminal window titled "2. vlsi-cmp-00.egr.duke.edu". The window displays the output of the command "source /opt/scripts/FirstTimeConfig.sh ;tcsh". The output includes the MobaXterm logo and version information, followed by a list of SSH session configurations (Direct SSH, SSH compression, SSH-browser, X11-forwarding) each marked with a green checkmark. A note at the bottom suggests for more information, to ctrl+click on help or visit the website. Below this, the terminal shows the user's last login details ("Last login: Fri Aug 25 14:30:44 2023 from 10.197.62.36") and the command being run again ("source /opt/scripts/FirstTimeConfig.sh ;tcsh"). The terminal concludes with the message "---Environment has been successfully setup---".

Next, we need to make a new directory as your working space. Type the following command and press enter:

```
mkdir workspace
```

Afterwards, type the following and press enter:

```
cd workspace
```

This command will allow you to change your current directory from the ‘desktop’ (~) to the ‘workspace’ directory you just made. Then, we need to set up the TSMC 65nm PDK. Type the following command while in your ‘workspace’ directory and press enter.

```
source /opt/scripts/setup_TSMC65.sh
```

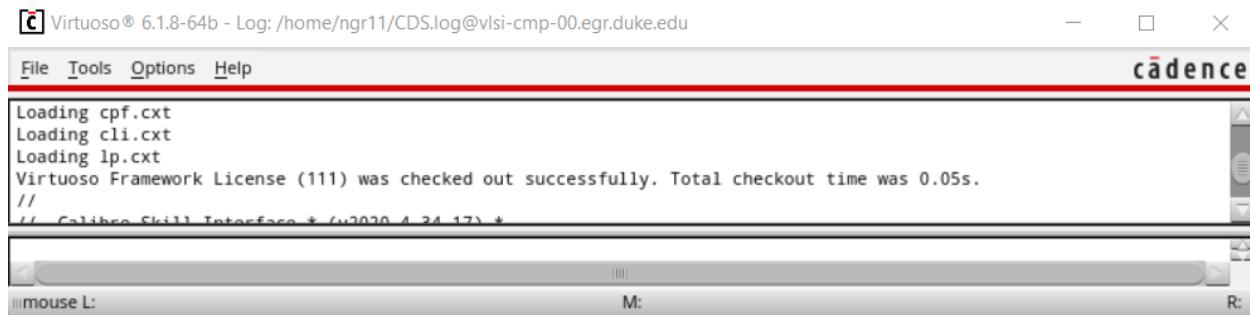
Please note that you only need to do this step once. Do not repeat this step in the same directory, because it will initialize the *cds.lib* and make Cadence lose track of your own libraries.

```
[ngr11@vlsi-cmp-00 ~]$ mkdir workspace
[ngr11@vlsi-cmp-00 ~]$ cd workspace
[ngr11@vlsi-cmp-00 ~/workspace]$ source /opt/scripts/setup_TSMC65.sh
```

Now we have setup all the files and we are ready to launch Cadence. Make sure you are either connected to Duke's Wi-Fi or Duke's VPN environment. To open the Cadence tool, enter the following into your terminal and press enter:

## **virtuoso &**

The following startup window should appear in a separate X11 window (not the terminal).



Now you are ready to use Cadence Virtuoso.

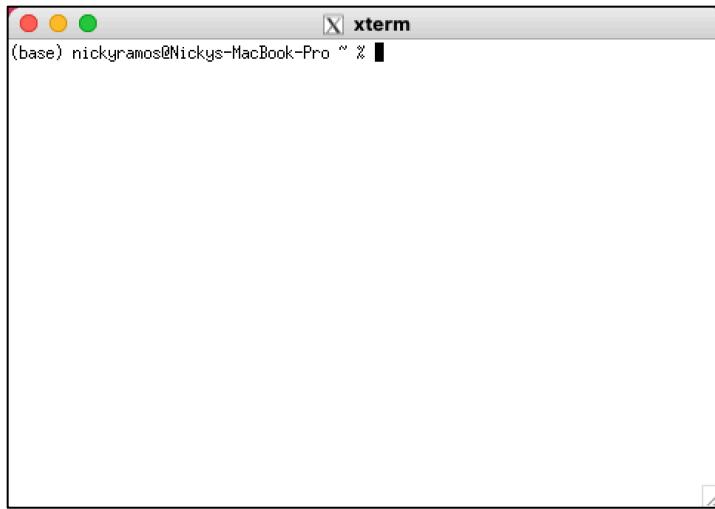
## **Mac Users**

To access the CAD tools using the server, download XQuartz:

<https://www.xquartz.org/>

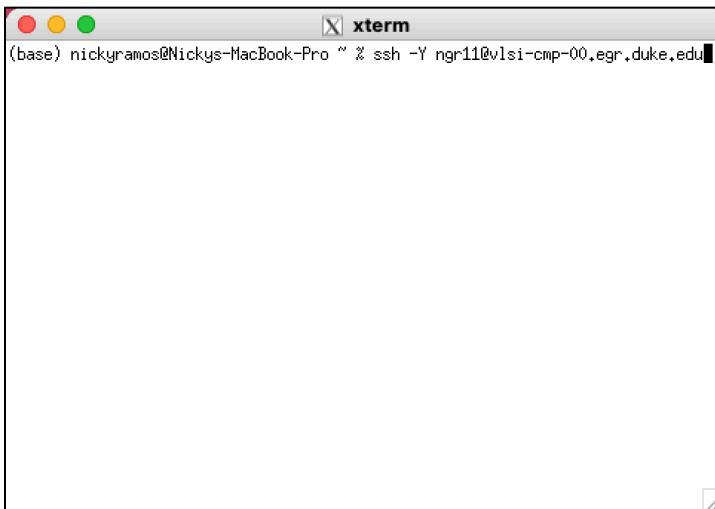
A screenshot of the XQuartz project website. The header features the XQuartz logo. The left sidebar has links for Home, Releases, Support, Contributing, Bug Reporting, and GitHub. The main content area starts with a paragraph about the project: "The XQuartz project is an open-source effort to develop a version of the X.Org X Window System that runs on macOS. Together with supporting libraries and applications, it forms the X11.app that Apple shipped with OS X versions 10.5 through 10.7." Below this is a "Quick Download" section with a table showing a package named "XQuartz-2.8.5.pkg". The table columns are "Download", "Version", "Released", and "Info". The "Download" column contains a link to the package. The "Version" column shows "2.8.5". The "Released" column shows "2023-01-26". The "Info" column states "For macOS 10.9 or later". At the bottom of the page is a "License Info" section with a note about the various licenses included in the distribution.

Click on the **XQuartz-2.8.5.pkg** package and follow the instructions to complete the setup. You may be asked to log out when the installation finishes. When you start XQuartz, you will see the following terminal:

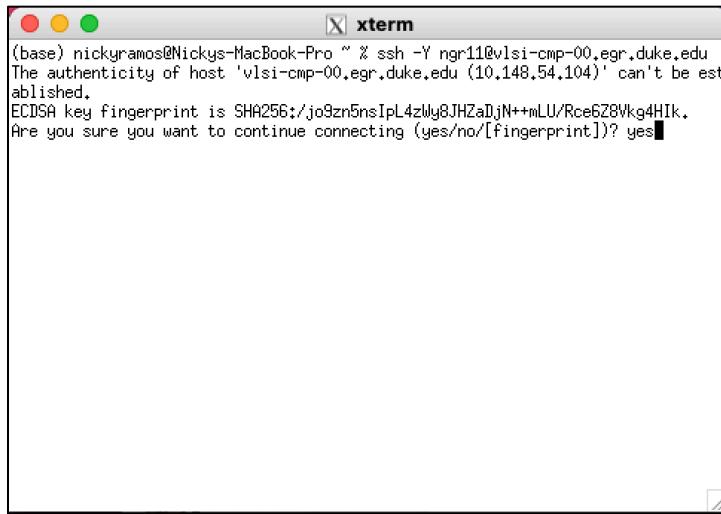


Type the following command into the terminal:

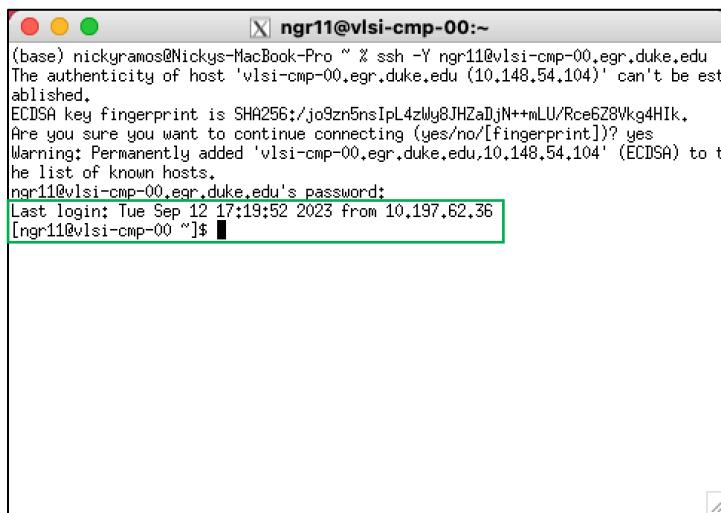
**ssh -Y <NetId>@vlsi-cmp-00.egr.duke.edu**



You may get a message saying that the authenticity of the host cannot be established. If you are asked to continue connecting, enter **yes** into the terminal.



You will then be prompted to enter your net ID password. Linux will automatically mask passwords, so it is normal if the terminal does not show what you type. If you successfully log in, you may see a message telling you when you last logged in. Most importantly, you should see that your directory is now <NetId>@vlsi-cmp-00.



Since this is your first time starting up the server, we will need to setup the Cadence environment. Type the following in the terminal and press enter:

**tcs**

Then type the following command and press enter:

**source /opt/scripts/FirstTimeConfig.sh ;tcs**

“---Environment has been successfully setup---” should appear, otherwise please alert the TA or CAD admins. Please note that you do not need to repeat this step every time you log in.

```

[nickylam@Nickys-MacBook-Pro ~] % ssh -Y ngr11@vlsi-cmp-00.egr.duke.edu
The authenticity of host 'vlsi-cmp-00.egr.duke.edu (10.148.54.104)' can't be established.
ECDSA key fingerprint is SHA256:/jo9zn5nsIpL4zW8JHZaDjN++mLU/Rce6Z8Vkg4HIk.
Are you sure you want to continue connecting (yes/no/[fingerprint])? yes
Warning: Permanently added 'vlsi-cmp-00.egr.duke.edu,10.148.54.104' (ECDSA) to t
he list of known hosts.
ngr11@vlsi-cmp-00.egr.duke.edu's password:
Last login: Tue Sep 12 17:19:52 2023 from 10.197.62.36
[ngr11@vlsi-cmp-00 ~]$ tcsh
[ngr11@vlsi-cmp-00 ~]$ source /opt/scripts/FirstTimeConfig.sh ;tcsh
---Environment has been successfully setup---
[ngr11@vlsi-cmp-00 ~]$ 

```

Next, we need to make a new directory as your working space. Type the following command and press enter:

**mkdir workspace**

Afterwards, type the following and press enter:

**cd workspace**

This command will allow you to change your current directory from the ‘desktop’ (~) to the ‘workspace’ directory you just made. Then, we need to set up the TSMC 65nm PDK. Type the following command while in your ‘workspace’ directory and press enter.

**source /opt/scripts/setup\_TSMC65.sh**

Please note that you only need to do this step once. Do not repeat this step in the same directory, because it will initialize the *cds.lib* and make Cadence lose track of your own libraries. I named my directory ‘workspace2’ for this reason.

```

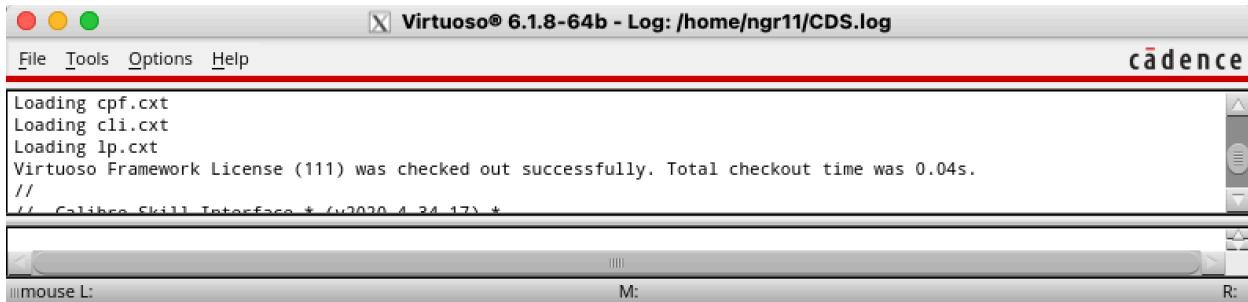
[ngr11@vlsi-cmp-00 ~]$ mkdir workspace2
[ngr11@vlsi-cmp-00 ~]$ cd workspace2
[ngr11@vlsi-cmp-00 ~/workspace2]$ source /opt/scripts/setup_TSMC65.sh

```

Now we have setup all the files and we are ready to launch Cadence. Make sure you are either connected to Duke’s Wi-Fi or Duke’s VPN environment. To open the Cadence tool, enter the following into your terminal and press enter:

**virtuoso &**

The following startup window should appear in a separate X11 window (not the terminal).

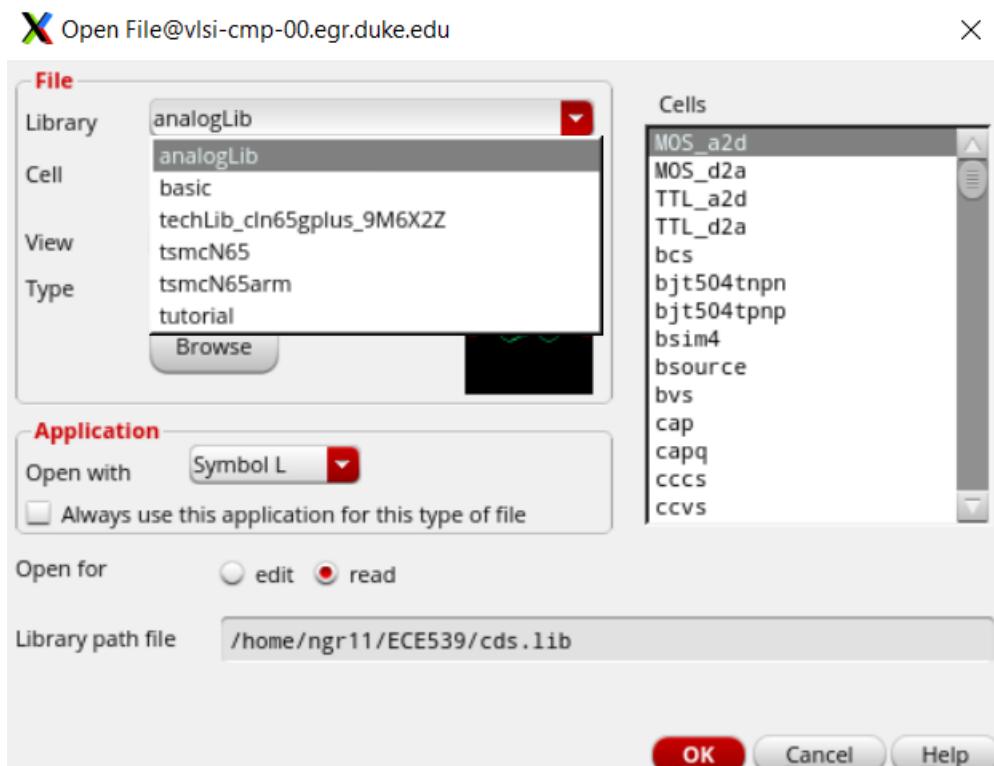


Now you are ready to use Cadence Virtuoso. Special thank you to Tergel Molom-Ochir and Tom Napoles for help with figuring out the Mac setup.

## 2. Open an Existing Design in Virtuoso

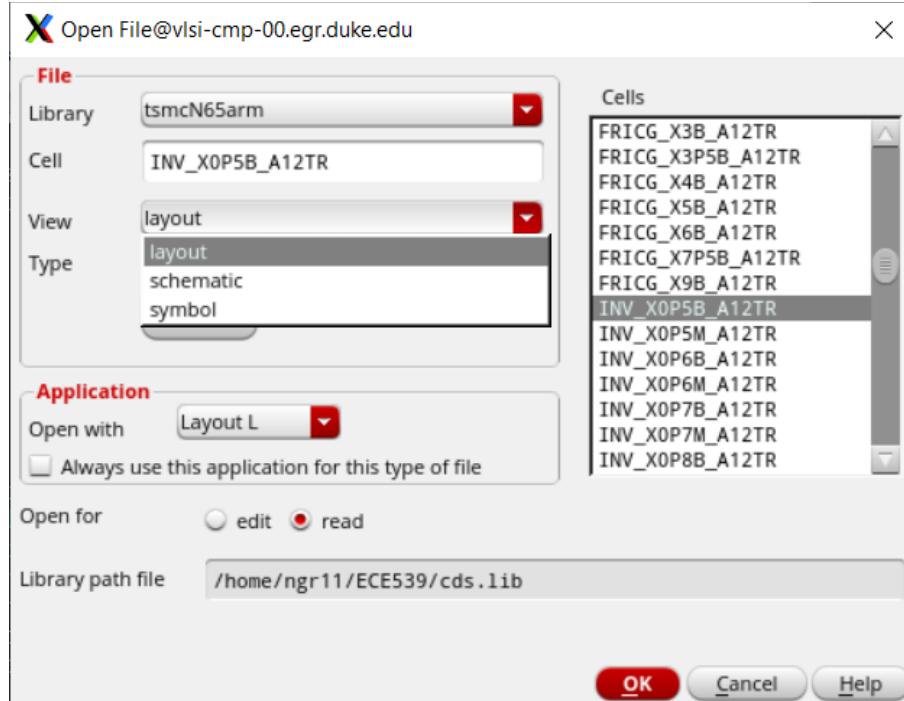
Click the following:

- *File -> Open*

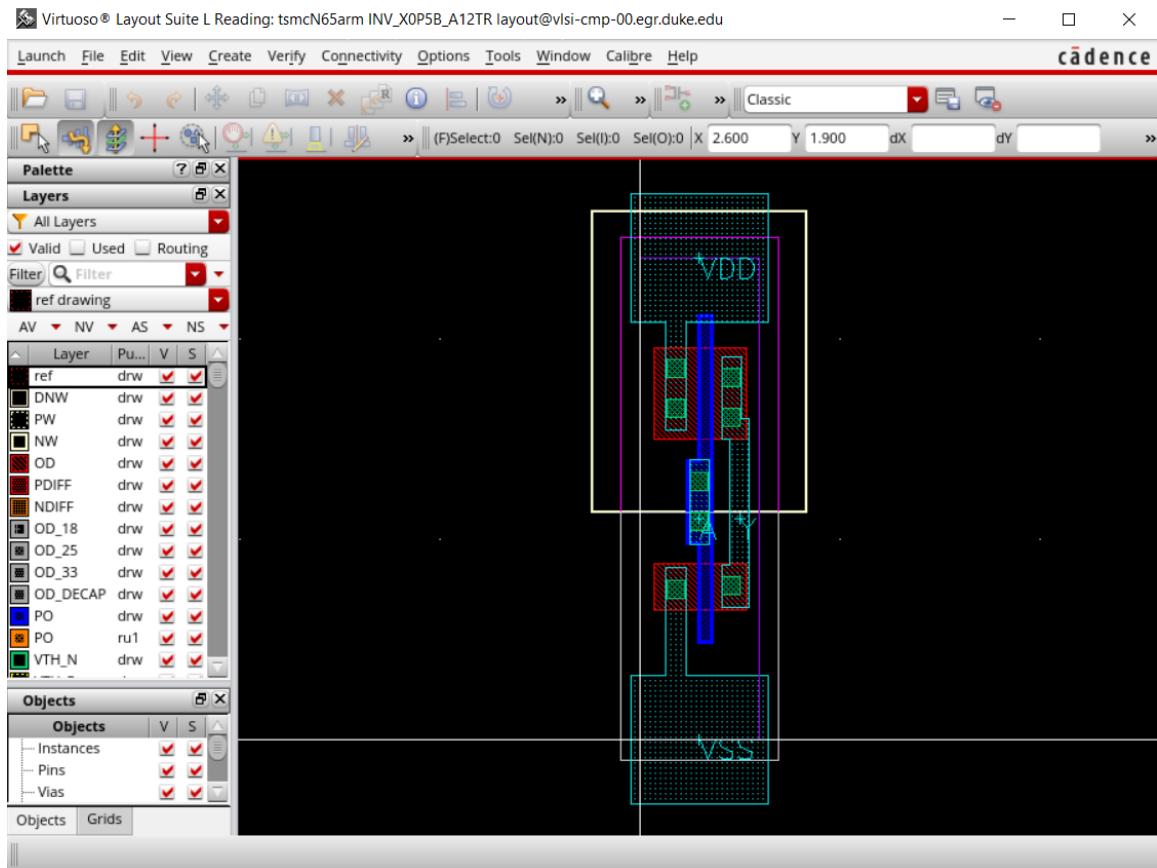


- Click ‘tsmcN65arm’ in the *Library* tab. Type ‘INV\_X0P5B\_A12TR’ in the *Cell* tab. Choose ‘Layout’ in the *View* tab.

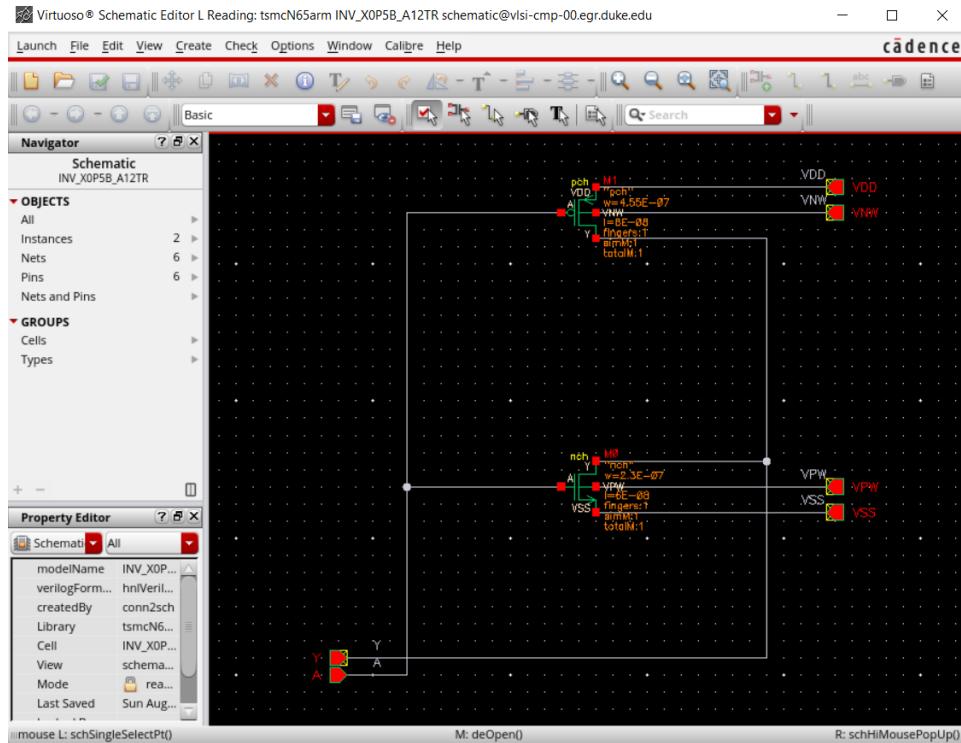
In Cadence, there are usually three key views for one circuit component: Schematic, Symbol, and Layout.



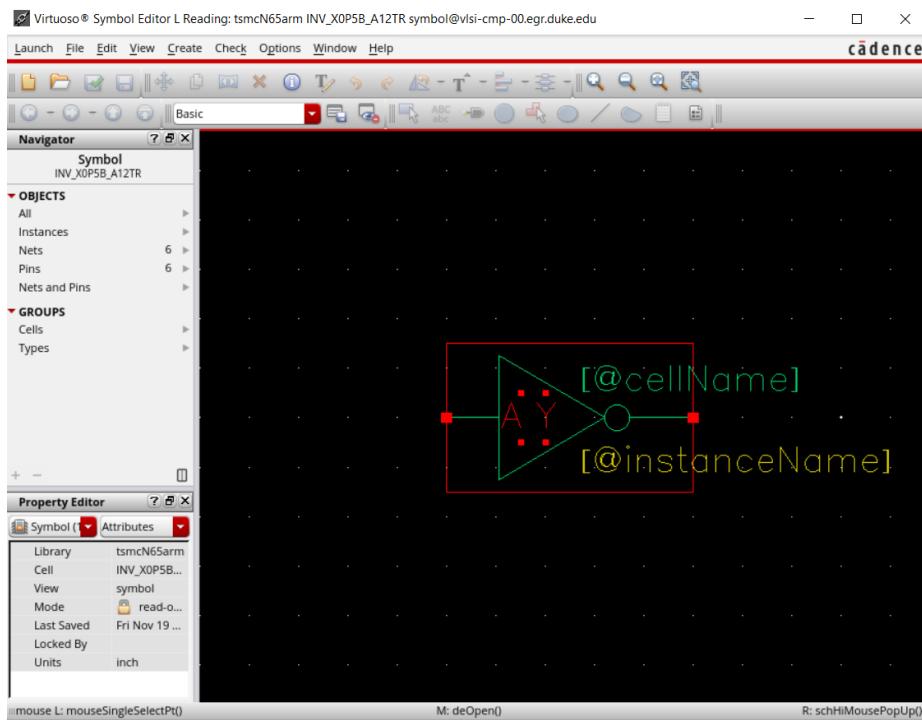
- Click *OK* and we can launch the ‘Layout L’ to view the layout.



- Close the layout and open the file again. This time, change the view to Schematic to open the schematic editor.



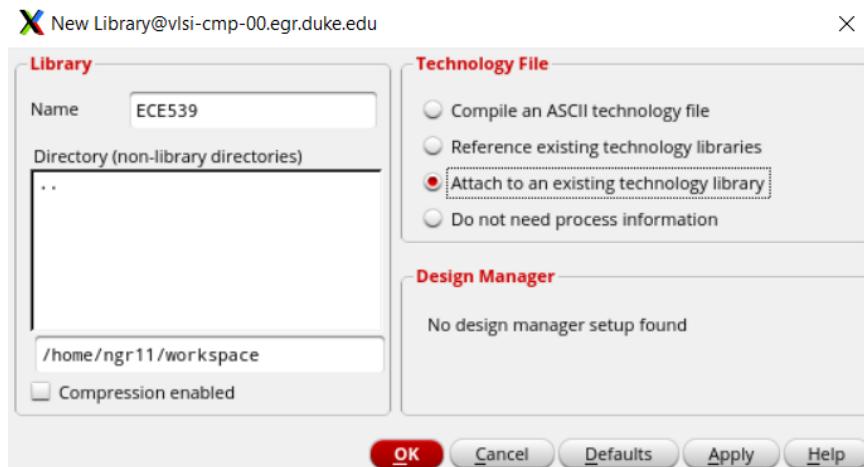
- Close the schematic and open the file again. This time, change the view to Symbol to open the symbol editor.



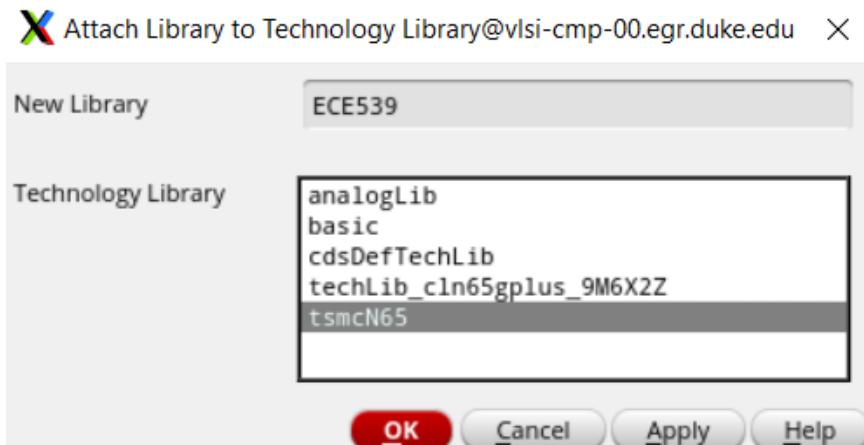
### 3. Create a New Project in Cadence Virtuoso

Now we need to create a new library by clicking the following (edit the new library name and choose ‘Attach to an existing technology library’), then click *OK*.

- *File -> New -> Library*



- In the Technology File section, select ‘Attach to an existing technology library.’

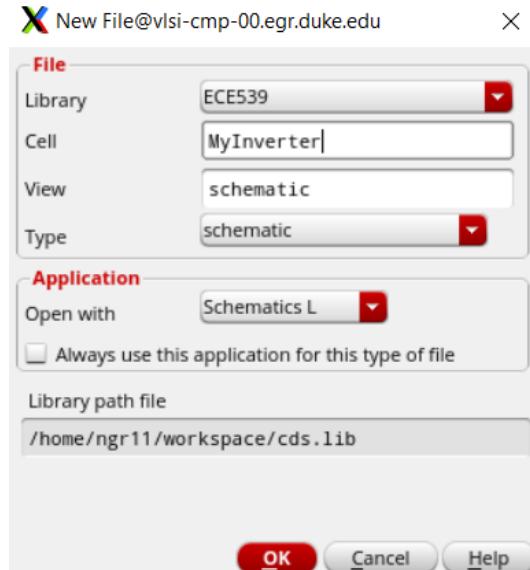


- Click ‘tsmcN65’ and then click *OK*.
- After this, you can also check your cds.lib file to see if the newly created library is there.

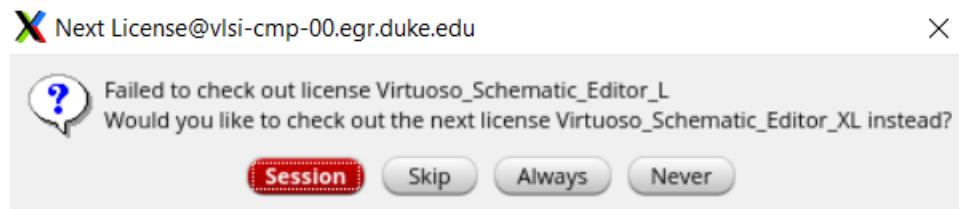
### 4. Schematic Design of an Inverter

Create a new project by clicking the following:

- *File -> New -> Cellview*

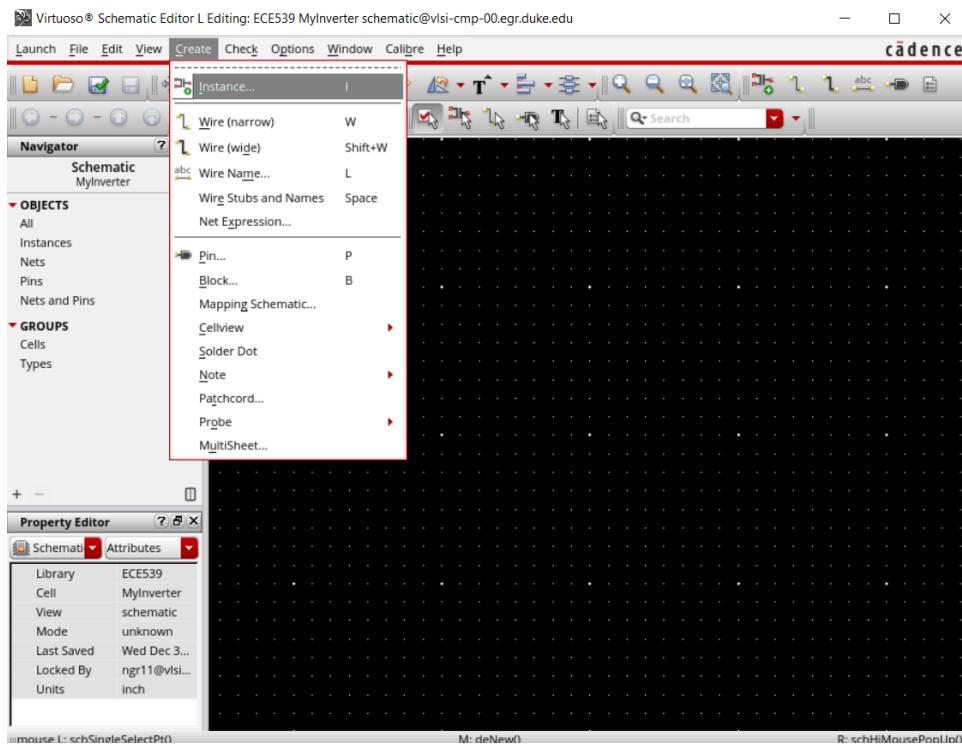


Type the name of the cell and click *OK*. You may receive a notice indicating that Cadence has failed to check out a schematic license. If this happens, click *Session* and then the Schematic editor will appear.

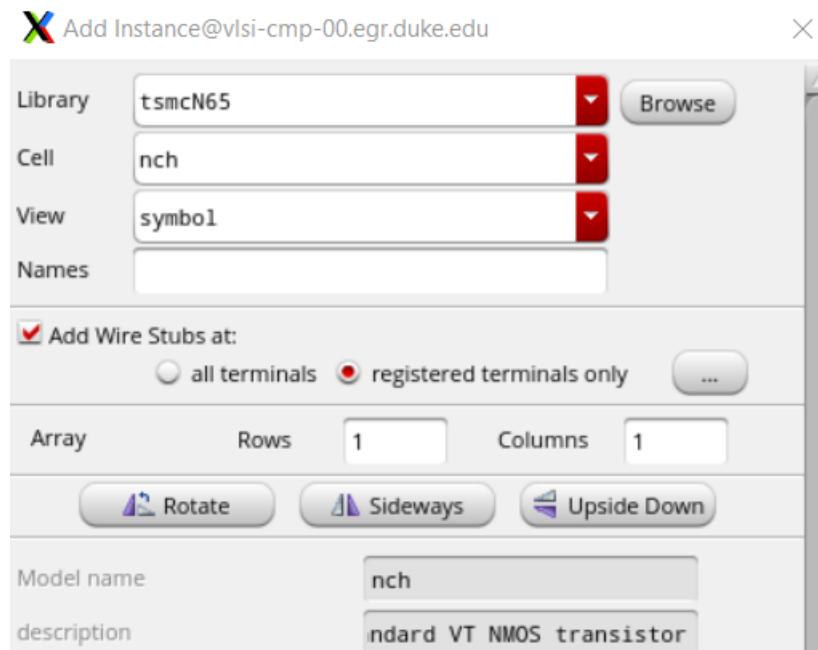


Now you need to add the circuit instance in the schematic editor:

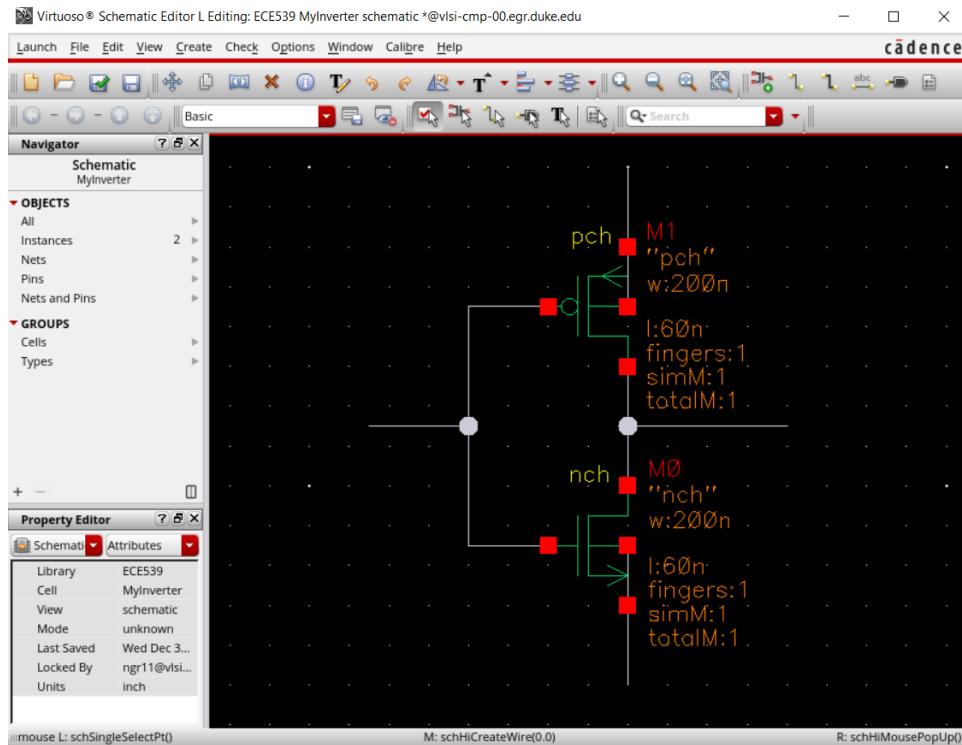
- *Create -> Instance* (or press the 'I' key).



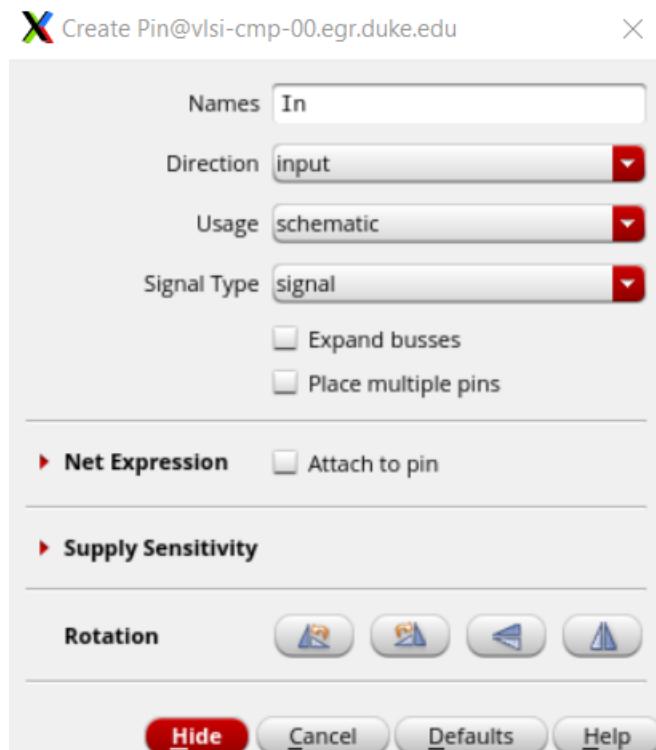
- Type tsmcN65 in *Library*.
- Type nch (pch) in *Cell* to create a NMOS (PMOS) transistor, then click the schematic window once you choose an instance to place it on the schematic.



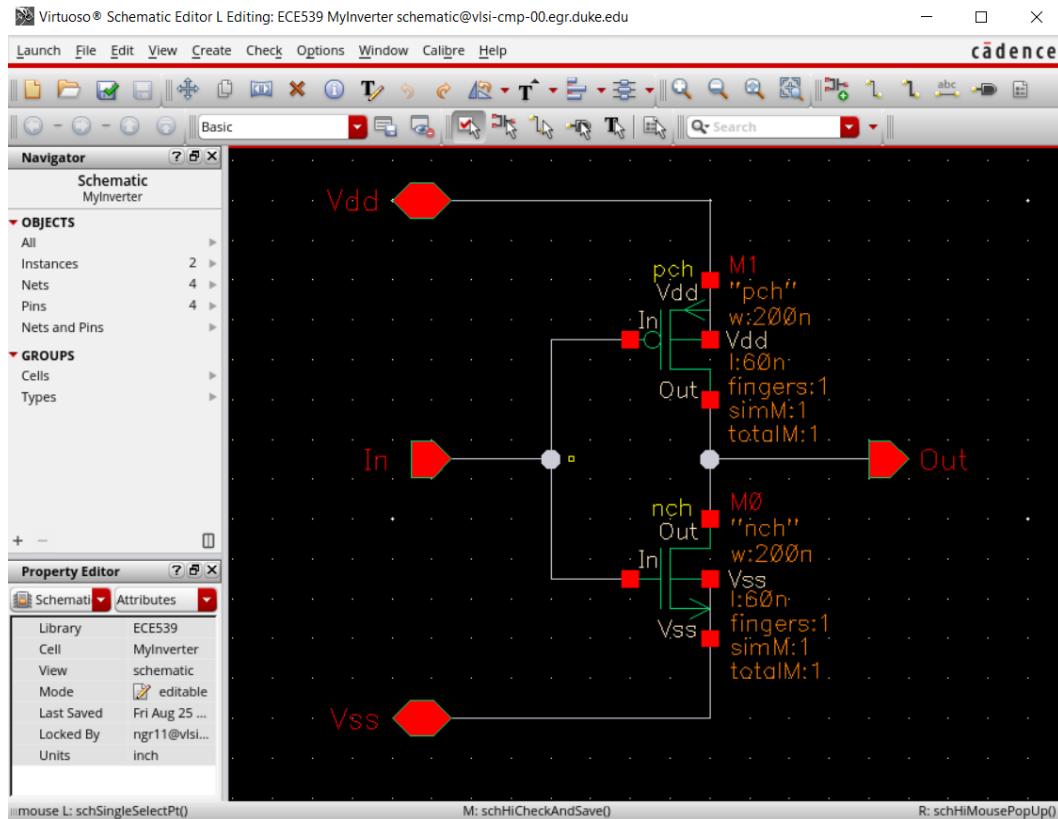
- Connect two transistors to form an inverter by using the hot key ‘W’. Do not forget to wire the bulk to Vdd (Vss) for pch (nch) in this example circuit.



- Create ports for In, Out, Vdd and Vss. The hot key is ‘P’.



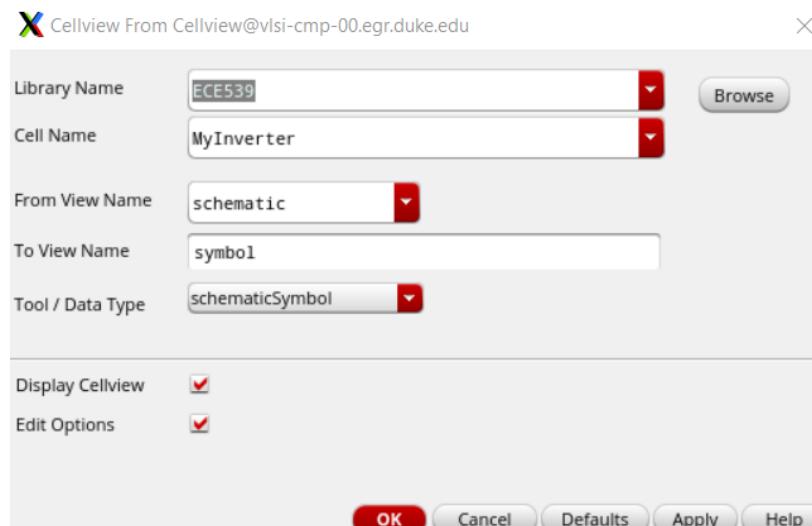
- The port (Direction) for In is ‘input,’ Out is ‘output’ and the Vdd and Vss is ‘inputOutput,’ and click *Check and Save*. The instance property can also be changed later in Property Editor shown on the left bottom corner of the schematic window.



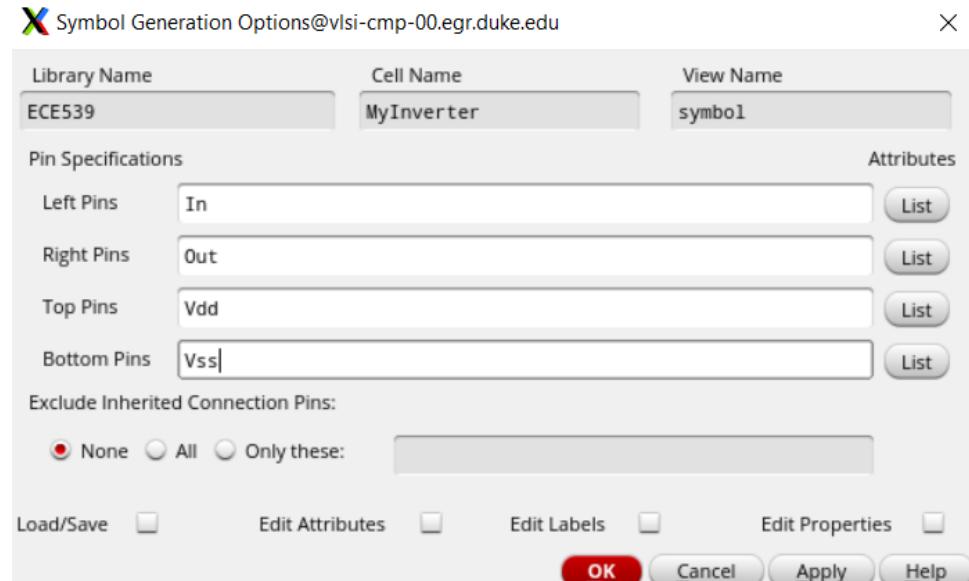
- There should be no errors or warnings if all the connections are correct.

Create the symbol for this component by clicking the following:

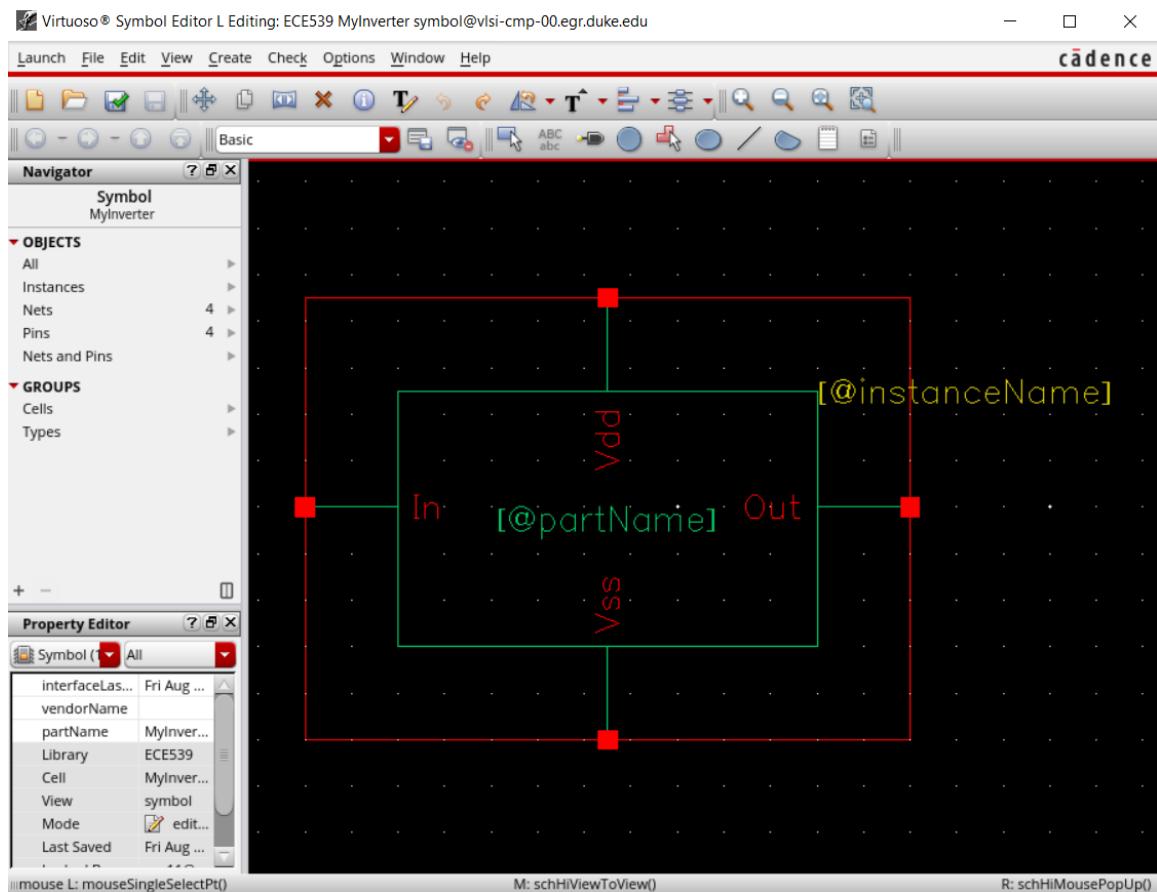
- Create -> Cellview -> From Cellview*



- Change the direction of the ports as follows:



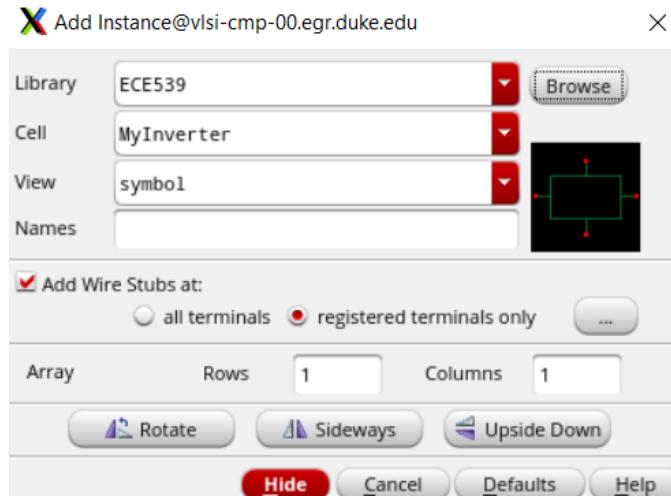
- Now you can edit the symbol (explore by yourself) or directly use the automatically generated symbol:



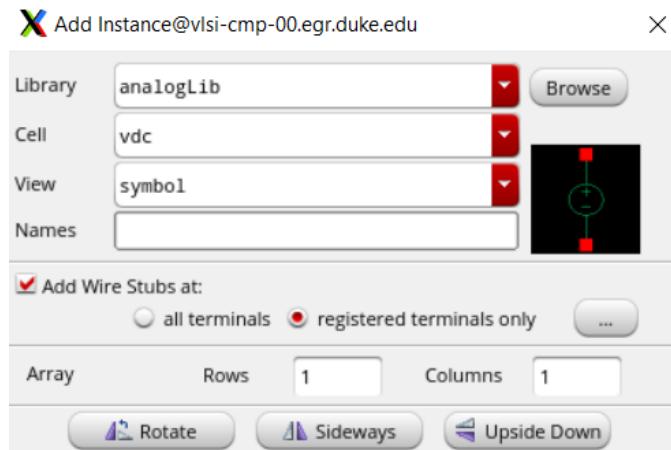
## 5. Simulate your Inverter

Create a new schematic called MyInverterTest and do the following:

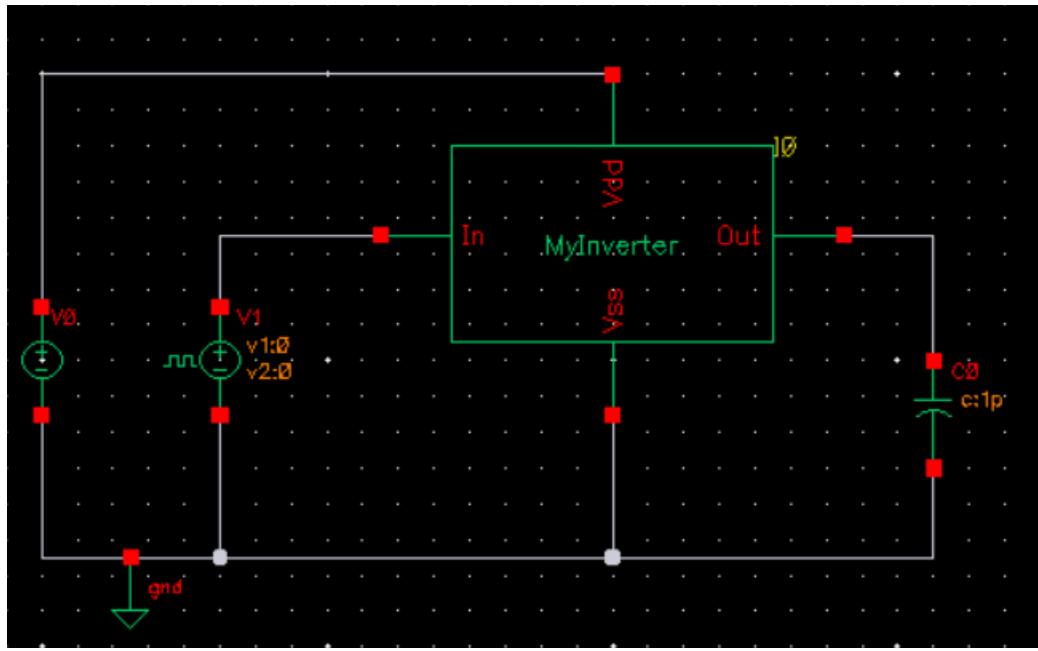
- Add your inverter to the schematic.



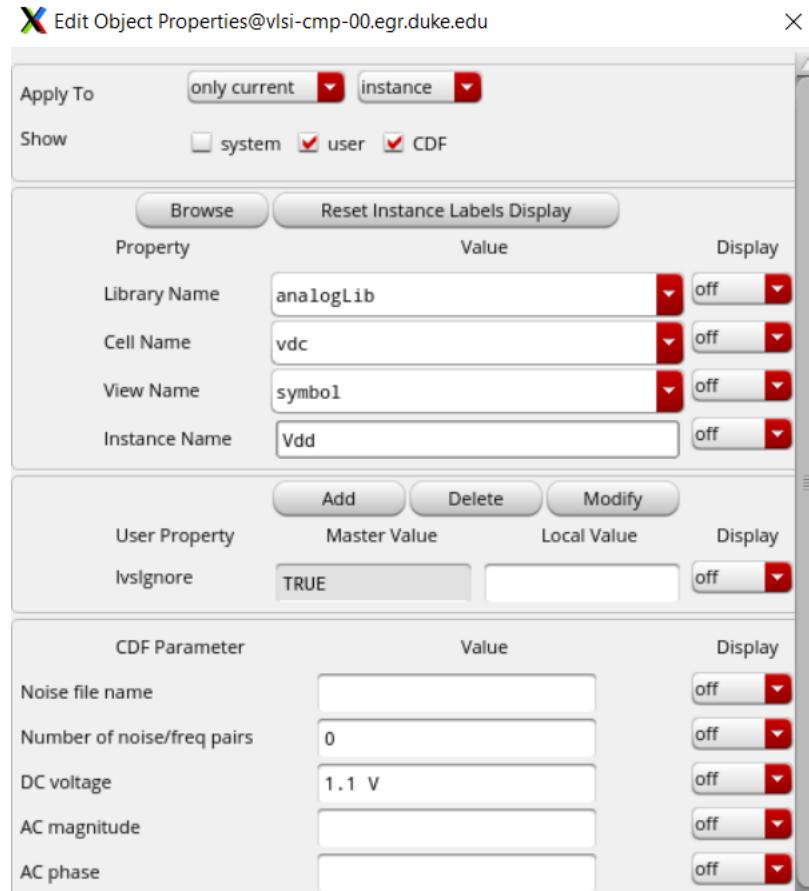
- Add a DC voltage source by using the 'vdc' component in the analogLib.



- Add a ground by using the 'gnd' component in the analogLib.
- Add a voltage pulse by using the 'vpulse' component in the analogLib.
- Add a capacitor by using the 'cap' component in analogLib.
- Connect all the circuit components as follows.

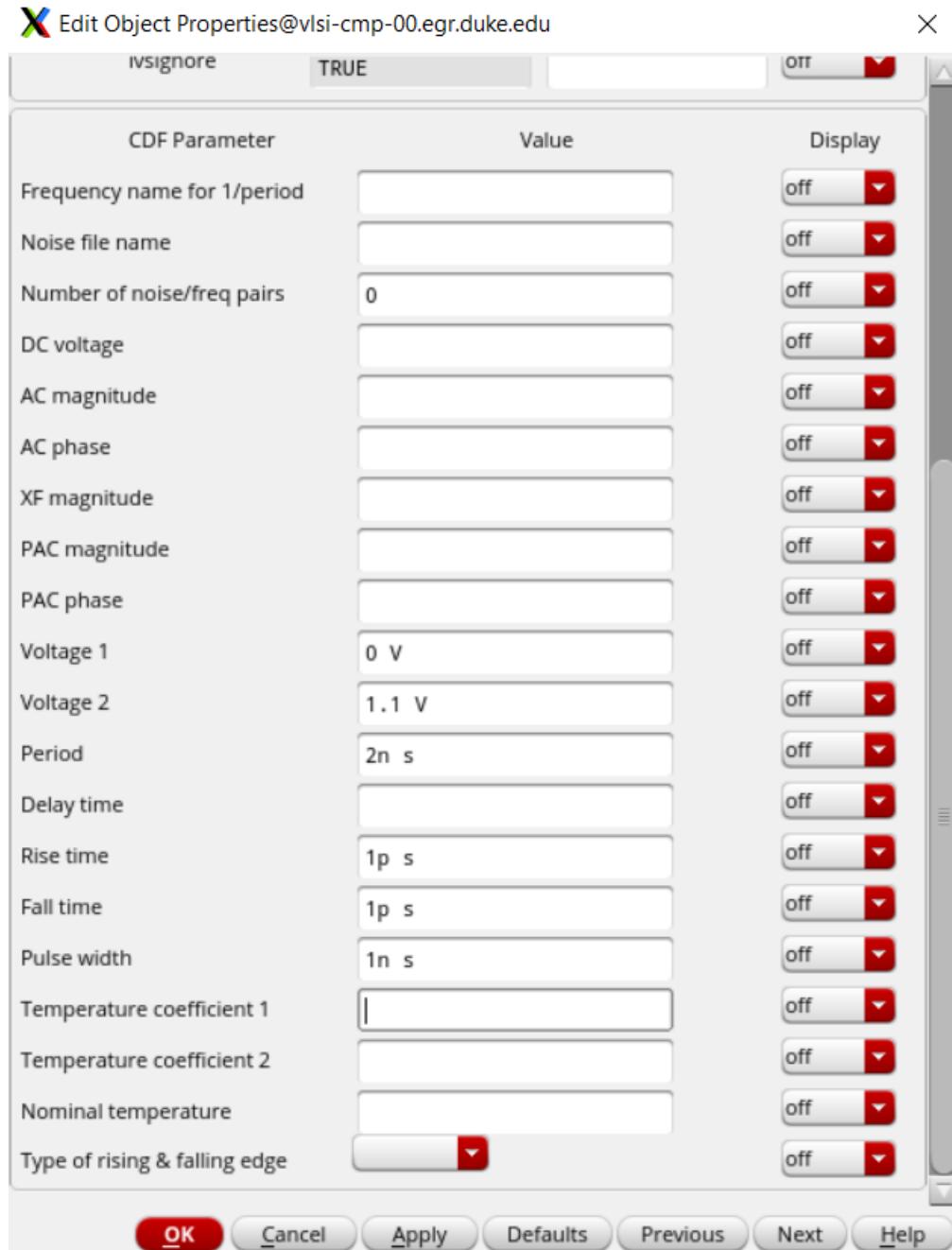


- Right click the ‘vdc’ instance and select *Properties* (the hot key is ‘Q’).



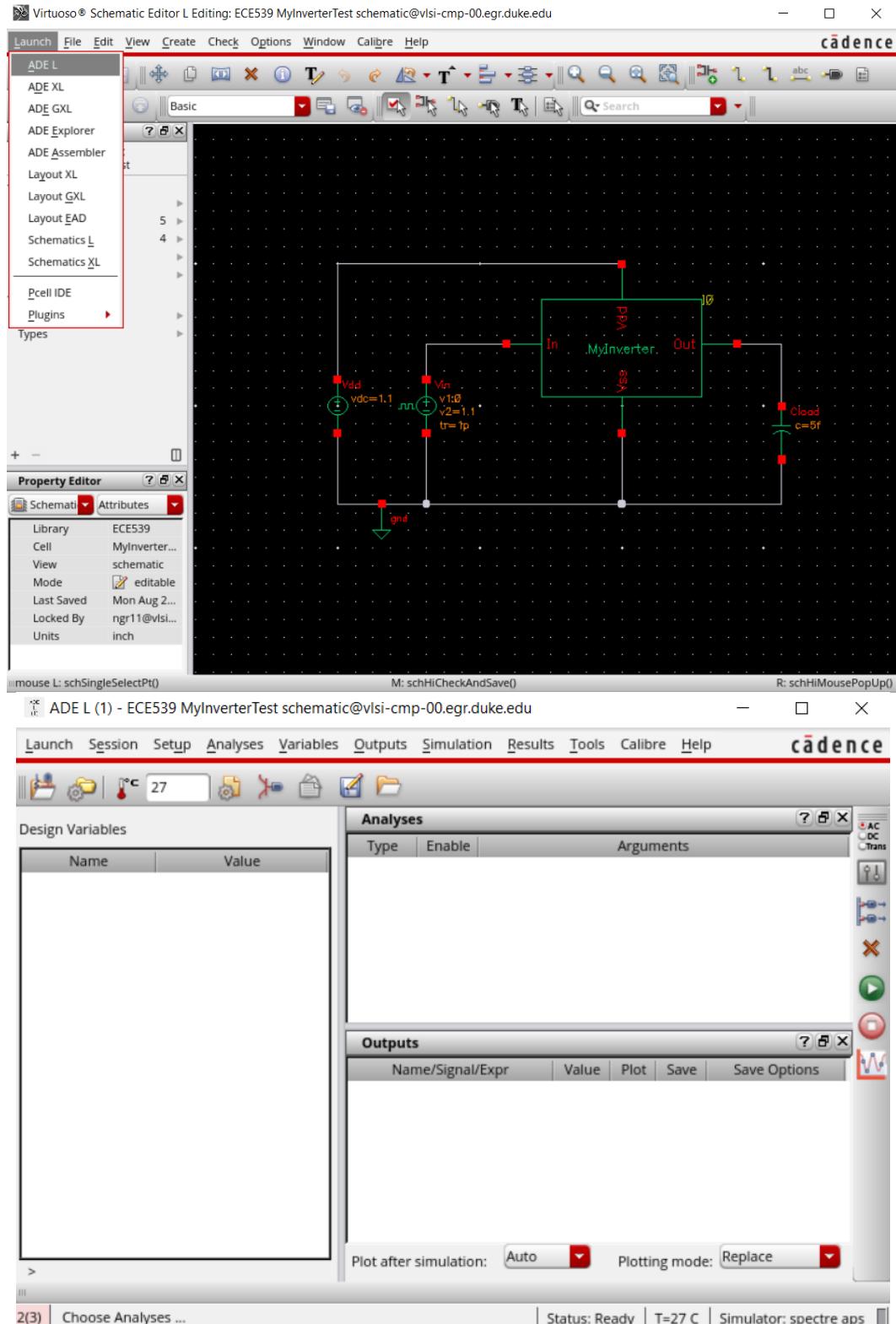
- Change the instance name to ‘Vdd’ (optional) and set the DC voltage to 1.1.

- Edit the property of the ‘vpulse’ instance. Change the instance name to ‘Vin’ (optional) and set Voltage1 to 0, Voltage2 to 1.1, and other parameters as follows. Notice that you do not need to type the units. For example, type 2n instead of 2n s.

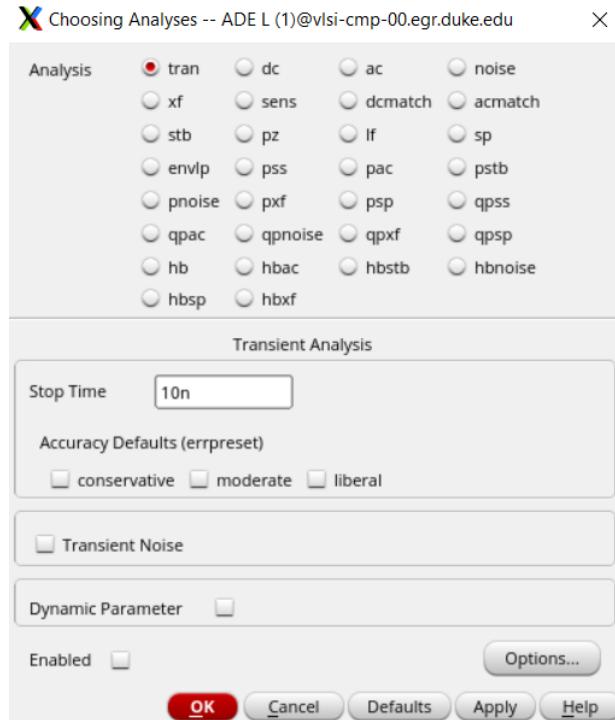


- Change the capacitor value to 5f. After this, click *Check and Save* and there should be no error or warning.

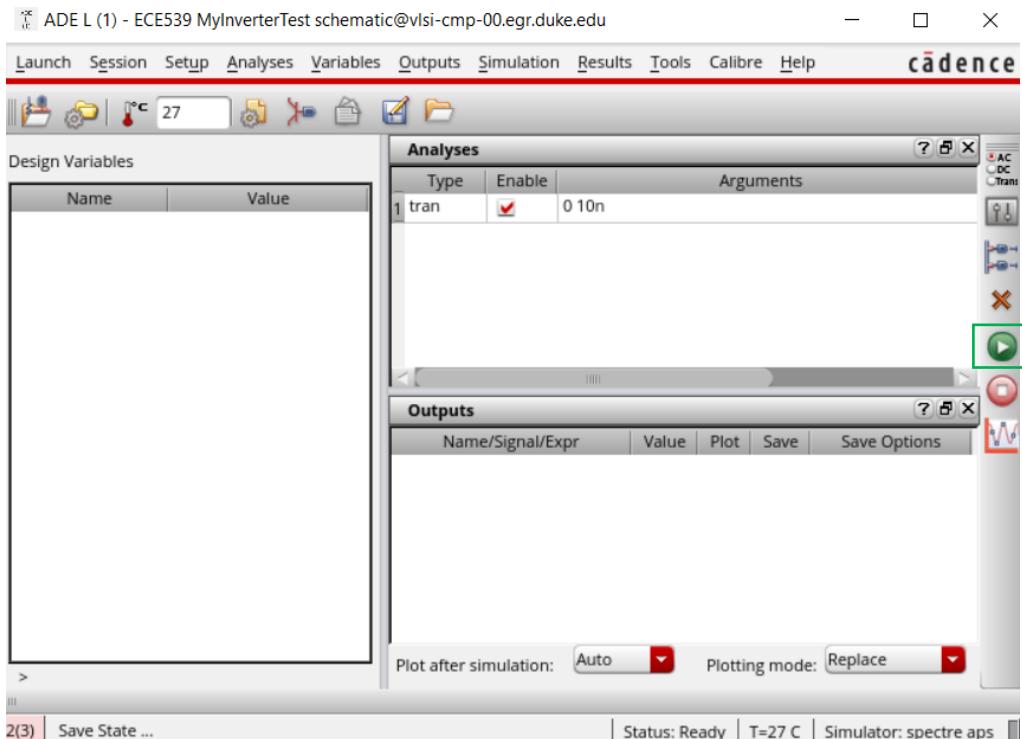
- Now we need to open the simulator: *Launch -> ADE L*. You may receive a notice indicating that Cadence has failed to check out a license. If this happens, click *Session* until the notice disappears.



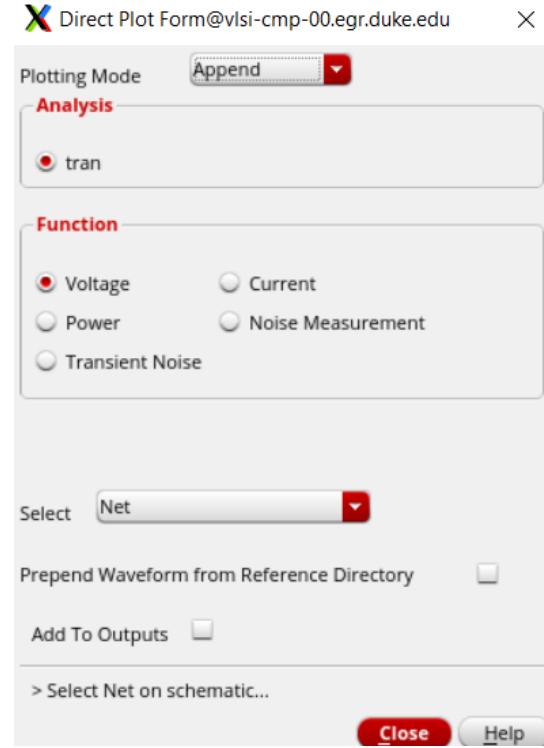
- Now we need to setup the simulation environment: *Analyses -> Choose*. Use the ‘tran’ simulation mode and set the stop time to 10n.



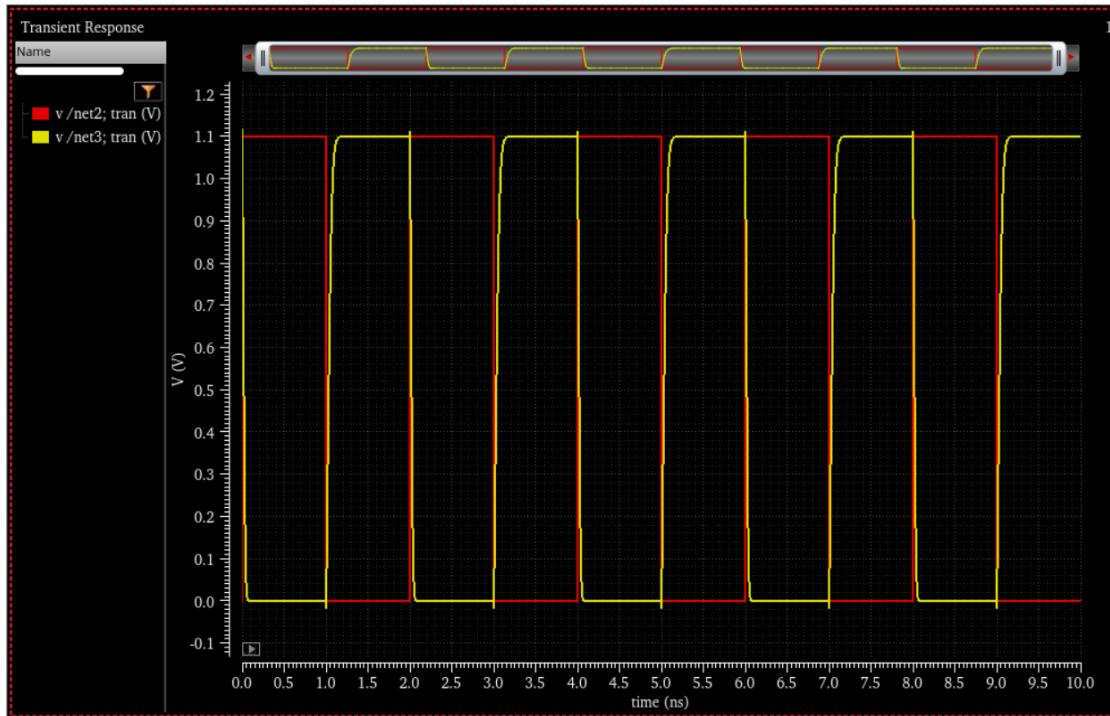
- Click *Simulation -> Netlist and Run* (the green play button) to simulate.



- To show the simulation result, click as follows: *Results -> Direct Plot -> Main Form*. The following window will appear. Please do not close it until you are done viewing the waveforms.



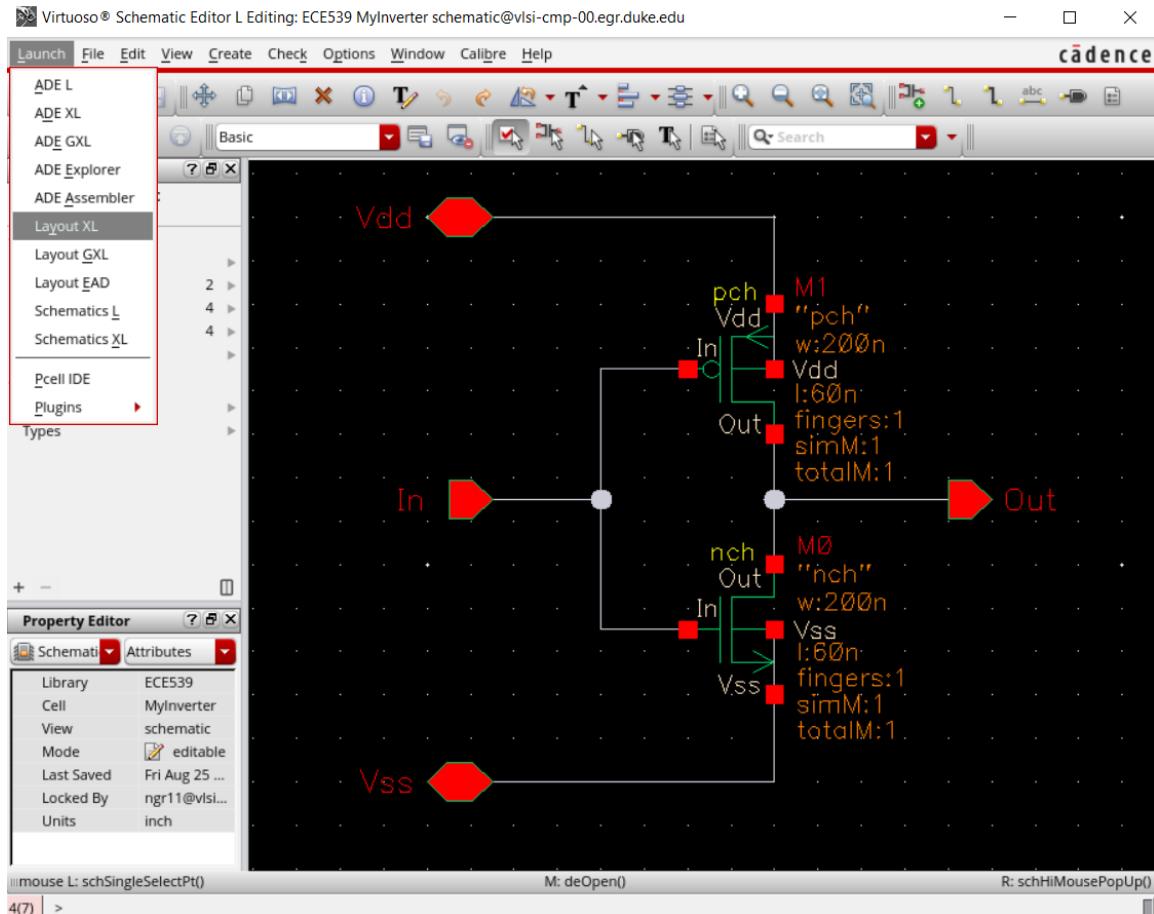
- Click the input and output wire of the inverter, and you can see the simulated waveform.



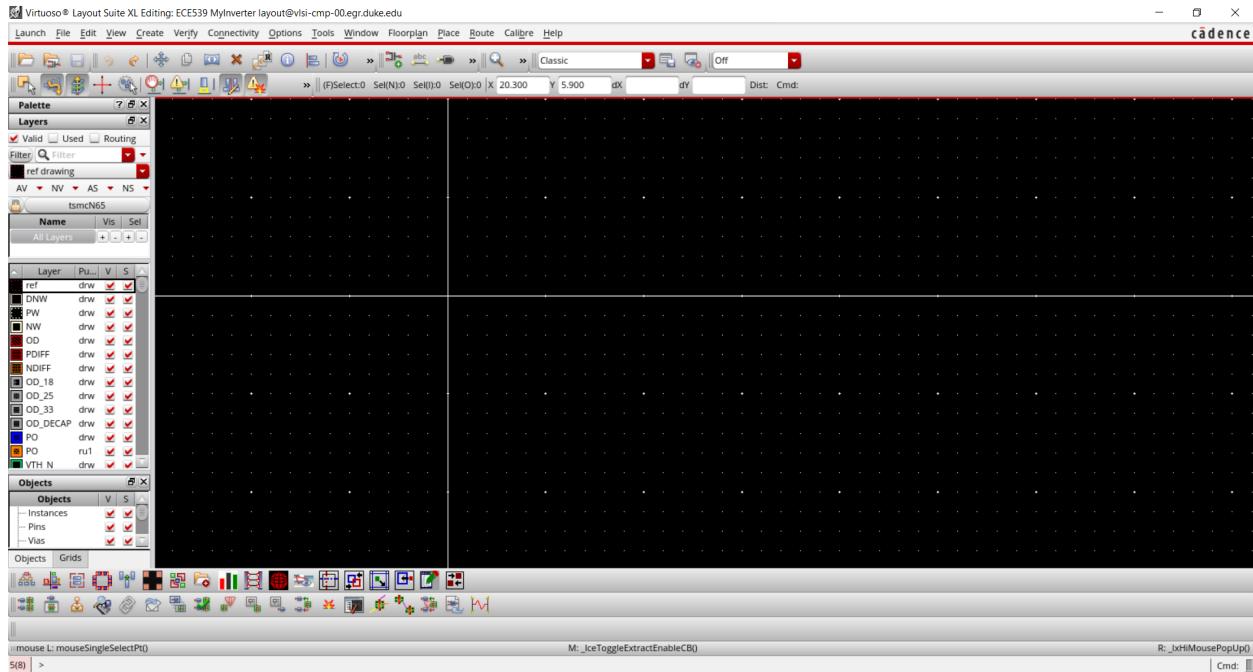
## 6. Create the Layout of your Inverter

Open the schematic of the MyInverter and click as follows to run the layout editor.

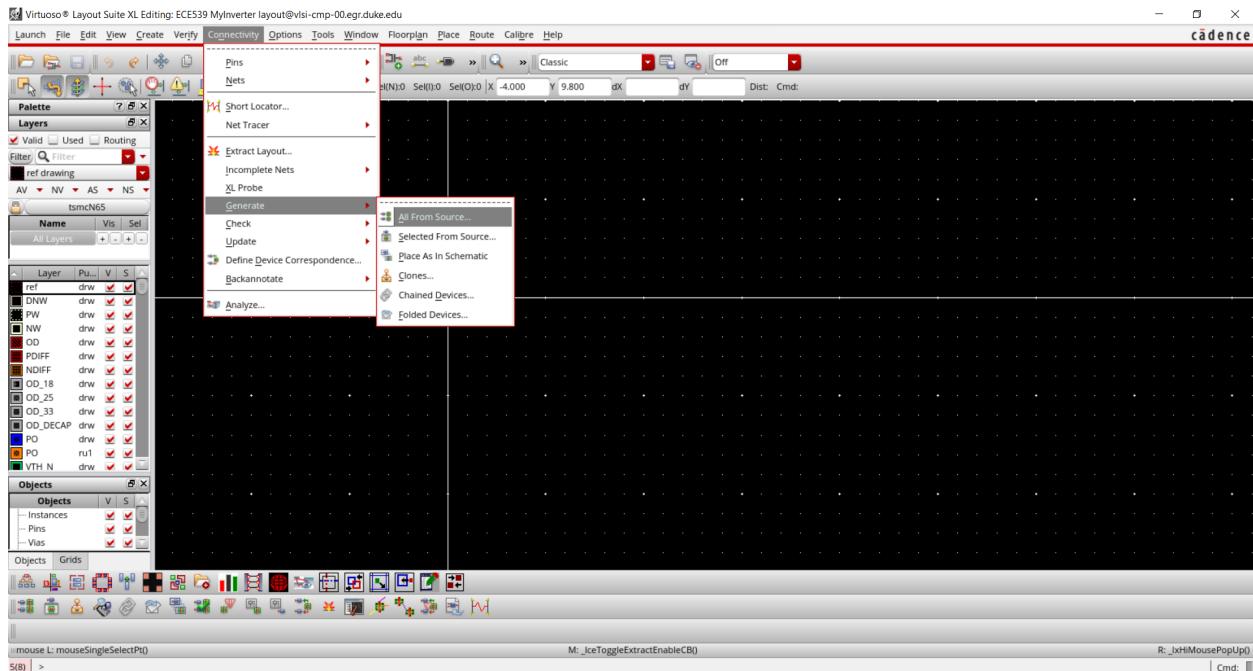
- *Launch -> Layout XL*

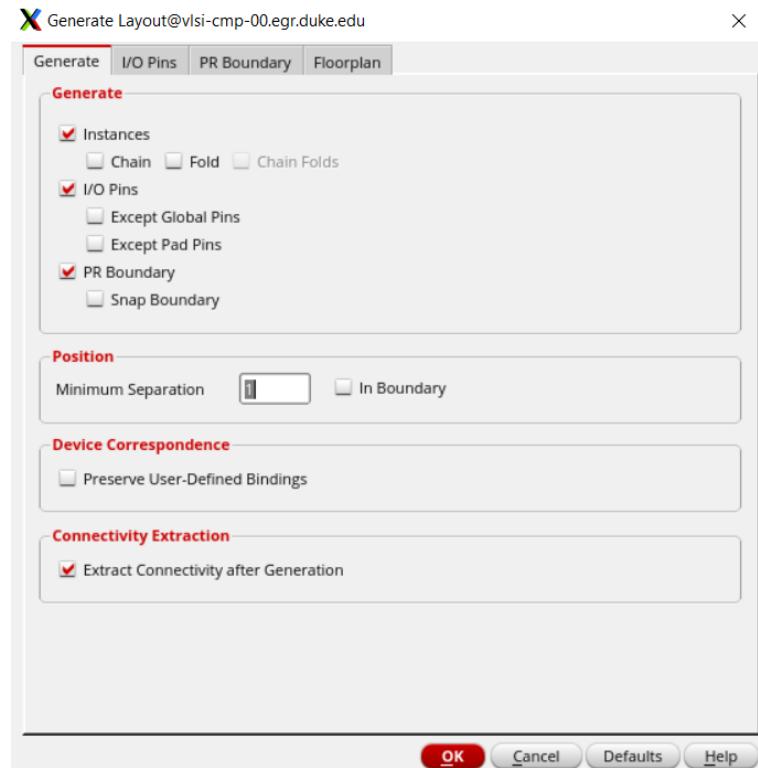


- You may receive a notice indicating that Cadence has failed to check out a license. If this happens, click *Session* until the notice disappears.

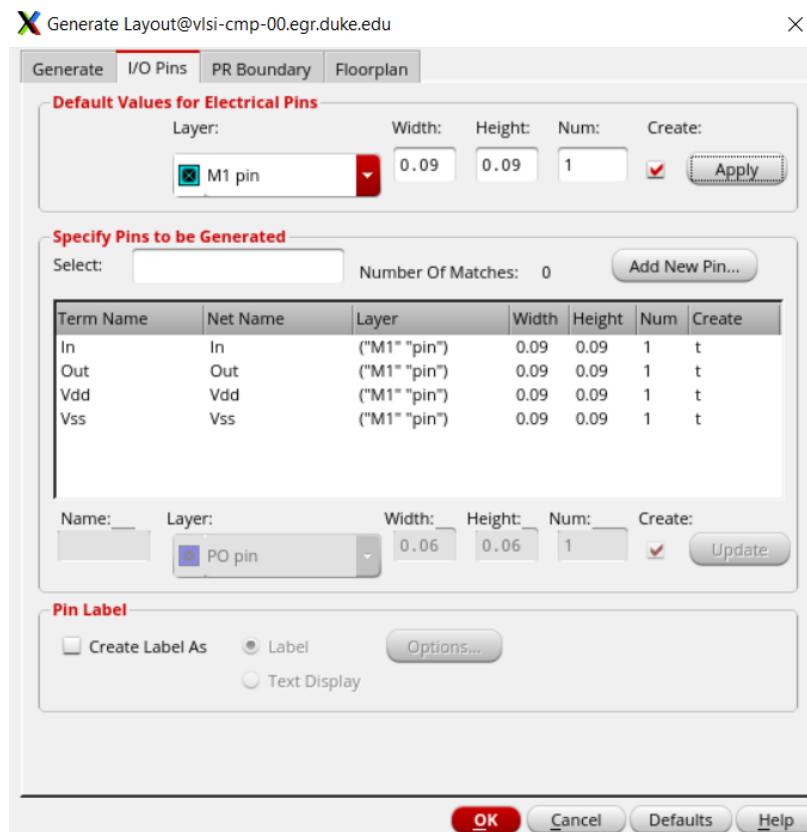


- The way to create the layout is very versatile. Here we introduce a common and simple way. The first step is to place the transistors in the layout editor: **Connectivity -> Generate -> All From Source**

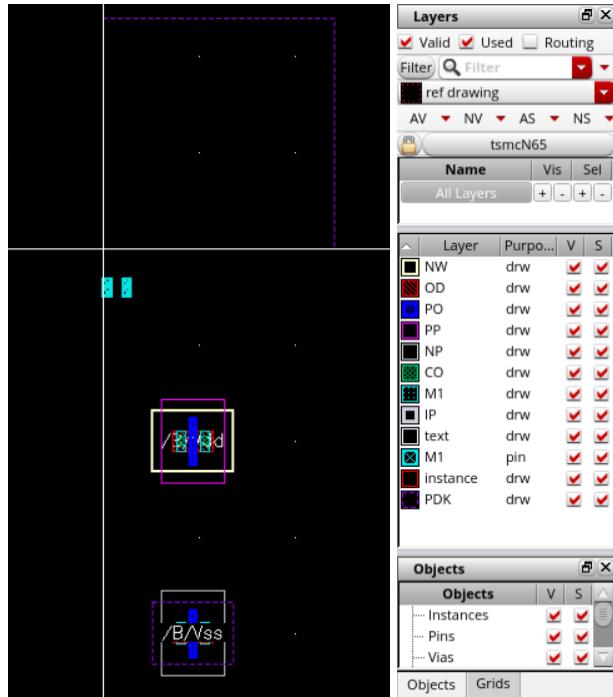




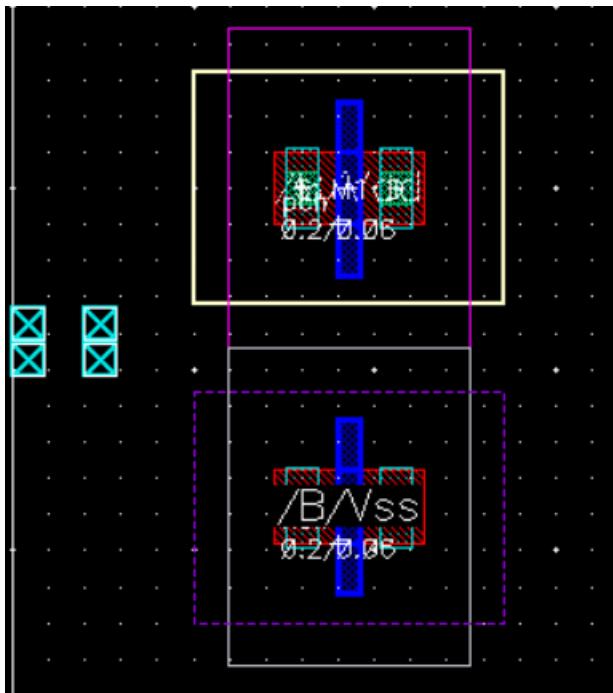
- Click I/O Pins and set as follows.



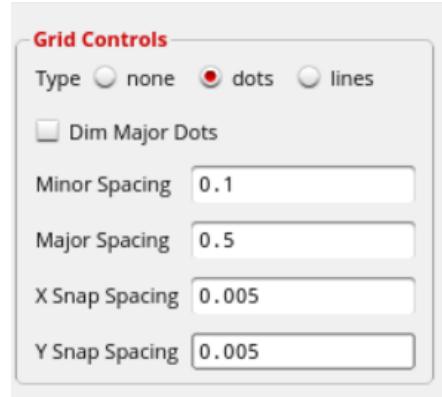
- The generated layout will be like this. If you cannot see the layer information, press 'shift+F' to see all the layers. You can also change the layer-wise view at the left panel. Keep the layout at the center of the screen by pressing 'F'.



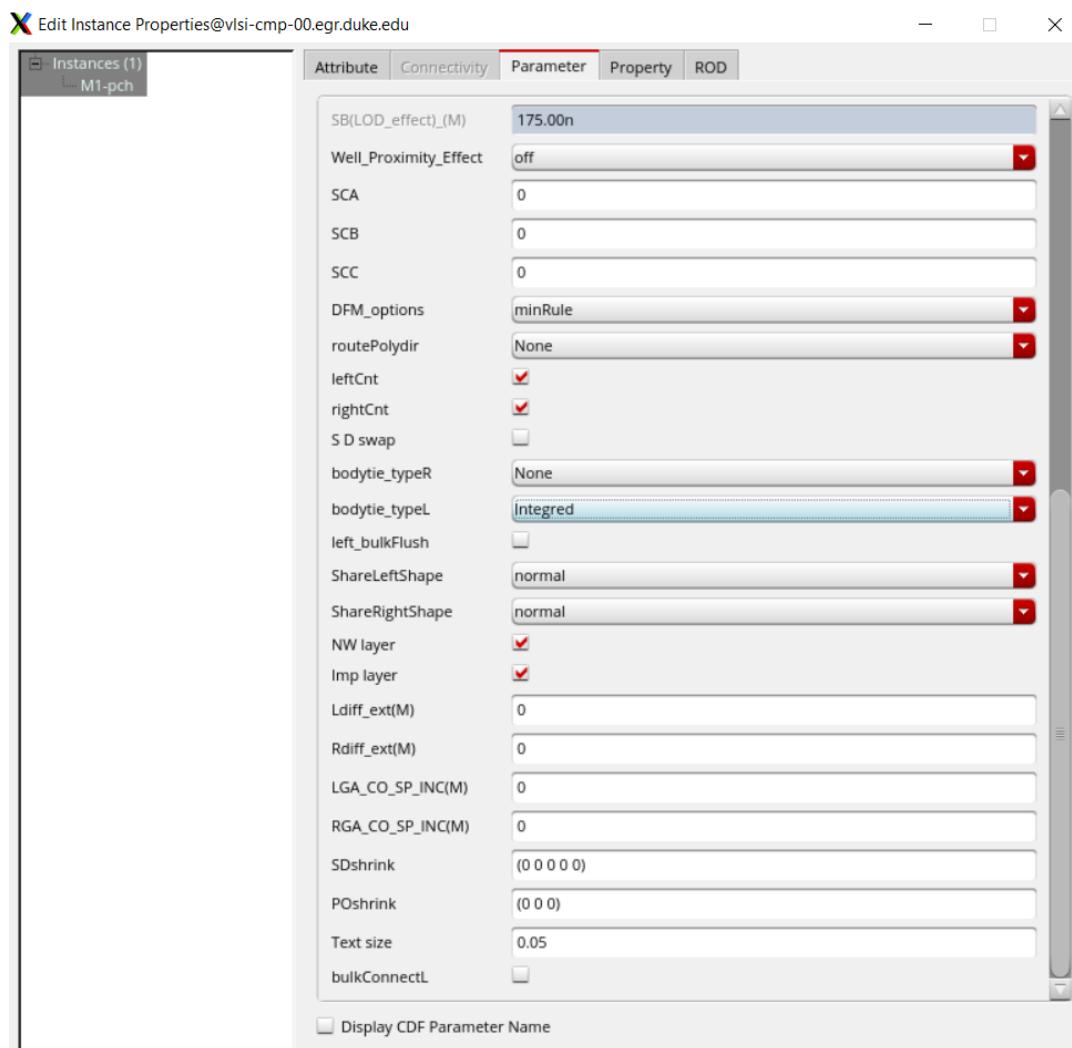
- Move the NMOS and PMOS devices closer to each other. A simple way is to place the PP and NP layer next to each other.



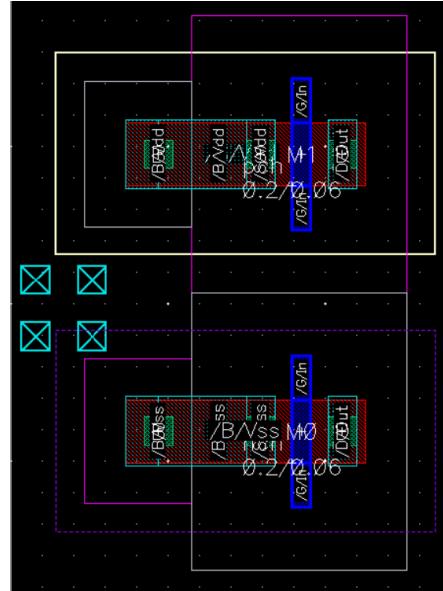
- If you have trouble placing the PP and NP layers next to each other, this means that you need to change the grid spacing. Click on *Options -> Display* and set the following:



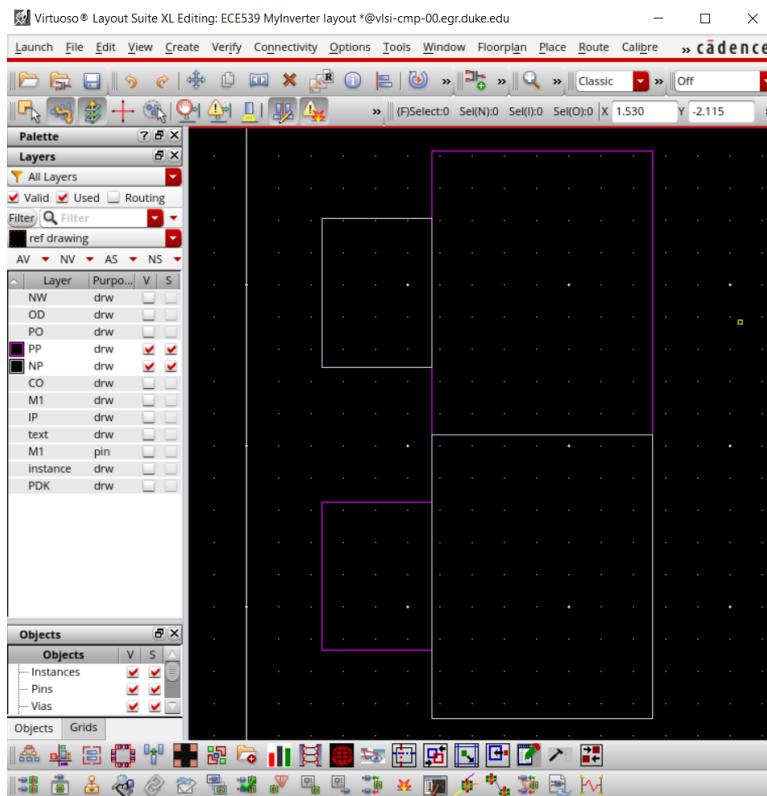
- Select the NMOS or PMOS device and press 'Q' to edit the property. Here we show a simple way to make a connection to the body. Change the bodytie\_typeL to 'integrated.'

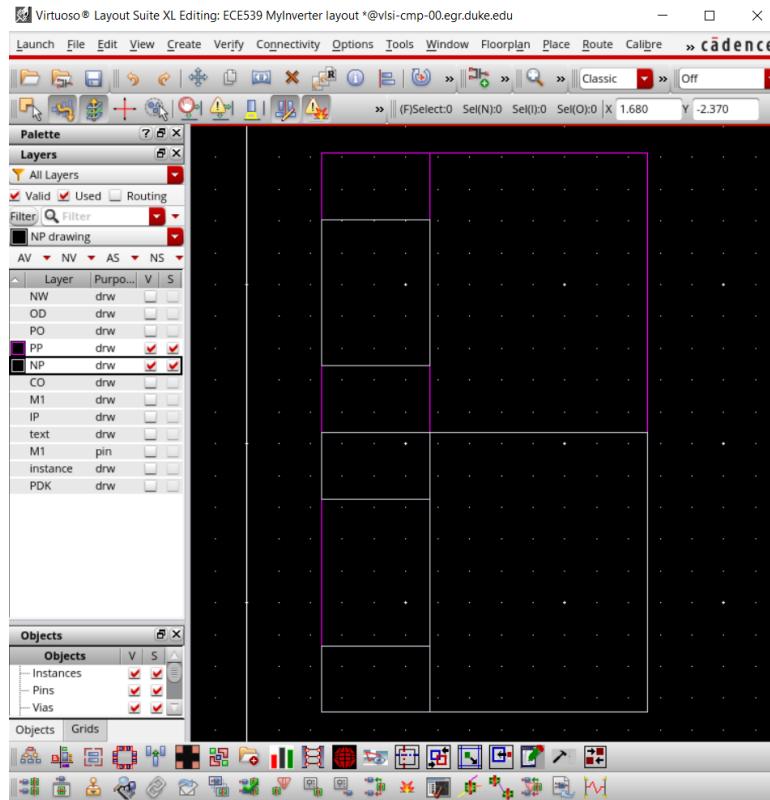


- The body connection will be automatically generated. Make sure the connection is correct. Do not connect the drain to the substrate or well. If the connection is not correct, maybe you should use bodytie\_typeR.

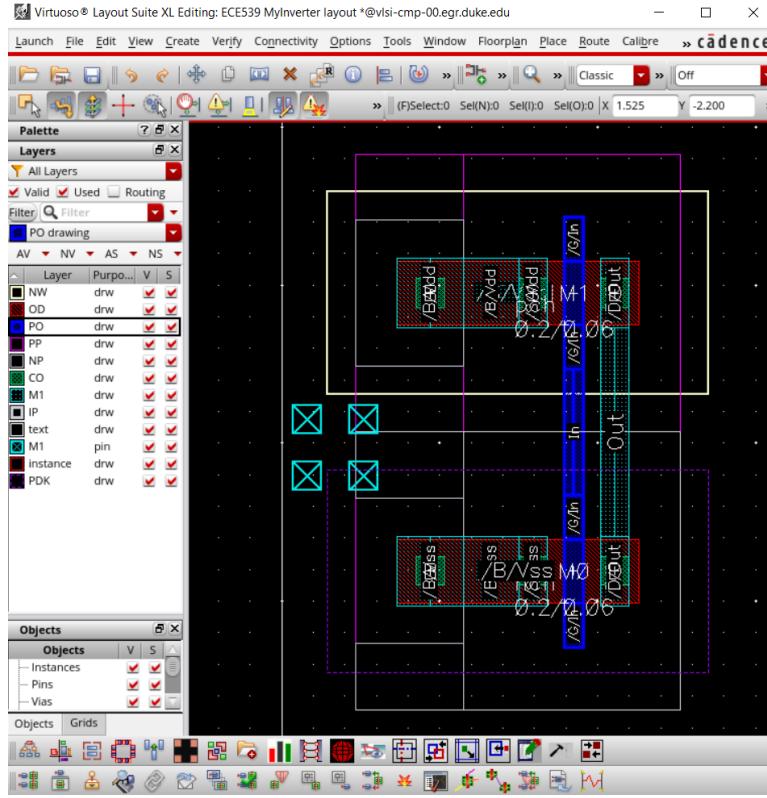


- Only select the NP and PP layer. Create some rectangular regions to fill it out (the hot key is 'R'). The reason we do this is because the Poly (PO) metal can only route in PP/NP regions. So, this makes it easy for us to route the Poly layer.

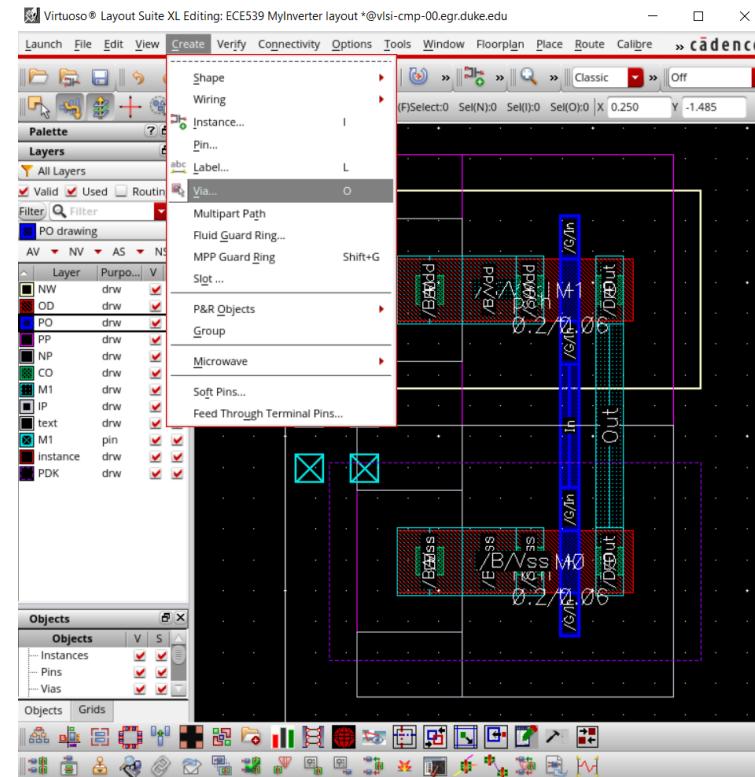




- Connect the input and output wire. Use the hot key ‘P’ to create an auto-path. The width of M1 and CO layer should be 0.09u. Use the hot key ‘K’ to draw rulers. To automatically erase all rulers, use ‘shift+K’.



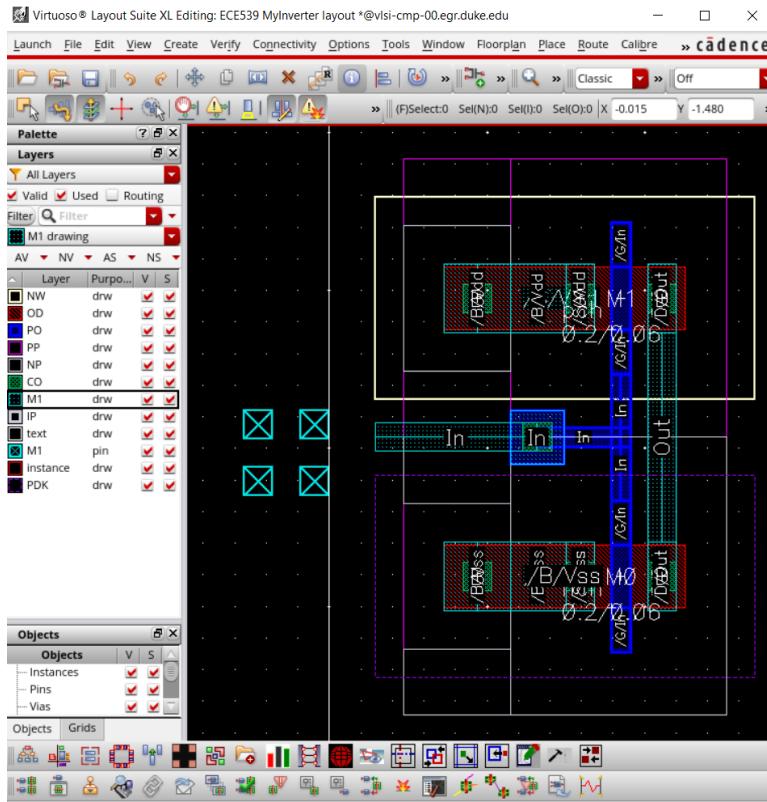
- Notice that the gate of our inverter is Poly, but our input pin is M1. To connect our input pin to the gate, we need to create a via. To do this, click *Create -> Via* (the hot key is ‘O’).



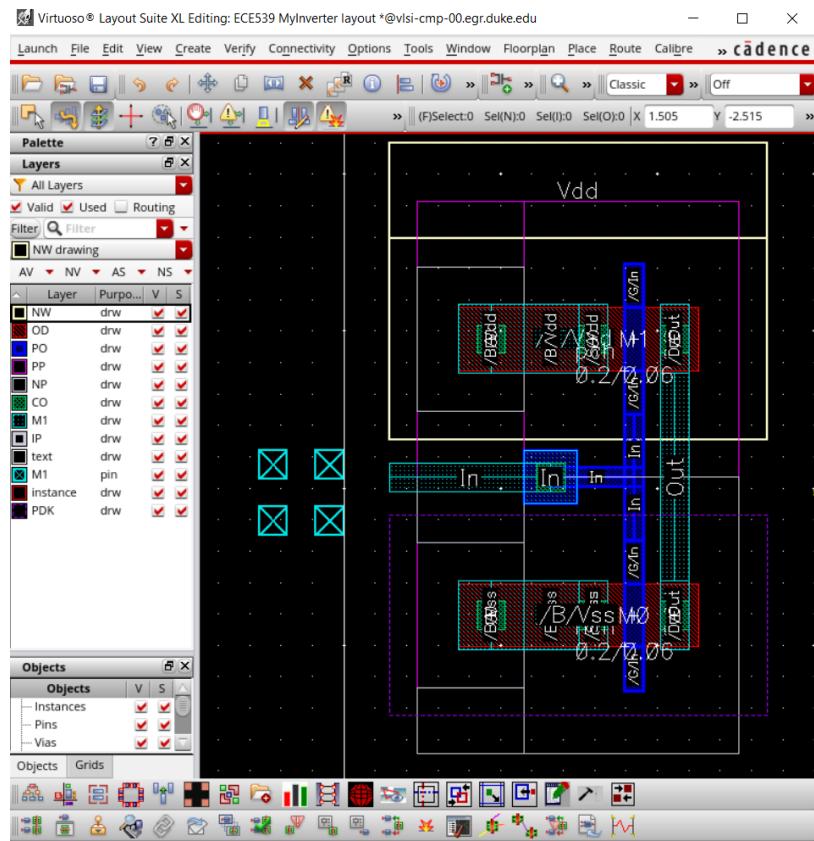
- Change the Via Definition to ‘M1\\_PO’ and click on the Layout. Do not change any other settings.



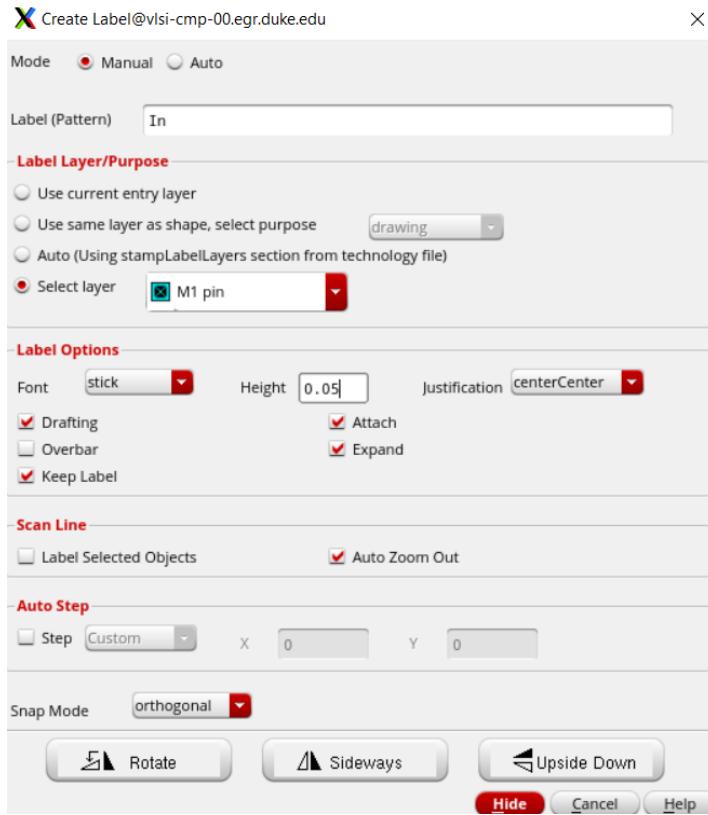
- Place the via to the left of the gate and connect the wires. Then, use M1 to create the input path.



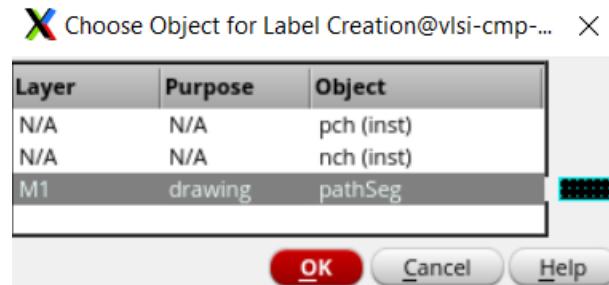
- Next, select the NW layer and draw a rectangle above the n-well. In this PDK, the n-well area must be larger than  $1\text{um}^2$  (the default area in this case is  $0.7712 \text{ um}^2$ ).

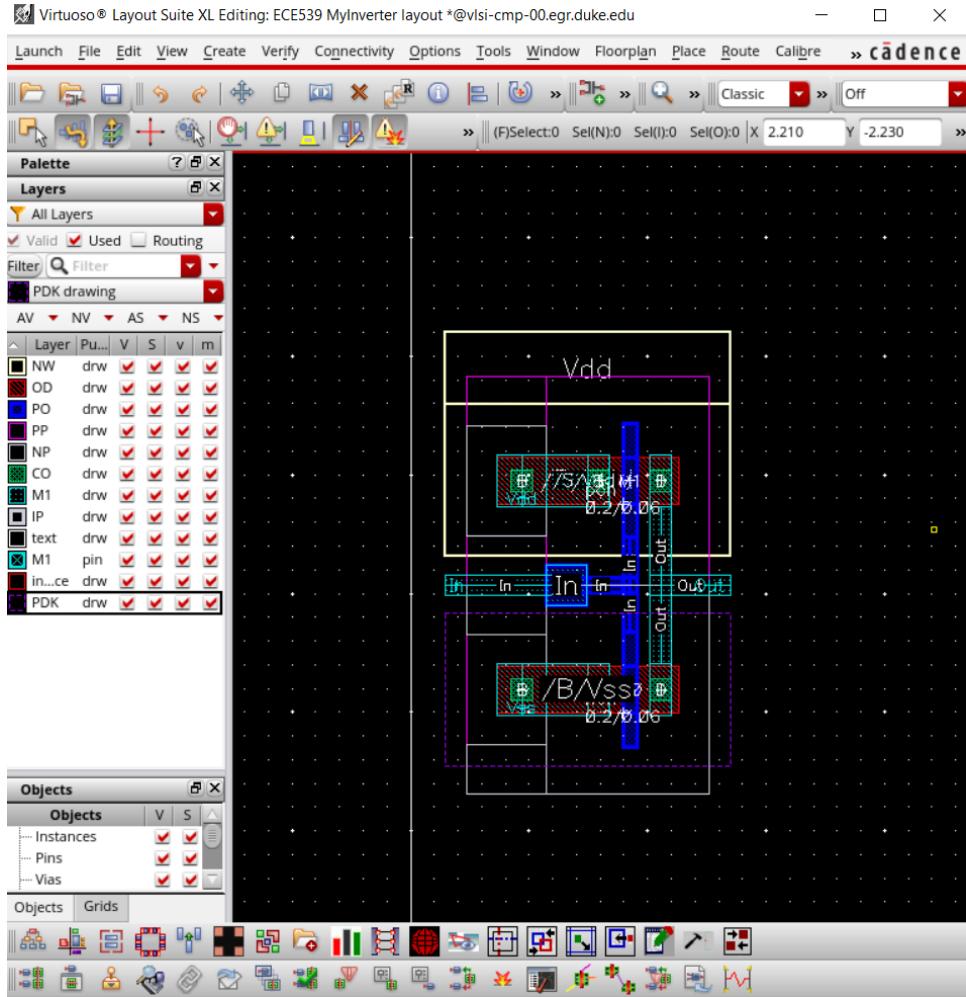


- Delete the four M1 pins and press the hot key 'L' to create a label.



- Type in the name of the pin, and make sure the layer is ‘M1 pin’. Then put all pins: Vdd, Vss, In, Out. If you are asked to choose an object for label creation, select the following and click *OK*.



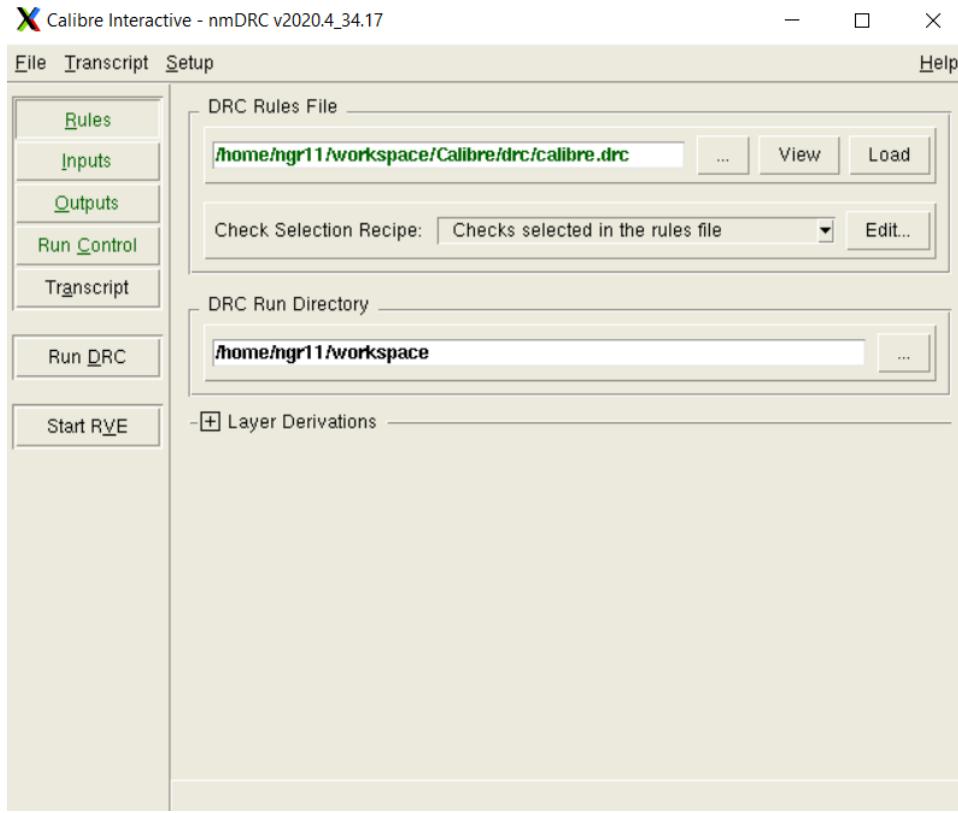


- Now that we have completed the layout, we need to ensure it is correct.

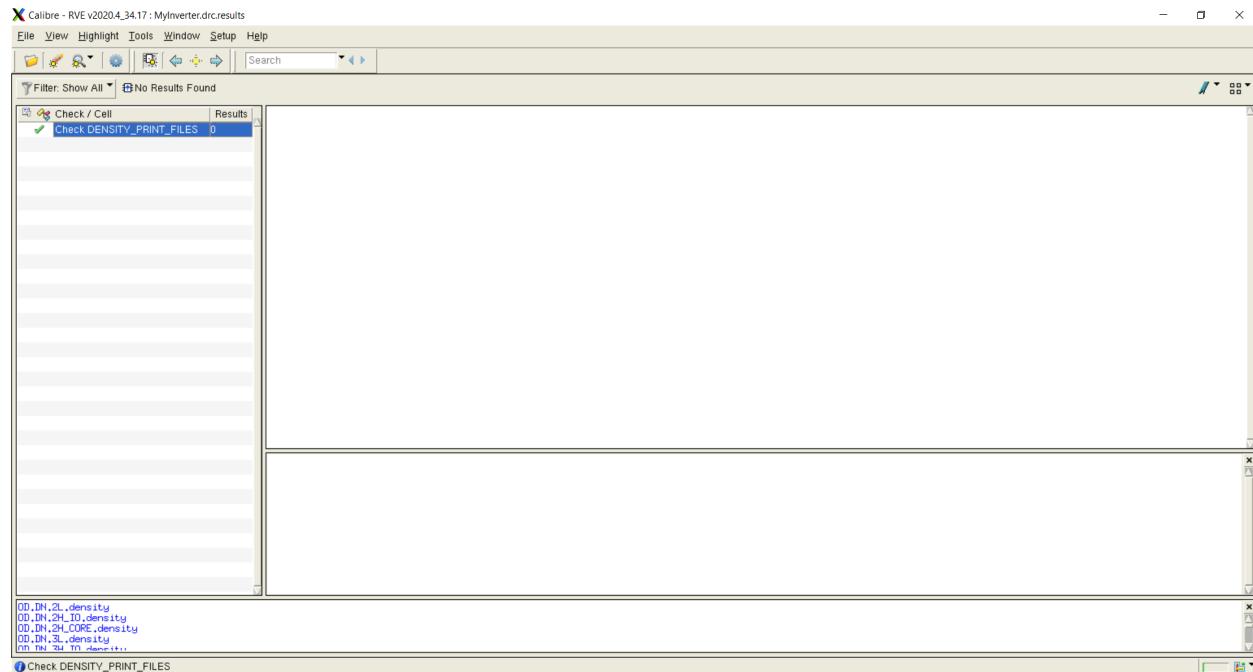
## 7. DRC, LVS, PEX

Launch the Calibre tool for DRC by clicking the following:

- Calibre -> nmDRC**
- Select the rule file at the following directory. If you are asked to load a runset file, click 'Cancel.'



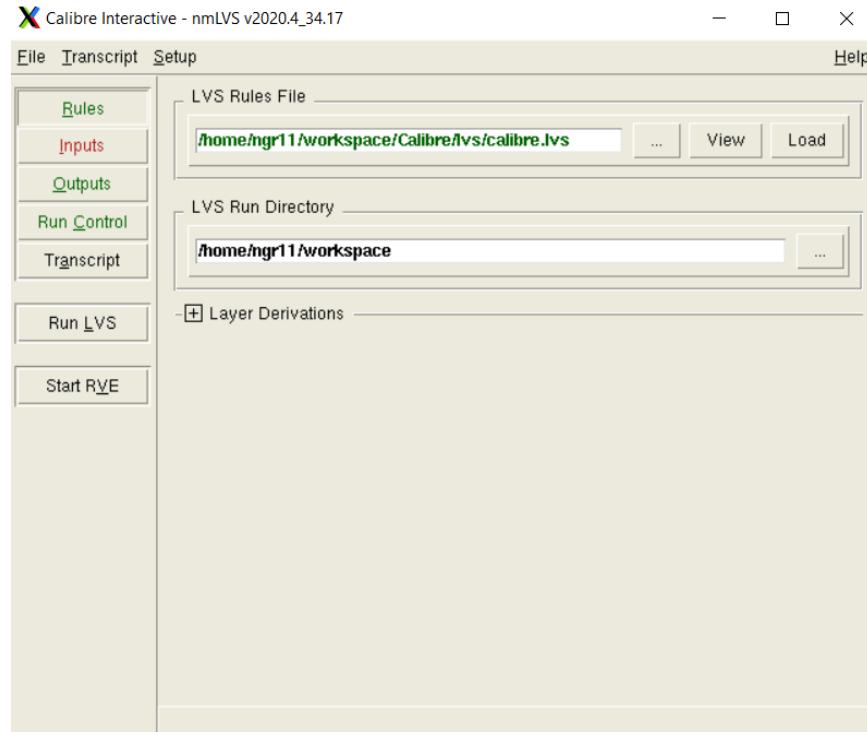
- Click ‘Run DRC.’ If your layout is correct, there will be no errors.



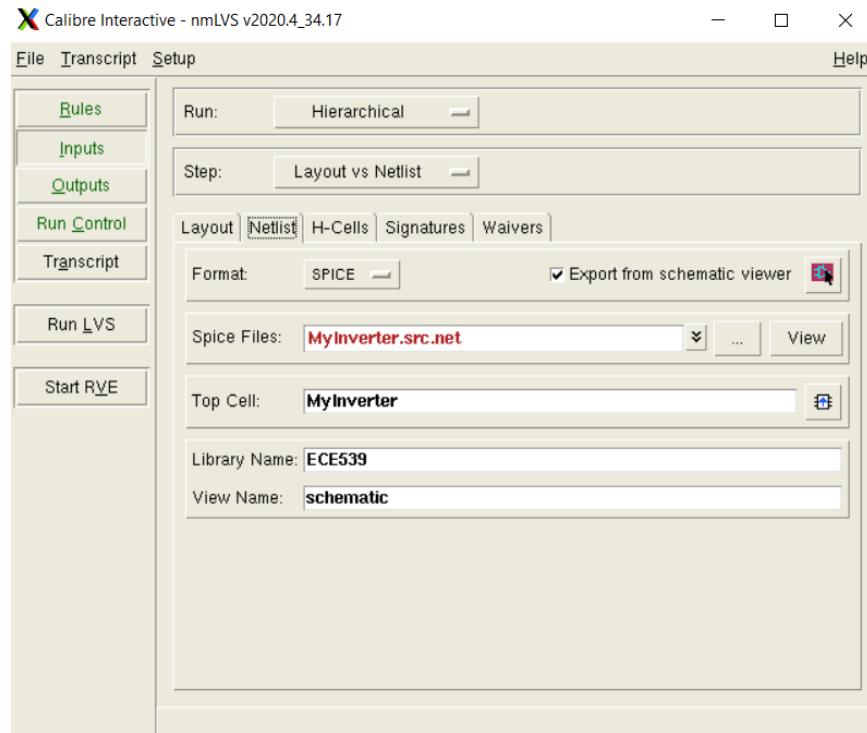
Launch the Calibre tool for LVS by clicking the following:

- **Calibre -> nmLVS**

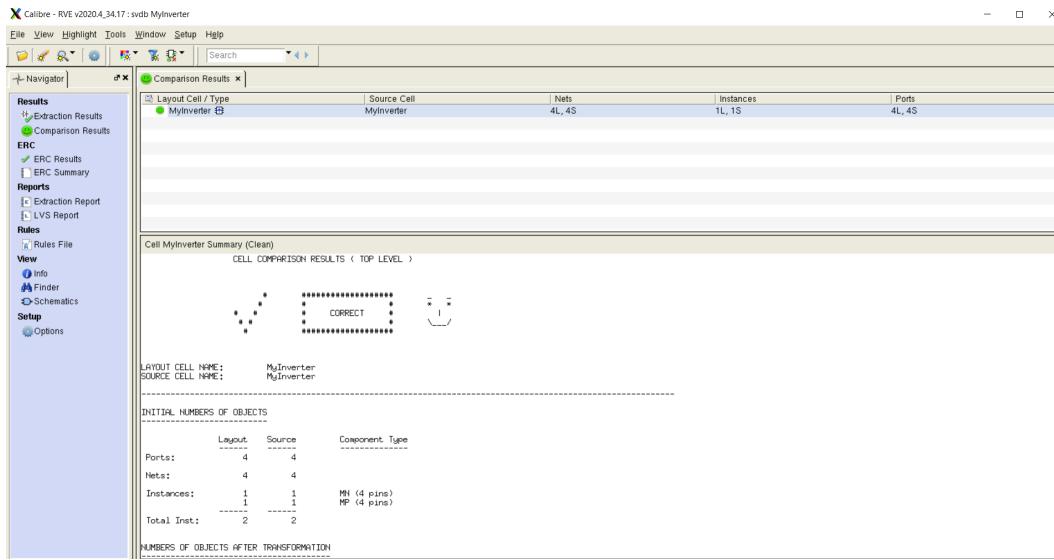
- Select the rule file at the following directory. If you are asked to load a runset file, click ‘Cancel.’



- Select ‘Inputs’ and make sure the design is exported from the schematic viewer.

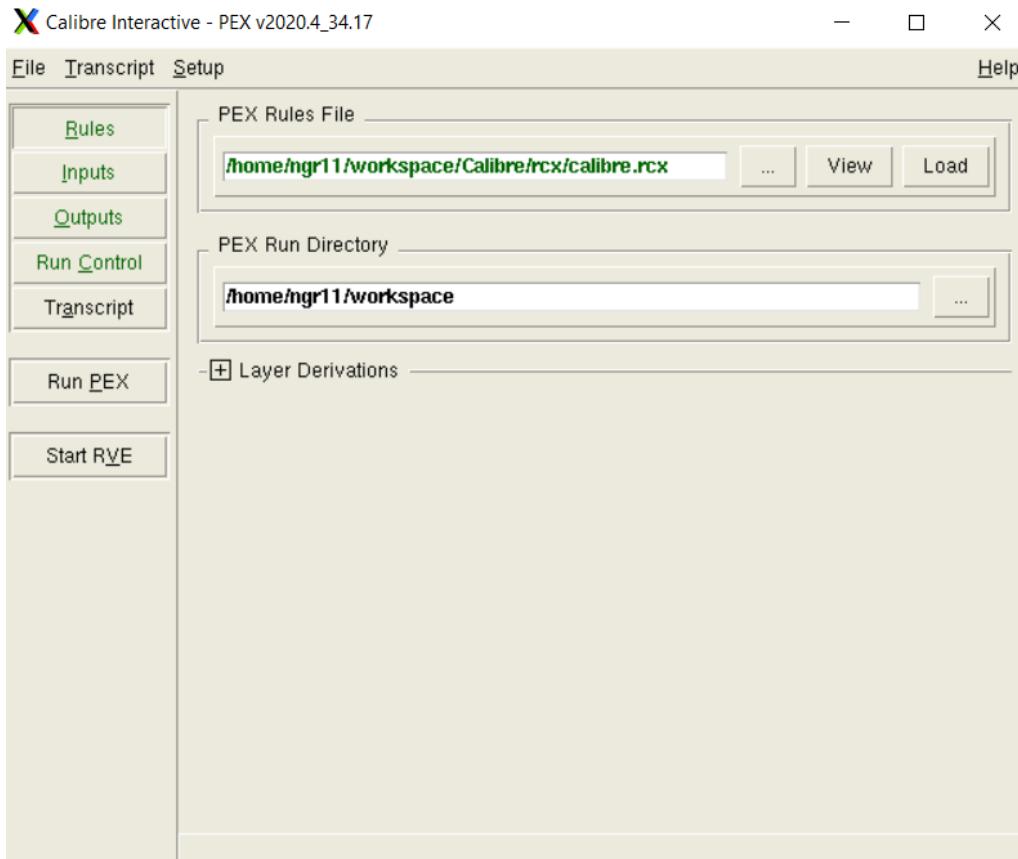


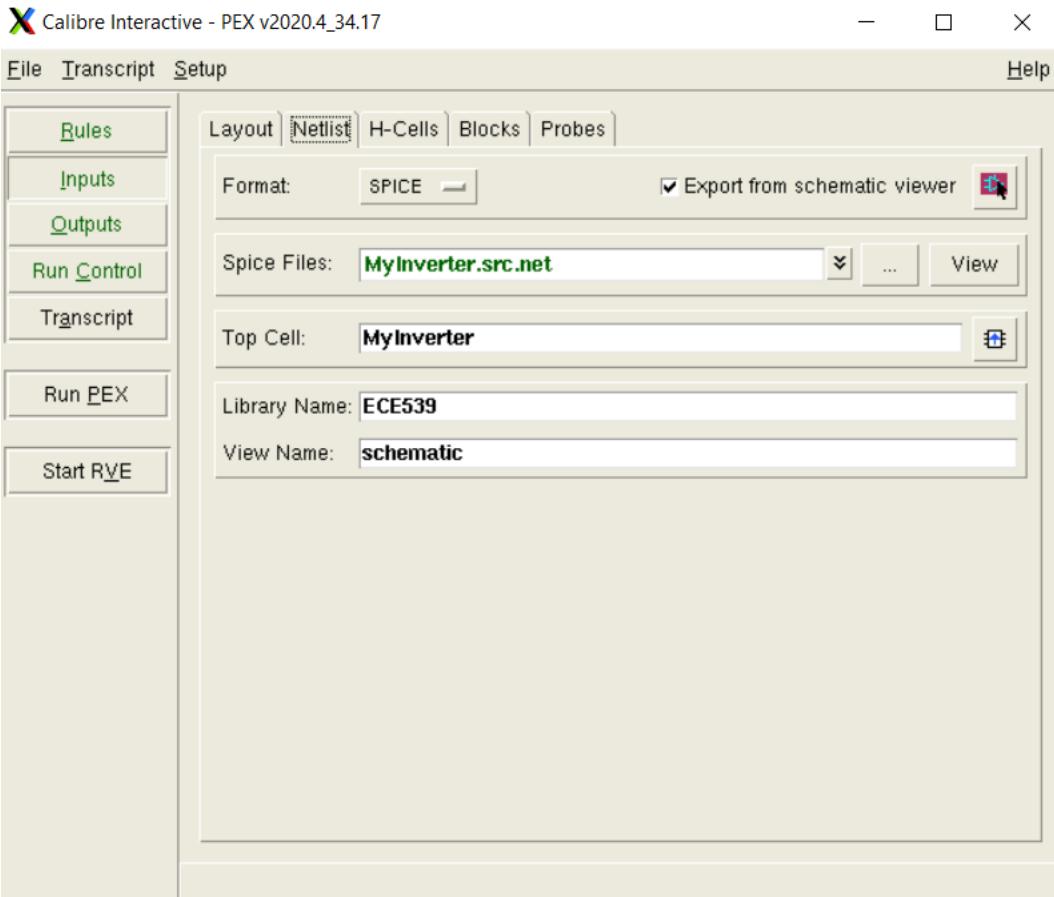
- Click ‘Run LVS.’ If your layout matches your schematic, there will be no errors.



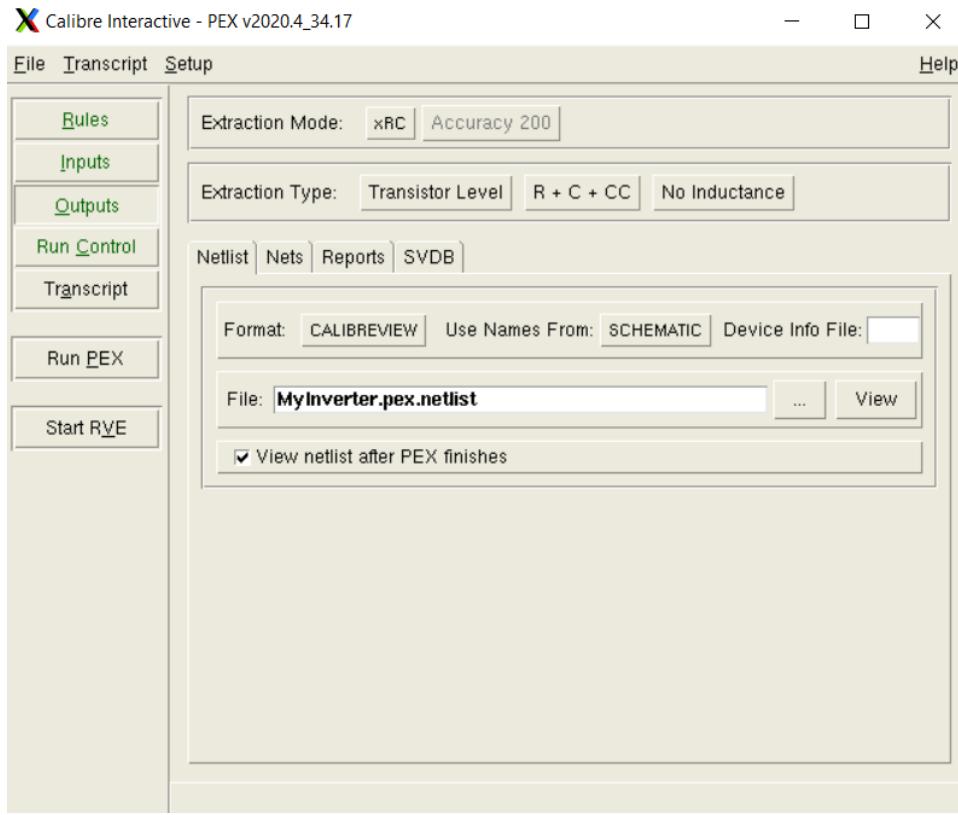
Launch the Calibre tool for PEX by clicking the following:

- **Calibre -> Run PEX.**
- Select the rule file at the following directory and following setup. If you are asked to load a runset file path, click ‘Cancel.’

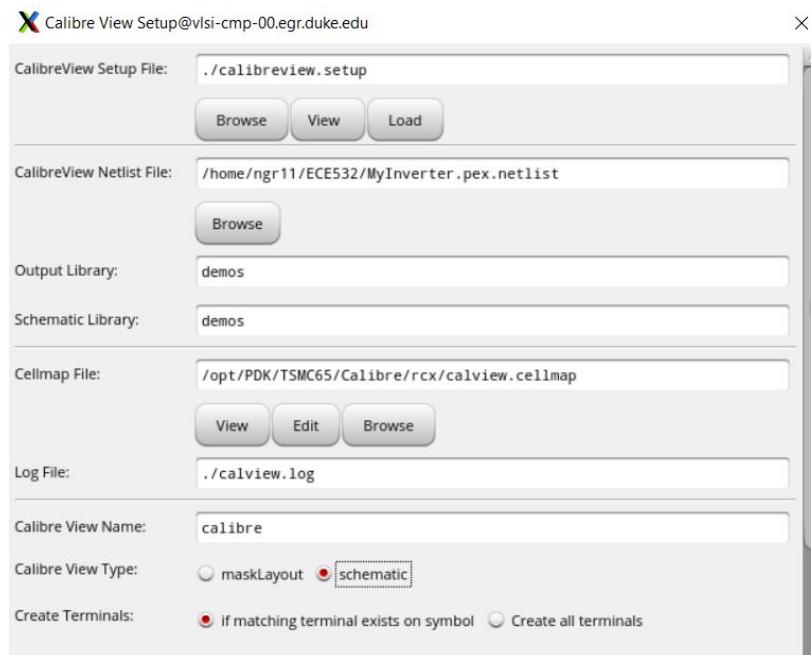




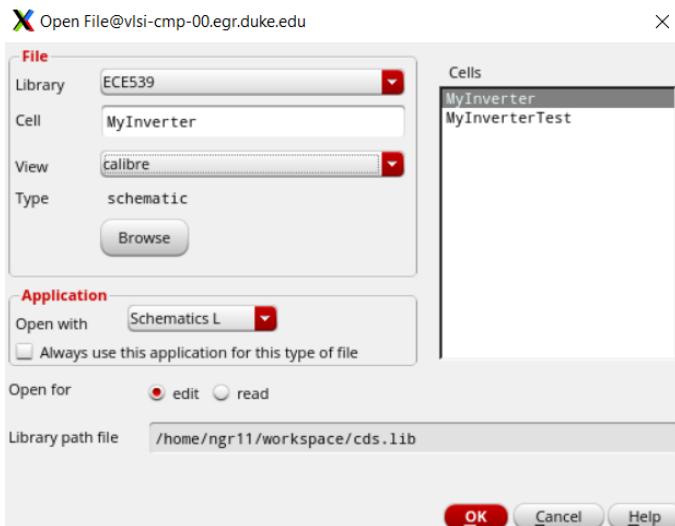
- In the ‘Outputs’ tab. Change the format from ‘ELDO’ to ‘CALIBREVIEW’ to make sure the output is compatible with Cadence format.



- Click ‘Run PEX.’ When the PEX finishes, there will be a setup file. Select the cell map in the following directory. Click *View* to check the cell map. If the cell map is blank, this means you are using the wrong directory. If the original output of PEX is a netlist, this cell map file is used to convert a netlist into a schematic (for example, tell the tool nmos will become nch). Click *OK*.

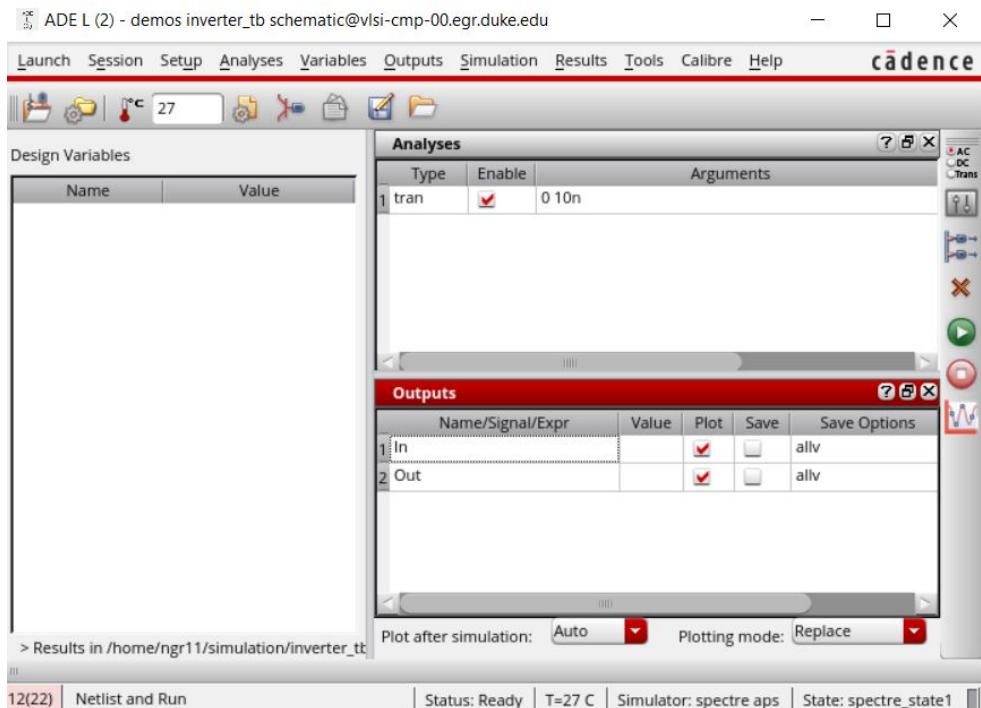


- If PEX ran correctly, Calibre will not give you any warnings or errors. Afterwards, you will find your inverter has another view called ‘calibre.’

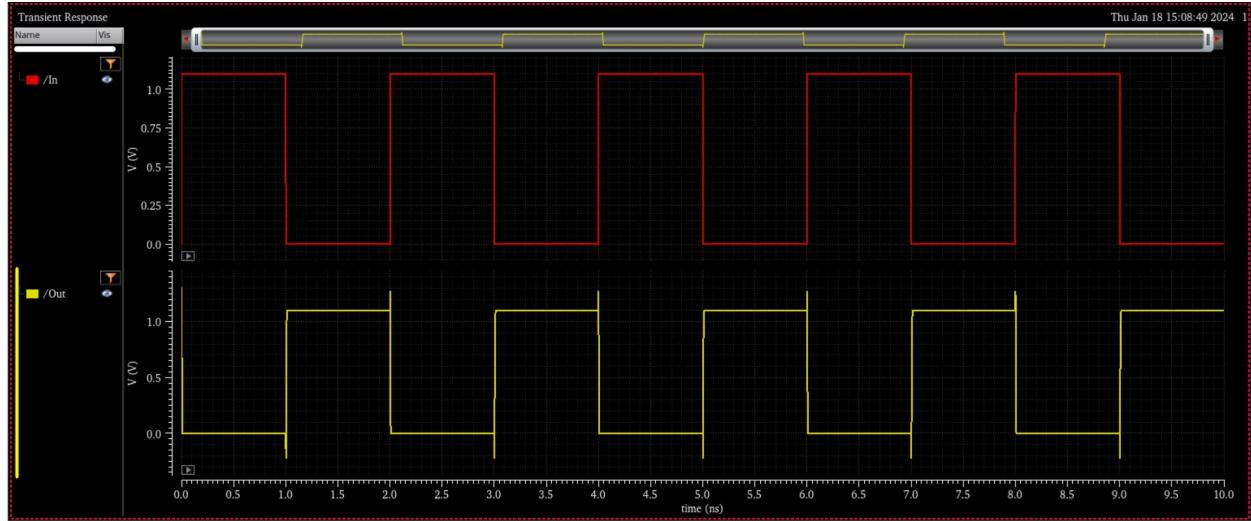


## 8. Post Layout Simulation

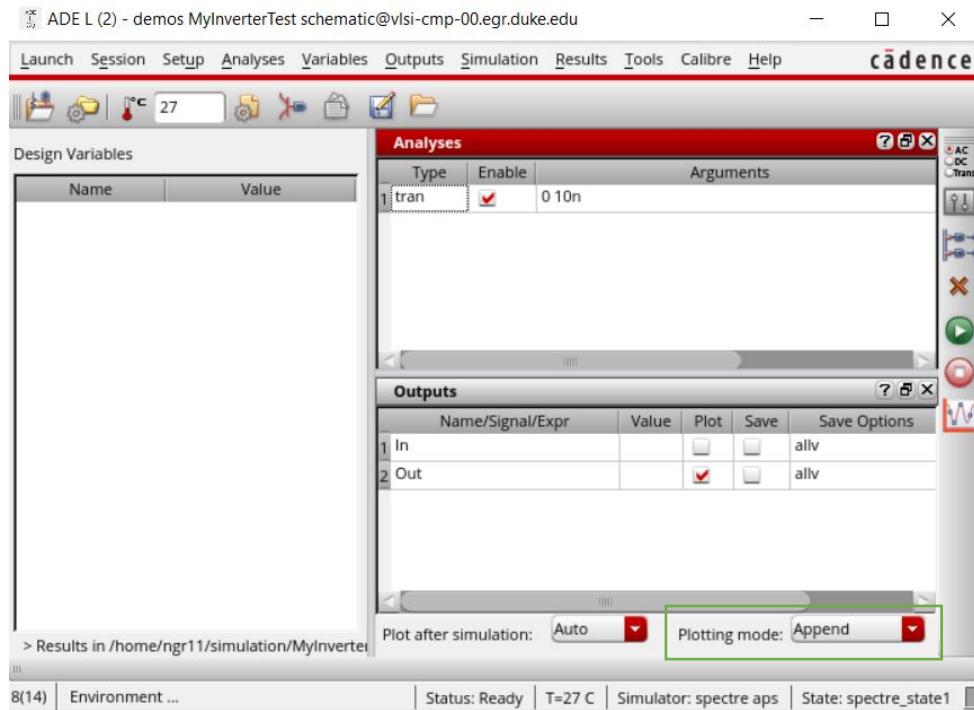
- Open the schematic for your MyInverterTest and launch the *ADE L*.
- Load or recreate the simulation settings from Page 22 (seen below).



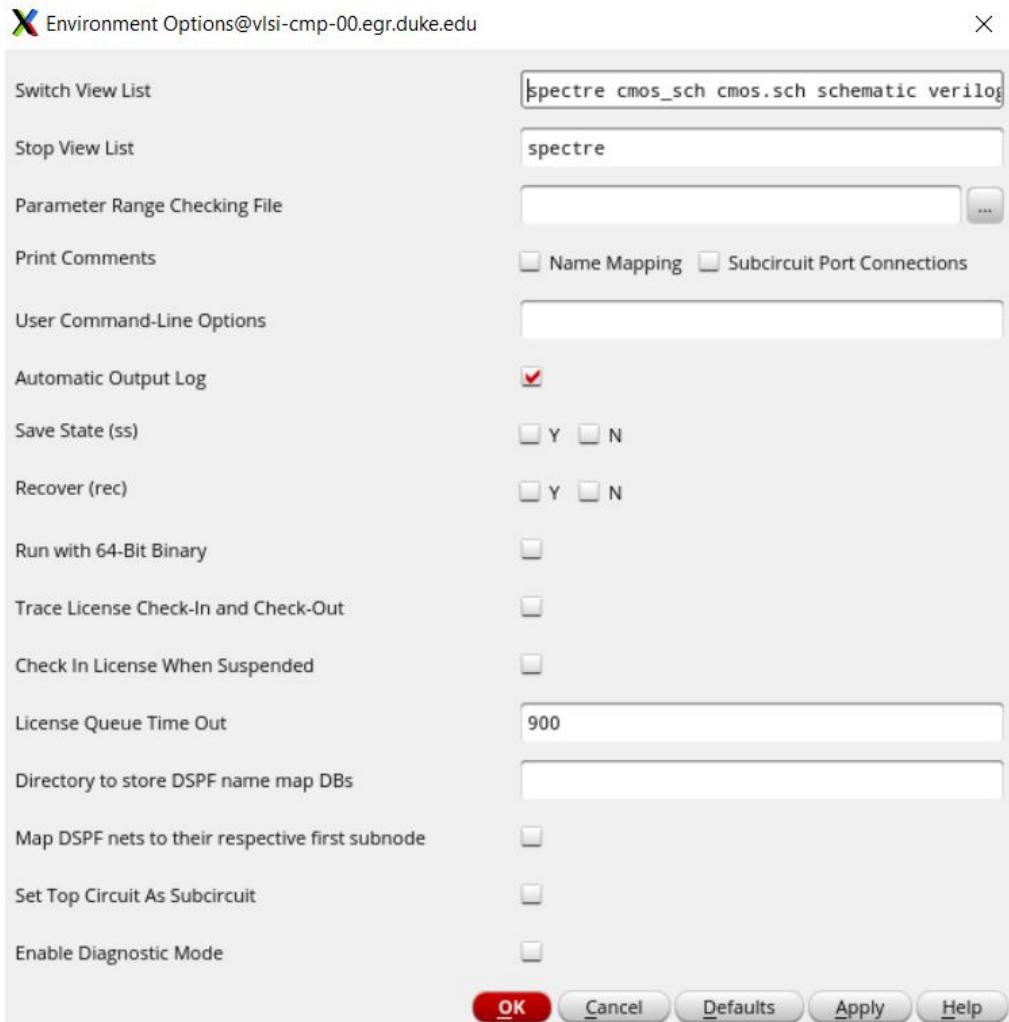
- Launch the simulation but do not close the window.



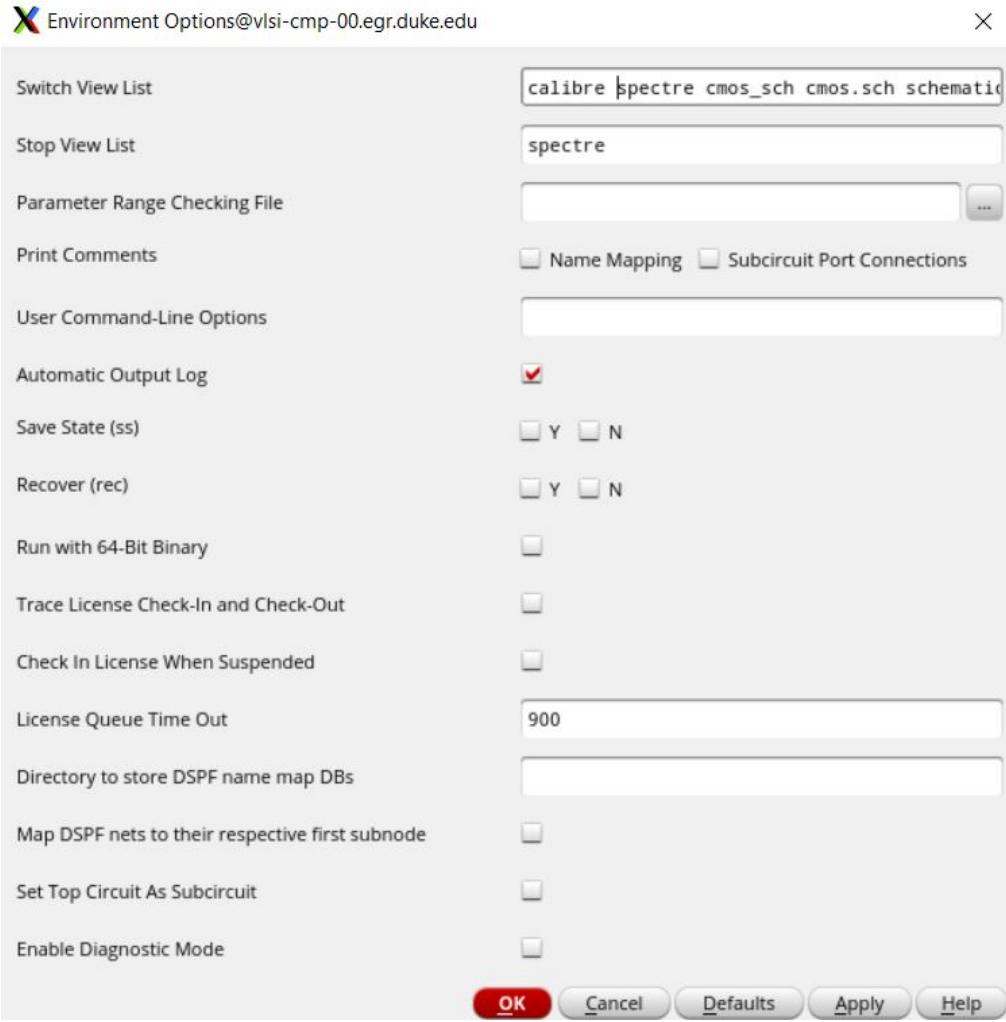
- Change the plotting mode to ‘Append’ and uncheck the ‘Plot’ box for the In signal.



- Click *Setup -> Environment* and the following window will appear.



- Type ‘calibre’ before ‘spectre’. This makes Cadence search for MyInverter’s calibre file before the schematic. Click *OK*.

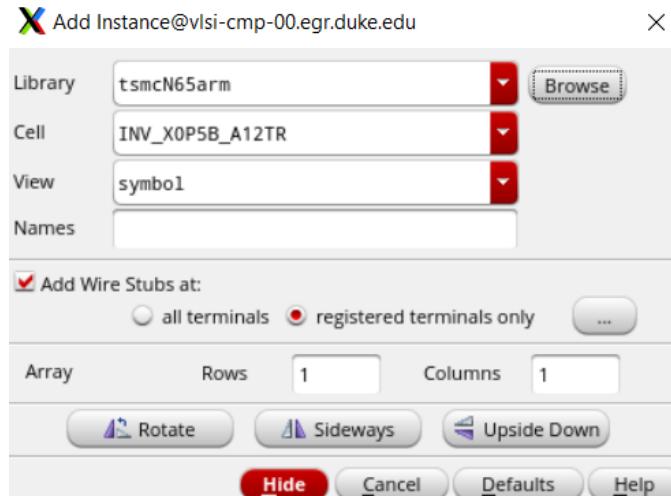


- Run the simulation again and observe the waveform. You should now see the pre- and post-layout simulations together. I zoomed into one section to show the impact of parasitics.

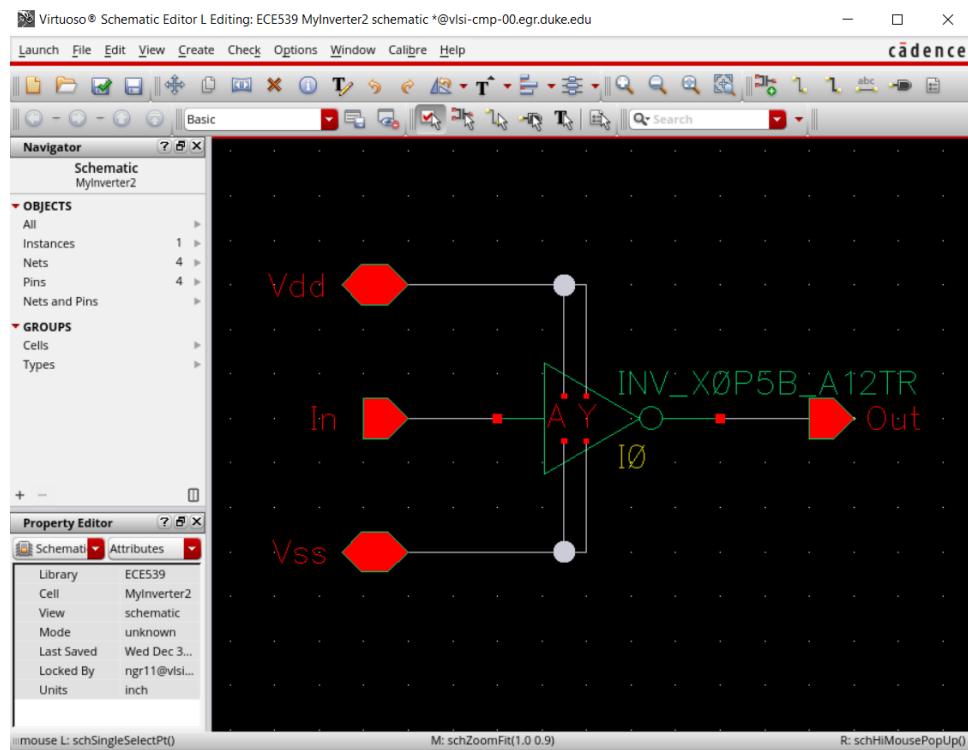


## 9. Design with Standard Cell Library

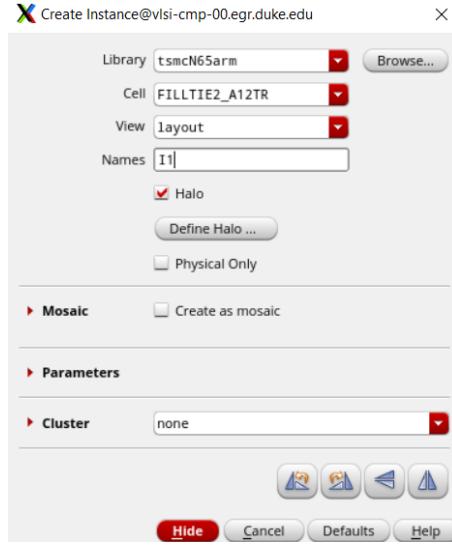
- Create a new cell called ‘myInverter2’ and add an inverter from the standard cell library.



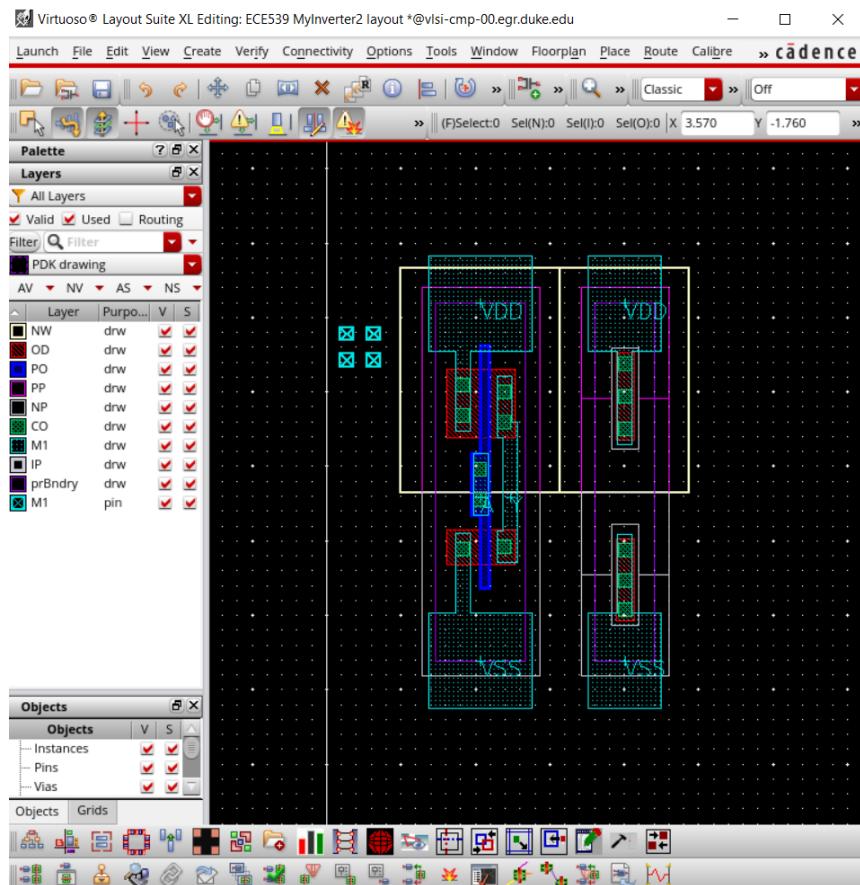
- Wire the inverter and assign pins as follows:



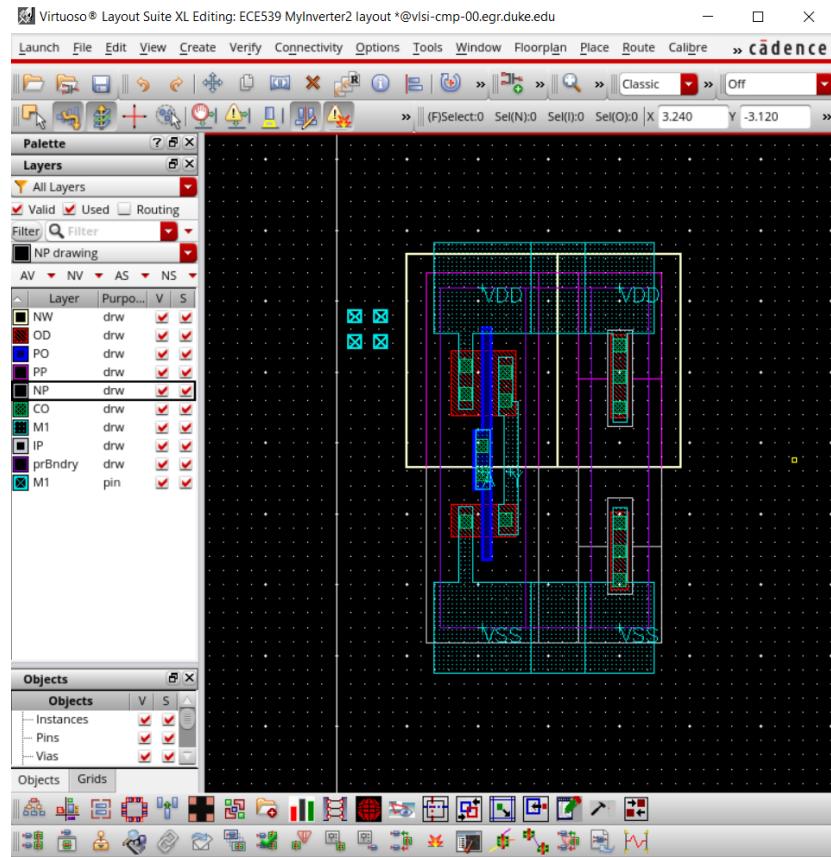
- Launch ‘Layout XL’ and place the standard cell.
- Note that the standard cell does not have a substrate/well connection. The library uses FILLTIE to automatically connect. This cell does not contain any transistors.



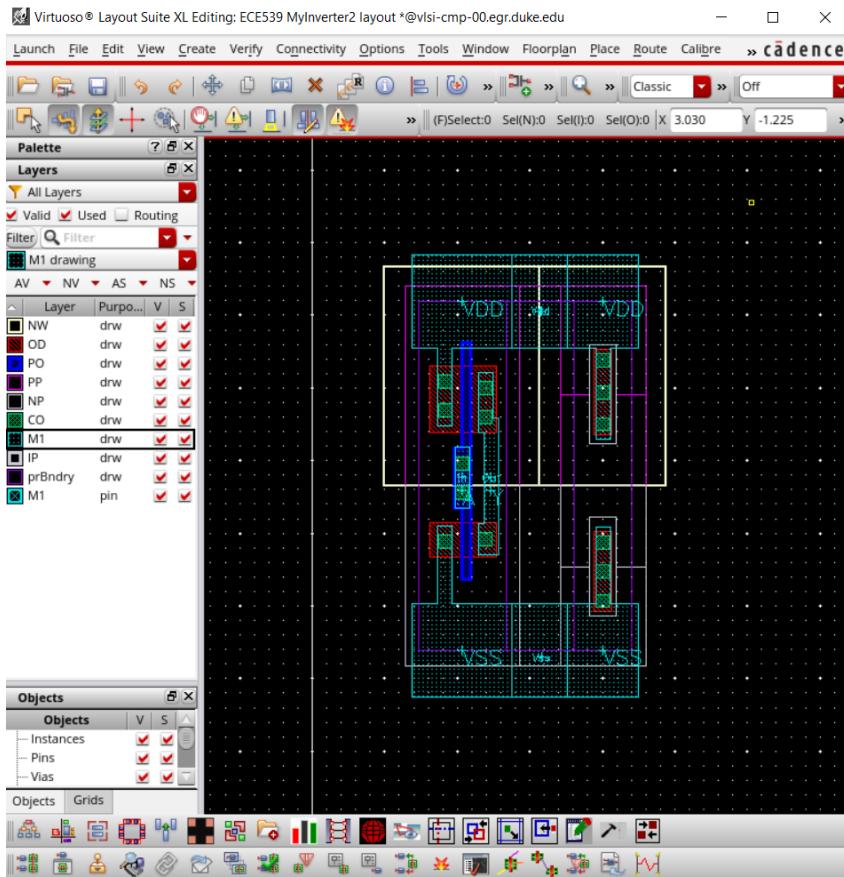
- Put the instance near the inverter. Make sure the PR boundary is tightly close to each other. This will give the minimum area.



- Next, connect the Vdd/Vss of the inverter to the Vdd/Vss of the tie. Afterwards, use the rectangle tool to connect the PP, PR boundary, and NP layers of the inverter and tie together.



- Label the Vdd, Vss, In and Out.



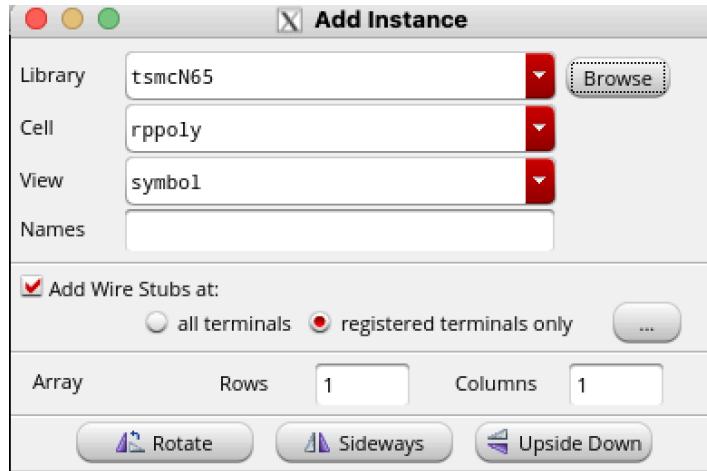
- Now you can run DRC and LVS to make sure the connection is correct.

## 10. Design with PDK Resistors and Capacitors

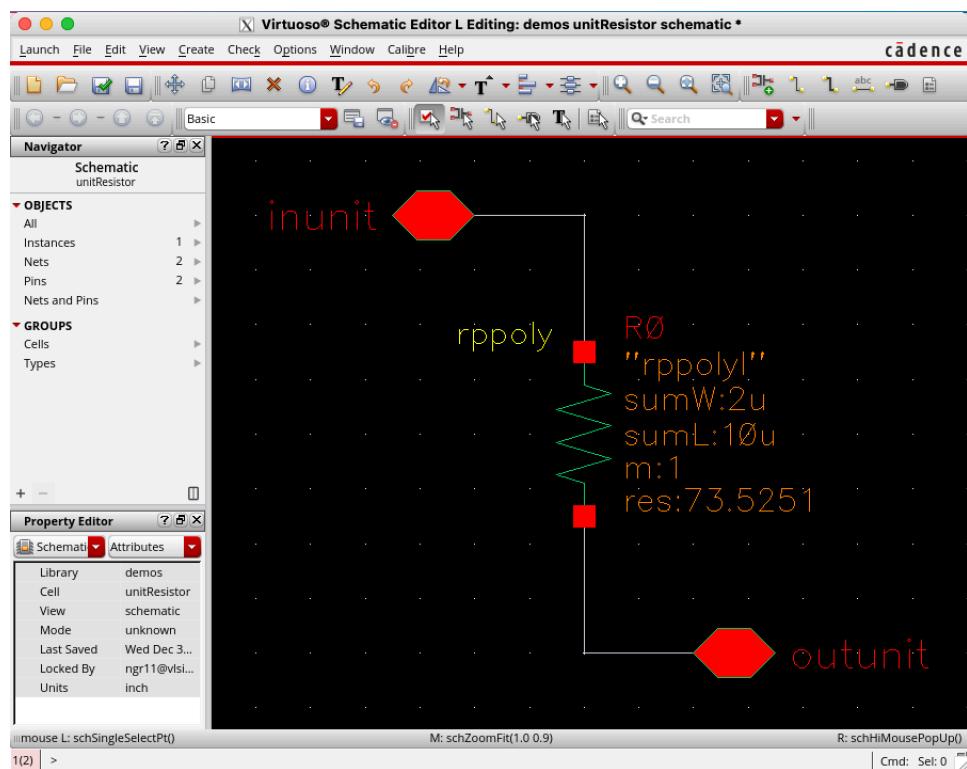
Due to the limitations of the PDK, it is not possible to get large resistances with only one resistor. Sometimes you will need to centroid multiple resistors in series (or capacitors in parallel) to achieve a certain resistance (or capacitance).

### Resistor

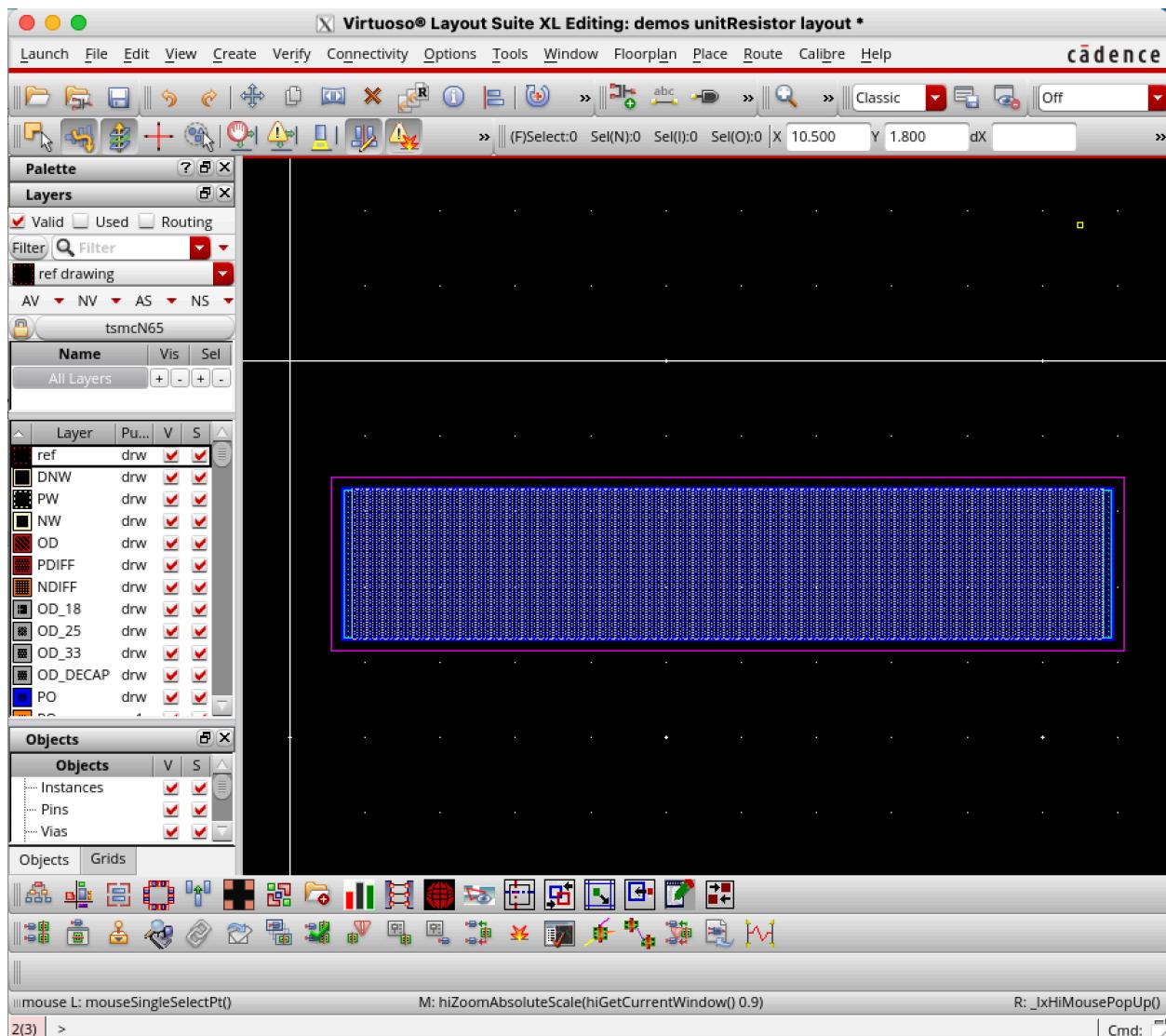
- Create a new cell called ‘unitResistor’ and add a rppoly instance from the tsmcN65 library.



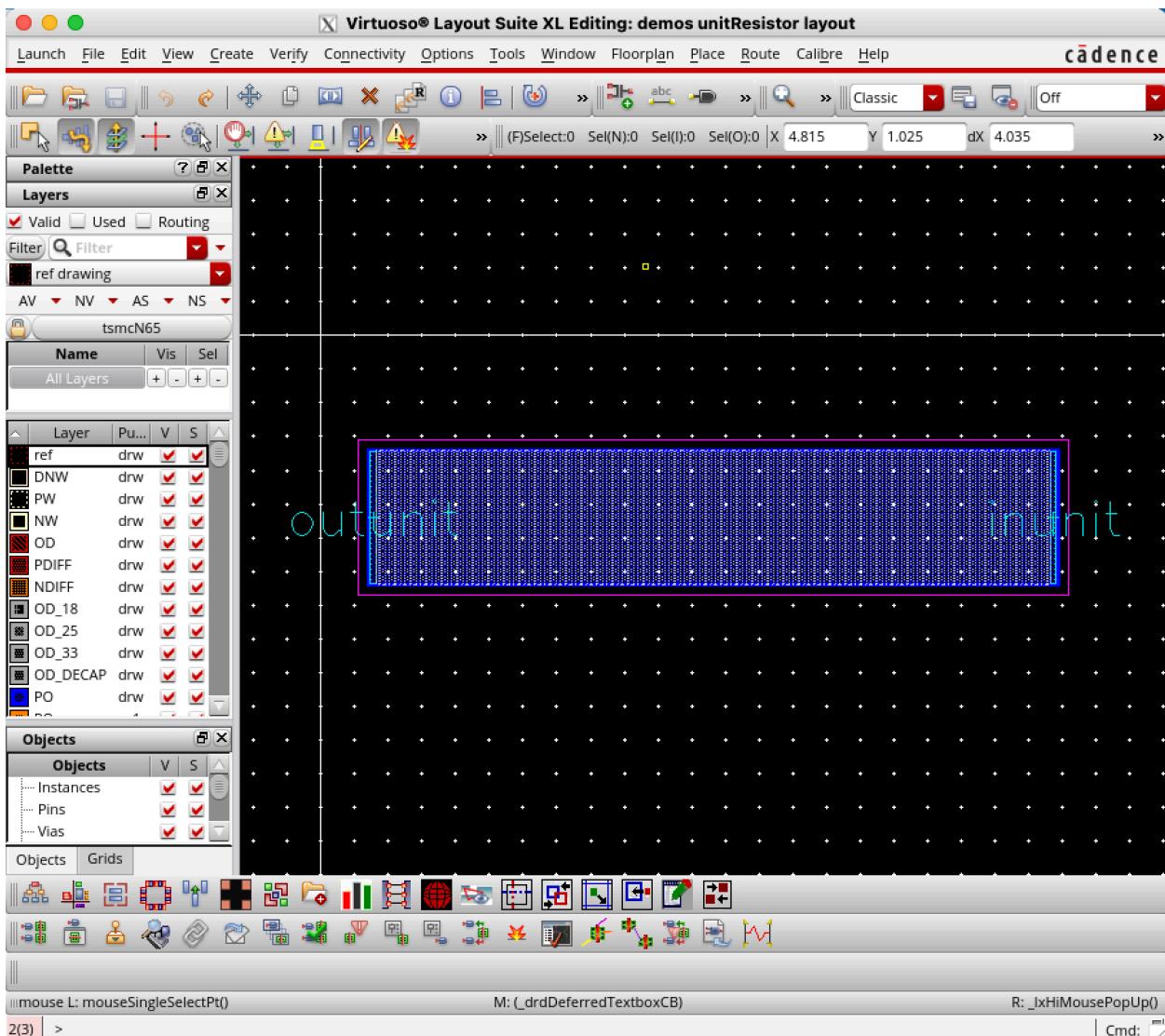
- Wire the resistor and assign pins as follows.



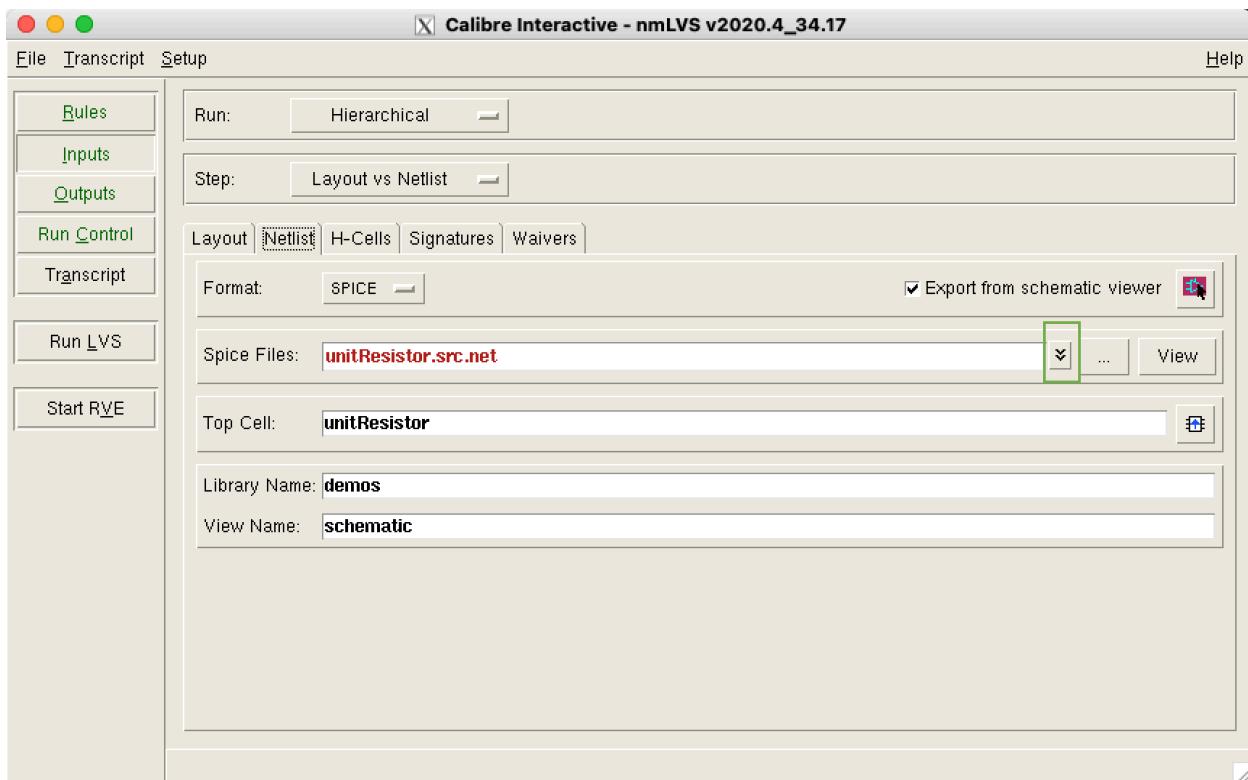
- Launch 'Layout XL' and place the resistor.



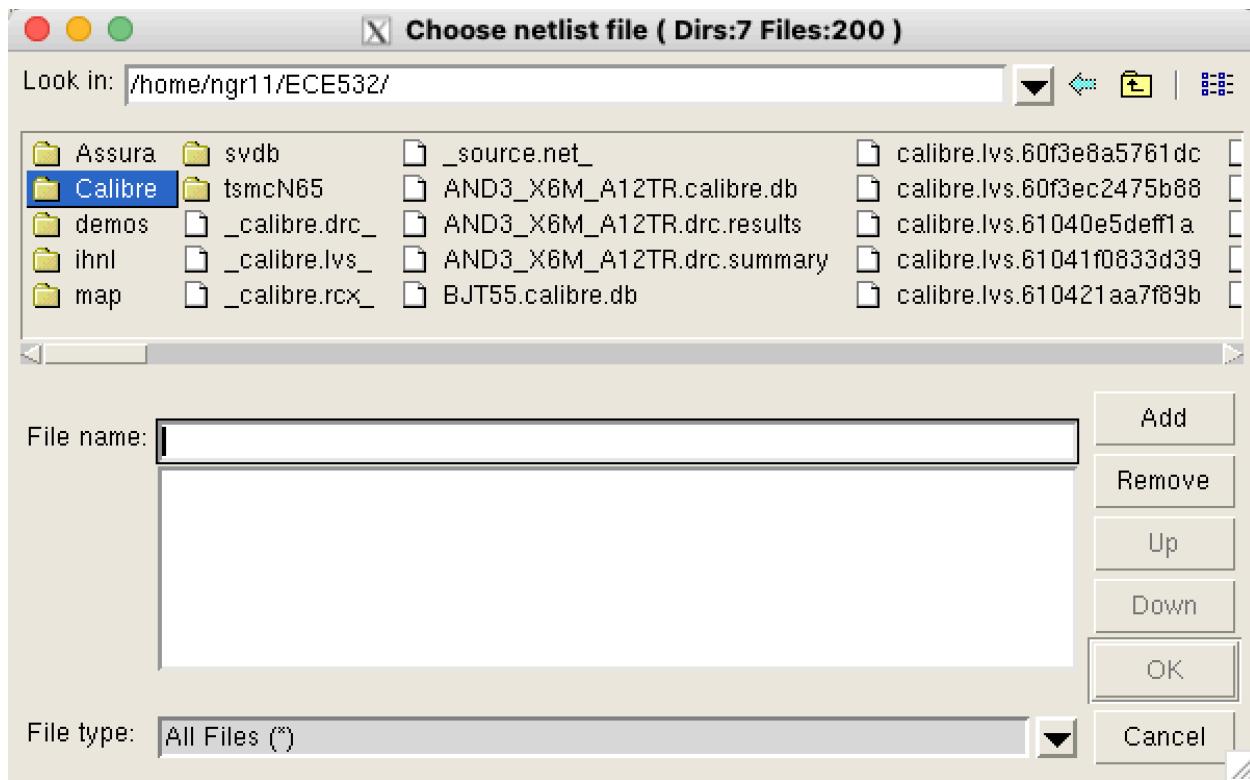
- Label the inunit and outunit.



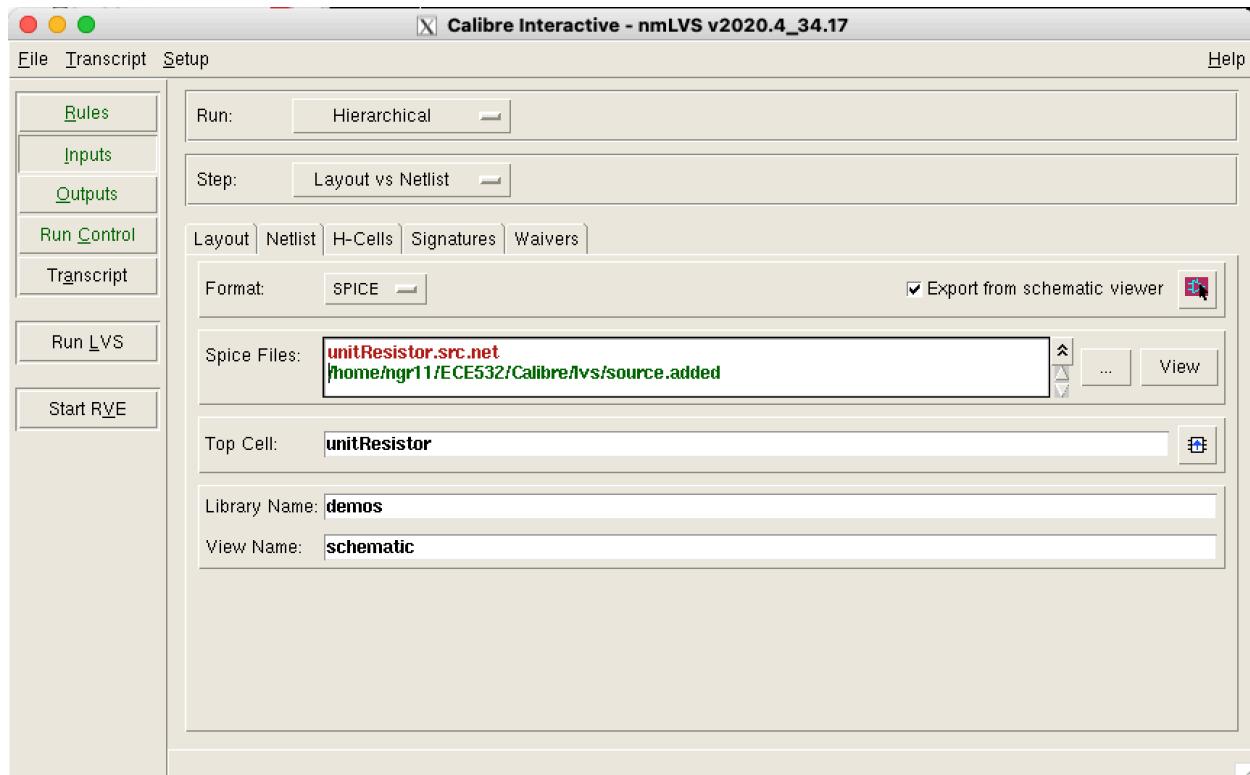
- Run the DRC to make sure there are no errors. Certain resistor sizes may produce Metal 1 area errors.
- Afterwards, open the LVS and select the rule file like normal. We will need to make a change in the Inputs section.



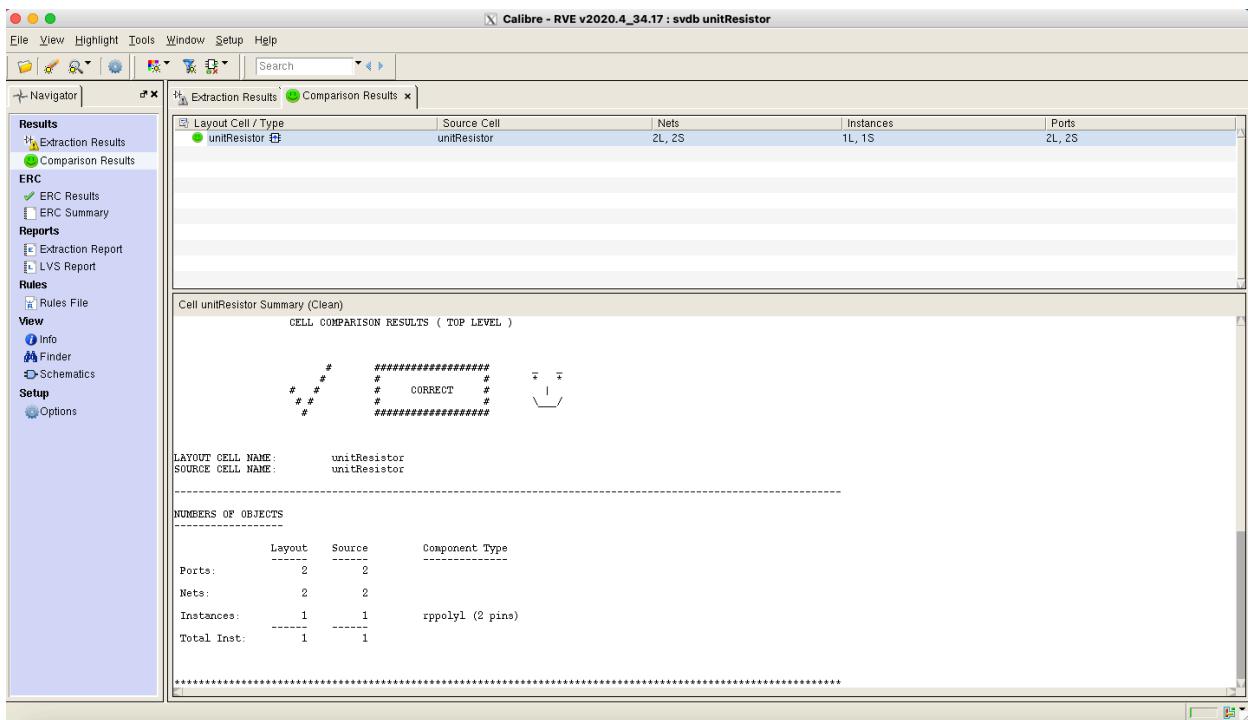
- Click on the button highlighted in the green box above to extend the spice file list. Next, click on the whitespace for spile file list and press enter. Make sure your cursor is on the new line you created. Then, click on the button with three dots (...). The following menu will pop up.



- Click on *Calibre->lvs->source.added* and then click ‘Add’.



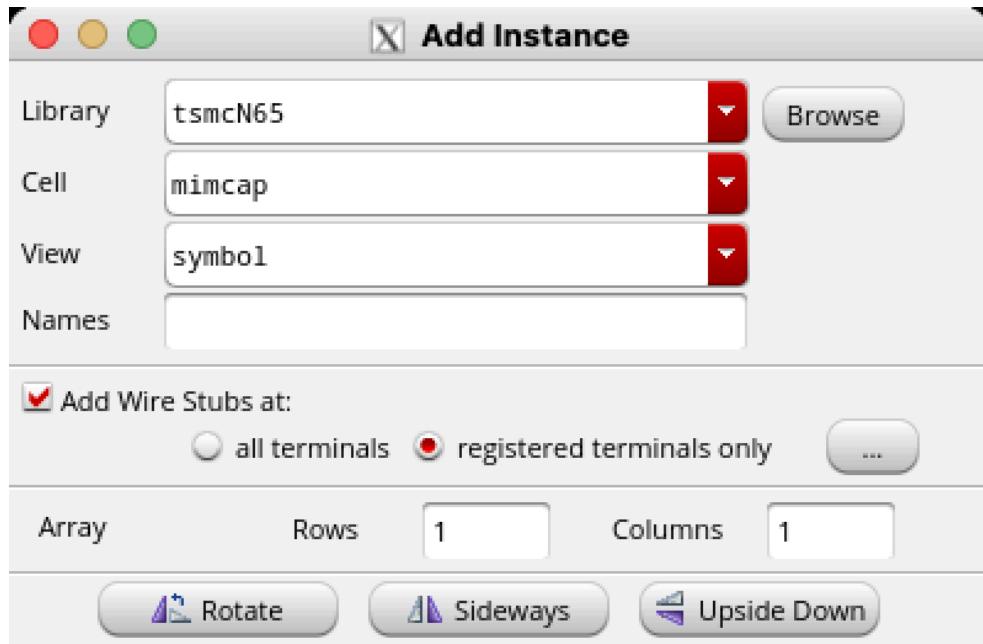
- Click ‘Run LVS.’ If your layout matches your schematic, there will be no errors.



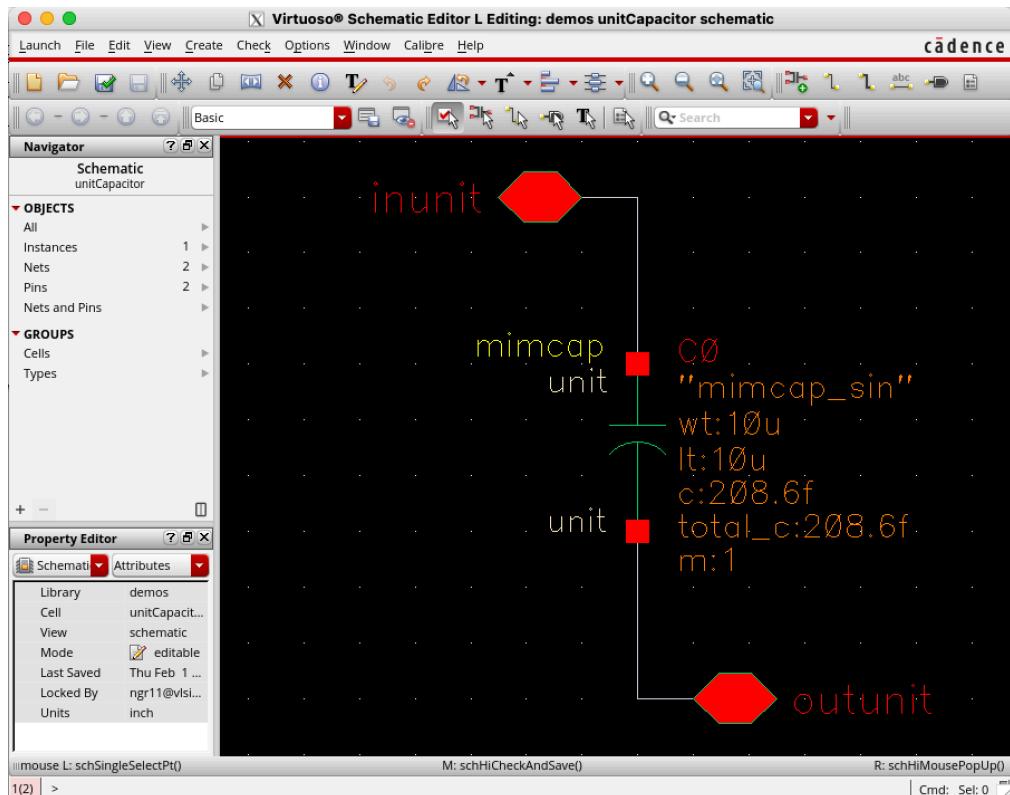
- You may get Extraction Result warnings. This is because there are no identifiable power and ground connections for the unit resistor. You can ignore those.

## Capacitor

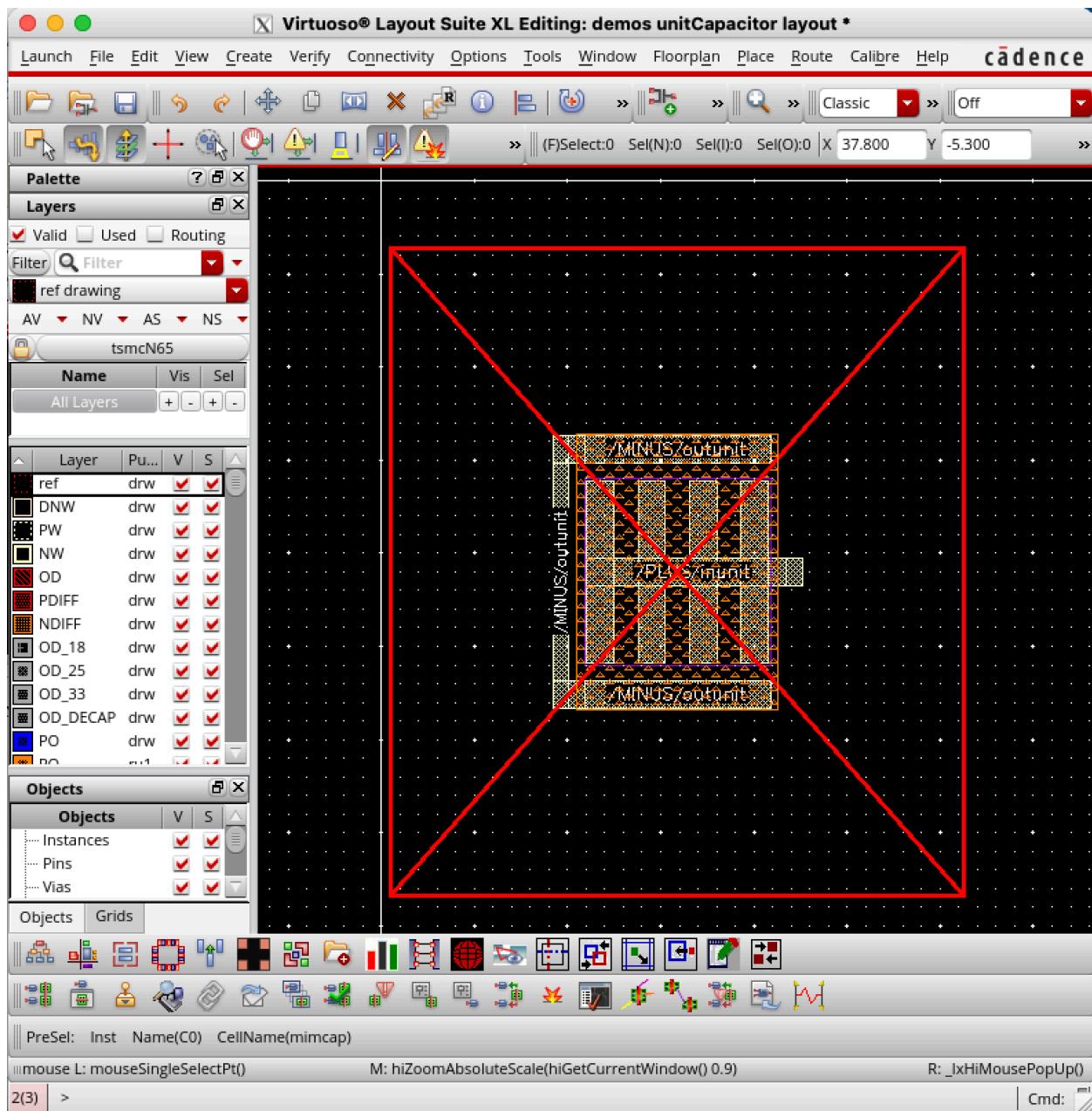
- Create a new cell called ‘unitCapacitor’ and add a mimcap instance from the tsmcN65 library.



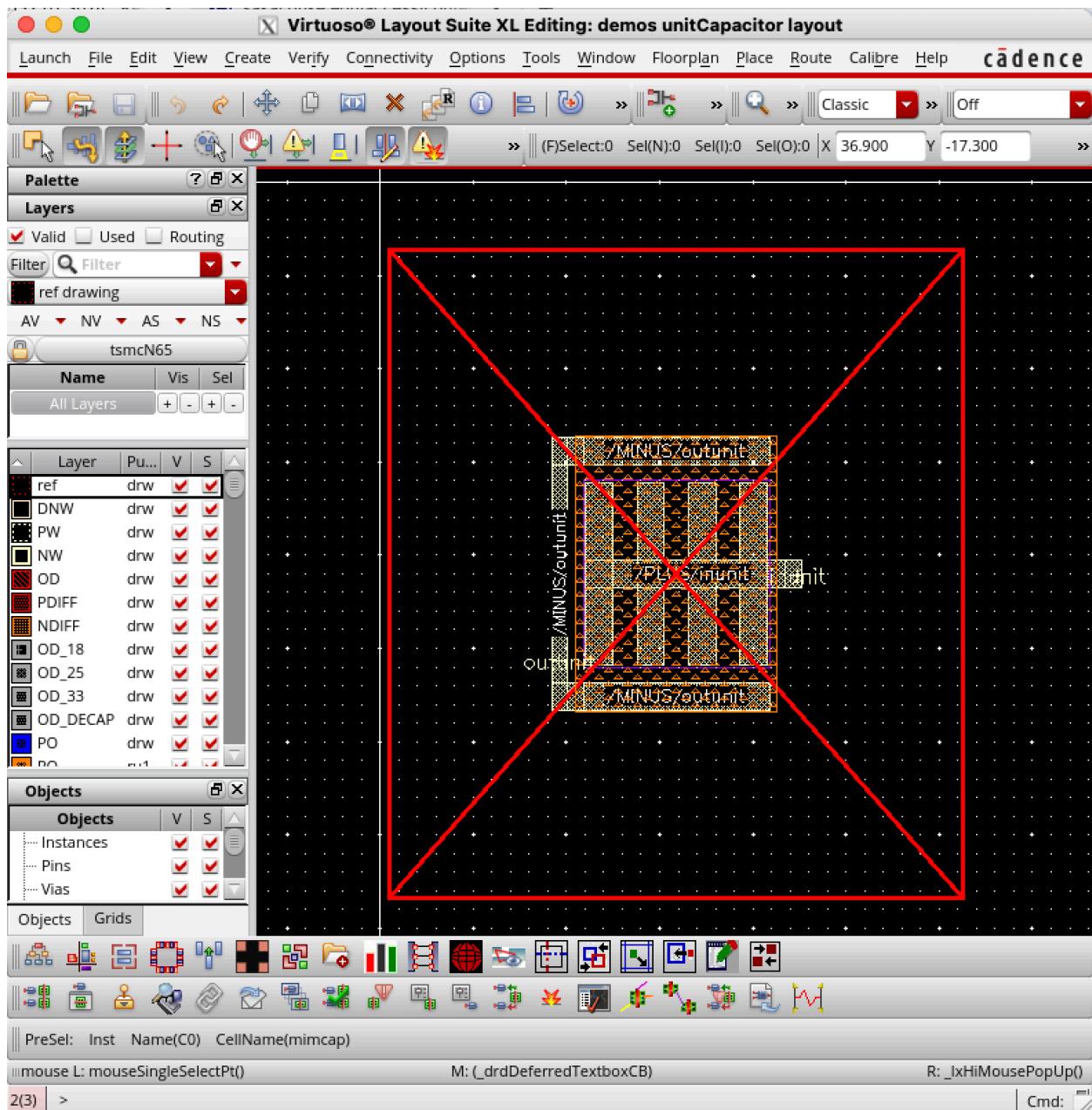
- Wire the capacitor and assign pins as follows.



- Launch ‘Layout XL’. When you generate from source, change the I/O pins to M8 pin before you place the capacitor.



- Unlike the resistors, capacitors in this PDK are created using the Metal 8 layer. The red box around the capacitor indicates the boundary in which you can only route Metal 8. If you try to route lower metals within the boundary, you will get a DRC error.
- Please see video 10\_ResCap.mp4 under the CAD Tutorials folder in the Resources tab on Sakai for more information.
- Label the inunit and outunit.



- Run the DRC to make sure there are no errors. Due to the size of the capacitor, you may get density (DN) errors. You can ignore those.
- Afterwards, open the LVS and select the rule file like normal. Follow the additional step like we did with the resistor (on Page 53) and run the LVS to make sure the connections are correct.