# ECE532: Integrated Analog Circuit Design

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Class Hours: Tues, Thurs 11:45 am – 1:00pm;
Class Room: Room Teer 106
Instructor Office hours: ½ hour before/after class

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Office Hours: TBD
Computer Cad administrator: Guanglei Zhou; **guanglei.zhou@duke.edu**
Prerequisites: instructor's consent

## Textbooks/References

B. Razavi, "**Design of Analog CMOS Integrated Circuits,**" 2nd Edition, McGraw Hill, 2017.
P. Allen and D. Holberg, "***CMOS Analog Circuit Design***" Oxford University Press, 2012.

## Course Objectives

This course covers the design and layout of CMOS integrated analog circuits. Lectures begin with a short review qualitative theory of pn junctions, bipolar and MOS devices and large and small signal models with emphasis on CMOS circuits. A variety of analog circuits are then described focusing on continuous time operational amplifiers. Frequency response, stability and compensation of the amplifier circuits will also be addressed. Lectures will conclude with special topics lectures on complex analog subsystems such as phase lock loops and A/D and D/A converters, switch capacitor circuits, and active filters. Emphasis of sub-circuit design will include schematic capture, circuit simulation, circuit layout, layout extraction and layout verification and Matlab, C or system modeling. All students will use the mixed-signal, full custom VLSI CAD software running on the Linux workstations in VLSI CAD lab for homeworks assignments and design projects.

## Analog Project Design

Student are required to be involved with the design and layout of a custom analog VLSI device using the VLSI design kit base on the .13um analog CMOS process technology for their project. Students will work in project teams of one to three depending on the complexity of their circuit macros and functionality. There will be many checkpoints during the semester to verify the progression of each of your analog macro design. Meeting and passing these checkpoints is crucial in order to successfully complete the project. Completion of the design is an important aspect of the project..

**Homework assignments and Exams**
There will be 6 HW assignments which include analog circuit design, analysis and circuit layout and layout verification using the VLSI CAD tools located on vlsi workstations in Room 160 of Hudson Hall. There will be 3 midterms during this semester.

**Course Grading**
Design Project: 25%; Homeworks: 20%  3 Midterm Exams: 55%

**ECE532 Design Project Information**
An analog circuit design project will collectively be decided prior to individual work groups are finalized. You will work in groups of one to three to specify, design, verify, and layout your custom macro on the device. The complexity and functionality of the design is more important than the number of transistors. All projects will take advantage of hierarchy of the sub-macros so that these individual sub-macros can be first implemented and completed for partial credit. Thus, you will have at minimum, completed sub-macros, rather than an incomplete top level system if time becomes a problem. Your group should discuss your project with the professor to check the magnitude and scope of the project, and give any required design assistance if needed.

There will be several checkpoints during the semester to verify the progress of your design project using a powerpoint presentation that is uploaded to each of your Sakai Dropbox. For each checkpoint in the presentation show the project and describe the state of the design and verification. The presentation should be expanded as progress is made. The final report should discuss 1) the function of the macro, 2) the architecture of the macro, 3) relevant cell designs, 4) the pin map, 5) the size of the macro, 6) meaningful results of testing the design and how the final macro will be tested, and 7) the status of the design. The first checkpoint is to verify that you have a good idea of what you will design, and have a vague idea of how you will design and test it.

For the second checkpoint you should have high-level design complete using Matlab or C or some Spectre model. You should simulate this high-level design to verify the functionality of your design. Also, try to estimate the layout size and power consumption of various aspects of the design. The third checkpoint is to verify that the design has progressed to a more detailed schematic level. You must have a more detailed (such as device level) design implemented and simulated using the Spectre circuit simulator of the Cadence design kit. The detailed operation of your macro must be complete. You should have begun the layout of some of smaller circuit cells. The fourth checkpoint is to verify that the design of the circuit modules are complete. The Spectre simulator tools will be used to simulate all the circuits. They should also be simulated with DC, AC and Transient simulations. The final checkpoint is when the project is due. The entire layout should be complete and tested. All verification tools must have been run on the layout (DRC and LVS). The report should be complete and the design should be ready to send in to be fabricated. Note that going from checkpoint 4 to checkpoint 5 is usually not easy. Sometimes cells do not fit together in the proposed floorplan, routine is very complex, or module interfaces are incompatible. Each group will give oral presentations of their project status during the last week of school. Your final project presentation will be during the ECE532 final exam time slot (or sooner) with each group team presenting to Dr. Morizio and the TAs.

# ECE532 Project Checkpoints

## Table 1: Student Design Project Checkpoint

| Date | Task Guidelines |
|---|---|
| 2/1 | analog macro function - what is your team's macro project<br>high-level outline - what functional units are required<br>- how will the design be tested |
| 3/1 | detail analog macro specification function<br>high-level system description using Matlab<br>high level design complete; high level simulation<br>initial macro sizing complete: Area, Power,<br>testing of the high-level design |
| 3/15 | analog macro specification and floorplan complete - detailed function complete<br>device level design - Mentor schematic complete<br>device simulation complete - Hspice simulation complete<br>macro layout begin - Analog layout of primitive cells |
| 4/10 | macro layout and module design complete<br>module testing complete: simulation, static verification |
| Final Exam date/time | Final Project Presentation; submit project report to your Dropbox on Sakai |

Some analog design project ideas are below:

Low power clock generation circuit using off chip crystal.
High Order Active Filters; Analog Phase Lock Loop (PLL), 5-bit Flash A/D converter 100Mhz, or D/A converter; 10-bit Audio A/D converter, Switch Capacitor Bandpass Filters; DC-DC Converter, High Gain Audio Amplifier with analog selector
10 MS/s Modem Transceiver; Sigma Delta A/D converter

Some project reports from previous semesters can be viewed shown below:

http://people.ee.duke.edu/~jmorizio/ee299/projects_2009/2009.projects.html

http://people.ee.duke.edu/~jmorizio/ee299/projects_2010/2010.projects.html

# ECE532 Course Outline

## Section 1: Integrated Analog CMOS Fundamentals

Week 1) Introduction
- Overview of Integrated Analog Circuits
- Effects VLSI Technology Evolution on Analog Circuit Design
- CMOS Physics, CMOS Device Models, Small Signal Model,
- CMOS Current Mirrors/Source Follower Amplifier
- Common-sources Amplifier

Week 2) Analog CMOS Process and Layout Techniques
- CMOS Process Ground Rules, CMOS Processing Steps
- Passive Components (Resistors, Capacitors, Inductors)
- Layout Matching and Common Centroid Techniques
- Parasitic Extraction, Mixed Signal Guard Rings
- CAD VLSI training

Week 3) Basic OPamp Design, Theory and Compensation
- Two-Stage Operational Amplifier
- Feedback and Compensation

Week 4-5) Advanced Opamps
- Folded Cascode
- Fully Differential Opamp
- Rail to Rail
- Class AB
- Common Mode Feedback Circuits

Week 6) Noise Sources
- Thermal, Flicker, Shot, Substrate, Power Supply, etc.
- Modeling Techniques
- Noise Analysis Examples

Week 7) Midterm and Project Presentations

# Section II: Analog Subsystems and Circuits

Week 8) Comparators and Voltage Reference Circuits
- Simple Opamp Comparator, Latched Comparators
- Bias Generators and BandGaps

Week 9) Switched Capacitor Circuits
- Operation and Analysis
- First Order Integrators and Gain Circuits
- Biquad Filters

Week 10-11) A/D Conversion Techniques
- Ideal A/D converter, Quantization Noise
- Nyquist Rate Sampling A/Ds
- Integrating, Successive Approximation
- Flash A/Ds, Interpolating, Folding, Time-Interleaved
- Pipeline A/Ds
- Oversampling Conversion
- Noise Shaping and Sigma Delta A/Ds
- Multi-Bit, Hybrid, Cascoded Architectures

Week 12) D/A Conversion Techniques
- Ideal D/A converter
- Binary Scaled D/As
- Decoder Based Converters
- Hybrid and Oversampling D/As

Week 13) PLLs and Frequency Synthesizers
- Digital PLLs versus Analog
- Phase/Frequency Detector, Charge Pumps and VCO circuits
- 1st order and 2nd Order Loop Filters, Linear Modeling

Week 14) Miscellaneous
- Charge Pumps
- Receiver/Transmitter

Final Exam, Final Project Presentation