计算机组织与体系结构实习报告

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cache管理策略优化

请填写以下参数。(10分)

默认配置下,32nm工艺节点下,L1 Cache的 Hit Latency 为(1.48)ns,约等于(3)cycle 默认配置下,32nm工艺节点下,L2 Cache的 Hit Latency 为(1.92)ns,约等于(4)cycle

默认配置下,运行trace2017中的两个trace,结果如下:(20分)

将trace拷贝至项目根目录

```
cd sim && make && cd ..
./sim/build/CacheSimulator3-2 01-mcf-gem5-xcg.trace
./sim/build/CacheSimulator3-2 02-stream-gem5-xaa.trace
```

DRAM配置Hit Latency 80 cycle, Bus Latency 20 cycles. L1/L2和配置和上一问一致 L1 Hit Latency 3 cycles, Bus Latency 0 cycles L2 Hit Latency 4 cycles, Bus Latency 6 cycles

```
root@585b0cdf36e6:/workspaces/Workspace# ./sim/build/CacheSimulator3-2 01-mcf-
gem5-xcg.trace
L1 Total Reads: 181708
L2 Total Read Misses: 41626
L1 Total Writes: 50903
L1 Total Write Misses: 5002
L1 Miss Rate: 20.05%
L1 Extra Info:
L2 Total Reads: 46628
L2 Total Read Misses: 22247
L2 Total Writes: 9540
L2 Total Write Misses: 0
L2 Miss Rate: 39.61%
L2 Extra Info:
Main Memory Total Reads: 22247
Main Memory Total Writes: 2535
Total Latency: 3737713
Average Latency: 16.07
root@585b0cdf36e6:/workspaces/Workspace# ./sim/build/CacheSimulator3-2 02-stream-
gem5-xaa.trace
L1 Total Reads: 113651
L2 Total Read Misses: 12314
L1 Total Writes: 49245
L1 Total Write Misses: 6159
```

```
L1 Miss Rate: 11.34%
L1 Extra Info:
L2 Total Reads: 18473
L2 Total Read Misses: 18473
L2 Total Writes: 5989
L2 Total Write Misses: 0
L2 Miss Rate: 75.52%
L2 Extra Info:
Main Memory Total Reads: 18473
Main Memory Total Writes: 4624
Total Latency: 3043008
Average Latency: 18.68
```

01-mcf-gem5-xcg

运行trace共(1)遍 L1 Cache: 平均 Miss Rate = (20.05%) L2 Cache: 平均 Miss Rate = (39.61%) Theoretical AMAT = (12.95) Simulated AMAT = 16.07

02-stream-gem5-xaa

运行trace共(1)遍 L1 Cache: 平均 Miss Rate = (11.34%) L2 Cache: 平均 Miss Rate = (75.52%) AMAT = (12.70) Simulated AMAT = 18.68

> 程序运行结果平均延时大于上面的数值。因为上面的数值使用公式计算，而模拟器是用总延迟除以总访问次数，其中包含了驱逐块的延迟. 即使将evict时间设置为0，模拟器的平均延迟也会大于理论值，因为统计的miss rate包含了驱逐操作，所以miss rate偏低.(驱逐dirty块写基本都会命中) 为了方便后续优化均采用Simulated AMAT

单项优化测试

1. 预取4行

覆盖率和准确性均以块为单位

> L1, L2预取后4行(包含访问请求的行)

```
root@585b0cdf36e6:/workspaces/Workspace# ./sim/build/CacheSimulator3-2 01-mcf-gem5-xcg.trace --opt1
L1 Total Reads: 181708
L2 Total Read Misses: 37468
L1 Total Writes: 50903
L1 Total Write Misses: 3542
L1 Miss Rate: 17.63%
L1 Extra Info:
Prefetch count: 89027
Prefetch cover count: 98865
Prefetch hit count: 13296
Coverage Rate: 0.425023
Prefetch Accuracy: 0.149348
L2 Total Reads: 130037
L2 Total Read Misses: 24113
```

```
L2 Total Writes: 13025
L2 Total Write Misses: 0
L2 Miss Rate: 16.85%
L2 Extra Info:
Prefetch count: 40678
Prefetch cover count: 77020
Prefetch hit count: 38582
Coverage Rate: 0.538368
Prefetch Accuracy: 0.948473
Main Memory Total Reads: 64791
Main Memory Total Writes: 4286
Total Latency: 3173963
Average Latency: 13.64
root@585b0cdf36e6:/workspaces/Workspace# ./sim/build/CacheSimulator3-2 02-stream-gem5-xaa.trace --opt1
L1 Total Reads: 113651
L2 Total Read Misses: 3081
L1 Total Writes: 49245
L1 Total Write Misses: 1541
L1 Miss Rate: 2.84%
L1 Extra Info:
Prefetch count: 13863
Prefetch cover count: 125952
Prefetch hit count: 13851
Coverage Rate: 0.773205
Prefetch Accuracy: 0.999134
L2 Total Reads: 18485
L2 Total Read Misses: 4622
L2 Total Writes: 5990
L2 Total Write Misses: 0
L2 Miss Rate: 18.88%
L2 Extra Info:
Prefetch count: 13863
Prefetch cover count: 18353
Prefetch hit count: 13863
Coverage Rate: 0.749867
Prefetch Accuracy: 1
Main Memory Total Reads: 18485
Main Memory Total Writes: 4624
Total Latency: 1127678
Average Latency: 6.92
```

提升分别为1.18x和2.70x

2. Non-Blocking Cache, L1 4 MSHR, L2 8 MSHR

```
root@585b0cdf36e6:/workspaces/Workspace# ./sim/build/CacheSimulator3-2 01-mcf-gem5-xcg.trace --opt2
L1 Total Reads: 181708
L2 Total Read Misses: 41626
L1 Total Writes: 50903
```

```
L1 Total Write Misses: 5002
L1 Miss Rate: 20.05%
L1 Extra Info:
Hit Under Miss: 26808
MSHR Coverage Rate: 0.57
L2 Total Reads: 46628
L2 Total Read Misses: 22247
L2 Total Writes: 9540
L2 Total Write Misses: 0
L2 Miss Rate: 39.61%
L2 Extra Info:
Hit Under Miss: 7157
MSHR Coverage Rate: 0.32
Main Memory Total Reads: 22247
Main Memory Total Writes: 2535
Total Latency: 1922413
Average Latency: 8.26
root@585b0cdf36e6:/workspaces/Workspace# ./sim/build/CacheSimulator3-2 02-stream-gem5-xaa.trace --opt2
L1 Total Reads: 113651
L2 Total Read Misses: 12314
L1 Total Writes: 49245
L1 Total Write Misses: 6159
L1 Miss Rate: 11.34%
L1 Extra Info:
Hit Under Miss: 15108
MSHR Coverage Rate: 0.82
L2 Total Reads: 18473
L2 Total Read Misses: 18473
L2 Total Writes: 5989
L2 Total Write Misses: 0
L2 Miss Rate: 75.52%
L2 Extra Info:
Hit Under Miss: 7782
MSHR Coverage Rate: 0.42
Main Memory Total Reads: 18473
Main Memory Total Writes: 4624
Total Latency: 868658
Average Latency: 5.33
```

提升分别为1.95x和3.50x

请填写最终确定的优化方案,并陈述理由。对于涉及到的算法,需要详细描述算法设计和实现思路,并给出优缺点分析。(20分)

L1，L2预取后四行 Non-Blocking Cache L1 4 MSHR, L2 8 MSHR

Overhead: 预取逻辑+额外MissRate * 3的线路带宽+12 MSHR+Non-Blocking的处理逻辑

优点是还算简单有效，缺点还是还是没能在线识别访存逻辑

```
root@585b0cdf36e6:/workspaces/Workspace# ./sim/build/CacheSimulator3-2 01-mcf-gem5-xcg.trace --opt5
L1 Total Reads: 181708
L2 Total Read Misses: 37468
L1 Total Writes: 50903
L1 Total Write Misses: 3542
L1 Miss Rate: 17.63%
L1 Extra Info:
Prefetch count: 89027
Prefetch cover count: 98865
Prefetch hit count: 13296
Coverage Rate: 0.425023
Prefetch Accuracy: 0.149348
Hit Under Miss: 25527
MSHR Coverage Rate: 0.62
L2 Total Reads: 130037
L2 Total Read Misses: 24113
L2 Total Writes: 13025
L2 Total Write Misses: 0
L2 Miss Rate: 16.85%
L2 Extra Info:
Prefetch count: 40678
Prefetch cover count: 77020
Prefetch hit count: 38582
Coverage Rate: 0.538368
Prefetch Accuracy: 0.948473
Hit Under Miss: 8506
MSHR Coverage Rate: 0.35
Main Memory Total Reads: 64791
Main Memory Total Writes: 4286
Total Latency: 1626773
Average Latency: 6.99
root@585b0cdf36e6:/workspaces/Workspace# ./sim/build/CacheSimulator3-2 02-stream-gem5-xaa.trace --opt5
L1 Total Reads: 113651
L2 Total Read Misses: 3081
L1 Total Writes: 49245
L1 Total Write Misses: 1541
L1 Miss Rate: 2.84%
L1 Extra Info:
Prefetch count: 13863
Prefetch cover count: 125952
Prefetch hit count: 13851
Coverage Rate: 0.773205
Prefetch Accuracy: 0.999134
Hit Under Miss: 4622
MSHR Coverage Rate: 1.00
L2 Total Reads: 18485
L2 Total Read Misses: 4622
L2 Total Writes: 5990
L2 Total Write Misses: 0
L2 Miss Rate: 18.88%
L2 Extra Info:
```

```
Prefetch count: 13863
Prefetch cover count: 18353
Prefetch hit count: 13863
Coverage Rate: 0.749867
Prefetch Accuracy: 1
Hit Under Miss: 4621
MSHR Coverage Rate: 1.00
Main Memory Total Reads: 18485
Main Memory Total Writes: 4624
Total Latency: 488688
Average Latency: 3.00
```

01-mcf-gem5-xcg 运行trace共(1)遍 L1 Cache: 平均 Miss Rate = (17.63%) L2 Cache: 平均 Miss Rate = (16.85%) Simulated AMAT =(6.99) 02-stream-gem5-xaa 运行trace共(1)遍 L1 Cache: 平均 Miss Rate = (2.84%) L2 Cache: 平均 Miss Rate = (18.88%) Simulated AMAT =(3.00)

提升分别为2.30x和6.23x