

JIAYONG LI | RESUME

Education

D-ITET(Electrical Engineering Department) - ETH Zürich, Switzerland

09/2021 - now

- MSc in Quantum Engineering

School of Physics - Peking University(PKU), China

09/2017 - 07/2021

- Bachelor of Science

Internship

Intern in Digital Design IC for Machine Learning Acceleration - Huawei Zürich Research Center

10/2022 - 03/2023

- Hardware-software codesign for smart data mover on Ascend platform
- Enhanced DMA design for Da Vinci Architecture in Huawei Ascend AI processor
- Custom operators development on both GPU and Ascend
- Up to **7x** acceleration for convolution operators in EfficientDet on MOT17 task
- Up to **10%** acceleration for the matrix-matrix multiplication operators for an internal recommender model **without any precision loss**

Project Experience

If you are interested in details, visit: jia-yli.github.io/projects.

On Going

Omni-directional Event-based Monitoring System - Prof. Luca Benini's Group, ETH

10/2023 - Now

- Interface board (PCB) design for event-based sensor array and Nvidia Jetson AGX Orin
- Image stitching and object detection algorithm

FPGA Acceleration for Storage Deduplication - Prof. Gustavo Alonso's group, ETH

04/2023 - Now

- A transparent FPGA-based layer between CPU and SSD, which is dedicated to storage deduplication
- Support all common requests (write/read/erase) and implemented fully in hardware
- Single board: 100Gbps throughput and $< 30 \mu s$ latency for all requests (**10x** faster than previous result)
- Implementing multi-board version with distributed hash table utilizing RDMA
- **Finalizing project and preparing for submission**

Dynamic Rendering of Neural Implicit Representations in VR - Course Project, Mixed Reality, ETH

10/2023 - Now

- Time series geometry and color information extraction from SDF-based models
- Real-time rendering of dynamic meshes in VR

2022 - 2023

Eclipse: Tapeout and Testing - Prof. Luca Benini's group, ETH

05/2022 - 07/2023

- A SoC using PULPissimo architecture, which features SR extension, X-interface, and T-head DIV/SQRT unit
- Tapeout: system integration and full backend process in TSMC 65nm
- Testing: real chip is tested on the tester for speed and power, 370MHz@1.2V and room temperature
- [Link to Eclipse in IIS Chip Gallery](#), [link to more details on Eclipse architecture and testing results](#)

RISC-V Stochastic Rounding(SR) Extension - Prof. Luca Benini's group, ETH

02/2022 - 07/2022

- First open-source hardware SR implementation
- Design of rounding unit that supports the five existing RISC-V rounding modes and SR extension
- Transprecision capability: supports different floating-point(FP) formats from FP64 to custom FP8.
- **Integrated into OpenHW Group's CVFPU as an extension for the RISC-V FP specification:** [link to GitHub](#)

2021 and Before

Undergraduate Research in Topological Photonics - Prof. Renmin Ma's Group, PKU

02/2018 - 07/2021

- The first exploration of polarization vortices outside the first Brillouin zone
- Design and simulation of photonic crystal nano-cavities with novel polarization characteristics
- Theoretical analysis of higher-order Bloch waves and generic model for polarization singularities
- **Follow-up work published in Nature Communications:** [link to publication](#)

Skills

- **Software:** COMSOL Multiphysics, MATLAB, Wolfram Mathematica, Unity, Blender.
- **Coding and scripting:** C, C#, C++, CUDA, Python, Java, Scala, SystemVerilog, Tcl, Bash
- **Industry-standard VLSI design tools:** QuestaSim, Verilator, Vivado, Synopsys Design Compiler, Innovus, Calibre

Others

- Silver medal in 33rd Chinese Physics Olympiad, CPhO 11/2016
- Silver medal in 32nd Chinese Physics Olympiad, CPhO 11/2015