Jialin (Jayleen) **Yuan**

https://jia2lin3yuan1.github.io/
linkedin.com/in/jialinyuan github.com/jia2lin3yuan1 yuanjial@oregonstate.edu +1 (541) 602-4658

Education

Sep.2016 - EXP. Spring 2023	**Oregon State University**, Oregon, U.S	Ph.D student in Computer Science ·**Computer Vision**
Sep.2010- Mar.2013	**Xidian University**, Xi'an, China	M.S in Computer Science ·**Artificial Intelligence**
Sep.2006- Jun.2010	**Xidian University**, Xi'an, China	B.S. in Computer Application Technology

Skills

Programming Languages :	(Proficient) C/C++, Python; (Familiar) Matlab, Java, Bash
Deep Learning Frameworks :	PyTorch, Tensorflow, Keras
Others Tools and Languages :	Git, LaTeX, FPGA, RTL

Projects

- **Research on topic 'Deep Object Discovery'**
  - Research on Vision-Language understanding task and proposed a method to effectively learn the united semantic information from asymmetric modalities. A paper submitted to ICCV 2023.
  - Research on Unsupervised Video Object Discovery task and proposed a method to efficiently improve performance in the detect-propagate paradigm. A paper submitted a paper to ICCV 2023.
  - Research on Instance Segmentation task, Proposed a search-free Instance semantic Segmentation algorithm accepted on NeurIPS 2020 (Paper Link).
- **Lead on developing the Plant Phenotyping method for GWAS in Populus trichocarpa**
  - Developed a web-based image annotator for fast and accurate pixel-wise object and category annotation (Link).
  - Performed plant phenotype analysis with the tool and submitted a paper to PlantPhenomics (Paper Link).
  - Developed an algorithm for root analysis in a GWAS study (Paper Link).
- **Contribute to the DARPA Machine Common Sense Project**
  - Built perception system for the DARPA Machine Common Sense Project for discovering novel objects of interest from videos.
- **Contribute to the design of 4K chip solution on FRC (Frame Rate Conversion) function**
  - Developed the C model for FRC and support the digital designer to develop its chip solution.
  - Led on FPGA validation and chip validation on FRC.
  - Supported on PQ tuning and customer support.

Experience

Jun. 2022 – Mar. 2022 | **Research Intern | Microsoft Inc, Bellevue, Washington, U.S**
- Interned in the ROAR team under Decision AI. Research on the problem of video object segmentation (Paper Link, ECCV 2022) and the problem of Vision-Language content moderation detection (a submission to ICCV 2023).

Sep. 2019 – Jul. 2019 | **Software Engineer Intern | Uber Technology Inc, Palo Alto, California, U.S**
- Developed Image Style Transfer algorithm using GAN, to augment data in minor categories and address the data imbalance problem.
- Included the generated data into the collected dataset to train a scene classification model, it obtained at least 8% improvement on the minor categories without influencing the other categories.

Jun. 2016 – Mar. 2014 | **Algorithm Engineer | Kiwi-image Technologies Co, Ltd., Shanghai, China**
- Developed algorithm for FRC(Frame Rate Conversion) and OD(Over Drive) modules used in High-end TV solutions and co-worked with Digital Designers for porting to RTL(Register Transfer Language).
- Developed a phase-table tool to assist timing control analysis in the FRC module on the chip, it improved the timing tuning efficiency over 10X.
- Participated in the development of embedded dynamic software, chip validation, and PQ tuning for customer support.

Mar. 2014 – Apr. 2013 | **Algorithm Engineer | Novatek Co, Ltd., Shanghai, China**
- Maintained algorithms for 2d-to-3d, free-3d, and image compression modules used in TV solutions. Built their bit-true C-models for RTL comparison and the embedded dynamic software used in Chip.