

TABLE 25-2: PIC18(L)F2X/4XK22 INSTRUCTION SET

Mnemonic, Operands	Description	Cycles	16-Bit Instruction Word				Status Affected	Notes	
			MSb		LSb				
BYTE-ORIENTED OPERATIONS									
ADDWF	f, d, a	Add WREG and f	1	0010	01da	ffff	ffff	C, DC, Z, OV, N	1, 2
ADDWFC	f, d, a	Add WREG and CARRY bit to f	1	0010	00da	ffff	ffff	C, DC, Z, OV, N	1, 2
ANDWF	f, d, a	AND WREG with f	1	0001	01da	ffff	ffff	Z, N	1, 2
CLRF	f, a	Clear f	1	0110	101a	ffff	ffff	Z	2
COMF	f, d, a	Complement f	1	0001	11da	ffff	ffff	Z, N	1, 2
CPFSEQ	f, a	Compare f with WREG, skip =	1 (2 or 3)	0110	001a	ffff	ffff	None	4
CPFSGT	f, a	Compare f with WREG, skip >	1 (2 or 3)	0110	010a	ffff	ffff	None	4
CPFSLT	f, a	Compare f with WREG, skip <	1 (2 or 3)	0110	000a	ffff	ffff	None	1, 2
DECf	f, d, a	Decrement f	1	0000	01da	ffff	ffff	C, DC, Z, OV, N	1, 2, 3, 4
DECFSZ	f, d, a	Decrement f, Skip if 0	1 (2 or 3)	0010	11da	ffff	ffff	None	1, 2, 3, 4
DCFSNZ	f, d, a	Decrement f, Skip if Not 0	1 (2 or 3)	0100	11da	ffff	ffff	None	1, 2
INCF	f, d, a	Increment f	1	0010	10da	ffff	ffff	C, DC, Z, OV, N	1, 2, 3, 4
INCFSZ	f, d, a	Increment f, Skip if 0	1 (2 or 3)	0011	11da	ffff	ffff	None	4
INFSNZ	f, d, a	Increment f, Skip if Not 0	1 (2 or 3)	0100	10da	ffff	ffff	None	1, 2
IORWF	f, d, a	Inclusive OR WREG with f	1	0001	00da	ffff	ffff	Z, N	1, 2
MOVF	f, d, a	Move f	1	0101	00da	ffff	ffff	Z, N	1
MOVFF	f <sub>s</sub> , f <sub>d</sub>	Move f <sub>s</sub> (source) to f <sub>d</sub> (destination) 2nd word	2	1100	ffff	ffff	ffff	None	
				1111	ffff	ffff	ffff		
MOVWF	f, a	Move WREG to f	1	0110	111a	ffff	ffff	None	
MULWF	f, a	Multiply WREG with f	1	0000	001a	ffff	ffff	None	1, 2
NEGF	f, a	Negate f	1	0110	110a	ffff	ffff	C, DC, Z, OV, N	
RLCF	f, d, a	Rotate Left f through Carry	1	0011	01da	ffff	ffff	C, Z, N	1, 2
RLNCF	f, d, a	Rotate Left f (No Carry)	1	0100	01da	ffff	ffff	Z, N	
RRCF	f, d, a	Rotate Right f through Carry	1	0011	00da	ffff	ffff	C, Z, N	
RRNCF	f, d, a	Rotate Right f (No Carry)	1	0100	00da	ffff	ffff	Z, N	
SETF	f, a	Set f	1	0110	100a	ffff	ffff	None	1, 2
SUBFWB	f, d, a	Subtract f from WREG with borrow	1	0101	01da	ffff	ffff	C, DC, Z, OV, N	
SUBWF	f, d, a	Subtract WREG from f	1	0101	11da	ffff	ffff	C, DC, Z, OV, N	1, 2
SUBWFB	f, d, a	Subtract WREG from f with borrow	1	0101	10da	ffff	ffff	C, DC, Z, OV, N	
SWAPF	f, d, a	Swap nibbles in f	1	0011	10da	ffff	ffff	None	4
TSTFSZ	f, a	Test f, skip if 0	1 (2 or 3)	0110	011a	ffff	ffff	None	1, 2
XORWF	f, d, a	Exclusive OR WREG with f	1	0001	10da	ffff	ffff	Z, N	
LITERAL OPERATIONS									
ADDLW	k	Add literal and WREG	1	0000	1111	kkkk	kkkk	C, DC, Z, OV, N	
ANDLW	k	AND literal with WREG	1	0000	1011	kkkk	kkkk	Z, N	
IORLW	k	Inclusive OR literal with WREG	1	0000	1001	kkkk	kkkk	Z, N	
LFSR	f, k	Move literal (12-bit) 2nd word to FSR(f) 1st word	2	1110	1110	00ff	kkkk	None	
				1111	0000	kkkk	kkkk		
MOVLB	k	Move literal to BSR<3:0>	1	0000	0001	0000	kkkk	None	
MOVLW	k	Move literal to WREG	1	0000	1110	kkkk	kkkk	None	
MULLW	k	Multiply literal with WREG	1	0000	1101	kkkk	kkkk	None	
RETLW	k	Return with literal in WREG	2	0000	1100	kkkk	kkkk	None	
SUBLW	k	Subtract WREG from literal	1	0000	1000	kkkk	kkkk	C, DC, Z, OV, N	
XORLW	k	Exclusive OR literal with WREG	1	0000	1010	kkkk	kkkk	Z, N	
DATA MEMORY ↔ PROGRAM MEMORY OPERATIONS									
TBLRD*		Table Read	2	0000	0000	0000	1000	None	
TBLRD*+		Table Read with post-increment		0000	0000	0000	1001	None	
TBLRD*-		Table Read with post-decrement		0000	0000	0000	1010	None	
TBLRD*+		Table Read with pre-increment		0000	0000	0000	1011	None	
TBLWT*		Table Write	2	0000	0000	0000	1100	None	
TBLWT*+		Table Write with post-increment		0000	0000	0000	1101	None	
TBLWT*-		Table Write with post-decrement		0000	0000	0000	1110	None	
TBLWT*+		Table Write with pre-increment		0000	0000	0000	1111	None	
BIT-ORIENTED OPERATIONS									
BCF	f, b, a	Bit Clear f	1	1001	bbba	ffff	ffff	None	1, 2
BSF	f, b, a	Bit Set f	1	1000	bbba	ffff	ffff	None	1, 2
BTFSC	f, b, a	Bit Test f, Skip if Clear	1 (2 or 3)	1011	bbba	ffff	ffff	None	3, 4
BTFSS	f, b, a	Bit Test f, Skip if Set	1 (2 or 3)	1010	bbba	ffff	ffff	None	3, 4
BTG	f, b, a	Bit Toggle f	1	0111	bbba	ffff	ffff	None	1, 2

d = 0 for result destination to be WREG register  
d = 1 for result destination to be file register (f)

a = 0 to force Access Bank  
a = 1 for BSR to select bank

CONTROL OPERATIONS									
BC	n	Branch if Carry	1 (2)	1110	0010	nnnn	nnnn	None	4
BN	n	Branch if Negative	1 (2)	1110	0110	nnnn	nnnn	None	
BNC	n	Branch if Not Carry	1 (2)	1110	0011	nnnn	nnnn	None	
BNN	n	Branch if Not Negative	1 (2)	1110	0111	nnnn	nnnn	None	
BNOV	n	Branch if Not Overflow	1 (2)	1110	0101	nnnn	nnnn	None	
BNZ	n	Branch if Not Zero	1 (2)	1110	0001	nnnn	nnnn	None	
BOV	n	Branch if Overflow	1 (2)	1110	0100	nnnn	nnnn	None	
BRA	n	Branch Unconditionally	2	1101	0nnn	nnnn	nnnn	None	
BZ	n	Branch if Zero	1 (2)	1110	0000	nnnn	nnnn	None	
CALL	k, s	Call subroutine 1st word	2	1110	110s	kkkk	kkkk	None	
		2nd word		1111	kkkk	kkkk	kkkk	None	
CLRWDT	—	Clear Watchdog Timer	1	0000	0000	0000	0100	TO, PD	
DAW	—	Decimal Adjust WREG	1	0000	0000	0000	0111	C	
GOTO	k	Go to address 1st word	2	1110	1111	kkkk	kkkk	None	
		2nd word		1111	kkkk	kkkk	kkkk	None	
NOP	—	No Operation	1	0000	0000	0000	0000	None	
NOP	—	No Operation	1	1111	xxxx	xxxx	xxxx	None	
POP	—	Pop top of return stack (TOS)	1	0000	0000	0000	0110	None	
PUSH	—	Push top of return stack (TOS)	1	0000	0000	0000	0101	None	
RCALL	n	Relative Call	2	1101	1nnn	nnnn	nnnn	None	
RESET		Software device Reset	1	0000	0000	1111	1111	All	
RETFIE	s	Return from interrupt enable	2	0000	0000	0001	000s	GIE/GIEH, PEIE/GIEL	
RETLW	k	Return with literal in WREG	2	0000	1100	kkkk	kkkk	None	
RETURN	s	Return from Subroutine	2	0000	0000	0001	001s	None	
SLEEP	—	Go into Standby mode	1	0000	0000	0000	0011	TO, PD	

## 27.8 DC Characteristics: Input/Output Characteristics, PIC18(L)F2X/4XK22

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature: -40°C ≤ Ta ≤ +125°C				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D140 D140A	V <sub>IL</sub>	<b>Input Low Voltage</b>					
		I/O PORT:					
		with TTL buffer	—	—	0.8	V	4.5V ≤ V <sub>DD</sub> ≤ 5.5V
D147 D147A	V <sub>IH</sub>	<b>Input High Voltage</b>					
		I/O ports:					
		with TTL buffer	2.0	—	—	V	4.5V ≤ V <sub>DD</sub> ≤ 5.5V
D159	V <sub>OL</sub>	<b>Output Low Voltage</b>					
		I/O ports	—	—	0.6	V	I <sub>OL</sub> = 8 mA, V <sub>DD</sub> = 5V I <sub>OL</sub> = 6 mA, V <sub>DD</sub> = 3.3V I <sub>OL</sub> = 1.8 mA, V <sub>DD</sub> = 1.8V
D161	V <sub>OH</sub>	<b>Output High Voltage<sup>(3)</sup></b>					
		I/O ports	V <sub>DD</sub> - 0.7	—	—	V	I <sub>OH</sub> = 3.5 mA, V <sub>DD</sub> = 5V I <sub>OH</sub> = 3 mA, V <sub>DD</sub> = 3.3V I <sub>OH</sub> = 1 mA, V <sub>DD</sub> = 1.8V
D155	I <sub>IL</sub>	<b>Input Leakage I/O and MCLR<sup>(2),(3)</sup></b>					
		I/O ports and MCLR	—	0.1	50	nA	V <sub>SS</sub> ≤ V <sub>PIN</sub> ≤ V <sub>DD</sub> , Pin at high-impedance
			—	0.7	100	nA	≤ +25°C <sup>(4)</sup>
			—	4	200	nA	+60°C
			—	35	1000	nA	+85°C
							+125°C

Total power dissipation (Note 1)	1.0W
Maximum current out of V <sub>SS</sub> pin (-40°C to +85°C)	300 mA
Maximum current out of V <sub>SS</sub> pin (+85°C to +125°C)	125 mA
Maximum current into V <sub>DD</sub> pin (-40°C to +85°C)	200 mA
Maximum current into V <sub>DD</sub> pin (+85°C to +125°C)	85 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>DD</sub> )	±20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>DD</sub> )	±20 mA
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by all ports (-40°C to +85°C)	200 mA
Maximum current sunk by all ports (+85°C to +125°C)	110 mA
Maximum current sourced by all ports (-40°C to +85°C)	185 mA
Maximum current sourced by all ports (+85°C to +125°C)	70 mA

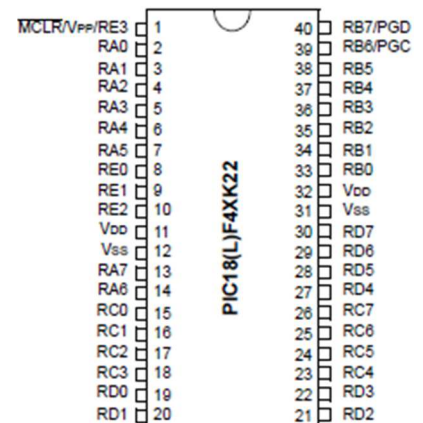
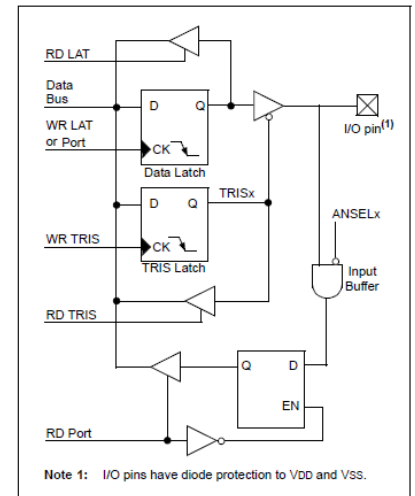
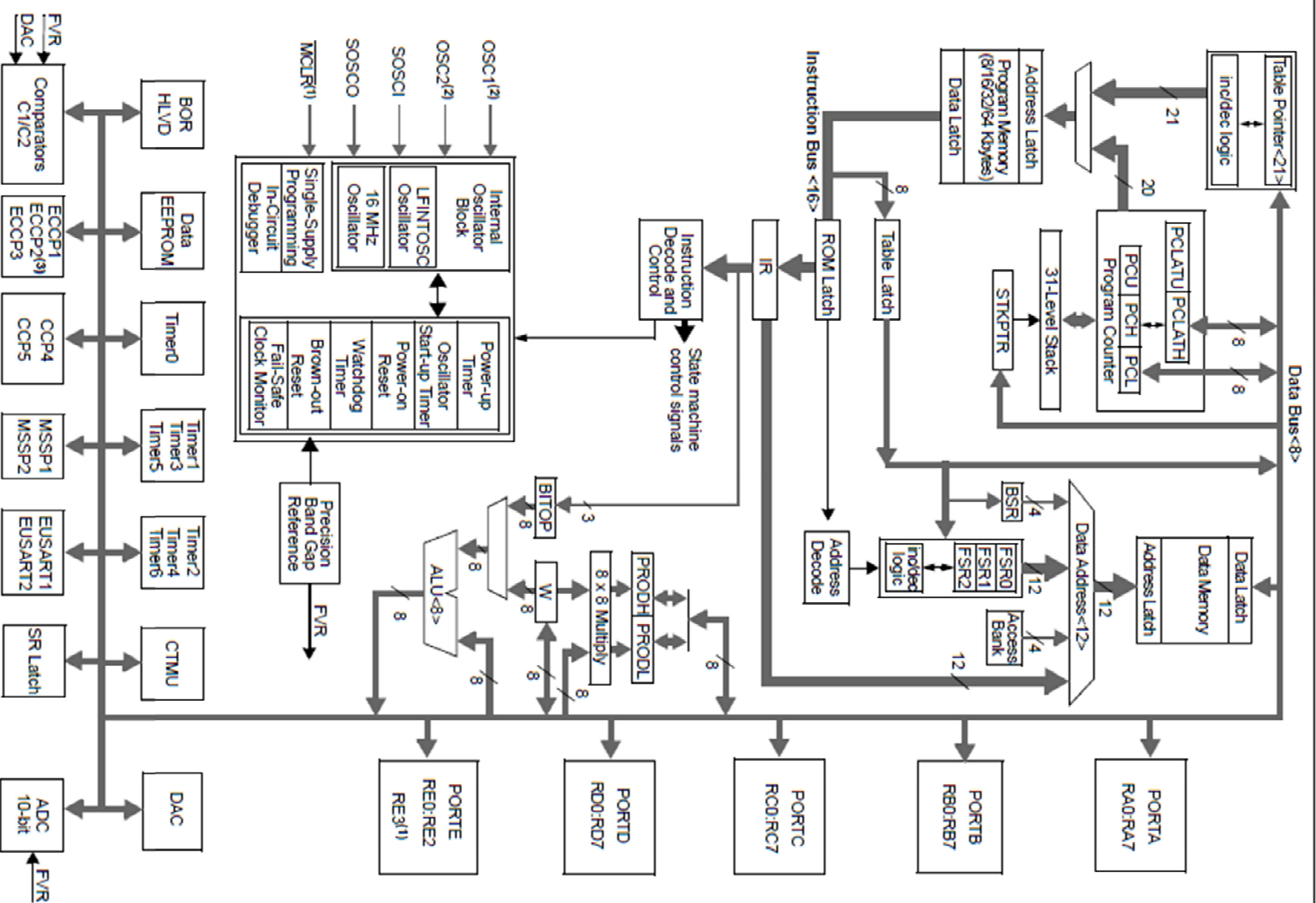


FIGURE 1-1: PIC18(L)F2X/4XK22 FAMILY BLOCK DIAGRAM

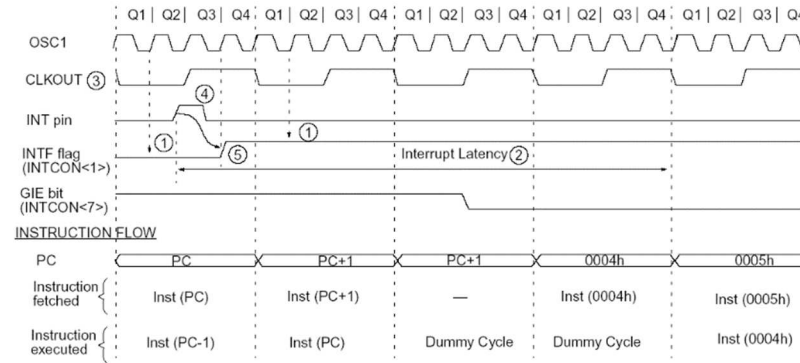


- Note 1: RE3 is only available when **MCLR** functionality is disabled.
- 2: OSC1/CLKIN and OSC2/CLKOUT are only available in select oscillator modes and when these pins are not being used as digital I/O. Refer to [Section 2.0 "Oscillator Module \(With Fail-Safe Clock Monitor\)"](#) for additional information.
- 3: Full-Bridge operation for PIC18(L)F4XK22, half-bridge operation for PIC18(L)F2XK22.

**TABLE 9-1: REGISTERS ASSOCIATED WITH INTERRUPTS**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ANSELB	—	—	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF
INTCON2	RBP1	INTEDG0	INTEDG1	INTEDG2	—	TMR0IP	—	RBIF
INTCON3	INT2IP	INT1IP	—	INT2IE	INT1IE	—	INT2IF	INT1IF
IOCB	IOCB7	IOCB6	IOCB5	IOCB4	—	—	—	—
IPR1	—	ADIP	RC1IP	TX1IP	SSP1IP	CCP1IP	TMR2IP	TMR1IP
IPR2	OSCFIP	C1IP	C2IP	EEIP	BCL1IP	HLVDIP	TMR3IP	CCP2IP
IPR3	SSP2IP	BCL2IP	RC2IP	TX2IP	CTMUIP	TMR5GIP	TMR3GIP	TMR1GIP
IPR4	—	—	—	—	—	CCP5IP	CCP4IP	CCP3IP
IPR5	—	—	—	—	—	TMR6IP	TMR5IP	TMR4IP
PIE1	—	ADIE	RC1IE	TX1IE	SSP1IE	CCP1IE	TMR2IE	TMR1IE
PIE2	OSCFIE	C1IE	C2IE	EEIE	BCL1IE	HLVDIE	TMR3IE	CCP2IE
PIE3	SSP2IE	BCL2IE	RC2IE	TX2IE	CTMUIE	TMR5GIE	TMR3GIE	TMR1GIE
PIE4	—	—	—	—	—	CCP5IE	CCP4IE	CCP3IE
PIE5	—	—	—	—	—	TMR6IE	TMR5IE	TMR4IE
PIR1	—	ADIF	RC1IF	TX1IF	SSP1IF	CCP1IF	TMR2IF	TMR1IF
PIR2	OSCFIF	C1IF	C2IF	EEIF	BCL1IF	HLVDIF	TMR3IF	CCP2IF
PIR3	SSP2IF	BCL2IF	RC2IF	TX2IF	CTMUIF	TMR5GIF	TMR3GIF	TMR1GIF
PIR4	—	—	—	—	—	CCP5IF	CCP4IF	CCP3IF
PIR5	—	—	—	—	—	TMR6IF	TMR5IF	TMR4IF
PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
RCON	IPEN	SBOREN	—	RI	TO	PD	POR	BOR

**Legend:** — = unimplemented locations, read as '0'. Shaded bits are not used for Interrupts.



- Note 1: INTF flag is sampled here (every Q1).  
 Note 2: Interrupt latency = 3-4 Tcy where Tcy = instruction cycle time.  
 Note 3: Latency is the same whether Instruction (PC) is a single cycle or a 2-cycle instruction.  
 Note 4: CLKOUT is available only in RC oscillator mode.  
 Note 5: For minimum width of INT pulse, refer to AC specs.  
 Note 6: INTF is enabled to be set anytime during the Q4-Q1 cycles.

	7	6	5	4	3	2	1	0
value after reset	TMR0ON	T08BIT	T0CS	T0SE	PSA	T0PS2	T0PS1	T0PS0
	1	1	1	1	1	1	1	1

**TMR0ON:** Timer0 on/off control bit

0 = stops Timer0

1 = Enables Timer0

**T08BIT:** Timer0 8-bit/16-bit control bit

0 = Timer0 is configured as a 16-bit timer

1 = Timer0 is configured as an 8-bit timer

**T0CS:** Timer0 clock source select

0 = Instruction cycle clock

1 = Transition on T0CKI pin

**T0SE:** Timer0 source edge select bit

0 = Increment on falling edge transition on T0CKI pin

1 = Increment on rising edge transition on T0CKI pin

**PSA:** Timer0 prescaler assignment bit

0 = Timer0 prescaler is assigned. Timer0 clock input comes from prescaler output.

1 = Timer0 prescaler is not assigned. Timer0 clock input bypasses prescaler.

**T0PS2:T0PS0:** Timer0 prescaler select bits

000 = 1:2 prescaler value

001 = 1:4 prescaler value

010 = 1:8 prescaler value

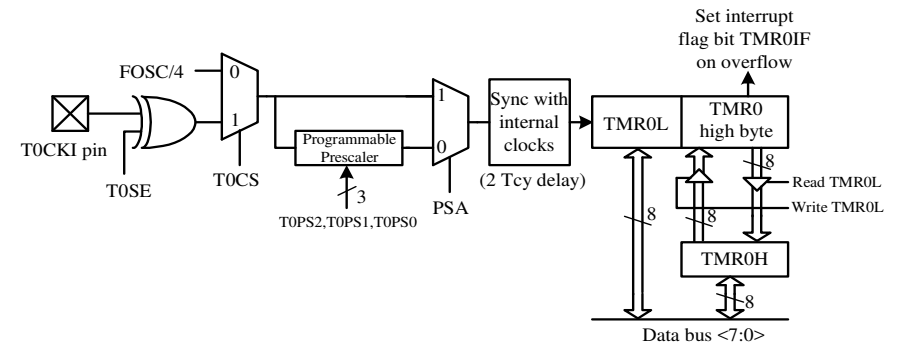
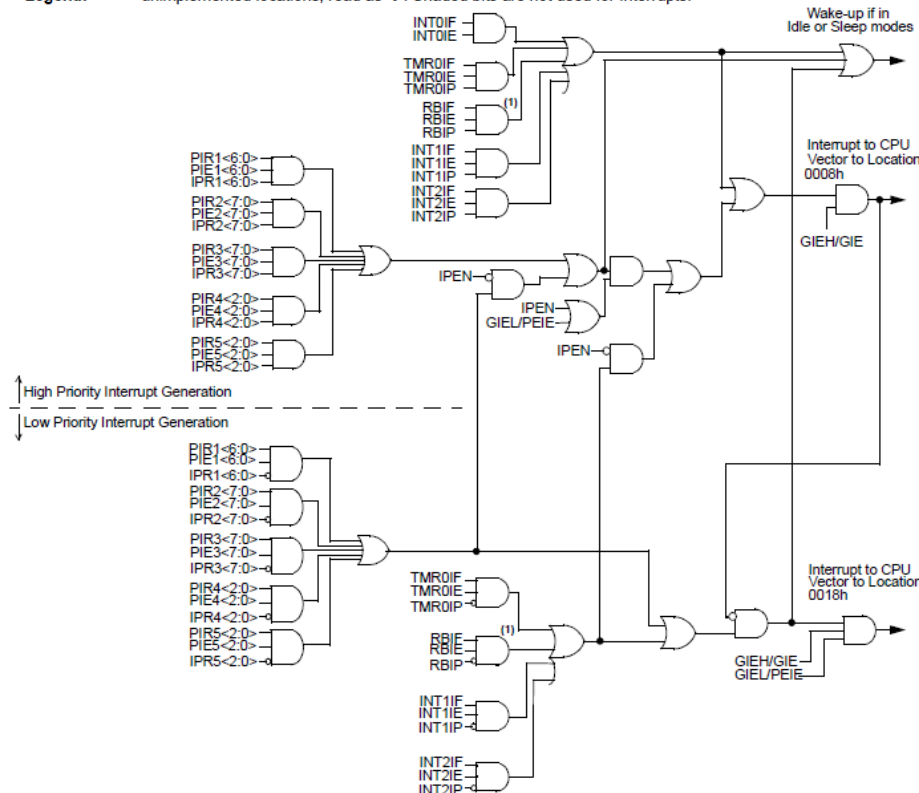
011 = 1:16 prescaler value

100 = 1:32 prescaler value

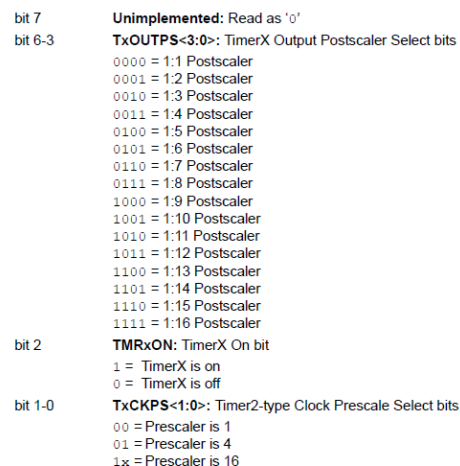
101 = 1:64 prescaler value

110 = 1:128 prescaler value

111 = 1:256 prescaler value







R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
C3TSEL<1:0>		—	C2TSEL<1:0>		—	C1TSEL<1:0>	
bit 7							bit 0

- |         |  |
|---------|--|
| bit 7-6 | <b>C3TSEL&lt;1:0&gt;:</b> CCP3 Timer Selection bits<br>00 = CCP3 – Capture/Compare modes use Timer1, PWM modes use Timer2<br>01 = CCP3 – Capture/Compare modes use Timer3, PWM modes use Timer4<br>10 = CCP3 – Capture/Compare modes use Timer5, PWM modes use Timer6<br>11 = Reserved |
| bit 5   | <b>Unused</b>  |
| bit 4-3 | <b>C2TSEL&lt;1:0&gt;:</b> CCP2 Timer Selection bits<br>00 = CCP2 – Capture/Compare modes use Timer1, PWM modes use Timer2<br>01 = CCP2 – Capture/Compare modes use Timer3, PWM modes use Timer4<br>10 = CCP2 – Capture/Compare modes use Timer5, PWM modes use Timer6<br>11 = Reserved |
| bit 2   | <b>Unused</b>  |
| bit 1-0 | <b>C1TSEL&lt;1:0&gt;:</b> CCP1 Timer Selection bits<br>00 = CCP1 – Capture/Compare modes use Timer1, PWM modes use Timer2<br>01 = CCP1 – Capture/Compare modes use Timer3, PWM modes use Timer4<br>10 = CCP1 – Capture/Compare modes use Timer5, PWM modes use Timer6<br>11 = Reserved |

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	C5TSEL<1:0>		C4TSEL<1:0>	
bit 7				bit 0			

- bit 7-4      **Unimplemented:** Read as '0'
- bit 3-2      **C5TSEL<1:0>:** CCP5 Timer Selection bits
- 00 = CCP5 – Capture/Compare modes use Timer1, PWM modes use Timer2
- 01 = CCP5 – Capture/Compare modes use Timer3, PWM modes use Timer4
- 10 = CCP5 – Capture/Compare modes use Timer5, PWM modes use Timer6
- 11 = Reserved
- bit 1-0      **C4TSEL<1:0>:** CCP4 Timer Selection bits
- 00 = CCP4 – Capture/Compare modes use Timer1, PWM modes use Timer2
- 01 = CCP4 – Capture/Compare modes use Timer3, PWM modes use Timer4
- 10 = CCP4 – Capture/Compare modes use Timer5, PWM modes use Timer6
- 11 = Reserved

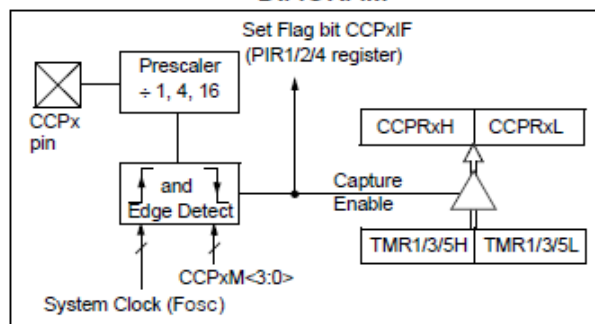
## 14.5 Register Definitions: ECCP Control

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DCxB<1:0>		CCPxM<3:0>			
bit 7		bit 0					

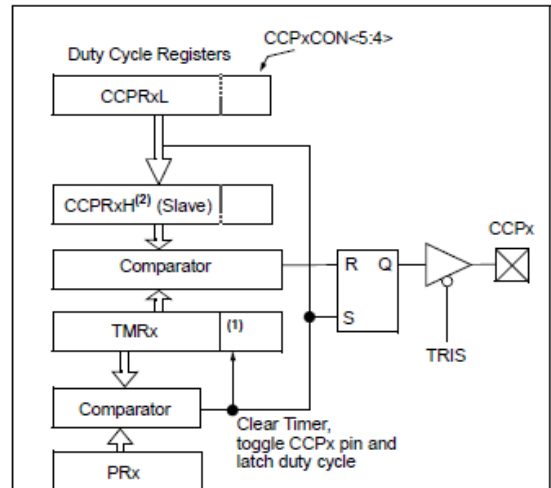
- bit 7-6 **Unused**
- bit 5-4 **DCxB<1:0>**: PWM Duty Cycle Least Significant bits  
Capture mode:  
Unused  
Compare mode:  
Unused  
PWM mode:  
These bits are the two LSBs of the PWM duty cycle. The eight MSBs are found in CCPRxL.
- bit 3-0 **CCPxM<3:0>**: ECCPx Mode Select bits
- 0000 = Capture/Compare/PWM off (resets the module)  
0001 = Reserved  
0010 = Compare mode: toggle output on match  
0011 = Reserved
- 0100 = Capture mode: every falling edge  
0101 = Capture mode: every rising edge  
0110 = Capture mode: every 4th rising edge  
0111 = Capture mode: every 16th rising edge
- 1000 = Compare mode: set output on compare match (CCPx pin is set, CCPxIF is set)  
1001 = Compare mode: clear output on compare match (CCPx pin is cleared, CCPxIF is set)  
1010 = Compare mode: generate software interrupt on compare match (CCPx pin is unaffected, CCPxIF is set)  
1011 = Compare mode: Special Event Trigger (CCPx pin is unaffected, CCPxIF is set)  
TimerX (selected by CxTSEL bits) is reset  
ADON is set, starting A/D conversion if A/D module is enabled<sup>(1)</sup>
- 11xx = PWM mode

**Note 1:** This feature is available on CCP5 only.

**FIGURE 14-1: CAPTURE MODE OPERATION BLOCK DIAGRAM**



**FIGURE 14-4: SIMPLIFIED PWM BLOCK DIAGRAM**



- Note 1:** The 8-bit timer TMRx register is concatenated with the 2-bit internal system clock (Fosc), or 2 bits of the prescaler, to create the 10-bit time base.
- 2:** In PWM mode, CCPRxH is a read-only register.

$$PWM\ Period = [(PRx) + 1] \cdot 4 \cdot T_{osc} \cdot (TMRx\ Prescale\ Value)$$

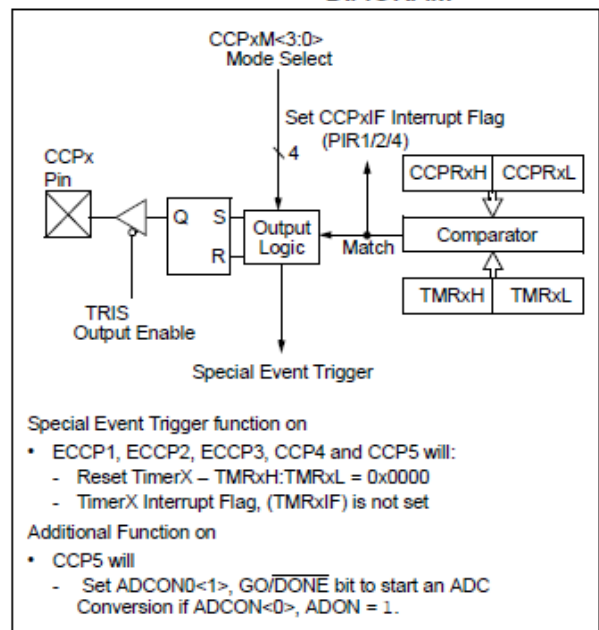
**Note 1:**  $T_{OSC} = 1/F_{OSC}$

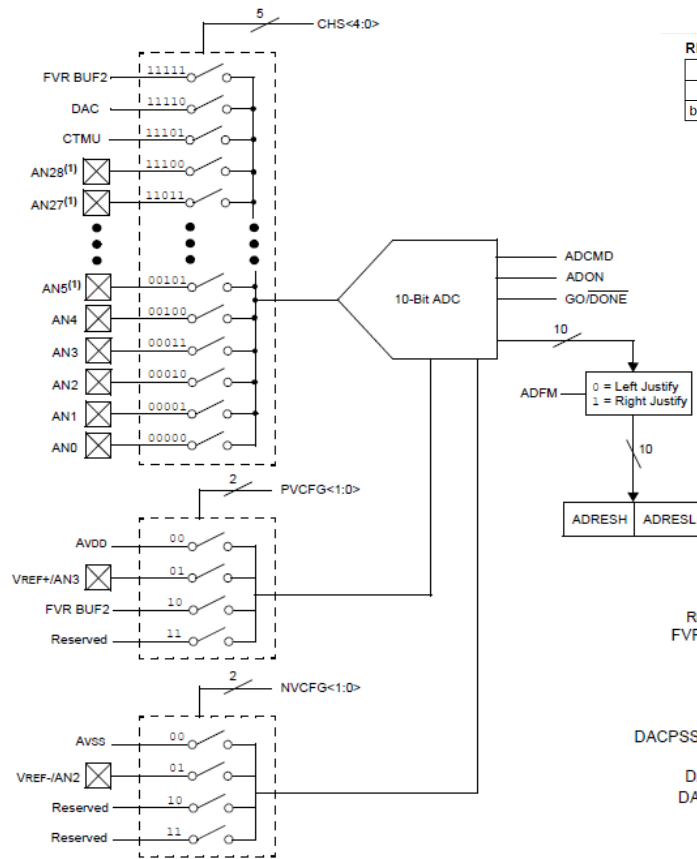
$$Resolution = \frac{\log[4(PRx + 1)]}{\log(2)} \text{ bits}$$

$$\text{Pulse Width} = (\text{CCPRxL}:\text{CCPxCON}\langle 5:4 \rangle) \cdot T_{\text{OSC}} \cdot (\text{TMRx Prescale Value})$$

$$\text{Duty Cycle Ratio} = \frac{(CCPRxL:CCPRxCON<5:4>)}{4(PRx + 1)}$$

**FIGURE 14-2: COMPARE MODE OPERATION BLOCK DIAGRAM**





REGISTER 17-2: ADON1: A/D CONTROL REGISTER 1

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
TRIGSEL	—	—	PVCFG<1:0>	NVCFG<1:0>	—

- bit 7 **TRIGSEL**: Special Trigger Select bit  
1 = Selects the special trigger from CTMU  
0 = Selects the special trigger from CCP5
- bit 6-4 **Unimplemented**: Read as '0'
- bit 3-2 **PVCFG<1:0>**: Positive Voltage Reference Configuration bits  
00 = A/D VREF+ connected to internal signal, AVDD  
01 = A/D VREF+ connected to external pin, VREF+  
10 = A/D VREF+ connected to internal signal, FVR BUF2  
11 = Reserved (by default, A/D VREF+ connected to internal signal, AVDD)
- bit 1-0 **NVCFG<1:0>**: Negative Voltage Reference Configuration bits  
00 = A/D VREF- connected to internal signal, AVSS  
01 = A/D VREF- connected to external pin, VREF-  
10 = Reserved (by default, A/D VREF- connected to internal signal, AVSS)  
11 = Reserved (by default, A/D VREF- connected to internal signal, AVSS)

REGISTER 17-1: ADON0: A/D CONTROL REGISTER 0

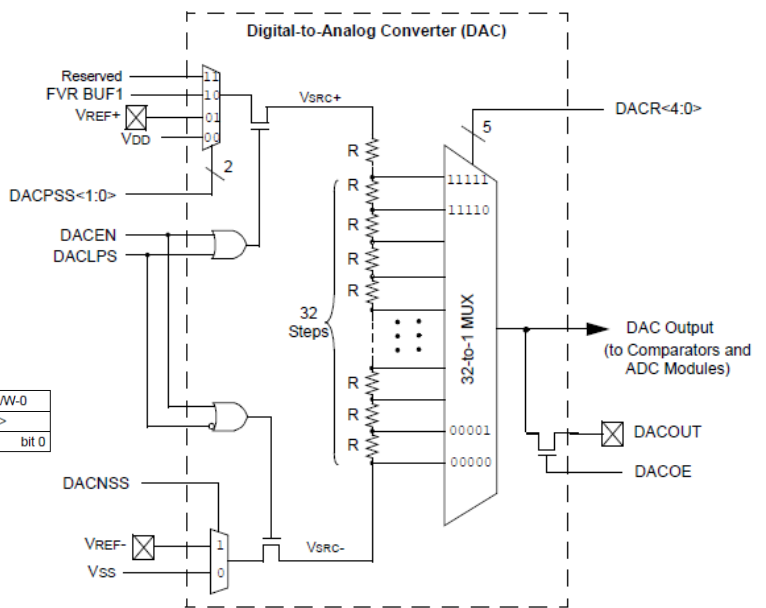
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	CHS<4:0>	GO/DONE	ADON

- bit 6-2 **CHS<4:0>**: Analog Channel Select bits  
00000 = AN0  
00001 = AN1  
00010 = AN2  
00011 = AN3  
00100 = AN4  
00101 = AN5<sup>(1)</sup>  
00110 = AN6<sup>(1)</sup>  
00111 = AN7<sup>(1)</sup>  
01000 = AN8  
01001 = AN9  
01010 = AN10  
01011 = AN11  
01100 = AN12  
01101 = AN13  
01110 = AN14  
01111 = AN15  
10000 = AN16  
10001 = AN17  
10010 = AN18  
10011 = AN19  
10100 = AN20<sup>(1)</sup>  
10101 = AN21<sup>(1)</sup>  
10110 = AN22<sup>(1)</sup>  
10111 = AN23<sup>(1)</sup>  
11000 = AN24<sup>(1)</sup>  
11001 = AN25<sup>(1)</sup>  
11010 = AN26<sup>(1)</sup>  
11011 = AN27<sup>(1)</sup>  
11100 = Reserved  
11101 = CTMU  
11110 = DAC  
11111 = FVR BUF2 (1.024V/2.048V/2.096V Volt Fixed Voltage Reference)<sup>(2)</sup>
- bit 1 **GO/DONE**: A/D Conversion Status bit  
1 = A/D conversion cycle in progress. Setting this bit starts an A/D conversion cycle.  
This bit is automatically cleared by hardware when the A/D conversion has completed.  
0 = A/D conversion completed/not in progress
- bit 0 **ADON**: ADC Enable bit  
1 = ADC is enabled  
0 = ADC is disabled and consumes no operating current

REGISTER 17-3: ADON2: A/D CONTROL REGISTER 2

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	—	ACQT<2:0>	—	ADCS<2:0>	—	—

- bit 7 **ADFM**: A/D Conversion Result Format Select bit  
1 = Right justified  
0 = Left justified
- bit 6 **Unimplemented**: Read as '0'
- bit 5-3 **ACQT<2:0>**: A/D Acquisition time select bits. Acquisition time is the duration that the A/D charge holding capacitor remains connected to A/D channel from the instant the GO/DONE bit is set until conversions begins.  
000 = 0<sup>(1)</sup>  
001 = 2 TAD  
010 = 4 TAD  
011 = 6 TAD  
100 = 8 TAD  
101 = 12 TAD  
110 = 16 TAD  
111 = 20 TAD
- bit 2-0 **ADCS<2:0>**: A/D Conversion Clock Select bits  
000 = Fosc/2  
001 = Fosc/8  
010 = Fosc/32  
011 = Frc<sup>(1)</sup> (clock derived from a dedicated internal oscillator = 600 kHz nominal)  
100 = Fosc/4  
101 = Fosc/16  
110 = Fosc/64  
111 = Frc<sup>(1)</sup> (clock derived from a dedicated internal oscillator = 600 kHz nominal)



REGISTER 22-1: VREFCON1: VOLTAGE REFERENCE CONTROL REGISTER 0

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0
DACEN	DACLPS	DACOE	—	DACPSS<1:0>	—	DACNSS	—

- bit 7 **DACEN**: DAC Enable bit  
1 = DAC is enabled  
0 = DAC is disabled
- bit 6 **DACLPS**: DAC Low-Power Voltage Source Select bit  
1 = DAC Positive reference source selected  
0 = DAC Negative reference source selected
- bit 5 **DACOE**: DAC Voltage Output Enable bit  
1 = DAC voltage level is also an output on the DACOUT pin  
0 = DAC voltage level is disconnected from the DACOUT pin
- bit 4 **Unimplemented**: Read as '0'
- bit 3-2 **DACPSS<1:0>**: DAC Positive Source Select bits  
00 = VDD  
01 = VREF+  
10 = FVR BUF1 output  
11 = Reserved, do not use
- bit 1 **Unimplemented**: Read as '0'
- bit 0 **DACNSS**: DAC Negative Source Select bits  
1 = VREF-  
0 = VSS

REGISTER 22-2: VREFCON2: VOLTAGE REFERENCE CONTROL REGISTER 1

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	—	—	—

- bit 7-5 **Unimplemented**: Read as '0'
- bit 4-0 **DACR<4:0>**: DAC Voltage Output Select bits  
 $V_{OUT} = ((V_{SRC+}) - (V_{SRC-})) * (DACR<4:0> / (2^5)) + V_{SRC-}$

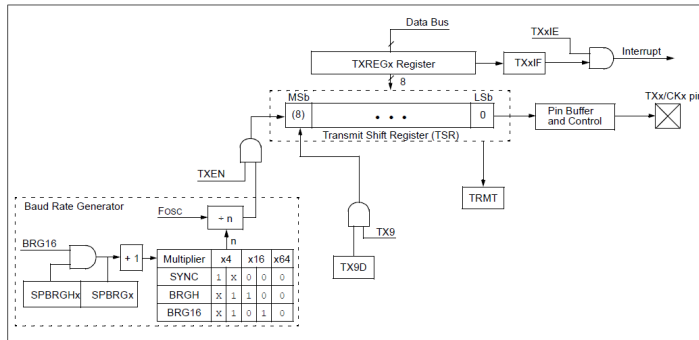
REGISTER 21-1: VREFCON0: FIXED VOLTAGE REFERENCE CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-1	U-0	U-0	U-0	U-0
FVREN	FVRST	FVRS<1:0>	—	—	—	—	—

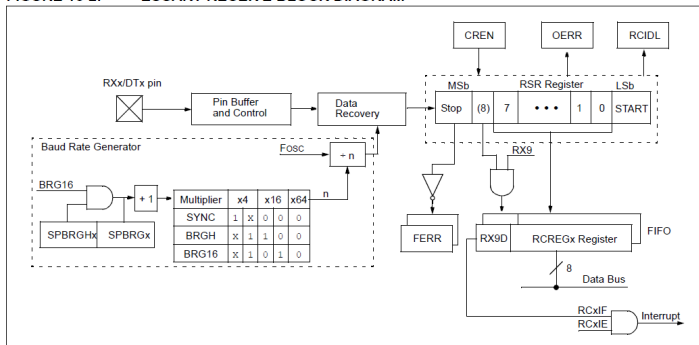
- bit 7 **FVREN**: Fixed Voltage Reference Enable bit  
0 = Fixed Voltage Reference is disabled  
1 = Fixed Voltage Reference is enabled
- bit 6 **FVRST**: Fixed Voltage Reference Ready Flag bit  
0 = Fixed Voltage Reference output is not ready or not enabled  
1 = Fixed Voltage Reference output is ready for use
- bit 5-4 **FVRS<1:0>**: Fixed Voltage Reference Selection bits  
00 = Fixed Voltage Reference Peripheral output is off  
01 = Fixed Voltage Reference Peripheral output is 1x (1.024V)  
10 = Fixed Voltage Reference Peripheral output is 2x (2.048V)<sup>(1)</sup>  
11 = Fixed Voltage Reference Peripheral output is 4x (4.096V)<sup>(1)</sup>
- bit 3-2 **Reserved**: Read as '0'. Maintain these bits clear.
- bit 1-0 **Unimplemented**: Read as '0'.

**Note 1**: Fixed Voltage Reference output cannot exceed VDD.

**FIGURE 16-1: EUSART TRANSMIT BLOCK DIAGRAM**



**FIGURE 16-2: EUSART RECEIVE BLOCK DIAGRAM**



**TABLE 16-3: BAUD RATE FORMULAS**

Configuration Bits			BRG/EUSART Mode	Baud Rate Formula
SYNC	BRG16	BRGH		
0	0	0	8-bit/Asynchronous	$F_{osc}/[64(n+1)]$
0	0	1	8-bit/Asynchronous	
0	1	0	16-bit/Asynchronous	$F_{osc}/[16(n+1)]$
0	1	1	16-bit/Asynchronous	
1	0	x	8-bit/Synchronous	$F_{osc}/[4(n+1)]$
1	1	x	16-bit/Synchronous	

Legend: x = Don't care, n = value of SPBRGHx, SPBRGx register pair.

**EXAMPLE 16-1: CALCULATING BAUD RATE ERROR**

For a device with  $F_{osc}$  of 16 MHz, desired baud rate of 9600, Asynchronous mode, 8-bit BRG:

$$Desired\ Baud\ Rate = \frac{F_{osc}}{64(SPBRGHx:SPBRGx + 1)}$$

Solving for SPBRGHx:SPBRGx:

$$X = \frac{F_{osc}}{64 \times Desired\ Baud\ Rate} - 1$$

$$= \frac{16000000}{64 \times 9600} - 1$$

$$= [25.042] = 25$$

Calculated Baud Rate =  $\frac{16000000}{64(25 + 1)}$

$$= 9615$$

Error =  $\frac{Calc.\ Baud\ Rate - Desired\ Baud\ Rate}{Desired\ Baud\ Rate}$

$$= \frac{(9615 - 9600)}{9600} = 0.16\%$$

**REGISTER 16-1: TxSTAx: TRANSMIT STATUS AND CONTROL REGISTER**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-1	R/W-0
CSRC	TX9	TXEN <sup>(1)</sup>	SYNC	SENDB	BRGH	TRMT	TX9D
bit 7							bit 0

- bit 7 **CSRC**: Clock Source Select bit  
**Asynchronous mode**:  
 Don't care  
**Synchronous mode**:  
 1 = Master mode (clock generated internally from BRG)  
 0 = Slave mode (clock from external source)
- bit 6 **TX9**: 9-bit Transmit Enable bit  
 1 = Selects 9-bit transmission  
 0 = Selects 8-bit transmission
- bit 5 **TXEN**: Transmit Enable bit<sup>(1)</sup>  
 1 = Transmit enabled  
 0 = Transmit disabled
- bit 4 **SYNC**: EUSART Mode Select bit  
 1 = Synchronous mode  
 0 = Asynchronous mode
- bit 3 **SENDB**: Send Break Character bit  
**Asynchronous mode**:  
 1 = Send Sync Break on next transmission (cleared by hardware upon completion)  
 0 = Sync Break transmission completed  
**Synchronous mode**:  
 Don't care
- bit 2 **BRGH**: High Baud Rate Select bit  
**Asynchronous mode**:  
 1 = High speed  
 0 = Low speed  
**Synchronous mode**:  
 Unused in this mode
- bit 1 **TRMT**: Transmit Shift Register Status bit  
 1 = TSR empty  
 0 = TSR full
- bit 0 **TX9D**: Ninth bit of Transmit Data  
 Can be address/data bit or a parity bit.

**REGISTER 16-2: RCSTAx: RECEIVE STATUS AND CONTROL REGISTER**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0
SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D
bit 7							bit 0

- bit 7 **SPEN**: Serial Port Enable bit  
 1 = Serial port enabled (configures RXx/DTx and TXx/CKx pins as serial port pins)  
 0 = Serial port disabled (held in Reset)
- bit 6 **RX9**: 9-bit Receive Enable bit  
 1 = Selects 9-bit reception  
 0 = Selects 8-bit reception
- bit 5 **SREN**: Single Receive Enable bit  
**Asynchronous mode**:  
 Don't care  
**Synchronous mode – Master**:  
 1 = Enables single receive  
 0 = Disables single receive  
 This bit is cleared after reception is complete.  
**Synchronous mode – Slave**:  
 Don't care
- bit 4 **CREN**: Continuous Receive Enable bit  
**Asynchronous mode**:  
 1 = Enables receiver  
 0 = Disables receiver  
**Synchronous mode**:  
 1 = Enables continuous receive until enable bit CREN is cleared (CREN overrides SREN)  
 0 = Disables continuous receive
- bit 3 **ADDEN**: Address Detect Enable bit  
**Asynchronous mode 8-bit (RX9 = 1)**:  
 1 = Enables address detection, enable interrupt and load the receive buffer when RSR<8> is set  
 0 = Disables address detection, all bytes are received and ninth bit can be used as parity bit  
**Asynchronous mode 8-bit (RX9 = 0)**:  
 Don't care
- bit 2 **FERR**: Framing Error bit  
 1 = Framing error (can be updated by reading RCREGx register and receive next valid byte)  
 0 = No framing error
- bit 1 **OERR**: Overrun Error bit  
 1 = Overrun error (can be cleared by clearing bit CREN)  
 0 = No overrun error
- bit 0 **RX9D**: Ninth bit of Received Data  
 This can be address/data bit or a parity bit and must be calculated by user firmware.

**REGISTER 16-3: BAUDCONx: BAUD RATE CONTROL REGISTER**

R/W-0	R-1	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
ABDOVF	RCIDL	DTRXP	CKTXP	BRG16	—	WUE	ABDEN
bit 7							bit 0

- bit 7 **ABDOVF**: Auto-Baud Detect Overflow bit  
**Asynchronous mode**:  
 1 = Auto-baud timer overflowed  
 0 = Auto-baud timer did not overflow  
**Synchronous mode**:  
 Don't care
- bit 6 **RCIDL**: Receive Idle Flag bit  
**Asynchronous mode**:  
 1 = Receiver is Idle  
 0 = Start bit has been detected and the receiver is active  
**Synchronous mode**:  
 Don't care
- bit 5 **DTRXP**: Data/Receive Polarity Select bit  
**Asynchronous mode**:  
 1 = Receive data (RXx) is inverted (active-low)  
 0 = Receive data (RXx) is not inverted (active-high)  
**Synchronous mode**:  
 1 = Data (DTx) is inverted (active-low)  
 0 = Data (DTx) is not inverted (active-high)
- bit 4 **CKTXP**: Clock/Transmit Polarity Select bit  
**Asynchronous mode**:  
 1 = Idle state for transmit (TXx) is low  
 0 = Idle state for transmit (TXx) is high  
**Synchronous mode**:  
 1 = Data changes on the falling edge of the clock and is sampled on the rising edge of the clock  
 0 = Data changes on the rising edge of the clock and is sampled on the falling edge of the clock
- bit 3 **BRG16**: 16-bit Baud Rate Generator bit  
 1 = 16-bit Baud Rate Generator is used (SPBRGHx:SPBRGx)  
 0 = 8-bit Baud Rate Generator is used (SPBRGx)
- bit 2 **Unimplemented**: Read as '0'
- bit 1 **WUE**: Wake-up Enable bit  
**Asynchronous mode**:  
 1 = Receiver is waiting for a falling edge. No character will be received but RCxIF will be set on the falling edge. WUE will automatically clear on the rising edge.  
 0 = Receiver is operating normally  
**Synchronous mode**:  
 Don't care
- bit 0 **ABDEN**: Auto-Baud Detect Enable bit  
**Asynchronous mode**:  
 1 = Auto-Baud Detect mode is enabled (clears when auto-baud is complete)  
 0 = Auto-Baud Detect mode is disabled  
**Synchronous mode**:  
 Don't care