High-Speed Single-Port Synchronous SRAM

sram
256X16, Mux 8, Drive 12

Process Technology:
SMIC Logic018

Features

- Precise Optimization for SMIC's Six-Layer Metal 0.18µm Logic018 CMOS Process
- High Density (area is 0.064mm^2)
- Fast Access Time (1.18ns at typical process, 1.80V, 25˚C)
- Fast Cycle Time (1.12ns at typical process, 1.80V, 25˚C)
- One Read/Write Port
- Completely Static Operation
- Near-Zero Hold Time (Data, Address, and Control Inputs)

Memory Description

The 256X16 SRAM is a high-performance, synchronous single-port, 256-word by 16-bit memory designed to take full advantage of SMIC's six-layer metal, 0.18µm Logic018 CMOS process.

The SRAM's storage array is composed of six-transistor cells with fully static memory circuitry. The SRAM operates at a voltage of 1.8V ± 10% and a junction temperature range of 0˚C to +125˚C.

Pin Description

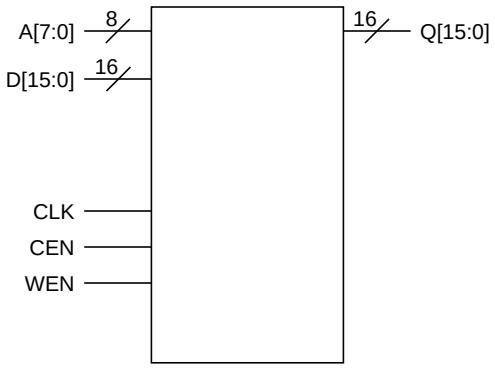
Pin	Description
A[7:0]	Addresses (A[0] = LSB)
D[15:0]	Data Inputs (D[0] = LSB)
CLK	Clock Input
CEN	Chip Enable
WEN	Write Enable
Q[15:0]	Data Outputs (Q[0] = LSB)

Area

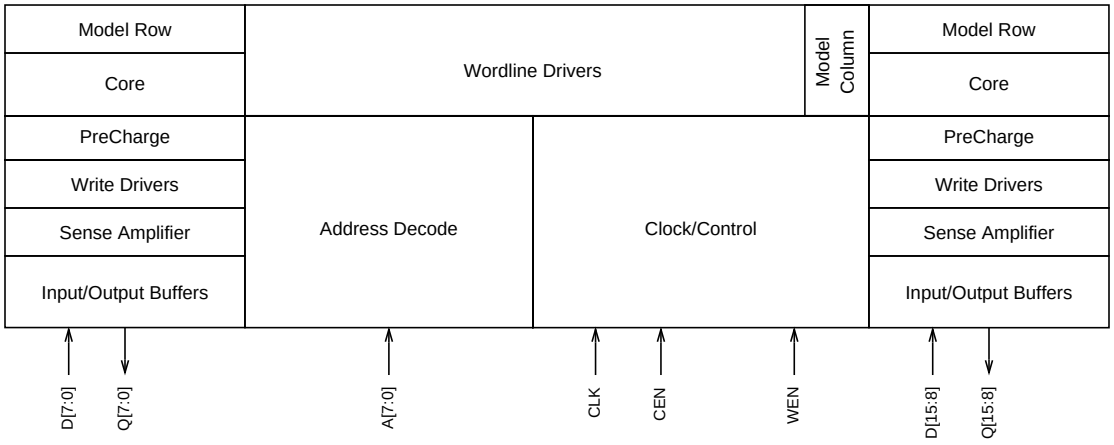
Area Type	Width (mm)	Height (mm)	Area (mm^2)
Core	0.326	0.195	0.064
Footprint	0.336	0.206	0.069

The footprint area includes the core area and user-defined power ring and pin spacing areas.

Symbol

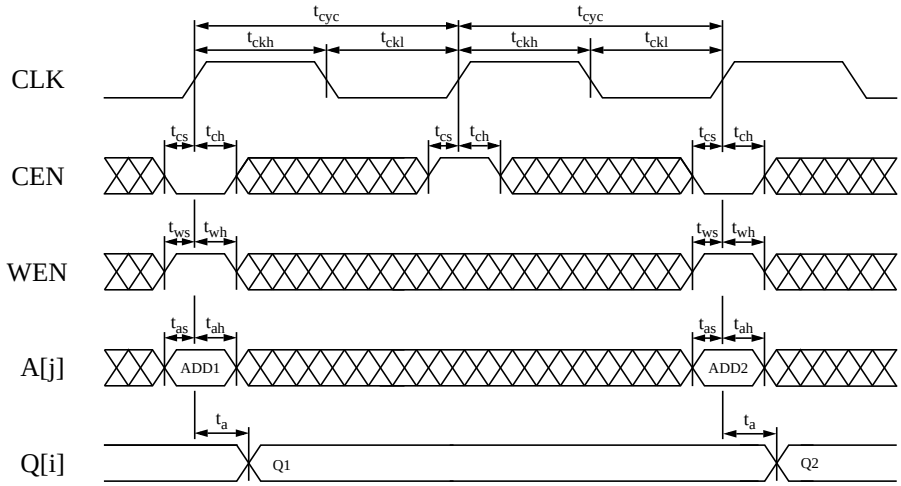


SRAM Block Diagram



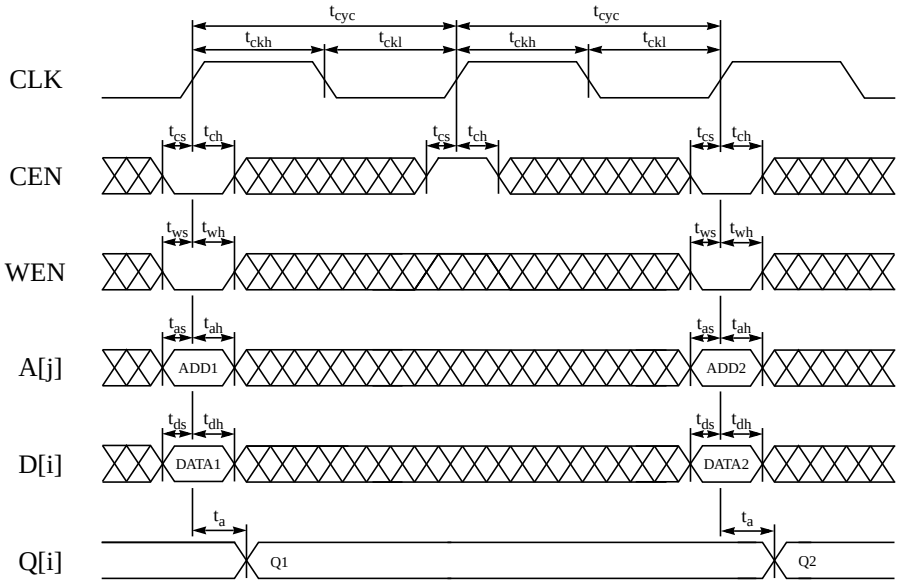
Mission Mode

Figure 1. Synchronous Single-Port SRAM Read-Cycle Timing



Rising delays are measured at 50% of VDD and falling delays are measured at 50% of VDD.
Rising and falling slews are measured from 10% VDD to 90% VDD.

Synchronous Single-Port SRAM Write-Cycle Timing



Rising signals are measured at 50% of VDD and falling signals are measured at 50% of VDD.
Rising and falling slews are measured from 10% VDD to 90% VDD.

SRAM Logic Table

CEN	WEN	Data Out	Mode	Function
H	X	Last Data	Standby	Address inputs are disabled; data stored in the memory is retained, but the memory cannot be accessed for new reads or writes. Data outputs remain stable.
L	L	Data In	Write	Data on the data input bus D[n-1:0] is written to the memory location specified on the address bus A[m-1:0], and driven through to the data output bus Q[n-1:0].
L	H	SRAM Data	Read	Data on the data output bus Q[n-1:0] is read from the memory location specified on the address bus A[m-1:0].

SRAM Timing: Mission Mode

Parameter	Symbol	Fast Process 1.98V, 0˚C		Typical Process 1.80V, 25˚C		Slow Process 1.62V, 125˚C	
		Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Cycle time	t_{cyc}	0.79		1.12		1.97	
Access time[1,2]	t_a	0.76			1.18		2.00
Address setup	t_{as}	0.21		0.31		0.59	
Address hold	t_{ah}	0.07		0.09		0.12	

Parameter	Symbol	Fast Process 1.98V, 0˚C		Typical Process 1.80V, 25˚C		Slow Process 1.62V, 125˚C	
		Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Chip enable setup	t_{cs}	0.26		0.35		0.57	
Chip enable hold	t_{ch}	0.00		0.00		0.00	
Write enable setup	t_{ws}	0.24		0.35		0.53	
Write enable hold	t_{wh}	0.00		0.00		0.00	
Data setup	t_{ds}	0.12		0.19		0.34	
Data hold	t_{dh}	0.00		0.00		0.00	
Clock high	t_{ckh}	0.09		0.12		0.21	
Clock low	t_{ckl}	0.11		0.16		0.28	
Clock rise slew	t_{ckr}		4.00		4.00		4.00
Output load factor (ns/pF)	K_{load}		0.26		0.35		0.53

[1] Parameters have a load dependence (K_{load}), which is used to calculate: $TotalDelay = FixedDelay + (Kload \times Cload)$.

[2] Access time is defined as the slowest possible output transition for the typical and slow corners, and the fastest possible output transition for the fast corner.

Pin Capacitance

Pin	Fast Process 1.98V, 0˚C	Typical Process 1.80V, 25˚C	Slow Process 1.62V, 125˚C
	Value (pF)	Value (pF)	Value (pF)
A[j]	0.055	0.055	0.054
D[i]	0.004	0.004	0.003
CLK	0.193	0.180	0.158
CEN	0.015	0.015	0.015
WEN	0.015	0.015	0.015

Power

1.00MHz Operation

Condition	Fast Process 1.98V, 0˚C	Typical Process 1.80V, 25˚C	Slow Process 1.62V, 125˚C
	Value (mA)	Value (mA)	Value (mA)
AC Current[1]	0.076	0.066	0.061
Read AC Current	0.070	0.060	0.057
Write AC Current	0.081	0.071	0.066
Peak Current	232.540	151.214	83.780
Deselected Current[2]	0.024	0.020	0.021
Standby Current[3]	0.003	0.002	0.005

[1] Value assumes 50% read and write operations, where all addresses and 50% of input and output pins switch.

[2] Value assumes SRAM is deselected, all addresses switch, and 50% of input pins switch. The logic-switching component of deselected power becomes negligibly small if the input pins are held stable by externally controlling these signals with chip select.

[3] Value is independent of frequency and assumes all inputs and outputs are stable.

Clock Noise Limit

Signal	Fast Process 1.98V, 0˚C		Typical Process 1.80V, 25˚C		Slow Process 1.62V, 125˚C	
	Pulse Width (ns)	Voltage (V)	Pulse Width (ns)	Voltage (V)	Pulse Width (ns)	Voltage (V)
CLK	10.000	0.827	10.000	0.829	10.000	0.791

The clock noise limit is the maximum CLK voltage allowable for the indicated pulse width without causing a spurious memory cycle or other memory failure.

Power and Ground Noise Limit

Signal	Fast Process 1.98V, 0˚C	Typical Process 1.80V, 25˚C	Slow Process 1.62V, 125˚C
	Voltage (V)	Voltage (V)	Voltage (V)
Power	0.198	0.180	0.162
Ground	0.198	0.180	0.162

The power/ground noise limit is the maximum supply voltage transition allowable without causing a memory failure.