

潘佳诚

<http://jiacheng.space/about>

上海市杨浦区许昌路 1491 弄 2 号楼 504 室

Tel: 158 0095 2731 ◇ jiacheng.pan.sh@gmail.com

个人情况

潘佳诚是一个极富激情、充满好奇心的人，热衷于用编程解决问题。

他在 Synopsys 作为 R&D 工程师工作了三年，侧重于时钟树综合相关领域的测试以及测试工具的开发。此前他完成了在复旦大学的学业，获得了微电子学学士学位。

他不仅能够按时保质保量地完成工作，同时他还经常乐于开发新的工具、实现新的想法，用以简化工作流程、提高工作效率，并时常与同事们分享他的成果。

他当前的兴趣点包括并行/高性能计算及系统编程，并正在积极地寻找相关的工作机会。

教育经历

2009 年 9 月
至 2013 年 6 月

复旦大学
微电子学专业学士
经济学第二专业

工作经历

2013 年 2 月
至 2016 年 4 月

Synopsys, Inc. R&D Engineer II

- EDA 工具的自动测试开发 (Python) 以及黑盒测试 (Tcl)，主要关注领域包括时钟树综合及 *concurrent clock-data optimization*;
- 开发了测试用例搜索及分析工具，被上海及美国的同事广泛使用;
- 开发了自动测试用例产生工具，被上海的同事广泛使用;
- 编写了超过 800 份测试用例，维护超过 1000 份回归测试用例以及 2 个 QoR benchmarking suite;
- 发起并指导了暑期实习生项目，侧重于对测试用例及测试数据的数据挖掘。

2012 年 6 月
至 2012 年 9 月

复旦微电子有限公司 实习生

- 对在 NAND flash 上实现 ECC (错误纠正码) 的方法进行了调研。

2011 年 5 月
至 2013 年 6 月

复旦大学专用集成电路国家重点实验室 本科生

- 参与了 FPGA 相关的科研及软件开发;
- 开发扩展了一个轻量级操作系统，用于提供对 FPGA 上可重构硬件资源的抽象及管理，用于高性能计算的应用场景。(本科毕设，得分 A);
- 开发了一个错误注入模拟器，应用于实验室开发的 FPGA 上，使用了 MATLAB Simulink;
- 开发了一个内部信号观测工具，以及位流下载工具，应用于实验室开发的 FPGA 上。

个人项目

2016 年 4 月

CUDA-Accelerated Minimum Spanning Tree

- 基于 2 篇论文实现了 data-parallel Boruvka 算法以及 data-parallel Kruskal 算法;
- 重现了论文的实验，算法效率相比于 CMU benchmark suite 提升了 3 倍。

2016 年 4 月

CUDA-Accelerated Cloth Simulator (On-going)

- 实现了一个简单的基于质量弹性系统模型的 cloth simulator，并用 CUDA 进行了加速，实现了 lock-free 的数据结构。

2015 年 9 月
至 2015 年 10 月

Data Mining Capstone

- 分析了 Yelp 的评论数据，完成了用于餐饮推荐系统的基础功能任务;
- 完成了 6 项任务及 1 份结项报告，包含主题挖掘、菜系聚类及相似度分析、菜名识别、餐厅推荐、卫生状况预测。

2016 年 1 月
至 2016 年 2 月

Cloud Computing Capstone

- 分别使用 Hadoop 和 Spark 在 AWS EC2 集群上对美国航班数据进行了分析;
- 对机场及航空公司按准点率进行了排序，并对特定的时间条件下对飞经特定机场的飞行路线进行了查询。

2014 年 11 月

Social Network Analysis on Github Repositories

- 作为 Coursera 课程 **Social Network Analysis** 的课程项目，同行评审得分 98%;
- 对用户-项目库二分图进行了建模，分析了项目库使用的编程语言与项目库形成的社区的关系，以及随着时间的变化。

技术特长

语言技能
证书与荣誉

Tcl, Python, C++/C, CUDA, Java, scala

- TOFEL 105;
- Coursera 颁发的 Data Mining Specialization 证书以及 14 份 Certificates of Accomplishment;
- Synopsys STAR Award 2015, 颁与发现 bug 最多者之一;
- Synopsys Best Mentor 2016, 颁与优秀的暑期实习生项目的 mentor;
- Synopsys Special Award for XTAGE 2016, 颁与参与建设一个公司内部信息交流平台的人员;

活动组织

- 前 Synopsys Shanghai Python Special Interest Group 成员，积极参与了技术分享;
- 前 Synopsys Shanghai Engineer Forum 成员，协调联系资深工程师在上海 site 进行技术分享。

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Rm 504 Building 2, No.1491 Xuchang Rd. Yangpu, Shanghai

Tel: 158 0095 2731 ◇ jiacheng.pan.sh@gmail.com

SUMMARY

Jiacheng Pan is an enthusiastic person with strong interest in solving problems by programming and new technologies.

He was an R&D Engineer in Synopsys for three years, focusing on *clock tree synthesis* testing and test tools developments. Before that, he received his Bachelor degree from Fudan University.

He is capable of delivering projects with quality on time, and meanwhile, he also loves to develop and prototype new tools and ideas to improve working efficiency, and share them with coworkers.

He has strong interest in parallel and system programming, and is actively looking for relevant opportunities.

EDUCATION

SEPTEMBER 2009 - JUNE 2013	Fudan University, Shanghai Bachelor of Science in <i>Microelectronics</i> Minor in <i>Economics</i>
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EXPERIENCE

FEBRUARY 2013 - APRIL 2016	Synopsys, Inc. R&D Engineer II <ul style="list-style-type: none">· Test automation development (Python) and black-box testing (Tcl), focusing on <i>clock tree synthesis</i> and <i>concurrent clock-data optimization</i>;· Developed <i>tools for test case searching and analysis</i>, widely used by local and remote developers;· Developed <i>automatic test creation tools</i>, widely used by local testing teams;· Developed over 800, maintained over 1k regression cases and 2 QoR benchmarking suites;· Initiated a summer intern programme, on <i>data mining over test cases and data</i>.
JUNE 2012 - SEPTEMBER 2012	Fudan Microelectronics, Inc. Intern <ul style="list-style-type: none">· Investigated approaches of error correction code (ECC) implementations on NAND flash.
MAY 2011 - JUNE 2013	ASIC State Key Laboratory, Fudan University Undergraduate Student <ul style="list-style-type: none">· Participated FPGA-related researches and developments;· Developed <i>an extension of a light-weight OS running on FPGA</i>, providing abstraction and management of hardware reconfigurable computing resources for HPC applications. (undergraduate thesis, graded A);· Developed <i>a fault injection simulator</i> for lab-proprietary FPGA, using MATLAB Simulink;· Developed <i>an internal signal probing debugger and a bitstream downloader</i> for lab-proprietary FPGA.

PERSONAL PROJECTS

APRIL 2016	CUDA-Accelerated Minimum Spanning Tree <ul style="list-style-type: none">· Implemented data-parallel Boruvka's and data-parallel Kruskal's algorithm based on 2 papers;· Reproduced the performance of the papers and beat the benchmark suite by more than 3x.
APRIL 2016	CUDA-Accelerated Cloth Simulator (On-going) <ul style="list-style-type: none">· Implemented a simple cloth simulator based on spring-mass model and accelerated using CUDA.
SEPTEMBER 2015 - OCTOBER 2015	Data Mining Capstone <ul style="list-style-type: none">· Analysed Yelp reviews, finished fundamental tasks needed for a restaurant recommending system;· Finished 6 tasks and one final report, covering <i>topic mining</i>, <i>cuisine clustering and similarity analysis</i>, <i>dish recognition</i>, <i>restaurant recommendation</i>, <i>hygiene prediction</i>.
JANUARY 2016 - FEBRUARY 2016	Cloud Computing Capstone <ul style="list-style-type: none">· Used Hadoop and Spark to analyse US flight data, on AWS EC2 clusters;· Ranked airports and carriers by on-time-arrival performance, and searching for appropriate two-flight routes with specific temporal constraints.
NOVEMBER 2014	Social Network Analysis on Github Repositories <ul style="list-style-type: none">· Final project of Coursera course Social Network Analysis, graded 98% by peer;· Analysed the user-repository bipartite graph, its relationship with the community of language used by repositories, and its evolution over time.

TECHNICAL STRENGTHS

SKILLS	Tcl, Python, C++/C, CUDA, Java, scala
CERTIFICATES & AWARDS	<ul style="list-style-type: none">· TOFEL 105;· Data Mining Specialization and 14 Certificates of Accomplishment from Coursera;· Synopsys STAR Award 2015, for top bug finders;· Synopsys Best Mentor 2016, for excellent mentors of summer intern programmes;· Synopsys Special Award for XTAGE 2016, for setting up an internal idea-sharing platform;
AFFILIATIONS	<ul style="list-style-type: none">· Former Synopsys Shanghai Python Special Interest Group member, active lecturer;· Former Synopsys Shanghai Engineer Forum member, coordinating technical sharing in Shanghai site.