JIACHENG PAN

http://jiacheng.space/about
Building 49., No.1387 Zhangdong Rd., Pudong District , Shanghai
Tel: +86 158 0095 2731 ◇ jiacheng.pan.sh@gmail.com

Summary

Jiacheng Pan is an enthusiastic person with strong interest in solving problems using automation, programming, and new technologies.

He is an ASIC Design Engineer in AMD focusing on in-house EDA tool development. Before that, he worked at Synopsys for three years focusing on software testing and test development. He received his Bachelor of Science degree in Fudan University in 2013.

He is capable of delivering projects with quality on time, and meanwhile, he also loves to develop and prototype new tools and ideas to improve working efficiency, and share them with coworkers.

He has strong interest in EDA, ASIC design, and high-performance computing.

Education

September 2009 - June 2013 | **Fudan University, Shanghai**
Bachelor of Science in *Microelectronics*
Minor in *Economics*

Experience

June 2016 - Current | **Advanced Micro Devices, Inc.** *ASIC Design Engineer II*
· Software development (C, C++, Tcl, Ruby, Perl) and supporting for in-house EDA tools for:
· Defining inter- or intra- module connectivity and interface protocols;
· Design stitching, simulation, and verification code generation;
· Design Grouping and ungrouping for better physical design implementation;
· Low-power design generation using multi-voltage, power-gating, and clock-gating techniques.

February 2013 - April 2016 | **Synopsys, Inc.** *R&D Engineer II*
· Test automation development (Python) and black-box testing (Tcl), focusing on *clock tree synthesis* and *concurrent clock-data optimization* in *IC Compiler II*;
· Developed *tools for test case searching and analysis*, widely used by local and remote developers;
· Developed *automatic test creation tools*, widely used by local testing teams;
· Developed *UPF generation tool for testing*, used by local testing teams;
· Developed over 800, maintained over 1k regression cases and 2 QoR benchmarking suites;
· Initiated a summer intern programme, on *data mining over test cases and data*.

June 2012 - September 2012 | **Fudan Microelectronics, Inc.** *Intern*
· Investigated approaches of error correction code (ECC) implementations on NAND flash.

May 2011 - June 2013 | **ASIC State Key Laboratory, Fudan University** *Undergraduate Student*
· Participated FPGA-related researches and developments;
· Developed *an extension of a light-weight OS running on FPGA*, providing abstraction and management of hardware reconfigurable computing resources for HPC applications. (undergraduate thesis, graded A);
· Developed *a fault injection simulator* for lab-proprietary FPGA, using MATLAB Simulink;
· Developed *an internal signal probing debugger and a bitstream downloader* for lab-proprietary FPGA.

Personal Projects

April 2016 — CUDA-Accelerated Minimum Spanning Tree

· Implemented data-parallel Boruvka's and data-parallel Kruskal's algorithm;
· Reproduced the performance of the referencing papers and achieved 3x speedup than benchmark suite.

April 2016 — CUDA-Accelerated Cloth Simulator

· Implemented a cloth simulator based on spring-mass model and accelerated using CUDA.

January 2016 - February 2016 — Cloud Computing Capstone

· Used Hadoop and Spark to analyse US flight data, on AWS EC2 clusters;
· Ranked airports and carriers by on-time-arrival performance, and searching for appropriate two-flight routes with specific temporal constraints.

January 2016 — JOS

· MIT 6.828 JOS project, implementing a light-weight OS from scratch;
· Implemented memory management, user environment (processes), simple scheduling and multi-CPU support.

September 2015 - October 2015 — Data Mining Capstone

· Analysed Yelp reviews, finished fundamental functionalities needed by a restaurant recommending system;
· Finished six tasks and one final report, covering topic mining, cuisine clustering and similarity analysis, dish recognition, restaurant recommendation, hygiene prediction.

November 2014 — Social Network Analysis on Github Repositories

· Final project of Coursera course Social Network Analysis, graded 98% by peers;
· Analysed the user-repository bipartite graph, its relationship with the community of language used by repositories, and its evolution over time.

Technical Strengths

Skills

Tcl, Python, C++/C, CUDA, Java, scala
ASIC physical design, timing analysis, CUDA programming, FPGA design, data mining

Certificates & Awards

· TOFEL 105;
· Data Mining Specialization and 14 Certificates of Accomplishment from Coursera;
· **Synopsys** Best Mentor 2016, for excellent mentors of summer intern programmes;
· **Synopsys** Special Award for XTAGE 2016, for setting up an internal idea-sharing platform;
· **Synopsys** STAR Award 2015, for top bug finders;
· **Fudan University** 2012, Scholarship for Excellent Students of Fudan University, Third Prize;
· **Fudan University** 2011, 2010, People's Scholarship of Fudan University, Third Prize;
· **Fudan University** 2011, Outstanding Student of Fudan University;
· **Fudan University** 2010, National Scholarship for Encouragement.

Affiliations

· Former **Synopsys** Shanghai Python Special Interest Group member, active lecturer;
· Former **Synopsys** Shanghai Engineer Forum member, coordinating technical sharing in Shanghai site.