Efficient Implementations of SPHINCS⁺ on GPUs

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Abstract—The rapid increase in data transfer rates from gigabits per second to terabits per second necessitates efficient computational approaches for high-speed data processing. Traditional software and extended instruction set architectures prove inadequate under these conditions. A GPU-based software implementation of the AES is presented, employing bitslicing to compute substitutions on the fly and thereby reducing cache misses compared with look-up table methods. Additional gains are realized through a permutation optimization that mitigates thread stall time. Experimental results indicate that this implementation achieves throughput in xx.xx terabit-per-second when executed on a single NVIDIA RTX 4090 GPU.

Index Terms—Software implementation, Block cipher, GPU, Bitslicing, SAT.

I. INTRODUCTION

THE Advanced Encryption Standard (AES) is a widely adopted symmetric block cipher that provides essential security in diverse communication protocols [1]. Commonly used libraries such as OpenSSL and Libgcrypt employ T-table-based methods for both encryption and decryption, delivering adequate performance for megabit-per-second workloads [2], [3].

Performance shortcomings arise when data rates exceed gigabit-per-second thresholds [4]. Such high-throughput scenarios, including data centers and 5G networks, require more efficient and scalable solutions to preserve both speed and cryptographic strength.

A. Related Work

The parallel structure of GPUs supports the simultaneous execution of multiple threads, which significantly increases performance in comparison with standard CPU-based operations. Table I summarizes representative AES CTR mode implementations on GPUs. In [5], the overhead of the ShiftRows stage is minimized by rearranging input data, and a hardware-based S-box replaces look-up table resources in the Substitute Bytes stage. In [6], the necessity to embed round keys at compile time is eliminated, allowing more flexible code generation. This approach achieves 9% higher encryption throughput than bit-sliced references for CTR modes.

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TABLE I RELATED WORK ON AES CTR MODE IMPLEMENTATIONS ON GPUS

Ref	Throughput (Gbps)	Platform	Year
[5]	1478	Tesla V100	2019
[6]	1489	RTX 3080	2022
Ours	_	RTX 4090	_

- B. Motivation
- C. Contributions

REFERENCES

- J. Daemen and V. Rijmen, The Design of Rijndael The Advanced Encryption Standard (AES), Second Edition, ser. Information Security and Cryptography. Springer, 2020.
- [2] J. Jancar, M. Fourné, D. D. A. Braga, M. Sabt, P. Schwabe, G. Barthe, P. Fouque, and Y. Acar, "They're not that hard to mitigate: What cryptographic library developers think about timing attacks," in Software Engineering 2024, Fachtagung des GI-Fachbereichs Softwaretechnik, Linz, Austria, February 26 March 1, 2024, ser. LNI, R. Rabiser, M. Wimmer, I. Groher, A. Wortmann, and B. Wiesmayr, Eds., vol. P-343. Gesellschaft für Informatik e.V., 2024, pp. 143–144.
- [3] B. Marshall, G. R. Newell, D. Page, M. O. Saarinen, and C. Wolf, "The design of scalar AES instruction set extensions for RISC-V," *IACR Trans. Cryptogr. Hardw. Embed. Syst.*, vol. 2021, no. 1, pp. 109–136, 2021.
- [4] L. Li, J. Fang, J. Jiang, L. Gan, W. Zheng, H. Fu, and G. Yang, "Efficient AES implementation on sunway taihulight supercomputer: A systematic approach," J. Parallel Distributed Comput., vol. 138, pp. 178–189, 2020.
- [5] O. Hajihassani, S. K. Monfared, S. H. Khasteh, and S. Gorgin, "Fast AES implementation: A high-throughput bitsliced approach," *IEEE Trans. Parallel Distributed Syst.*, vol. 30, no. 10, pp. 2211–2222, 2019.
- [6] W.-K. Lee, H. J. Seo, S. C. Seo, and S. O. Hwang, "Efficient implementation of aes-ctr and aes-ecb on gpus with applications for high-speed frodokem and exhaustive key search," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 69, pp. 2962–2966, 2022.



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