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Dear Editor,

The manuscript titled "*Thread-Adaptive: Optimized Parallel Architectures of SLH-DSA on GPUs*" is submitted for consideration to *IEEE Transactions on Circuits and Systems Part II: Express Briefs*. All co-authors have reviewed and approved this submission, and the manuscript is not under consideration by any other publication.

The manuscript presents novel optimization techniques for implementing block ciphers on IoT microprocessors, with specific focus on bitsliced SPN-Cipher implementations. Three primary contributions are presented: (1) an innovative permutation layer optimization method for SPN-Ciphers, (2) a novel encoding model for SPN-Cipher S-boxes, and (3) a lightweight benchmarking framework for comprehensive performance evaluation. The proposed techniques achieved a 9.7% latency reduction in AES implementation, demonstrating significant performance improvements over existing approaches.

The manuscript has been prepared in accordance with *IEEE Transactions on Circuits and Systems Part II: Express Briefs* guidelines. All content has been thoroughly reviewed for technical accuracy and linguistic clarity. All necessary ethical approvals have been obtained, and all data and materials will be made available upon request.

The selection of *IEEE Transactions on Circuits and Systems Part II: Express Briefs* as the target venue was motivated by its established reputation in computer architecture and system optimization research. The manuscript's focus on microprocessor optimization and cryptographic implementation aligns with the journal's scope and readership.

Your time and consideration are greatly appreciated. Please do not hesitate to request any additional information or clarification.

Sincerely yours,

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