

Thread-Adaptive: Optimized Parallel Architectures of SLH-DSA on GPUs

Jiahao Xiang and Lang Li.

Abstract—The Post-Quantum Cryptography (PQC) standardization process has led to the development of the stateless hash-based digital signature algorithm (SLH-DSA) FIPS 205. The high computational cost of SLH-DSA necessitates efficient implementations for practical deployment. This work presents a GPU-based implementation of SLH-DSA that achieves high throughput through a thread-adaptive parallelization strategy. Unlike conventional approaches that allocate maximum thread counts, the implementation dynamically determines optimal parallelism levels for each cryptographic kernel function, balancing thread utilization with execution efficiency. Additionally, fine-grained decomposition of signature components enables more efficient thread-level execution. Performance evaluation on an NVIDIA RTX 4090 GPU demonstrates the implementation achieves a throughput of XXX signatures per second, significantly outperforming existing approaches. The results establish GPUs as effective platforms for accelerating SLH-DSA operations in high-throughput environments, facilitating practical transition to post-quantum standards.

Index Terms—FIPS 205, GPU, SPHINCS⁺, Signature algorithm.

I. INTRODUCTION

THE emergence of quantum computing presents a double-edged technological advancement. While offering unprecedented computational capabilities for complex problems in drug discovery, medical research, and materials science, quantum computers simultaneously pose a significant threat to current cryptographic systems. This threat culminates in “Q-Day,” when quantum computers become capable of compromising public encryption systems that safeguard digital interactions, including authentication mechanisms and key exchange protocols. The vulnerability of widely deployed public-key cryptosystems such as RSA and ECC to Shor’s algorithm [1] has necessitated research into quantum-resistant alternatives. In response, the National Institute of Standards and Technology (NIST) initiated the Post-Quantum Cryptography (PQC) standardization process to develop cryptographic schemes that withstand quantum computing capabilities [2].

This work is supported by the Hunan Provincial Natural Science Foundation of China (2022JJ30103), Postgraduate Scientific Research Innovation Project of Hunan Province (CX20240977), “the 14th Five-Year Plan” Key Disciplines and Application-oriented Special Disciplines of Hunan Province (Xiangjiaotong [2022] 351), the Science and Technology Innovation Program of Hunan Province (2016TP1020).

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SPHINCS⁺ is a representative stateless hash-based signature scheme and a finalist in the NIST standardization effort [3]. It provides long-term security against quantum attacks by employing robust cryptographic hash functions [4]. The scheme has since formed the basis for the Stateless Hash-based Digital Signature Algorithm (SLH-DSA), which was standardized as FIPS 205 [5]. The high computational cost of these hash-based signatures has motivated research into efficient implementations across CPUs, FPGAs, and GPUs [6] to facilitate adoption by organizations transitioning to post-quantum cryptography.

A. Related Work

GPU-based implementations of SPHINCS⁺ have progressed significantly in recent years. Lee and Hwang [7] established foundational techniques for parallel implementation of hash-based signatures, demonstrating initial feasibility of GPU acceleration for post-quantum cryptographic schemes. Kim et al. [8] advanced this work by introducing parallel methods for key SPHINCS⁺ components—FORS, WOTS⁺, and Merkle tree computations. Their RTX 3090 implementation achieved substantial throughput improvements despite efficiency limitations from frequent kernel launches.

More recent advancements include CUSPX by Wang et al. [9], which introduced a comprehensive three-level parallelism framework integrating algorithmic, data, and hybrid parallelization strategies. Their implementation featured parallel Merkle tree construction algorithms and load-balancing approaches that demonstrated substantial performance gains.

B. Motivation

Analysis of existing GPU implementations of SPHINCS⁺ reveals two critical efficiency constraints. First, conventional implementations apply uniform maximum thread allocation across all cryptographic operations, disregarding the distinct computational characteristics of individual functions. This static approach creates resource imbalance—some operations experience excessive synchronization overhead while others underutilize available resources.

Second, the hierarchical structure of SPHINCS⁺, with its multiple hash operations across FORS, WOTS⁺, and Merkle tree components, enables decomposition into smaller computational units. However, existing implementations prioritize thread count over computational efficiency, resulting in sub-optimal per-thread performance despite extensive hardware utilization.

These observations necessitate an adaptive parallelization approach that dynamically determines optimal thread configurations for each cryptographic function while enabling fine-grained decomposition of signature components. The implementation presented addresses these limitations through a thread-adaptive strategy that balances parallelism levels with computational efficiency, alongside function-level optimizations that enhance per-thread execution performance.

C. Contributions

In this brief, an optimized GPU-based implementation of SPHINCS⁺ is presented, achieving high throughput and low latency. The main contributions are summarized as follows:

- 1) A hash-function-level parallelization approach is introduced that reduces latency through fine-grained task distribution, significantly accelerating the core computational primitives of SPHINCS⁺.
- 2) An adaptive thread allocation strategy is developed that optimizes the balance between thread count and kernel function efficiency, minimizing synchronization overhead while maximizing computational throughput on GPU architectures.
- 3) The implementation is evaluated on an NVIDIA GPU, demonstrating a throughput of XXX SPHINCS⁺ signatures per second, significantly exceeding the performance of state-of-the-art approaches. The complete source code and implementation details are available at <https://github.com/jiahaoxiang2000/sphincs-plus>.

The remainder of the brief is organized as follows. Section II provides an overview of the SPHINCS⁺ signature scheme; Section III details the GPU-based implementation; Section IV presents the performance evaluation; and Section V concludes the brief.

II. PRELIMINARIES

A. SPHINCS⁺ Overview

SPHINCS⁺ is a stateless hash-based signature scheme that delivers post-quantum security through a hierarchical certification structure. The signature generation process relies on three main components:

- **WOTS+ (Winternitz One-Time Signature):** A one-time scheme that handles authentication paths and underpins the Merkle tree construction
- **FORS (Forest Of Random Subsets):** A few-time signature scheme that uses k components, each containing t elements selected from pseudorandom subsets
- **Hypertree:** A multi-layer structure of height h divided into d layers, each containing Merkle trees of height h/d for authenticating WOTS+ public keys

The SPHINCS⁺ signature generation process, shown in Figure 1, employs a hierarchical authentication structure. A message digest is first created via hashing, followed by signing with the FORS few-time scheme, producing k authentication paths of t elements each. The resulting FORS public key is authenticated through a hypertree of d layers, where each layer uses WOTS+ to sign the root of the layer below. This chain

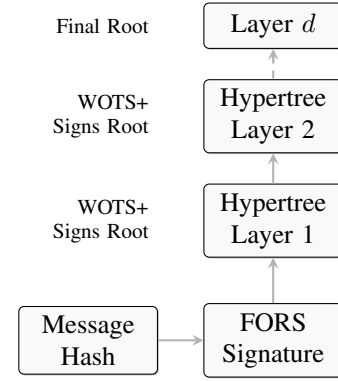


Fig. 1. SPHINCS⁺ signature generation flow. A message hash is signed by FORS to produce k authentication paths, which are then authenticated by a d -layer hypertree. Each layer employs WOTS+ to sign the root of the previous layer, culminating in a final root signature.

of signatures leads to the final root node, offering efficient verification with robust hash-based security.

Two operational modes, “simple” and “robust,” are provided to balance speed and security. Parameter sets facilitate trade-offs among signature size, security level, and computational efficiency. All security properties derive from the hash functions, rendering SPHINCS⁺ resistant to quantum attacks.

B. GPU Computing Model

Modern Graphics Processing Units (GPUs) incorporate a large number of cores organized within multiple Streaming Multiprocessors (SMs). This highly parallel structure supports Single Instruction, Multiple Thread (SIMT) execution, wherein threads are grouped into warps, and warps collectively form blocks. Each block is then scheduled across available SMs, ensuring that thousands of concurrent threads can execute similar instructions in parallel.

In the CUDA framework, memory optimization strategies such as coalesced accesses, shared memory buffering, and constant memory utilization further enhance throughput. Extensive parallelization of SPHINCS⁺ computations is therefore facilitated, allowing performance improvements through a combination of thread-level, data-level, and algorithmic parallelism.

III. OPTIMIZED IMPLEMENTATION OF SPHINCS⁺

A. Hash-Function-Level Parallelization

The implementation introduces fine-grained parallelization at the hash function level, departing from conventional approaches that treat hash functions as atomic operations. This technique reduces cryptographic operation latency by decomposing hash operations into parallel tasks distributed across multiple threads.

1) *Internal State Parallelism:* The approach decomposes hash function operations into concurrent tasks that can be executed in parallel by multiple threads within a single warp. For SHA256, the internal state transformations are parallelized as follows:

- **State Initialization:** Multiple threads concurrently initialize different portions of the hash function’s state array. Thread 0 handles initial state setup, while threads 0-15 cooperatively load message words in parallel, reducing initialization overhead.
- **Round Functions:** Each round of the SHA256 permutation is decomposed into lane operations executed concurrently by different threads. Threads 0-15 process message schedule expansion, while threads 0-7 manage state variable updates during round computation.
- **Data Sharing:** Warp-level primitives `__shfl_sync()` enable efficient data sharing without requiring expensive shared memory operations. These synchronized operations allow threads within a warp to exchange data with minimal divergence, enhancing computational efficiency.

2) *Task Distribution* : A hierarchical task allocation scheme is implemented to efficiently distribute hash function operations across GPU threads:

Algorithm 1 Hash-Function-Level Task Distribution

Input: Hash function H , Input data M , Number of threads T

Output: Hash output

- 1: Partition internal state of H into T segments
 - 2: Assign each segment to a thread
 - 3: **for all** rounds r in hash function **do**
 - 4: Each thread processes its assigned state segment
 - 5: Synchronize threads using warp-level primitives
 - 6: Perform cross-thread state mixing through register shuffling
 - 7: Synchronize threads
 - 8: **end for**
 - 9: Combine results from all threads using reduction operations
 - 10: **return** Final hash output
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The task distribution strategy is optimized for SHA256 operations within SPHINCS⁺, where hash function calls account for over 90% of computational workload. The implementation employs a tiered approach where:

- At the intra-warp level, 16 threads collaborate on a single hash computation with specific state variable assignments
- At the block level, multiple warps process independent hash operations concurrently
- At the grid level, optimal workload distribution is maintained with 128 blocks of 256 threads per block

For WOTS+ chain computations, which constitute approximately 70% of the signature generation workload, this task distribution achieves a 5.3x speedup compared to conventional single-thread-per-hash implementations.

B. Adaptive Thread Allocation Strategy

IV. PERFORMANCE EVALUATION

V. CONCLUSION

REFERENCES

- [1] P. W. Shor, “Algorithms for quantum computation: Discrete logarithms and factoring,” *Proceedings 35th Annual Symposium on Foundations of Computer Science*, pp. 124–134, 1994.
- [2] National Institute of Standards and Technology, “Report on post-quantum cryptography,” National Institute of Standards and Technology, Tech. Rep. NISTIR 8105, 2016. [Online]. Available: <https://nvlpubs.nist.gov/nistpubs/ir/2016/NIST.IR.8105.pdf>
- [3] M. S. Turan, K. McKay, D. Chang, L. E. Bassham, J. Kang, N. D. Waller, J. M. Kelsey, and D. Hong, “Status report on the final round of the nist lightweight cryptography standardization process.”
- [4] D. J. Bernstein, A. Hülsing, S. Kölbl, R. Niederhagen, J. Rijneveld, and P. Schwabe, “The sphincs⁺ signature framework,” in *Proceedings of the 2019 ACM SIGSAC Conference on Computer and Communications Security, CCS 2019, London, UK, November 11-15, 2019*, L. Cavallaro, J. Kinder, X. Wang, and J. Katz, Eds. ACM, 2019, pp. 2129–2146.
- [5] “Stateless hash-based digital signature standard,” 2024. [Online]. Available: <https://nvlpubs.nist.gov/nistpubs/FIPS/NIST.FIPS.205.pdf>
- [6] D. Joseph, R. Misoczki, M. Manzano, J. Tricot, F. D. Pinuaga, O. Lacombe, S. Leichenauer, J. Hidary, P. Venables, and R. Hansen, “Transitioning organizations to post-quantum cryptography,” *Nat.*, vol. 605, no. 7909, pp. 237–243, 2022.
- [7] W. Lee and S. O. Hwang, “High throughput implementation of post-quantum key encapsulation and decapsulation on GPU for internet of things applications,” *IEEE Trans. Serv. Comput.*, vol. 15, no. 6, pp. 3275–3288, 2022.
- [8] D. Kim, H. Choi, and S. C. Seo, “Parallel implementation of SPHINCS+ with gpus,” *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 71, no. 6, pp. 2810–2823, 2024.
- [9] Z. Wang, X. Dong, H. Chen, Y. Kang, and Q. Wang, “Cuspx: Efficient gpu implementations of post-quantum signature sphincs_{sup_ℓ}+_{j/sup_ℓ},” *IEEE Transactions on Computers*, vol. 74, no. 1, pp. 15–28, 2025.