Organization of Digital Computers Lab
EECS 112L
Lab 4: Synthesis

University of California, Irvine

Due date: June 9^{th}, 2019

1 Before Synthesis

Pull the changes from the github. The scripts for synthesis purposes are added in the folder qip/syn/. Your code may have the implementation of register read, write, or reset in different clock edges. Using both positive edge and negative edge of a clock in a module makes some problem for the synthesis. because it means that you have 2 clocks. So you may need to modify your code before moving to the synthesis part. Visit ./logs/ to see the syntax issues that you may be facing.

Make sure to add all of your new designed modules to the rtl.cfg file. simulate your design to see if everything works well.

2 Synthesis

Change directory to the syn folder by cd $syn. Open the synth.tcl and change the clock period.

```
#==========================================================================
#                    D E S I G N   P A R A M E T E R S
#==========================================================================
#
#
#
set PROJECT_NAME               "112L-RISCV"
set TOP                        "design_top"
#set TOP                        "alu"
#set TOP                        "Datapath"
#set TOP                        "Controller"
set FILES                      "files_design_top"
set clock_period              4.0
```

By this change we are increasing the clock period from 0.9 to 4. Your design may not fit with 4ns clock period but it is ok.

```
#redirect -file ${REPORTS}/${TOP}.power_flat.rpt { \
#        report_power -net -cell -analysis_effort medium -verbose -nosplit -flat \
#}


# clean up
exec rm -rf *.syn *.mr *.pvl rtl.f
exec rm -rf WORK rtl.f  incdir.list default.svf command.log alib-52



exit
```

Now go the scripts folder and open the files_riscv.tcl . All of your modules should be listed here. A script automatically populates necessary files in this list. However, check the list and if you have other modules make sure to add them to this list.

```
analyze -format sverilog { \
  adder.sv \
  flopr.sv \
  imm_Gen.sv \
  mux2.sv \
  datamemory.sv \
  instructionmemory.sv \
  ALUController.sv \
  alu.sv \
  RegFile.sv \
  Controller.sv \
  Datapath.sv \
  RISC_V.sv \
}
```

Now, go back to the syn folder and run the command: source run.sh. The dc shell-t -f synth.tcl command with the run.sh will invoke the Synopsys Design Compiler (the synthesizer tool) and pass the synth.tcl script to run. This may take several minutes.

When the synthesis completed go to 112L-RISCV. There will be a reports folder contains all synthesis reports of your design. Check the riscv.elab.rpt. In this report see if all your design modules synthesis completed successfully. Then open the riscv.qor.rpt. In this report you will find information about timming and area of your design. Put the critical path length, critical path slack, and area in your report.

3 Material to be submitted

- A report comparing the single-cycle and pipeline synthesis and comparison (Frequency/Area/Power)
- QoR power report from Single-cycle pipeline synthesis.
- Deadline Sunday June 9th.
- One report per team.
- No Errors in their synthesis