A 9-bit Resistor-based Thermal Sensor

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I. Introduction

This sensor is for on-chip thermal detection. It uses differential low pass filter (DLPF) as the sensing elements. While the readout circuit is a SAR ADC. The CDAC was embedded in the DLPF, which can eliminate CDAC reference circuits and utilize the ADC whole dynamic range. The design was implemented in a 65nm CMOS process.

II. System Level Architecture

The system-level architecture was shown in Fig.1. It has 5 submodules that summarized in Table I. The circuit of each submodule is described in Section III.

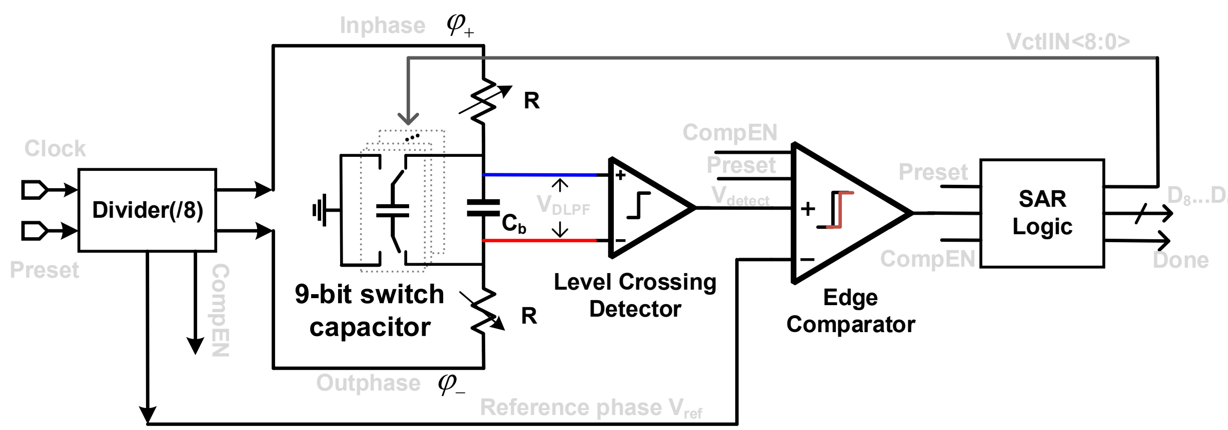


Figure.1 Block diagram of the DLPF-based SAR quantization embedded thermal sensor architecture.

Table I. The submodules in the thermal sensor and its functionality.

Submodule	**Function**
Clock Divider by 8	Generate complementary clock to drive DLPF, Comparison enable signal, and reference clock
CDAC Embedded DLPF	The sensing element with embedded CDAC
Resistance Tuning Configuration	Logic to tune resistance in the DLPF
Level Crossing Detector	To detect the crossing point of the output from DLPF
Edge Comparator	To compare the crossing point with the reference clock
SAR Logic	To control the bit capacitor in CDAC in/out of the DLPF

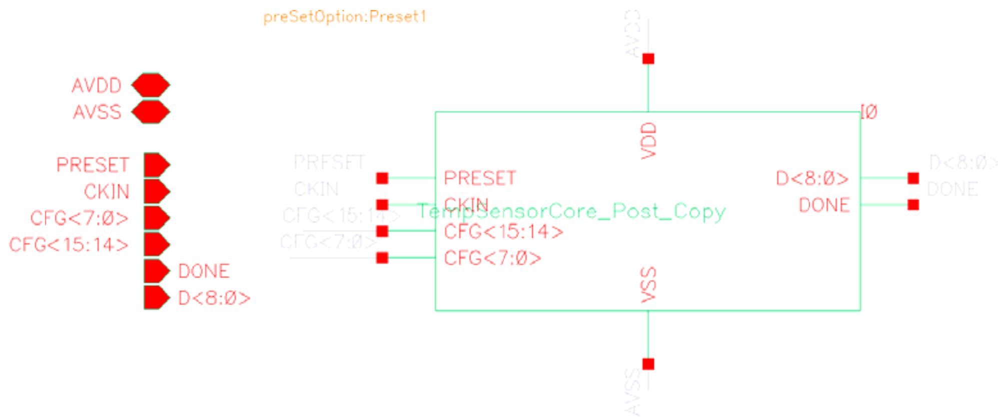


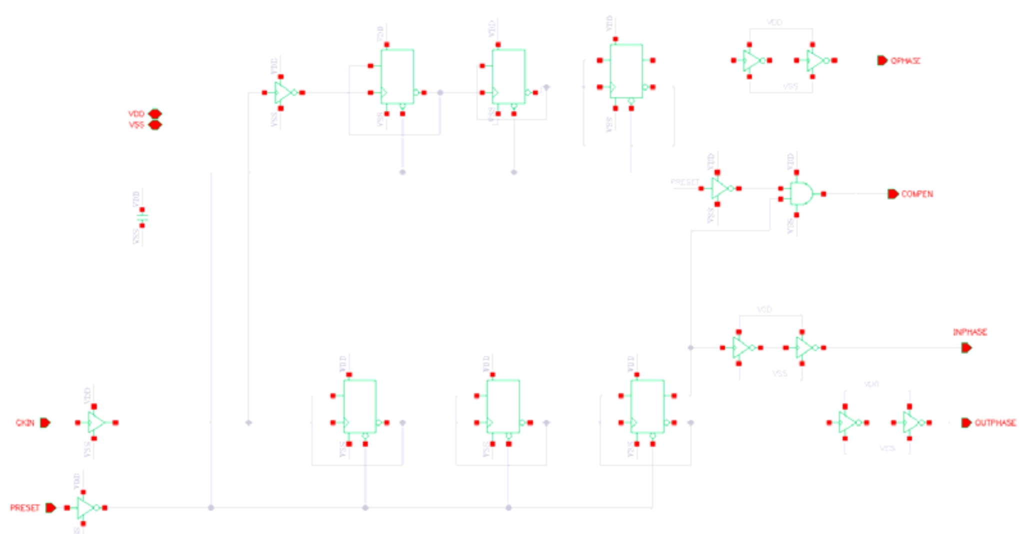
Figure.2 The top-level symbol of the thermal sensor

Table II. Pin configuration

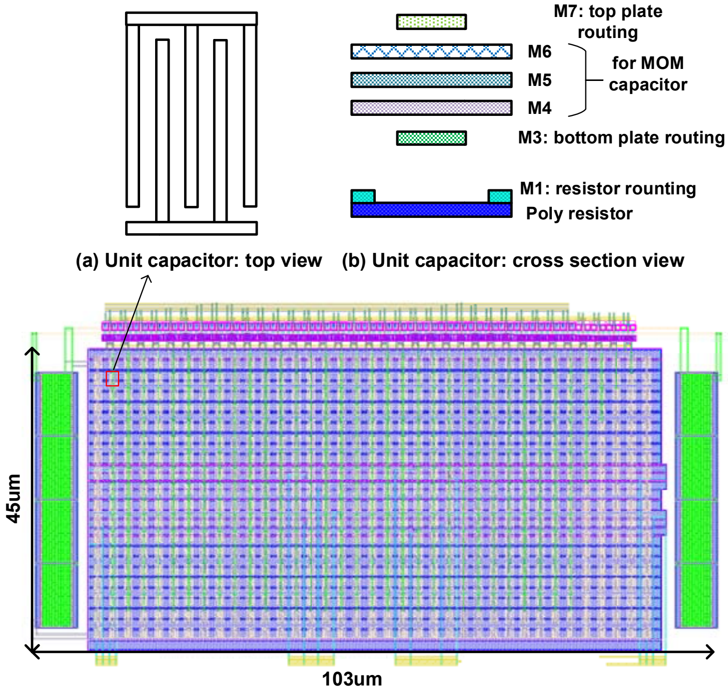
Pin Name	Input / Output	Specification
AVDD	Input	Power supply, 1.0~1.2V
AVSS	Input	Ground
PRESET	Input	A pulse signal
CKIN	Input	32MHz 50% duty cycle clock
CFG<7:0>	Input	Only 1-bit can be high, from SPI
CFG<15:14>	Input	4 possible combinations, from SPI
DONE	Output	Notify conversion is done
D<8:0>	Output	9-bit output code

III. Submodules

3.1 Clock divider



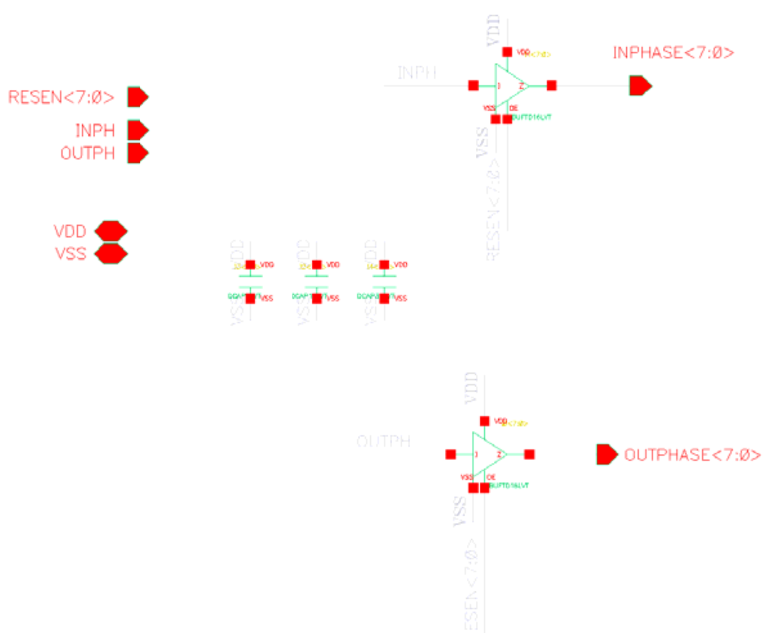
3.2 CDAC embedded DLPF



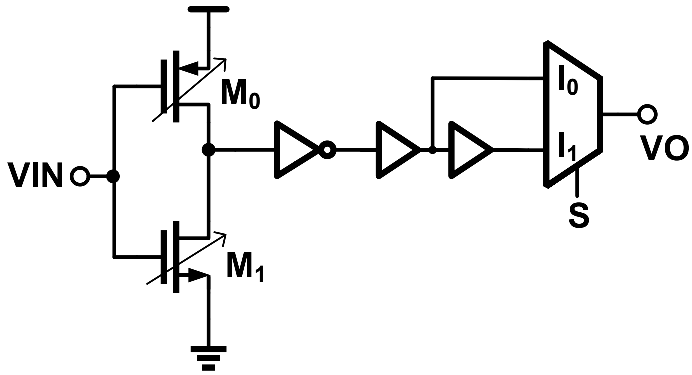
(a) Unit capacitor: top view (b) Unit capacitor: cross section view

(c) The DLPF layout

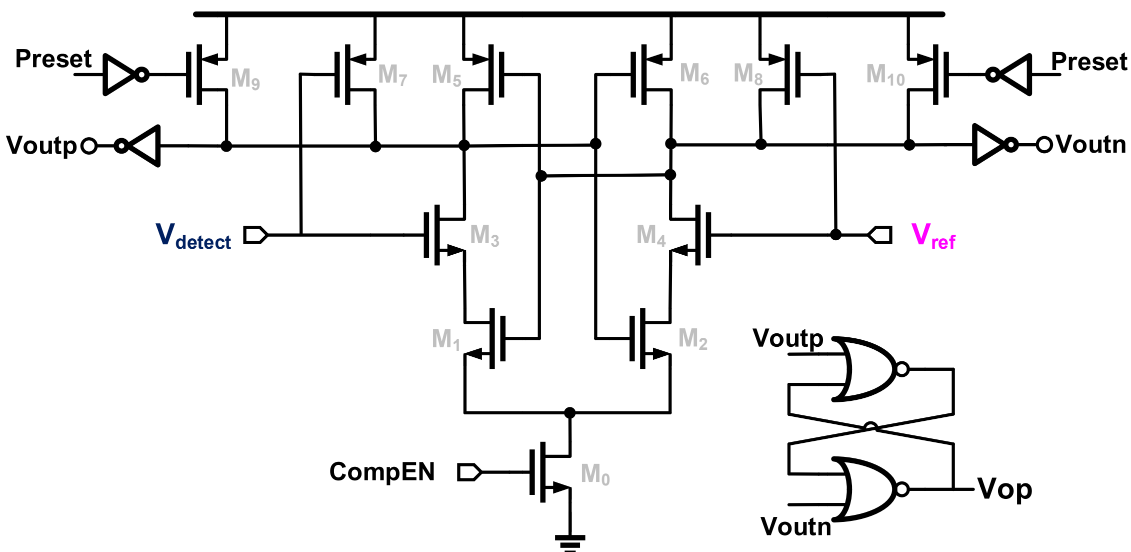
3.3 Resistance Tuning Configuration



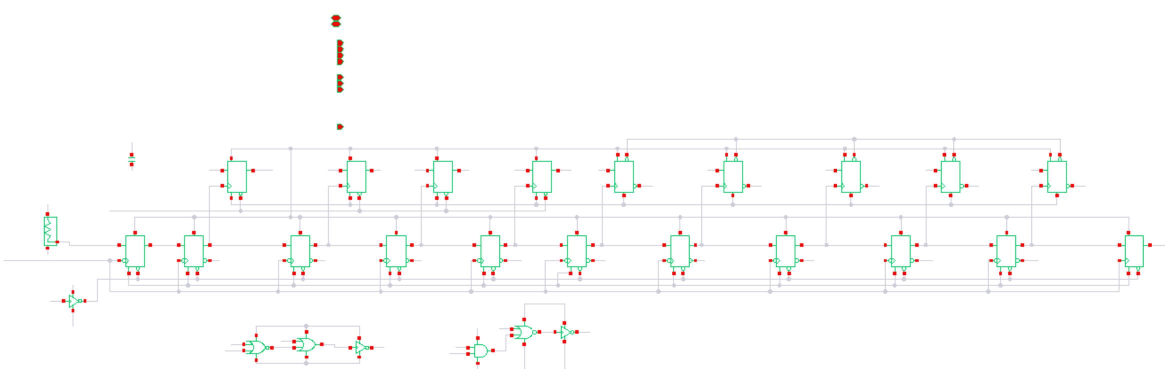
3.4 Level Crossing Detector



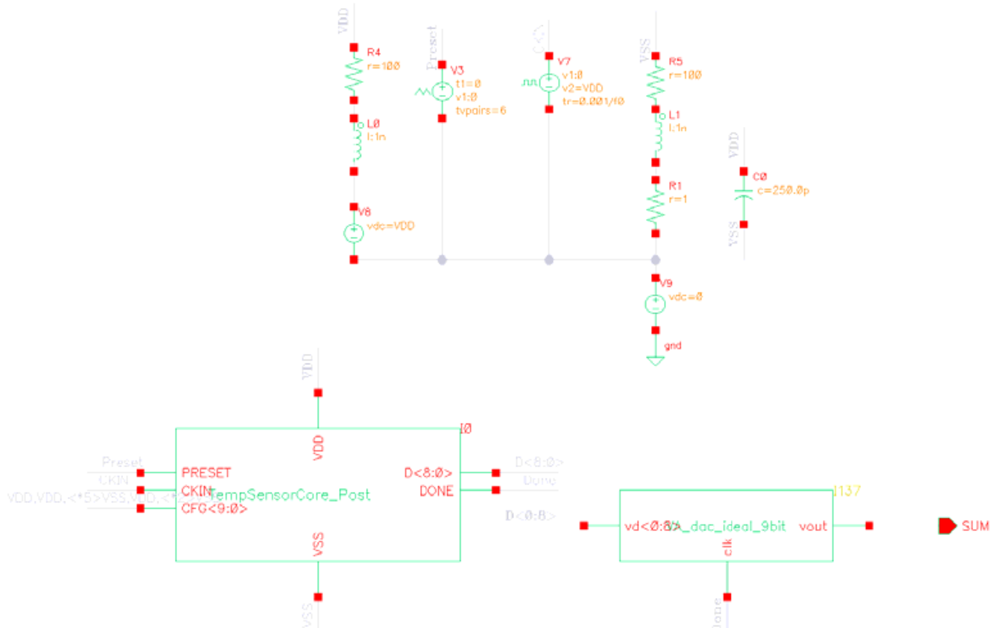
3.5 Edge Comparator



3.6 SAR Logic



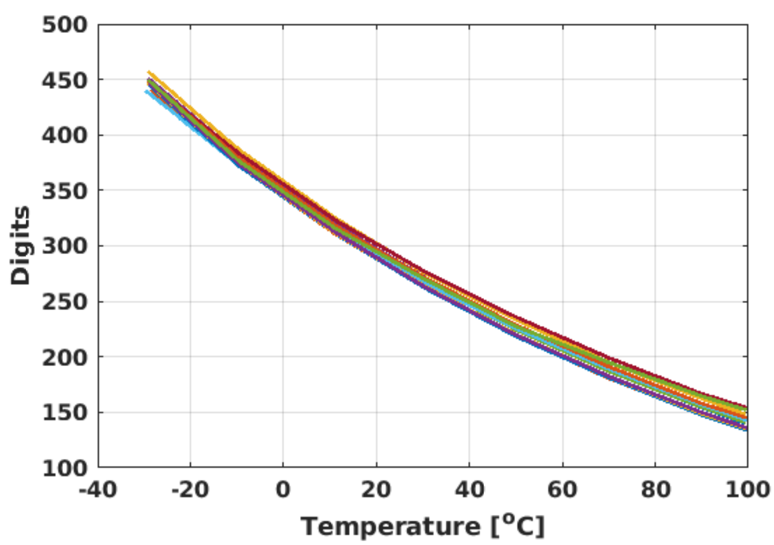
IV. Simulation Setup--Testbench



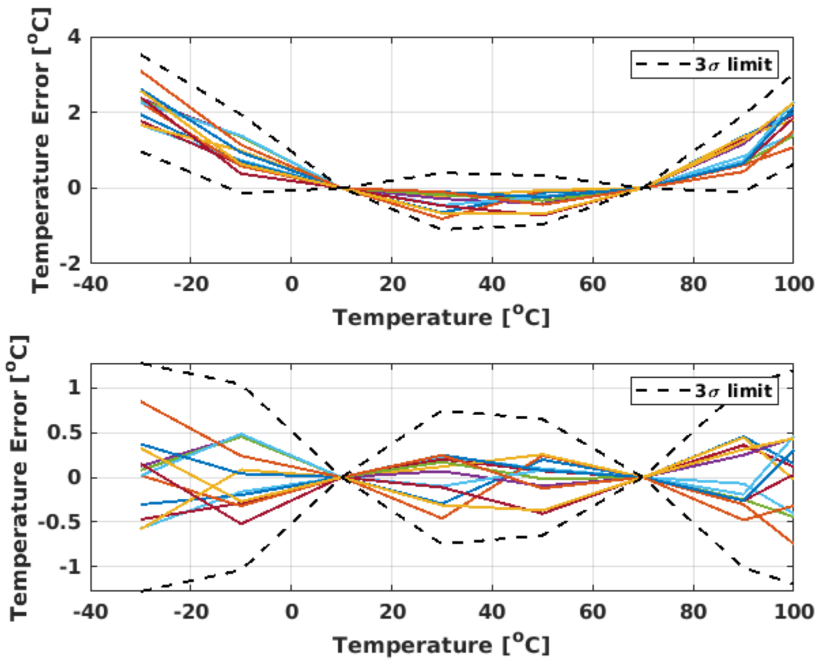
V. Measurement Results

The temperature sensor prototype was fabricated in a 65nm LP CMOS technology.The chip has an SPI interface,which is used to connect to a micro-controller/FPGA board (PYNQ-Z1) for testing. The clock is provided by the PLL on the micro-controller, acting like the SoC master clock with noisy jitters in practice.The measurement was done by placing the test board in a temperature-controlled Tenney environmental chamber, and the PYNQ-Z1 board drivenby a computer connecting to the test board is placed outside of the chamber. No extra measurement equipment is required.

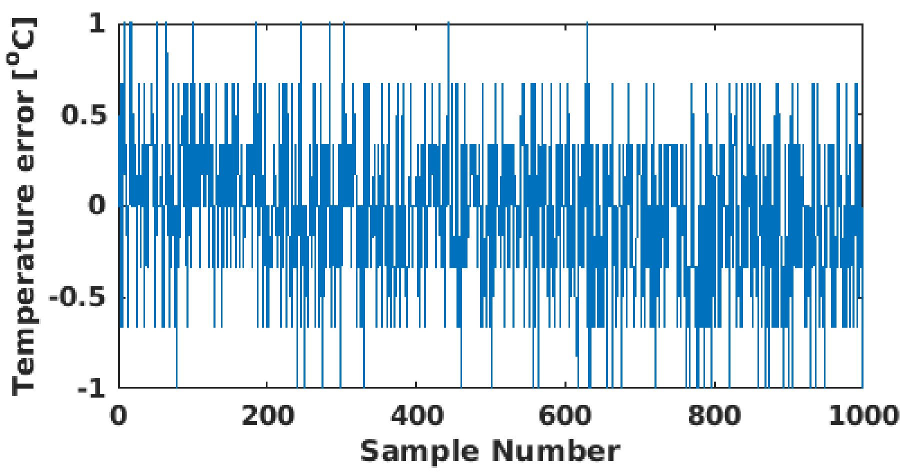
5.1 Raw digits versus temperature



5.2 Inaccuracy



5.3 Resolution



Measured temperature error at 25 °C→ 1-σ resolution 0.4 °C