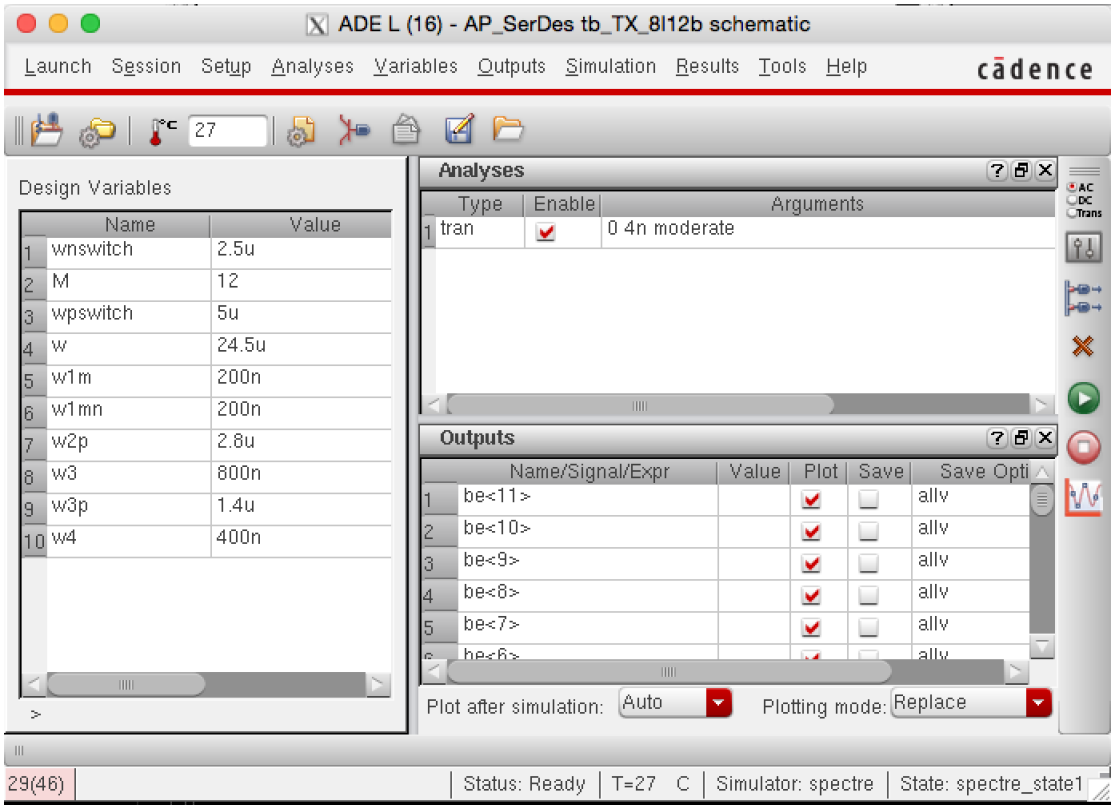
12-bit 8-wire 8-level transmitter

1. Schematic structure

Cell Name	Description
TX_8l12b	Top-level cell.
ENC_8l12b_v2_tspc	Encoder to enable 12b8w8l signaling.
ENC_8l12b_v2_tspc_stage2_v2	Sub-circuit of ENC_8l12b_v2_tspc.
MUX2to1_dig	Massive 2-to-1 MUX.
mux	Sub-circuit of MUX2to1_dig.
Equalizer_8l12b_v7_ctrl	Pre-amphasis equalizer.
PreDriver_PAM8_v4	Pre-driver.
CML_Driver_PAM8_woCS_v3	Driver.
Bias_v2	Bias circuit.

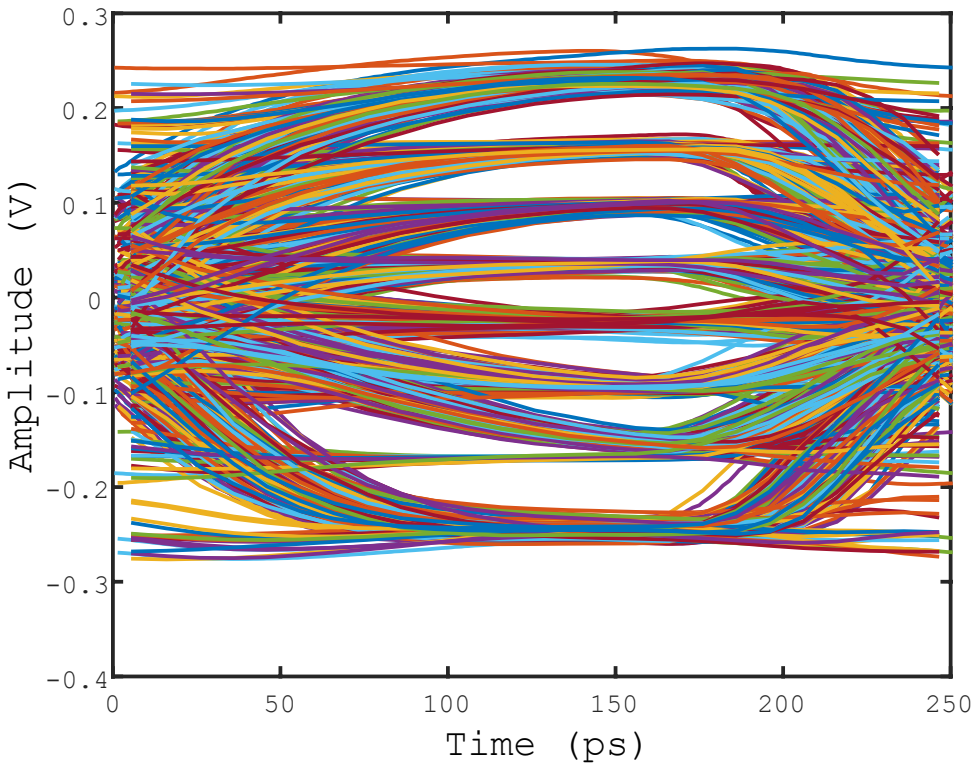
2. Testbench

Use tb_TX_8l12b.ckt to simulate the top-level cell TX_8l12b. The simulation settings are as shown below.



3. Simulation results

The eye diagram is simulated at 2GHz clock frequency. The data rate is 8x6Gb/s/pin. The smallest eye opening is 70ps and 37mV horizontally and vertically. The energy efficiency is 0.79pJ/bit.


0.3
0.2
0.1
0
-0.1
-0.2
-0.3
-0.4
Amplitude (V)
0
50
100
150
200
250
Time (ps)