A 12-bit Segmented SAR ADC in TSMC 65nm LP CMOS

The provided IP of a12-bit SAR ADC is presented by both cdl netlist and the pdf print of the hierarchical schematics. Users need the following tools, libraries, and agreement to import the cdl netlist and view the original design. If you do not have all of the following requirements. You can still view the design through the pdf print of the hierarchical schematics.

- Tool: Cadence IC616 or later version
- Libraries: analogLib, basic, cdsDefTechLib, functional, US_8ths, **tsmcN65**
- Agreement: Signed Non-Disclosure Agreement (NDA) between users and TSMC

The testbench for top level is provided, which uses ADE and Spectre. The setup for ADE is provided in the "Simulation Setup and Results.docx". The hierarchical schematics are listed in Table 1.

#	Category	Cell	Description
1	testbench	tb_ADC_single	Testbench for 12b ADC
2	12b_ADC_TOP	12b_ADC	12bit SAR ADC
		ckt_CKGEN	Clock generation circuit
		DataCollector	Collector output data
3	12b_ADC	5b_ADC	5b coarse SAR ADC
		8b_ADC	8b fine SAR ADC
4	5b_ADC	CDAC_SW_Coarse	5-bit CDAC
		BTSW	Bootstrapped switch
		Coarse_SAR_Logic	Coarse SAR Logic
		Comp_Coarse_V3_Cali	Coarse comparator
		Coarse_Comp_CK	Asynchronous coarse comparator clock generator
5	8b_ADC	ckt_CpSkp_LOG_V3	Skip copy logic for setting 5-bit fine MSB
		CDAC_SW_Fine_P	8-bit CDAC
		BTSW_MOM	Bootstrapped switch
		FINE_SAR_Logic_V4	Fine SAR Logic
		Comp_Fine	Fine comparator
		Fine_Comp_CK_V3	Asynchronous fine comparator clock generator