L7 Analogue Input/Output

In many microprocessor applications input signals will come from sensors which provide an analogue signal. For example:

- modern mobile phones contain accelerometers
- all mobile phones digitise the output of their microphones
- the oxygen sensor used in engine management systems is analogue
- image sensors in cameras, phones, etc. produce analogue information

On the output side microprocessors must provide analogue signals to drive:

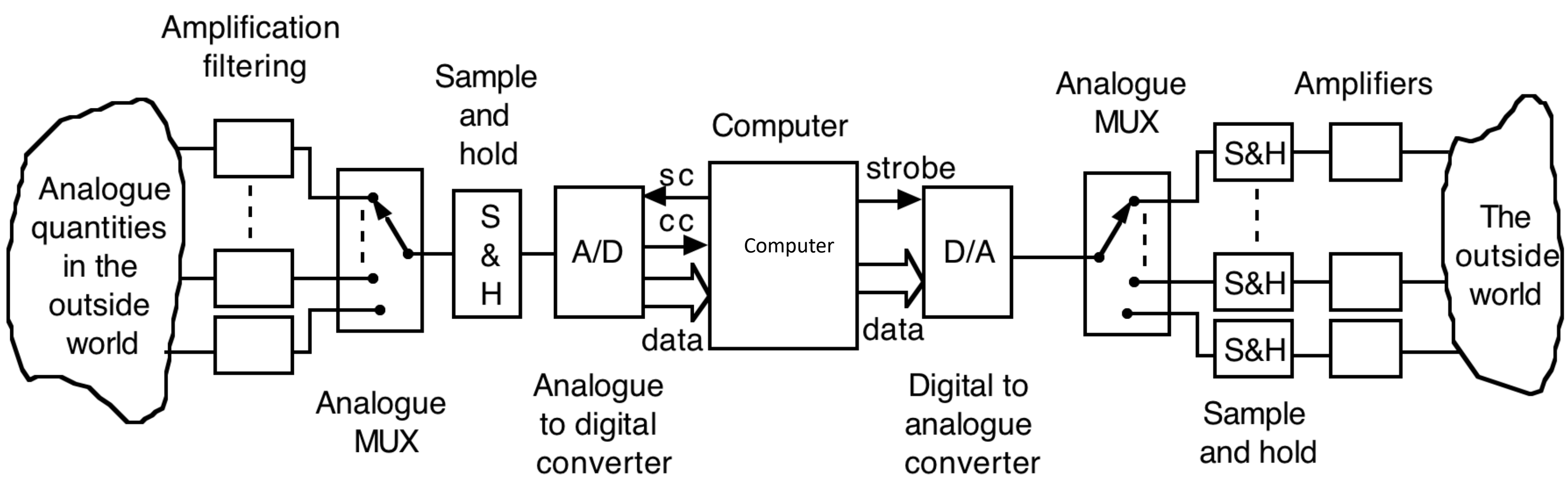
- speaker systems to produce speech and music.
- variable speed motors in air conditioning, electric drills, etc.

This section introduces the circuits required to interface a digital computer to the analogue world.

Analogue Interfacing

In this section we consider connecting a digital computer to an analogue world. Many quantities that a computer may be required to measure are of a continuous or analogue nature such as temperature, pressure, voltage, position. A computer may also be required to output analogue quantities such as desired temperature, target pressure, requested position.

A computer system equipped for analogue input and output may include the following components:

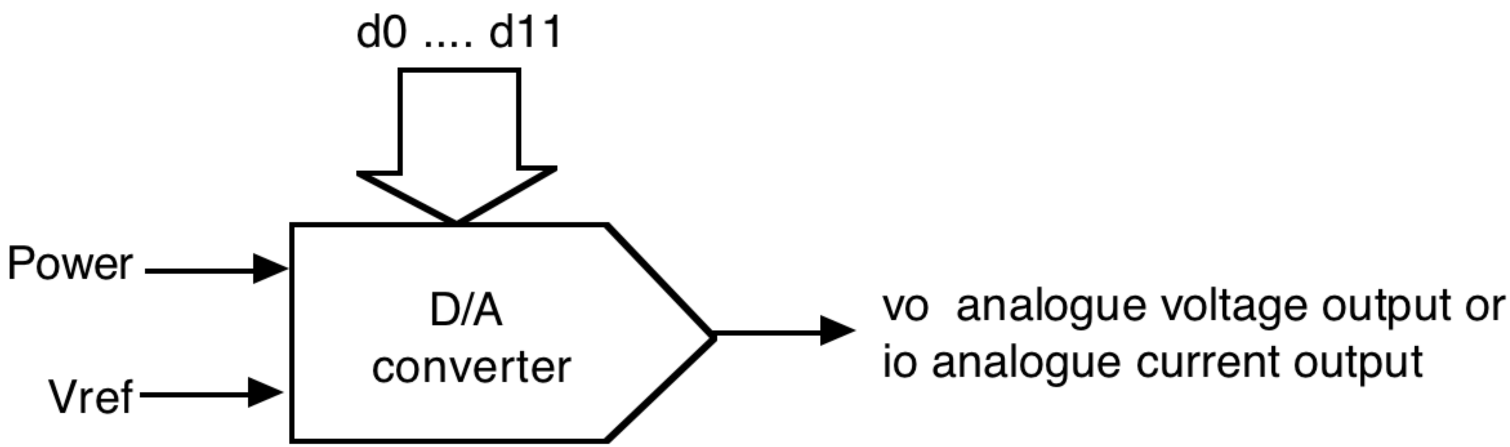


L07-1
Digital to Analogue Conversion

CLIVE MAYNARD

Digital to Analogue Conversion

Digital to analogue converter (DAC) schematic symbol:



DAC Transfer Characteristic

An ideal DAC has the following transfer characteristic:

$$vo = k\,(\bullet\, d_{n-1}\ \ldots..\ d_0)\ Vref$$

where $\bullet\, d_{n-1}\ \ldots..\ d_0$ is the binary input represented as a binary fraction
k is a gain factor which is often = 1
n is the number of bits in the binary input

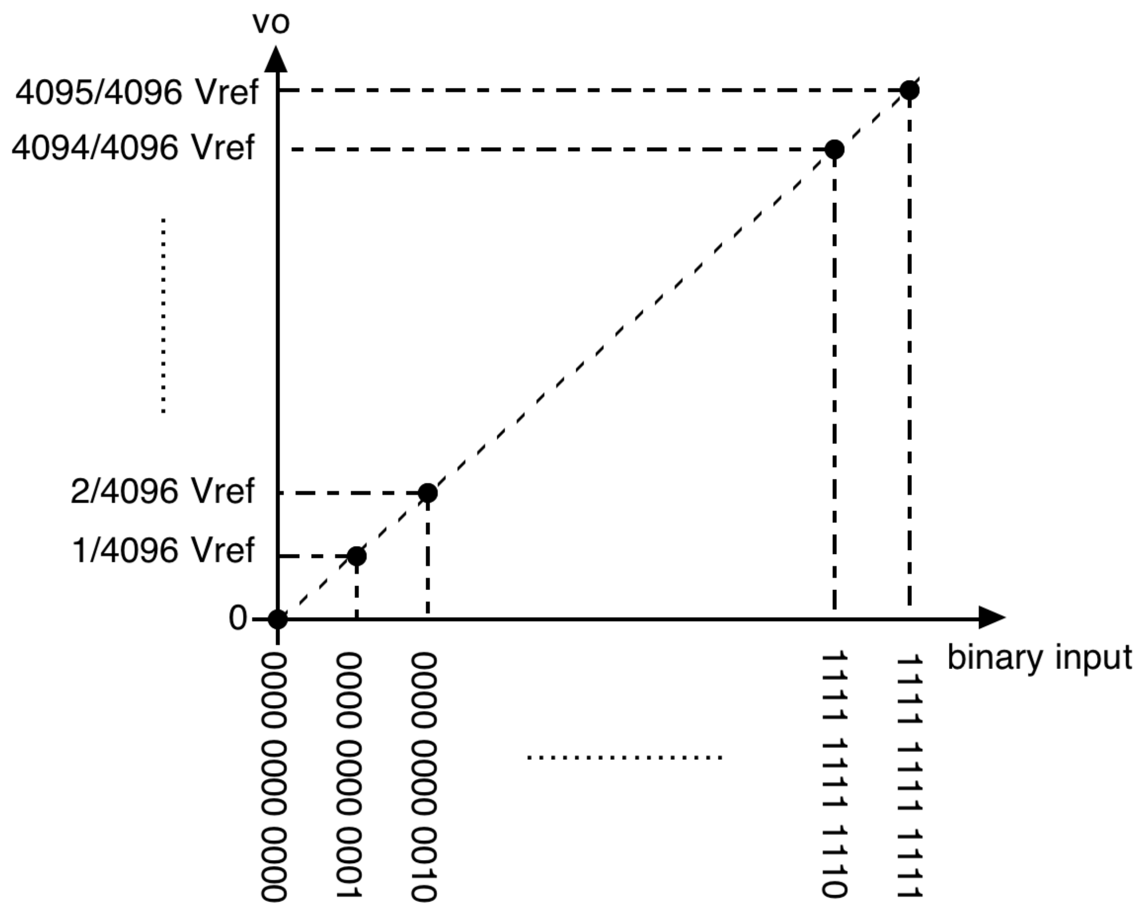
Step size =(k Vref) / 2^n is called the resolution

If reference voltage Vref = 5V
k = 1
n = 12

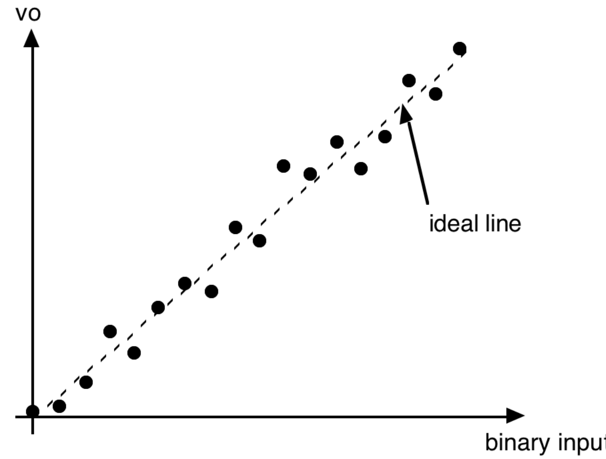
then step size 1 * 5 / 4096 = 1.22mV

In some D/A converters Vref is allowed to vary -
these are called multiplying D/A converters (output is the binary fraction multiplied by Vref)

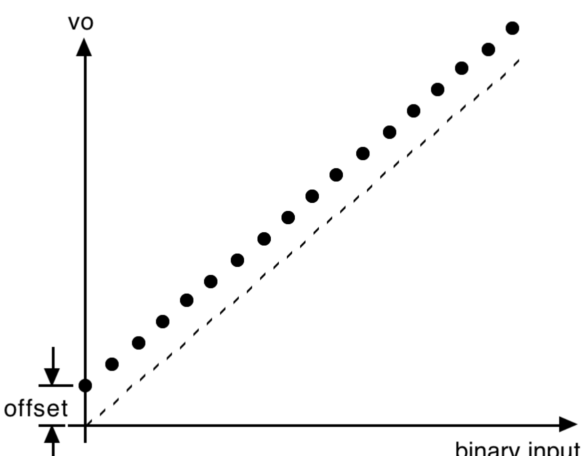
Ideal DAC Characteristic



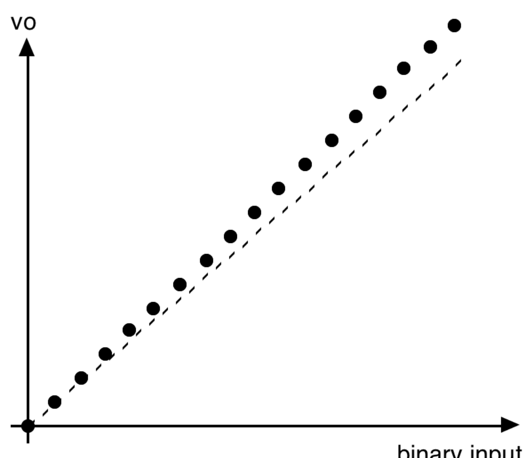
Practical Characteristics



Random variation



Offset error



Gain error

Gain errors and offset errors can be corrected by external circuitry.

Linearity Error

The static performance of a D/A converter is determined by measuring the deviation from a line fitted to the output points.

Line fitting methods:

1) Least-squares fit - minimises the sum of squares of deviation of output from the fitted line. This technique requires a lot of measurement and computation.

2) Zero-base method - fitted line passes through converter output for zero input and the slope minimises the maximum deviation of output points from the fitted line.

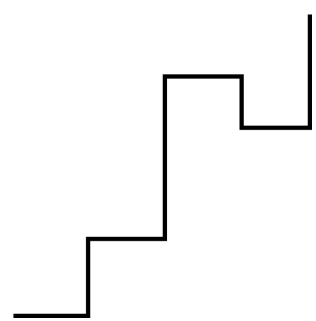
3) Terminal-point method - line passes through the points corresponding to the minimum and maximum converter output.

Types of Error

Linearity error - is the maximum deviation from the fitted line expressed in terms of the converter step size or as a percentage of the maximum converter output.

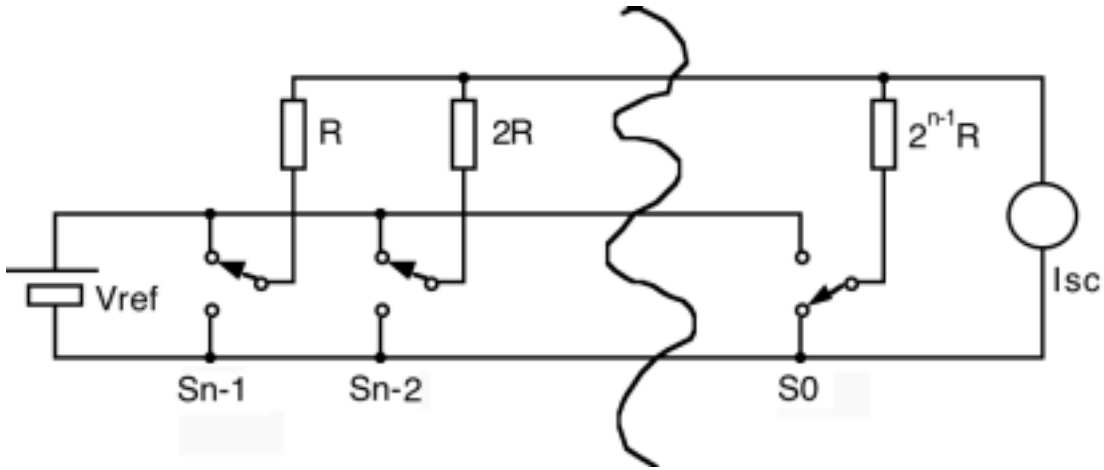
Differential linearity error - is the magnitude of the maximum difference between each output step of the converter and the ideal step size for a change in the least significant bit of the converter input.

Monotonicity - a D/A converter is monotonic if its output always increases for an increase in its binary input.



Parallel DACs

1) Binary weighted resistors

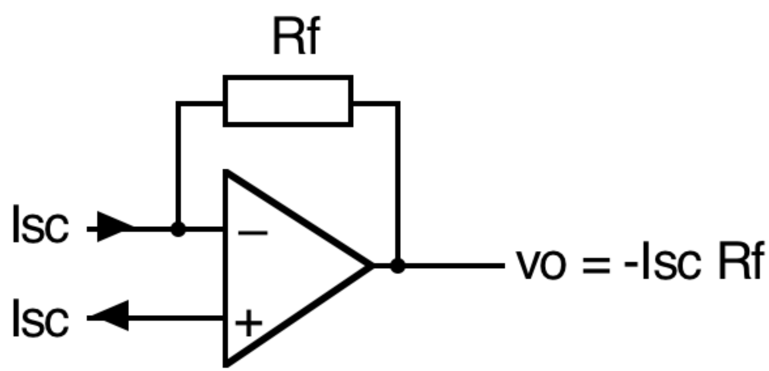


Sm is up if d_m = 1 Sm is down if d_m = 0

$$Isc = \frac{2Vref}{R}\left(d_{n-1}2^{-1} + d_{n-2}2^{-2} + \ldots + d_0 2^{-n}\right)$$

Current to Voltage

If a voltage output is required rather than a current output the following current to voltage converter can be attached to the output of the binary weighted resistor A/D converter.

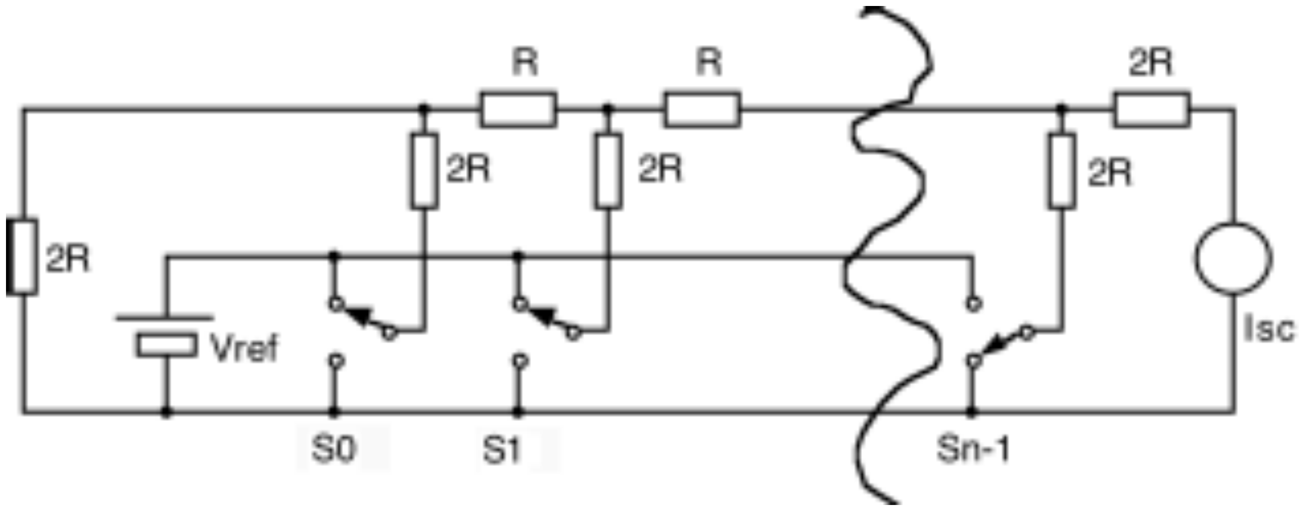


Problems with the binary weighted resistor DAC

- it is difficult to make resistors with a $1:2^n$ ratio (especially in an integrated circuit)

- a varying current is drawn from Vref (internal resistance of Vref will cause the effective Vref to change depending on the binary input to the converter)

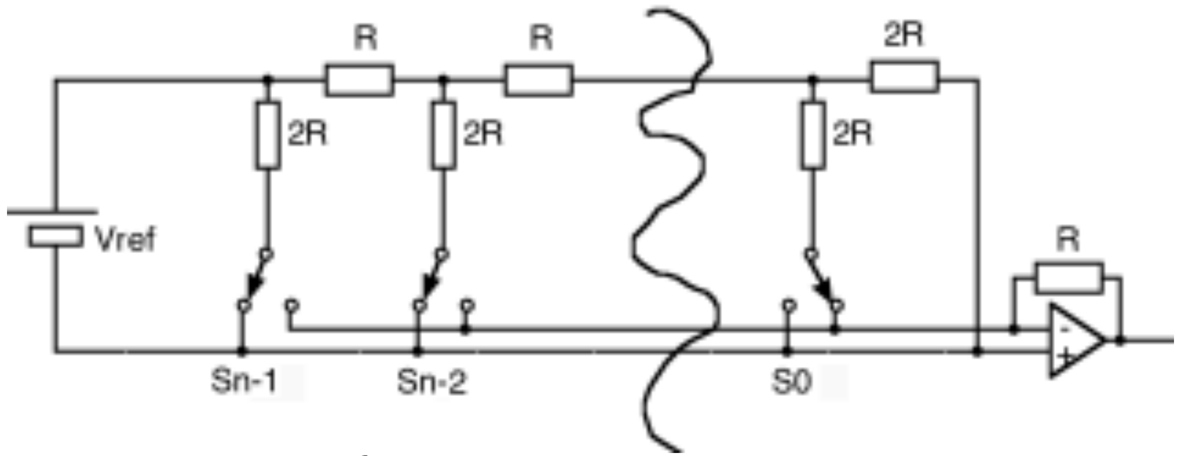
R–2R ladder



$$Isc = \frac{Vref}{3R}\left(d_{n-1}2^{-1} + \ldots. + d_1 2^{-(n-1)} + d_0 2^{-n}\right)$$

This design is better for IC fabrication because only two resistor values are required. However, the current drawn from Vref still varies.

Inverted R-2R Ladder



$$Isc = \frac{Vref}{R}\left(d_{n-1}2^{-1} + d_{n-2}2^{-2} + ... + d_0 2^{-n}\right)$$

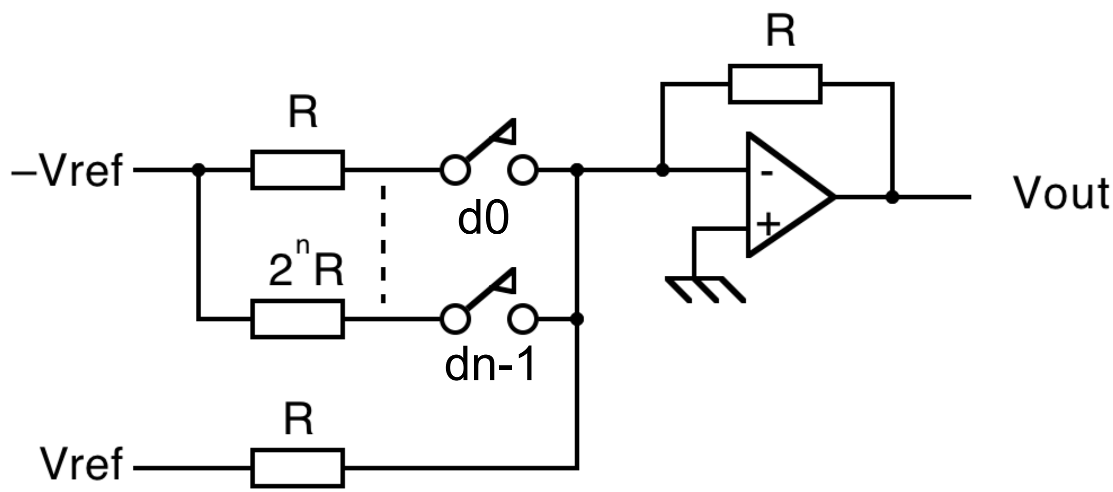
With this design the same current is drawn from Vref independent of the binary input.

Bipolar Coding

With the D/A converters considered so far the output is zero for a binary input of zero and then increases as the binary input is increased (treating the binary input as an unsigned number).

For many applications it would be useful to have an D/A output which could swing equally positive and negative and that would respond to the binary input as though it were a 2's complement number. To do this, two modifications are required to the basic D/A converter:

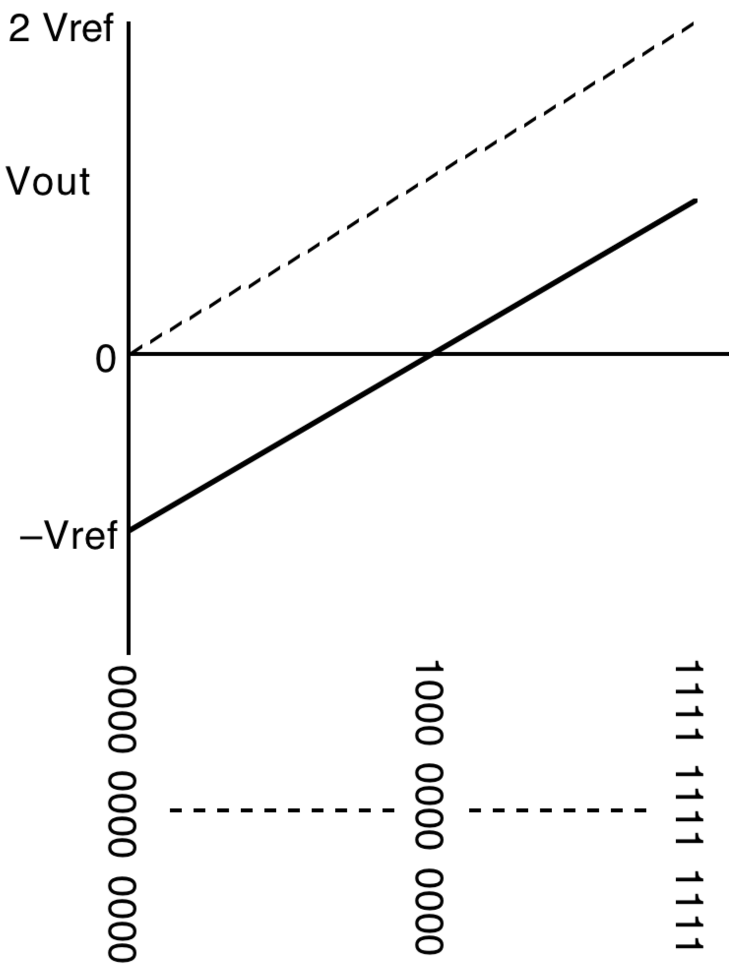
Offsetting the DAC output



$$\text{Vout} = \text{Vref}\left(d0\ 2^{-0} + d1\ 2^{-1} + \ldots. + dn\text{-}1\ \ 2^{n-1} - 2^{-0}\right)$$

By injecting an additional current into the current to voltage converter the D/A output can be shifted in the negative direction by half the full-scale value.

Offset Binary Coding



The result is called offset binary - the output is proportional to the binary input offset by a fixed amount.

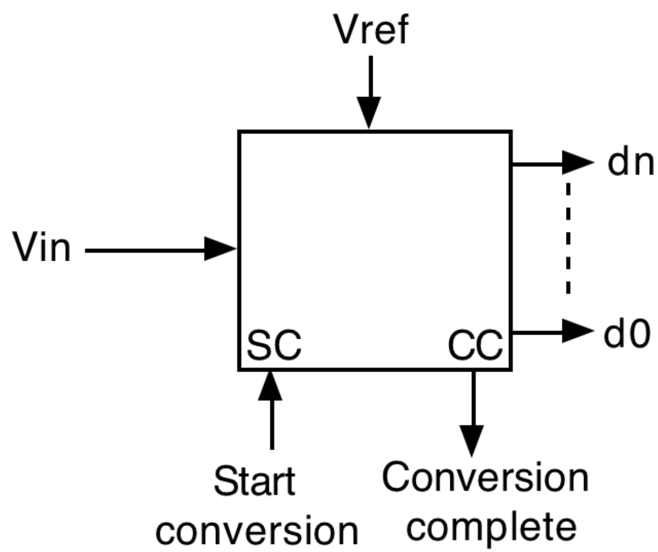
Look at the Table

	Offset binary	2's complement
+9.99V	1111 1111 1111	0111 1111 1111
	⋮	⋮
	1000 0000 0001	0000 0000 0001
0V	1000 0000 0000	0000 0000 0000
	0111 1111 1111	1111 1111 1111
	⋮	⋮
-10V	0000 0000 0000	1000 0000 0000

The only difference between offset binary and 2's complement is inversion of the most significant bit of the 2's complement number. Therefore to convert a DAC to bipolar coding we must offset the analogue output by half of full scale and invert the most significant bit of the binary input.

Analogue to Digital Conversion

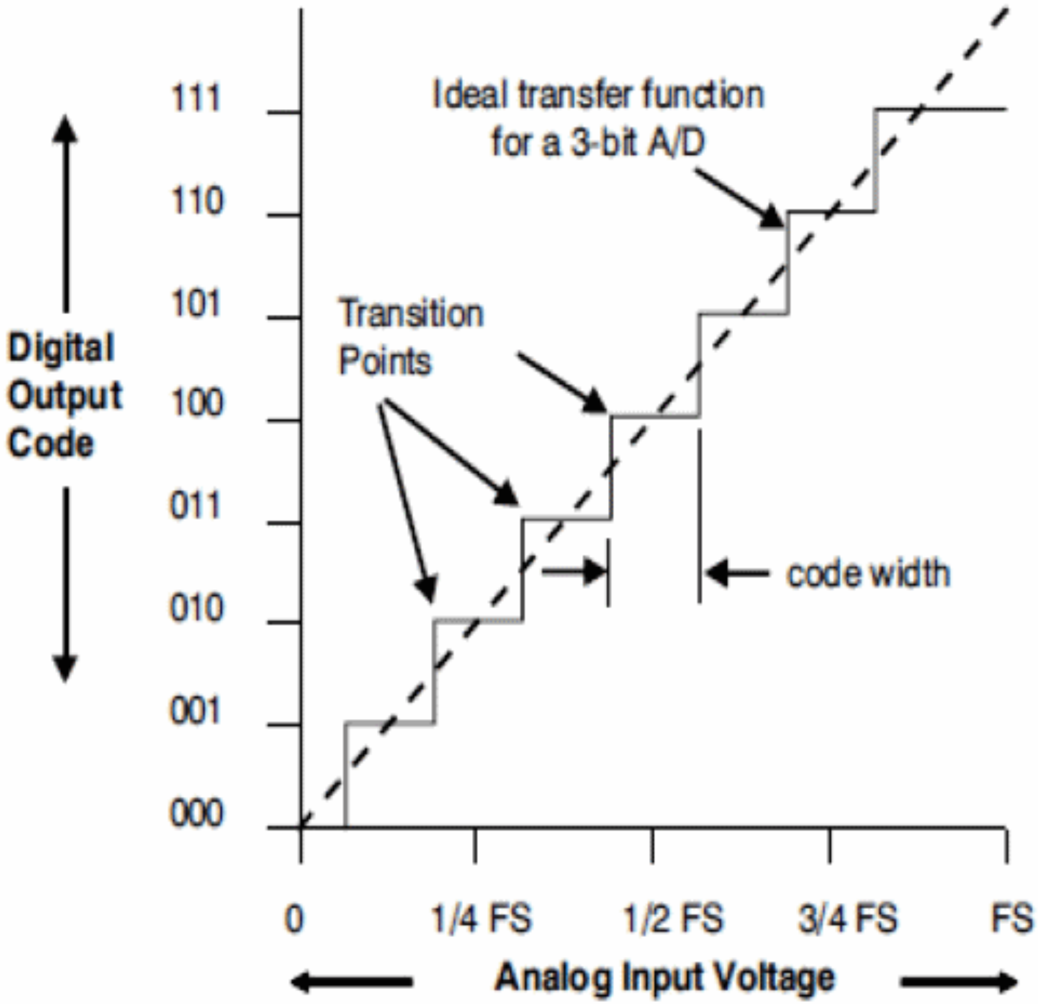
This is the schematic symbol for an analogue to digital converter (ADC):



L07-2
Analogue to Digital Conversion

CLIVE MAYNARD

Characteristics of Ideal ADC



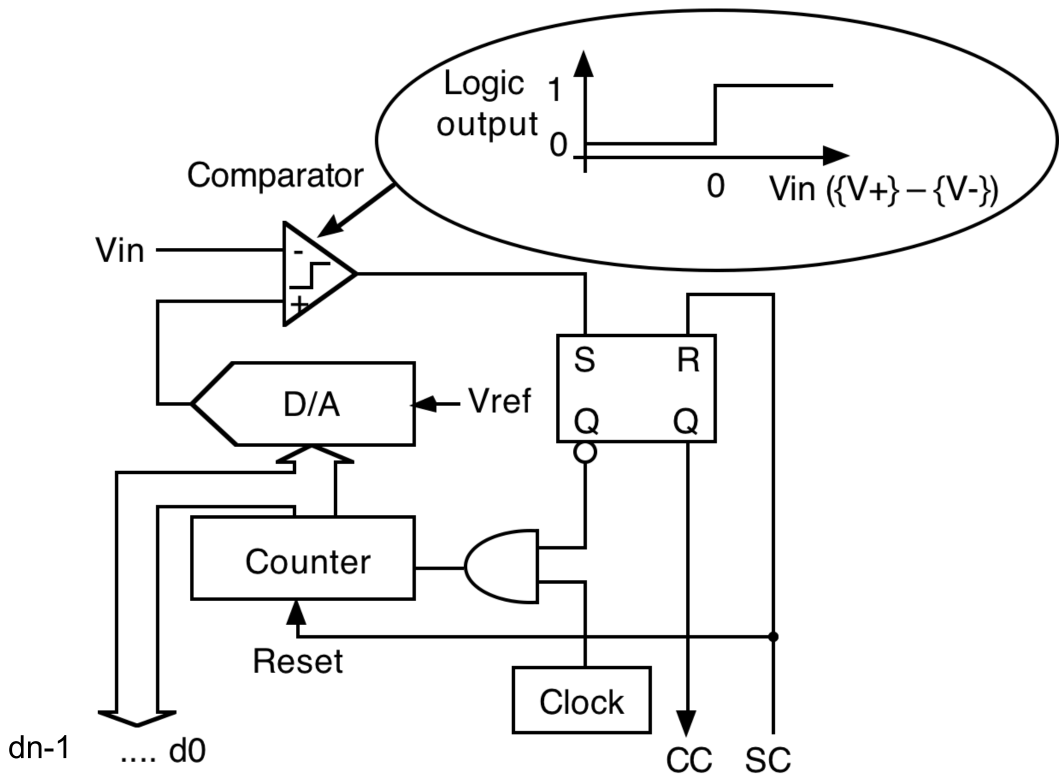
<u>Transition point</u> = where output code changes from one code to an adjacent code

<u>Ideal code width</u> = 1LSB

ADC Imperfections

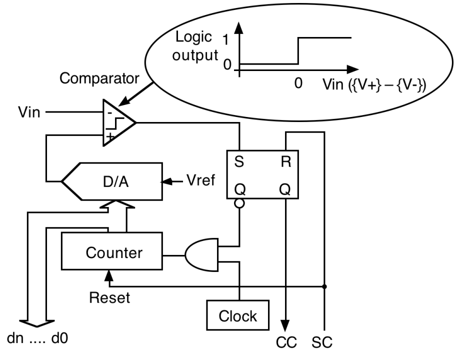
- being non-monotonic,
- having an offset,
- having gain error, and
- having missing codes (binary codes which never appear on the output).

Ramp-Up Converter

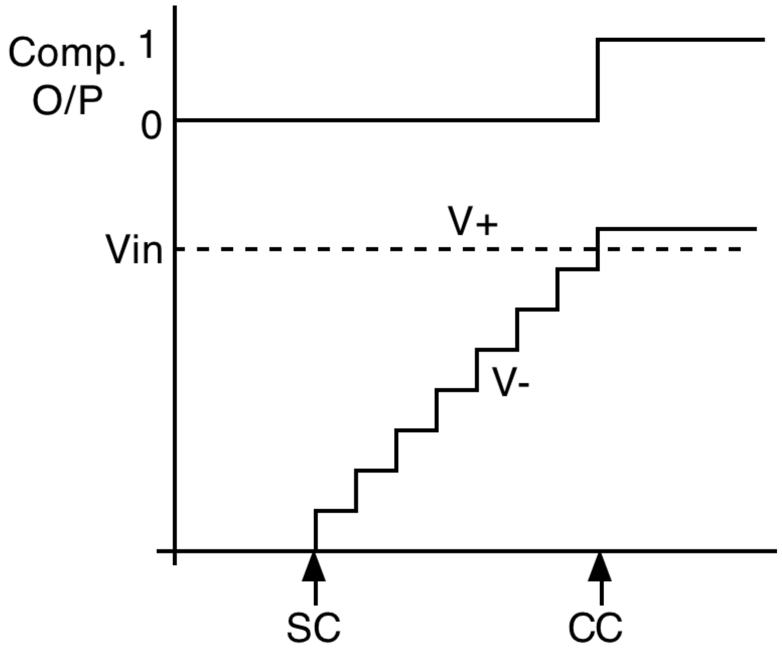


Ramp-Up Converter Algorithm

- Start conversion signal resets counter to zero and resets SR flip-flop.
- The zero input to the DAC is converted to the corresponding analogue voltage and this is applied to the positive terminal of the comparator.
- In normal operation unknown input Vin would be greater than this DAC output and therefore the comparator output will be 'not asserted' and the SR flip flop will not be set.
- The Q(L) output of the SR flip-flop enables the AND gate and clock pulses increment the counter causing the D/A converter output to increment in steps.
- When the D/A converter output exceeds the analogue input the comparator changes state setting the SR flip-flop.
- This stops clock pulses to the counter and asserts conversion complete.
- The counter value d0 .... dn-1 is the digital value that corresponds to the analogue input Vin.



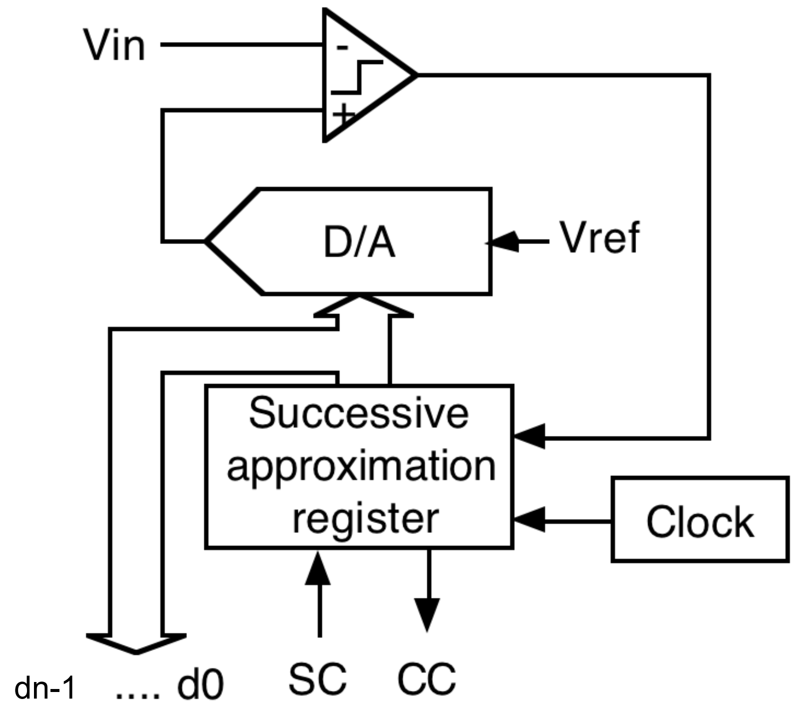
Conversion Process



- – The count-up A/D converter is slow. For large n it needs many clock pulses (up to 2^n).
- – The conversion time is variable.
- + This kind of converter is simple and therefore cheap to make.
- + With a small modification the converter can be made to track the input using an up/down counter.

Accuracy depends upon Vref and the D/A converter.

Successive Approximation Converter

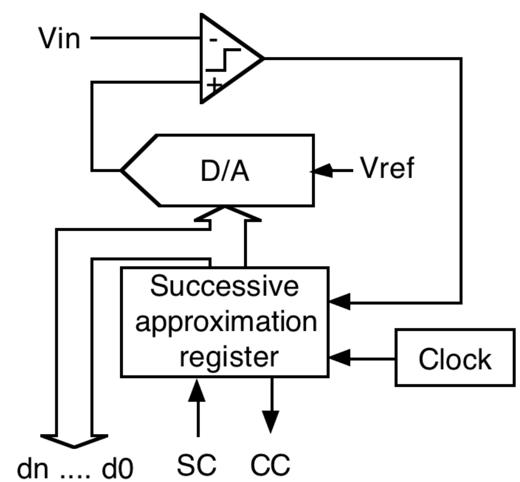


Similar to the count-up converter except that it uses a more efficient technique for estimating the analogue input. In this diagram the added complexity of this circuit is hidden in the box marked 'successive approximation register'.

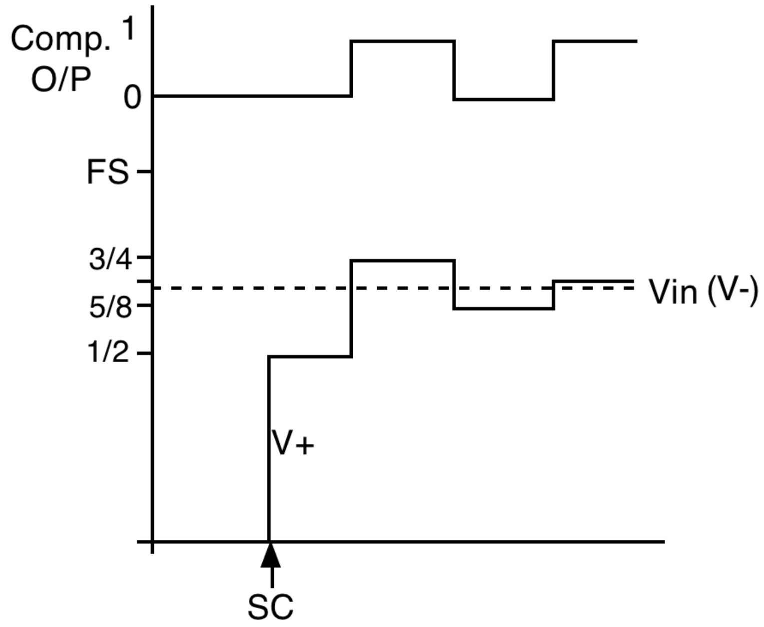
Conversion Algorithm

1) Most Significant Bit (MSB) of the D/A converter is turned on, all others turned off,
2) If the comparator output is asserted (ie. Vin < D/A output) then turn off MSB and turn on next bit,
3) If comparator output is not asserted (ie. Vin > D/A output) then leave MSB on and turn on next bit.

etc.



Conversion Process



- \+ This converter is faster than the count-up converter needing only n clock cycles.
- \+ Conversion time is constant.
- – The analogue input must be held constant during conversion time.

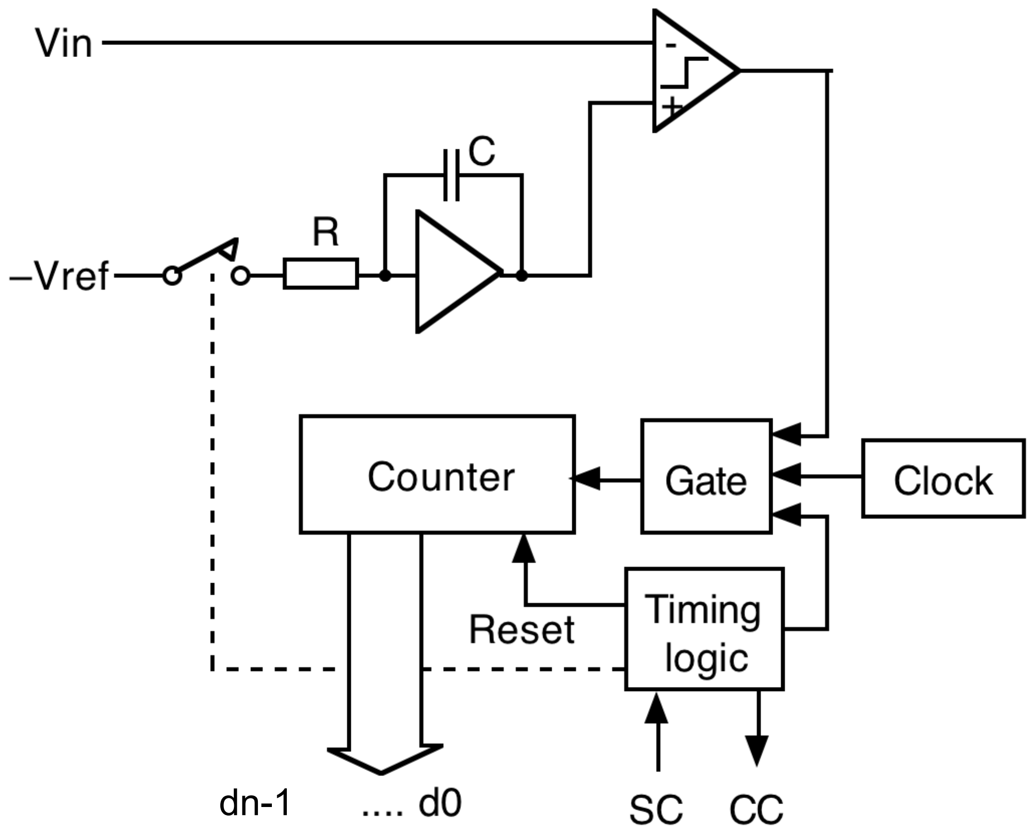
As before, accuracy depends upon Vref and the D/A converter.

Integrating Converters

Single slope

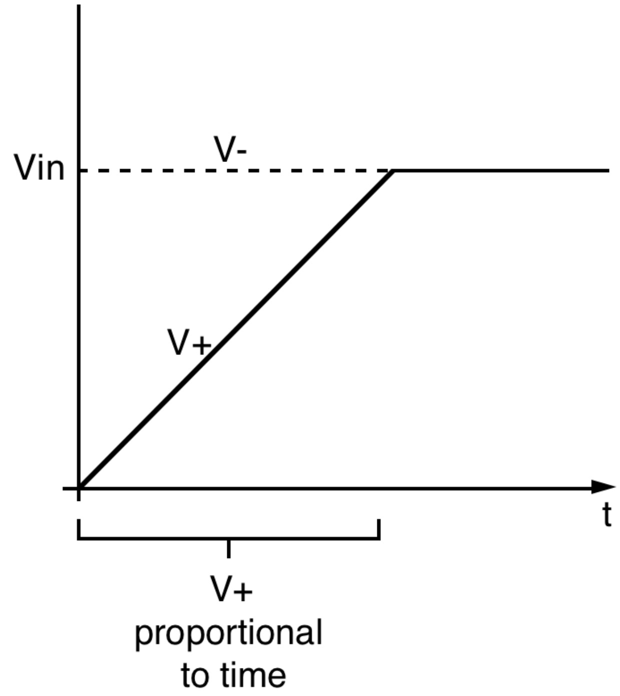
The operation of this converter is similar to the count-up converter. An integrator with constant voltage input is used to generate a linear ramp waveform to be compared with the analogue input. This is used in a similar way to the D/A converter and counter fed by a constant frequency input giving a regular staircase waveform which is compared with the analogue input.

Single-slope Schematic Diagram



Conversion Process

1) reset the counter, zero the integrator and open the switch.
2) close the switch and gate clock pulses to the counter.
3) stop the counter when the integrator voltage equals Vin.



Governing Equation

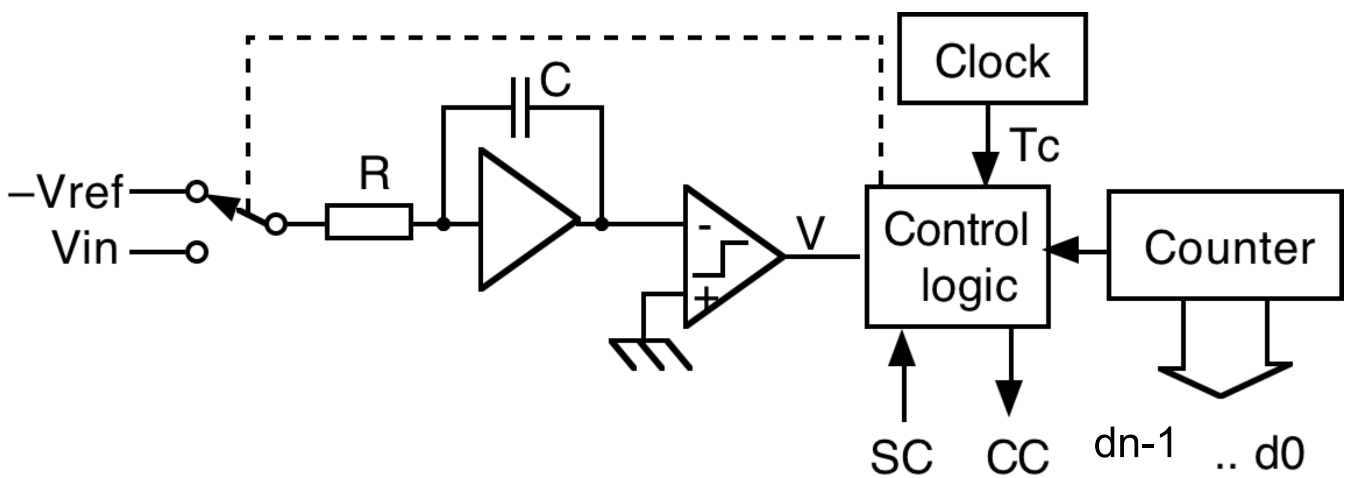
$$\mathrm{Vin} = -\frac{1}{RC}\int_0^T -\mathrm{Vref}\,dt = \frac{\mathrm{Vref}\,T}{RC}$$

Now Vref, R and C are constant and therefore the analogue input is proportional to T.

Accuracy depends upon Vref, R, C and precise measurement of time.

Dual Slope ADC

The dual slope converter is a modification to the single slope converter which aims to reduce the number of factors which influence converter accuracy.



Governing Equations

During the first phase of the conversion input voltage Vin is integrated for a fixed time Ti = Ni Tc. The resulting integrator voltage V is:

$$V = -\frac{1}{C\,R}\int_{0}^{Ti} Vin\,dt$$

The second measurement phase involves integrating the reference voltage -Vref until the integrator output returns to zero.

$$-\frac{1}{C\,R}\int_{0}^{Ti} Vin\,dt - \frac{1}{C\,R}\int_{Ti}^{Ti+Tr} -Vref\,dt = 0$$

Therefore

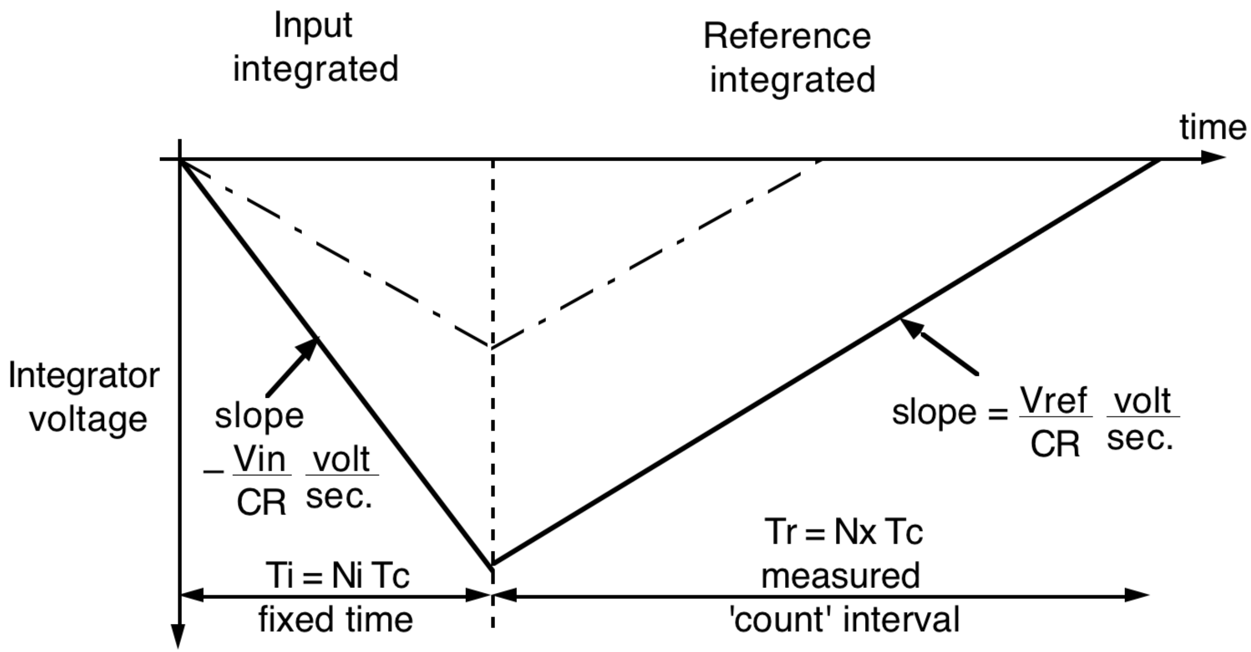
$$\int_{0}^{Ni\,Tc} Vin\,dt = Vref\,Nx\,Tc$$

If Vin is constant then:

$$Nx = \frac{Ni\,Vin}{Vref}$$

(ie Nx is proportional to Vin)

Conversion Process

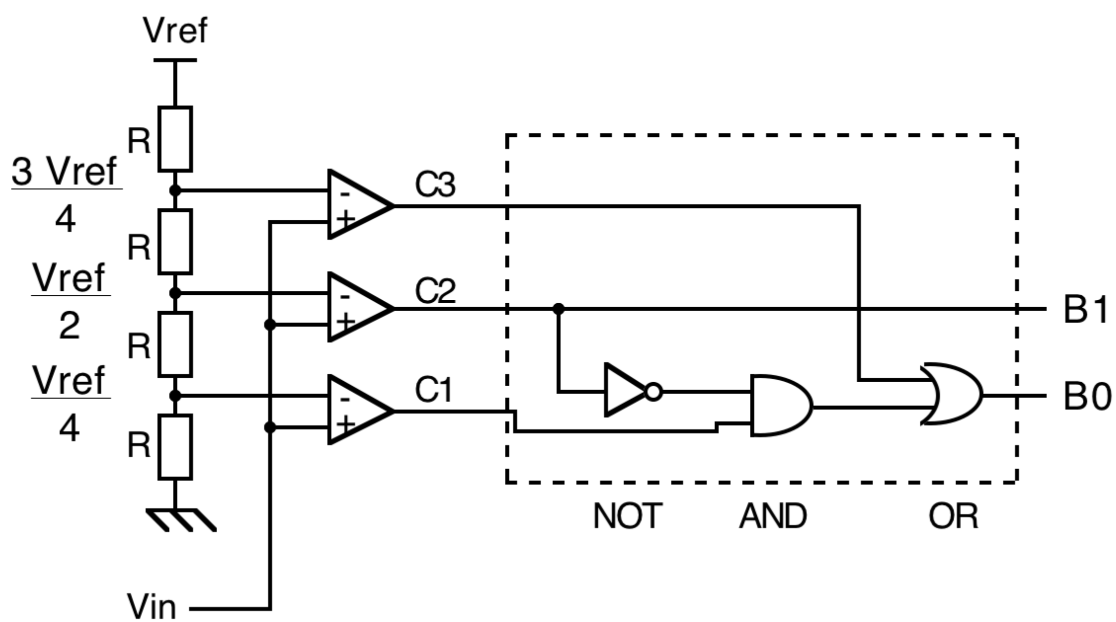


The accuracy of the dual slope converter depends on Vref and the short term stability of time measurement.

Integrating converters are relatively slow. However, because of the integration of the input they are able to reject high frequency noise (the integrator behaves like a low-pass filter). This is especially true if a whole number of noise cycles occur in the input integration period (because they integrate to zero).

Parallel Flash Converters

For digitising video signals (TV and radar pictures) the A/D converters discussed so far are too slow. A converter which duplicates circuitry in order to perform the conversion in parallel is much faster and obviously more expensive for a given resolution.



Flash Converter Operation

The parallel A/D converter compares the analogue input with different fractions of a reference voltage. The comparator outputs are a unary representation of the input voltage.

A small quantity of combinational logic converts this to the equivalent binary number.

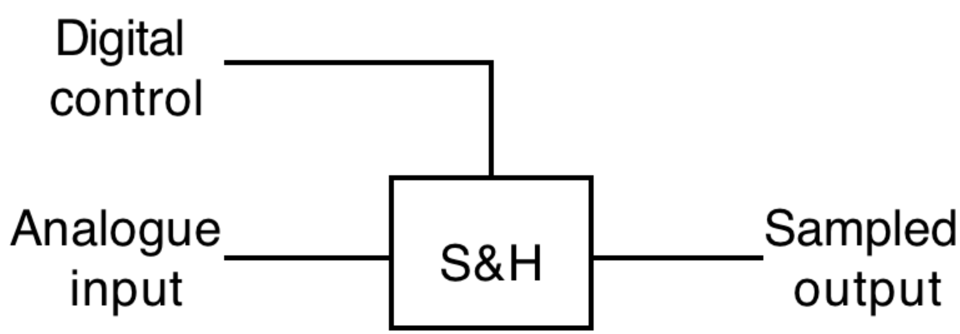
Vin	C1	C2	C3	B1	B0
$0 \rightarrow \frac{Vref}{4}$	0	0	0	0	0
$\frac{Vref}{4} \rightarrow \frac{Vref}{2}$	0	0	1	0	1
$\frac{Vref}{2} \rightarrow \frac{3\ Vref}{4}$	0	1	1	1	0
$\frac{3\ Vref}{4} \rightarrow Vref$	1	1	1	1	1

A converter with an n binary bit output requires 2^n -1 comparators and 2^n resistors.

Sample and Hold

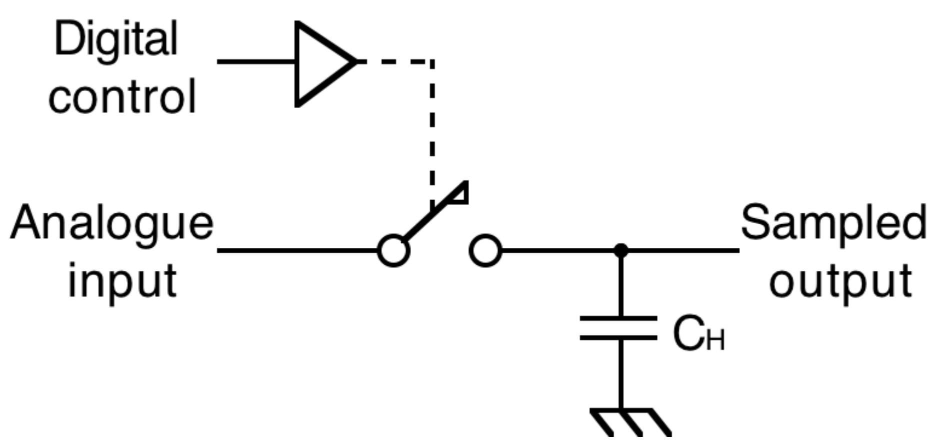
- Used on the input to ADCs to hold input steady during conversion.
- A number of analogue output channels can be generated by having many sample and hold circuits fed by a single D/A converter.

- Because the sample and hold outputs drift with time they must be regularly refreshed.

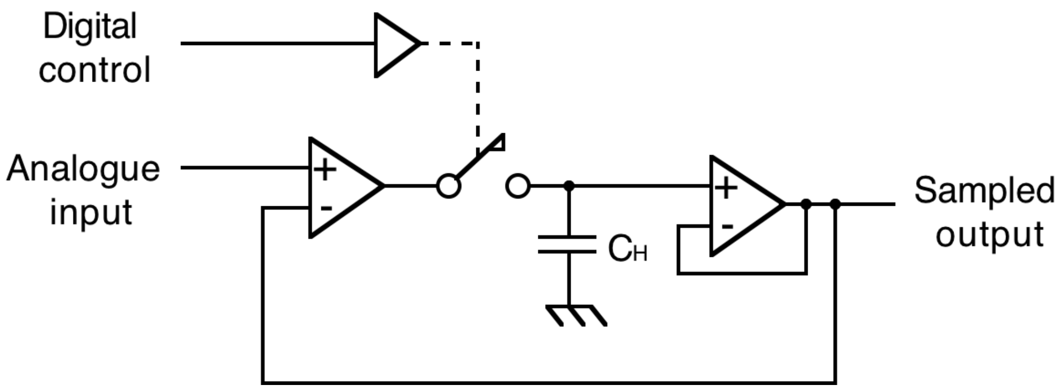


Simplified Circuit (not practical)

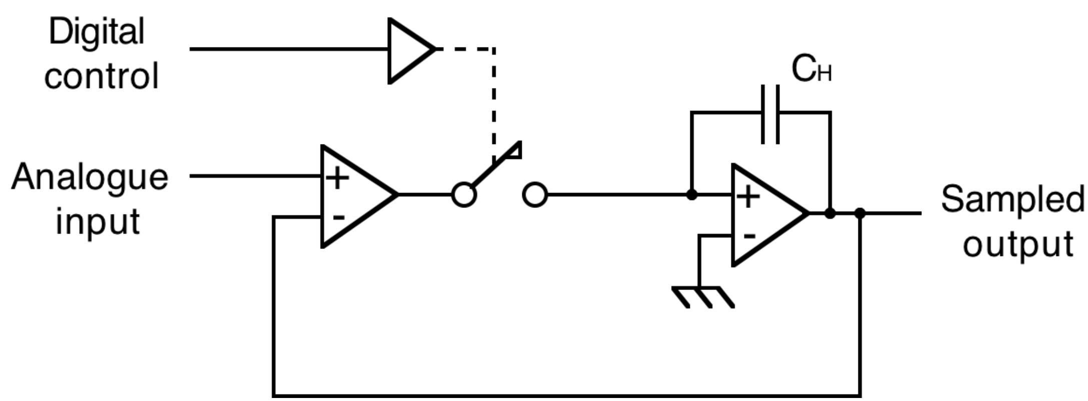
• A simple sample and hold circuit consists of an electrically controlled switch and a capacitor.
• The capacitor voltage follows the analogue input voltage until the switch opens.
• With the switch open the capacitor holds the output voltage at the value of the input just before the switch opened.
• Problems: If the analogue input comes from a high impedance source then it will take time for the capacitor to charge up to the source voltage. Unless the sampled output is connected to a very high input impedance then the capacitor will discharge quickly and not hold the required voltage.



Practical Circuits

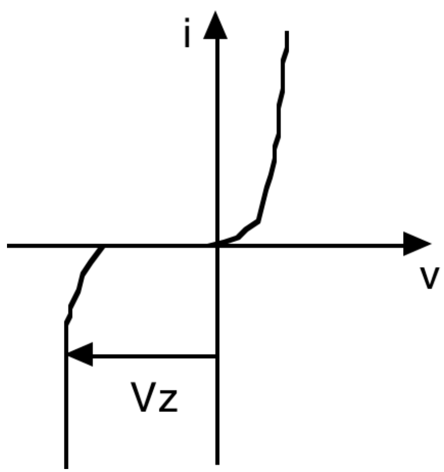


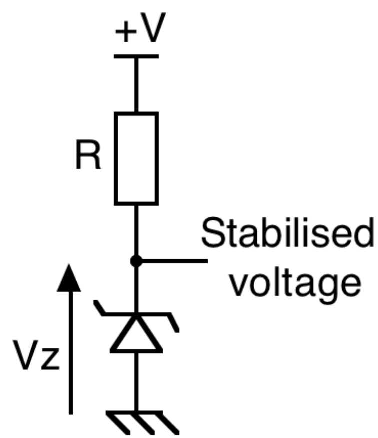
The output operational amplifiers have a high input impedance so that they do not discharge the capacitor quickly and a low output impedance to drive an external load. Feedback ensures that the whole circuit has a unity gain.



Voltage References

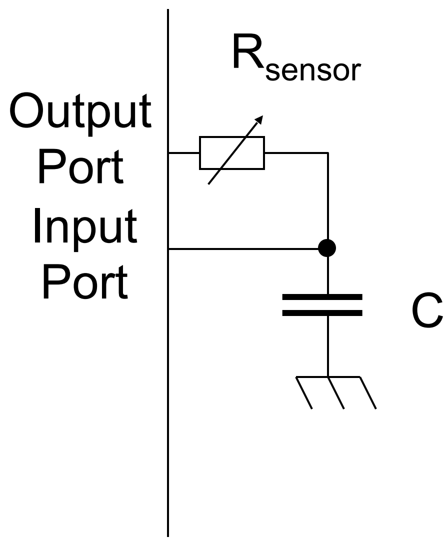
All D/A and A/D converters require a reference voltage. The most common semiconductor voltage reference is the Zenner diode:





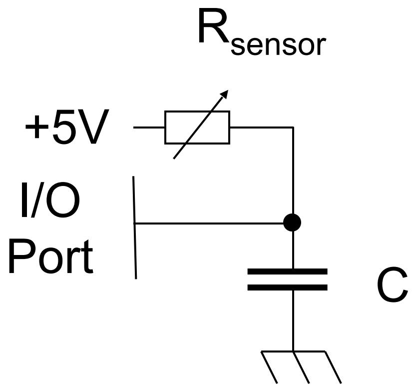
- Zenner reverse breakdown voltage Vz is quite accurate and stable
- If Vz < 6.2V breakdown is predominantly the Zenner effect which has a negative temperature coefficient.
- If Vz > 6.2V the breakdown effect is predominantly the avalanche effect which has a positive temperature coefficient.
- Temperature coefficient of these two effect cancels out at 6.2V giving good temperature stability.

Inexpensive ADC #1



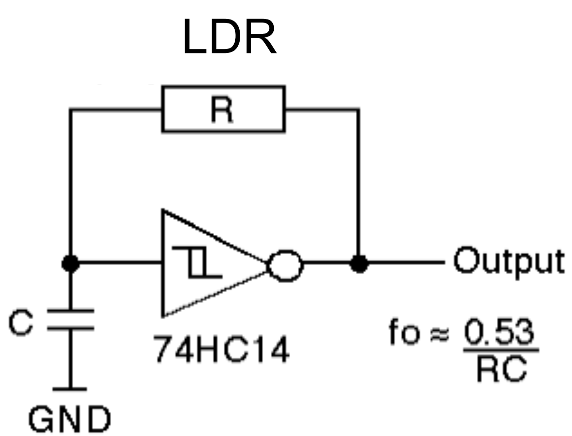
- For microcontrollers that only have dedicated digital input and output ports
- Output port outputs 0 until the capacitor is discharged
- Output port outputs 1 and the microcontroller times how long it takes for the input port to switch from 0 input to 1
- This time is proportional to the sensor resistance
- Relies on the input port switching at a well defined voltage and conversion is not linear

Inexpensive ADC #2



- I/O port switched to output and port outputs 0 until the capacitor is discharged
- I/O port switches to input and times how long it takes for the input port to switch from 0 input to 1
- This time is proportional to the sensor resistance
- As before relies on the input port switching at a well defined voltage and conversion is not linear
- Also the sensor resistance must never become so low that the I/O port cannot discharge C

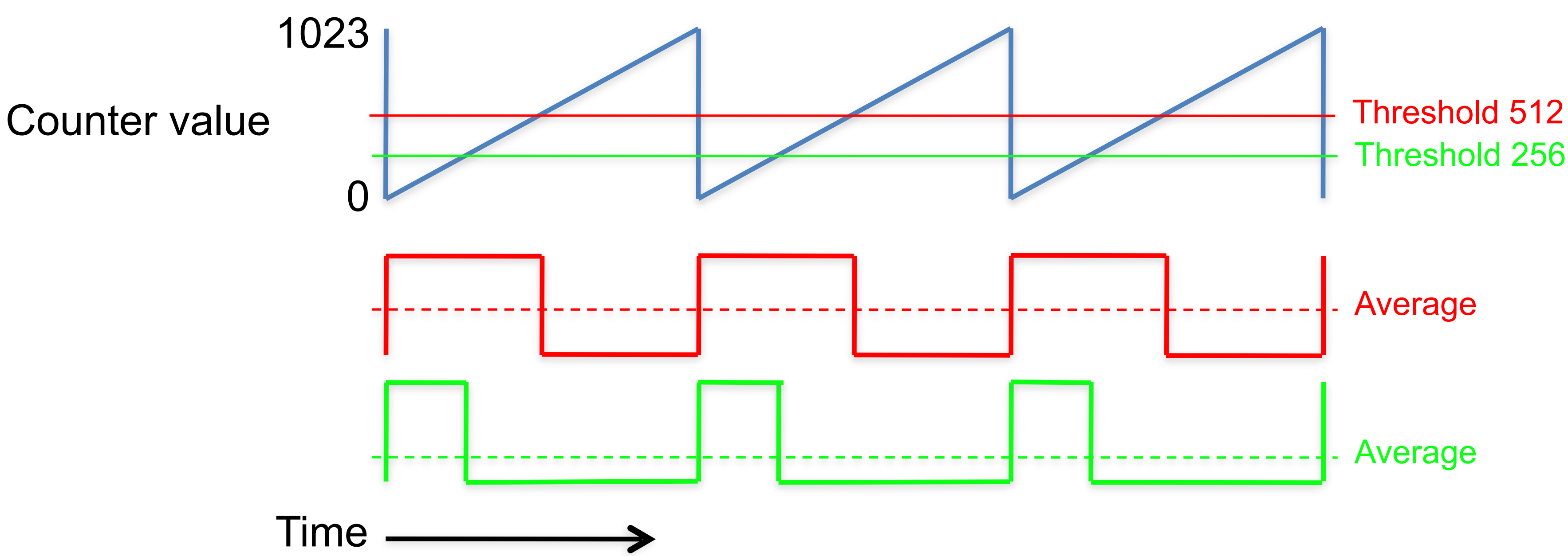
Inexpensive ADC #3



- Also for resistive sensors such as light dependent resistors a simple Schmitt oscillator can be used to measure resistance
- In this case the oscillator runs continuously and the microcontroller must measure its frequency (which is inversely proportional to resistance)

Pulse-Width Modulation

Pulse width modulation provides a means of achieving the fine control of output voltage that we would normally associate with a digital to analogue converter but instead using a simple digital system. The pulse width modulator switches a logic output with a variable mark-space ratio pulse train. When passed through a low-pass filter it produces a smoothly varying signal which can be used to control motors, play music, etc.



Next

The next part of the course will look at real-time control and real-time operating systems.