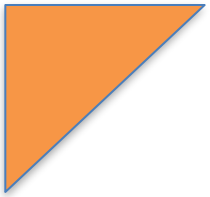


L04
Busses and Memory Systems

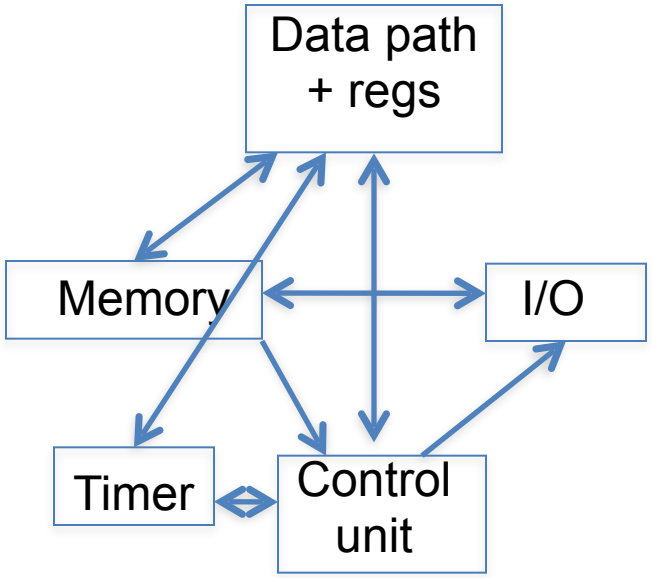
L04-1 Busses

Clive Maynard

L4 Busses and Memory Systems

Computer Internal Interconnections

Early computers had dedicated wires directly connecting the parts of the computer that required transfer of data/control. This was fast but required lots of wires and was not flexible.



L4 Busses and Memory Systems

Most modern computers interconnect their major components by means of data busses. These are usually groups of wires which transfer data in parallel. Peripheral devices such as timers, counters, pulse-width modulators, analogue to digital and digital to analogue converters are often interfaced to a computer bus system so that the computer can access them. This is particularly true of memory devices.

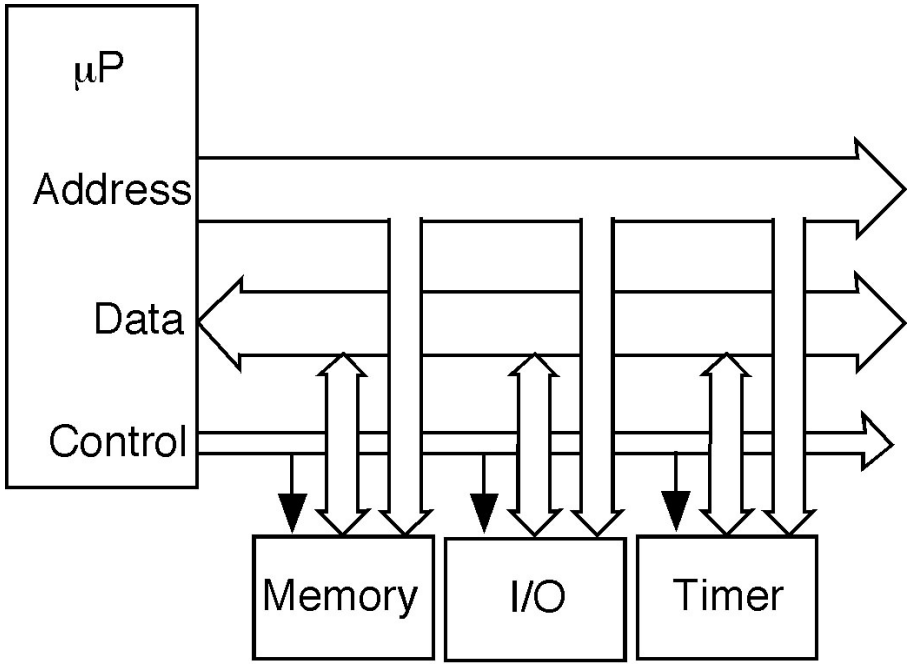
In this section we will look at bus systems and what is necessary to connect to them. There is additional information on memory devices.

This information is essential if you are building a microprocessor/ microcontroller system and need to interface additional memory/peripheral devices to the system.

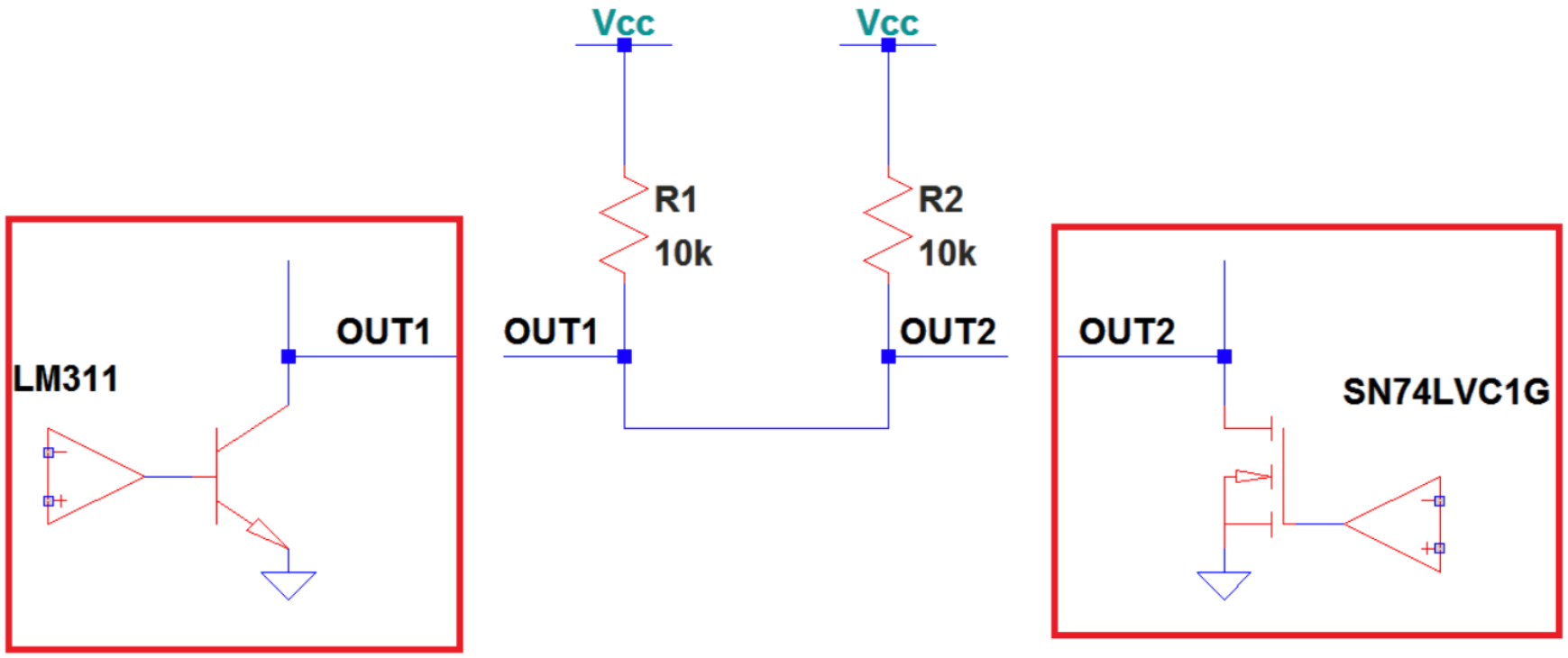
Bus Interfacing

In most modern computers peripheral circuits (memory, interface, peripheral support, etc.) are connected to the microprocessor via a parallel bus system.

Though not the first to have the idea, Digital Equipment Corp introduced the Unibus concept in 1969 and the rest is history.



Wired OR bus connections

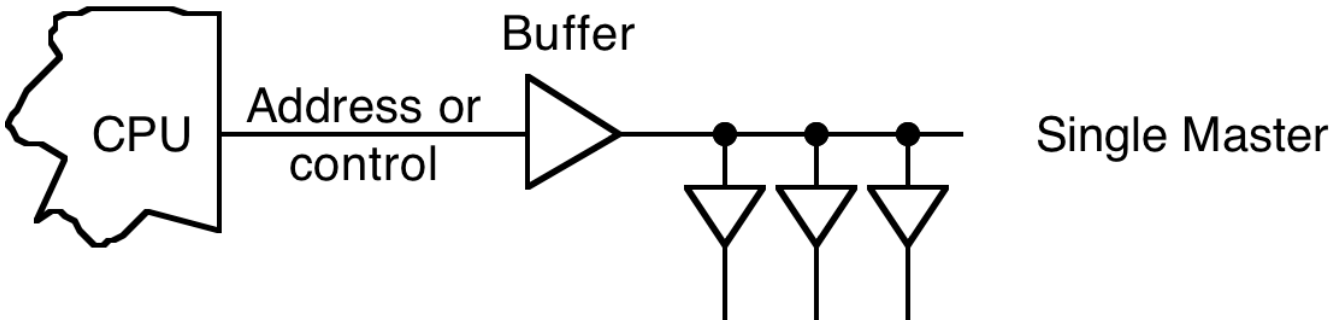


Early busses used the idea of an “open collector” with transistors to pull the signal to ground and resistors to passively pull the bus high. This was called the “Wired-OR” connection. The system was speed limited by the capacitance of the bus being charged through the pull up resistor.

External interrupt connections are still done this way

Bus architecture

For some bus lines only one device puts data on the bus but many take data from the bus. In this case the bus signal only requires buffering to drive the current required to drive the capacitance of the bus and provide the current required by the receivers.

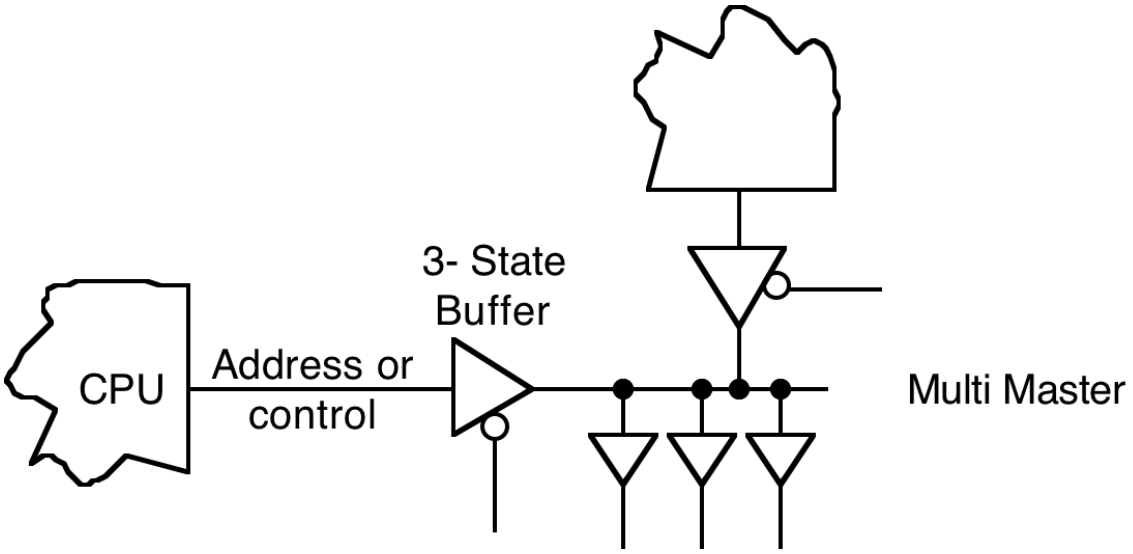


Active drive to both logic limits helped system speed but initially meant only one bus master.

Along came the tri-state buffer and multiple bus masters with active drive to both logic levels.

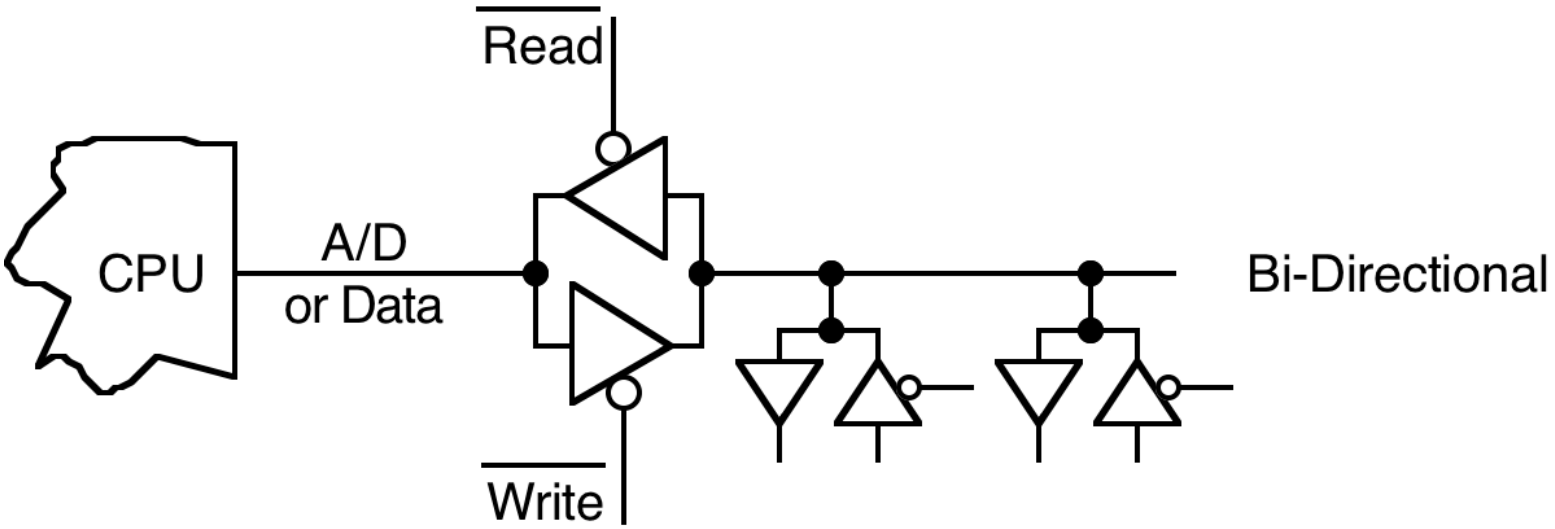
Multi-master bus

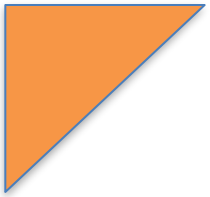
If more than one device is allowed to drive a bus line then it must be arranged that each master only drives the bus when the other master has released the bus. When not driving the bus a master must disconnect from the bus line.



Bi-Directional bus lines

If multiple master devices need to read data from a bus line as well as write to the line then bi-directional buffering is required.



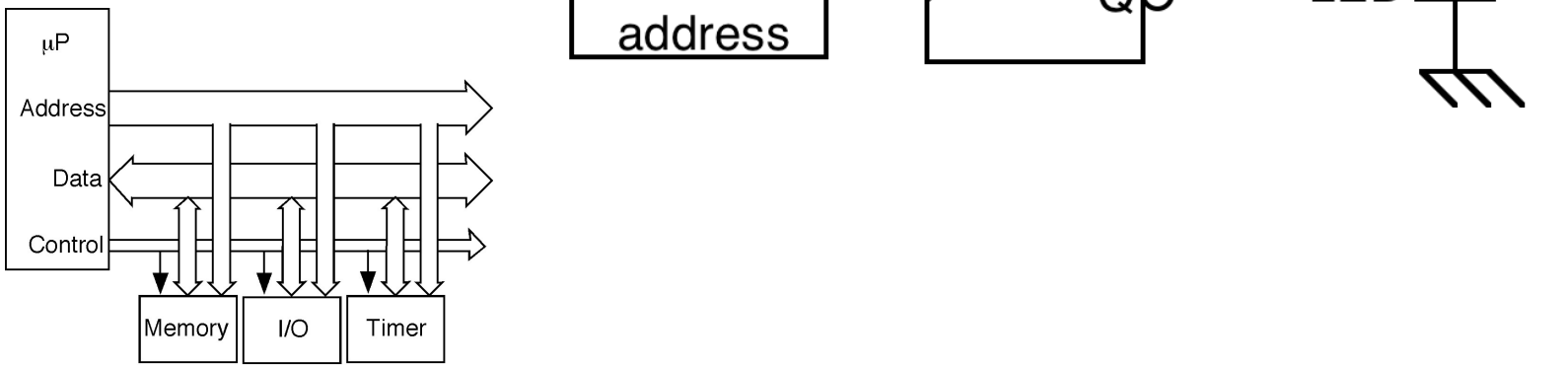


L04-2
Memory

Clive Maynard

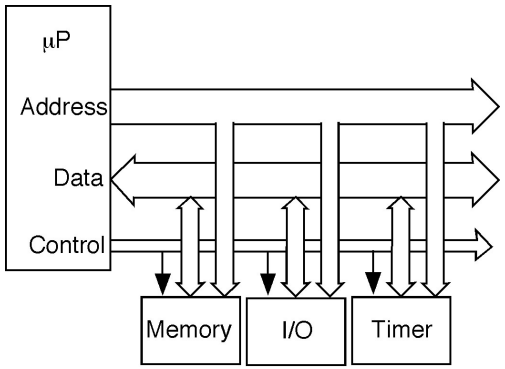
Simple Digital Output

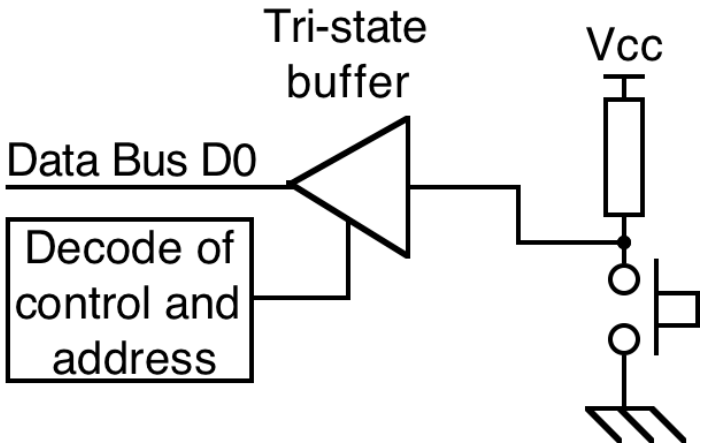
When the computer outputs a digital signal to the outside world, it appears on the computer data bus for only a short time. If we want the signal to persist for longer it must be latched into a flip-flop (perhaps to light an LED for long enough for us to see it):



Simple Digital Input

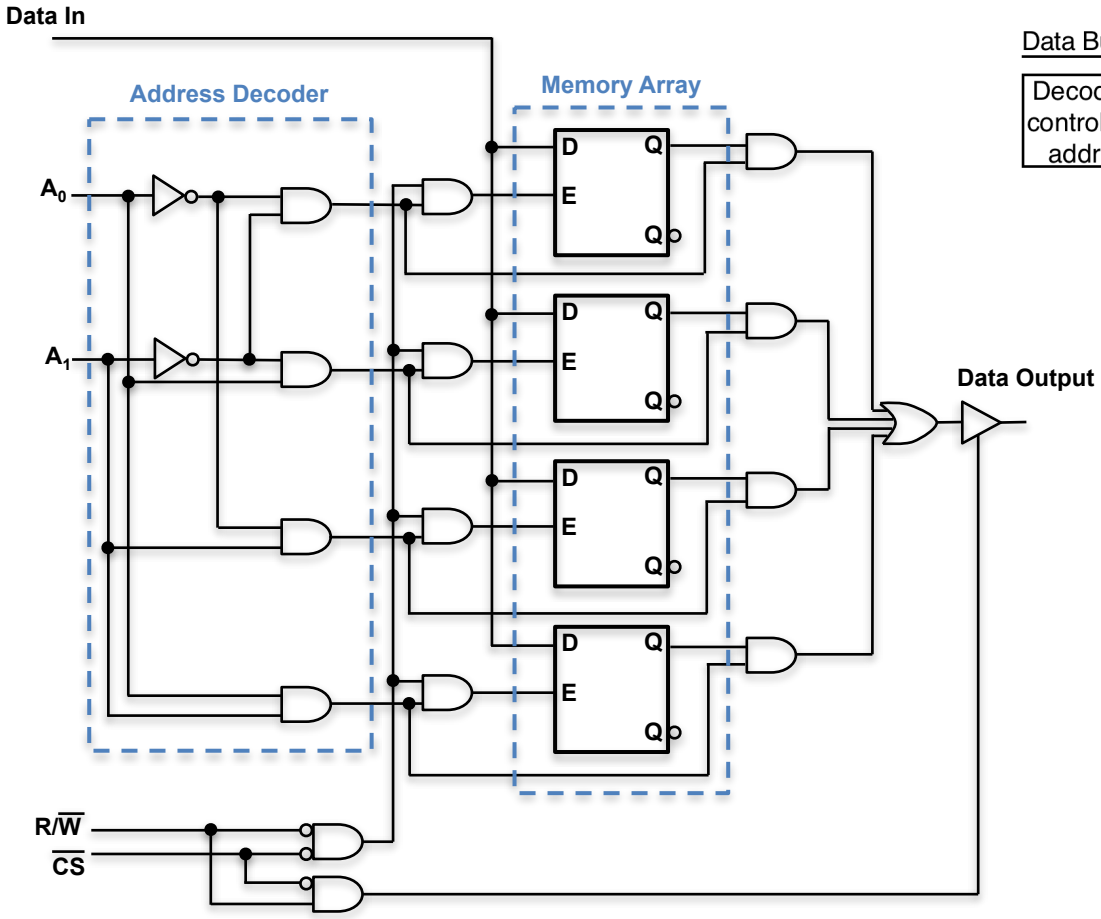
When the computer is reading a digital signal from the outside world there is only a very short timeslot during which input data will be read. A tri-state buffer can be used to allow an external signal onto the data bus for this short period:

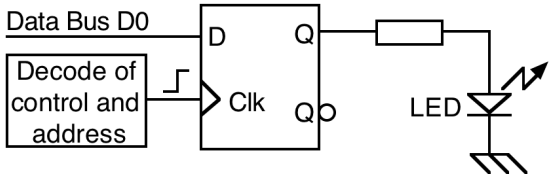


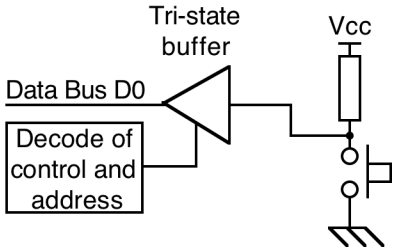


Memory and Digital I/0

Memory storage devices can be looked upon as good examples of simple digital I/O

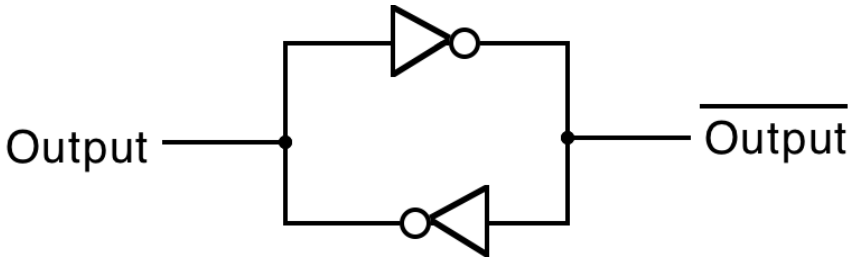






Semiconductor Memory Devices

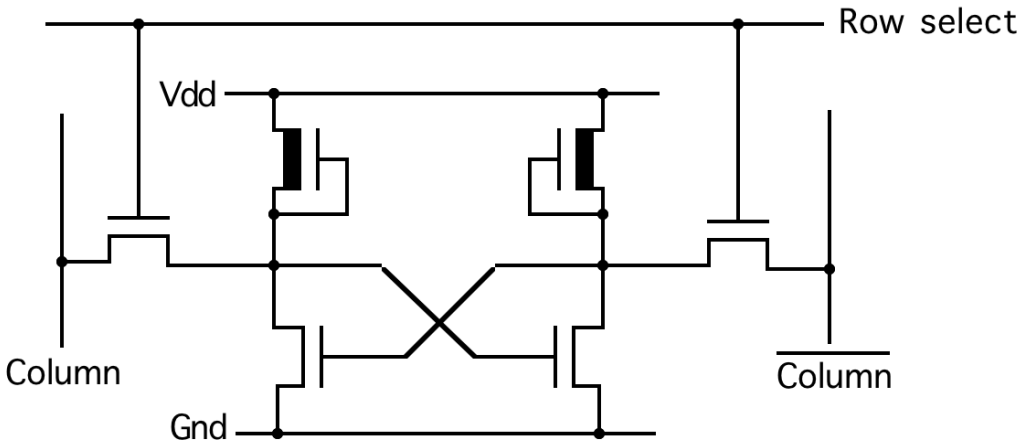
The 6-transistor static memory cell can be viewed as two inverters connected in a ring:



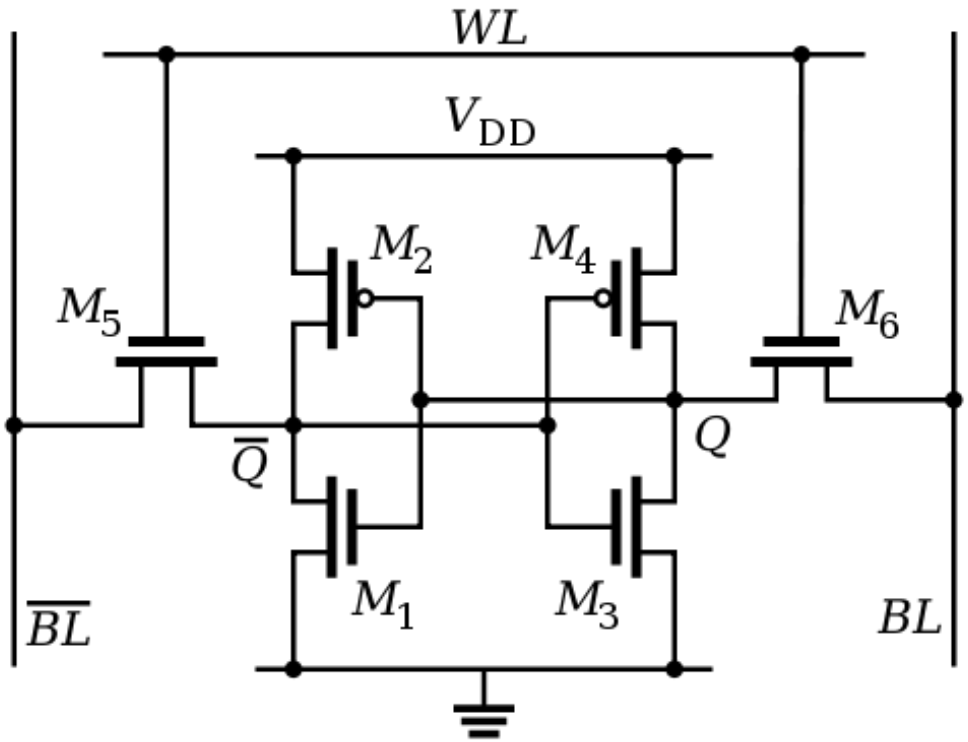
This circuit has two stable states with the output either HI or LO.

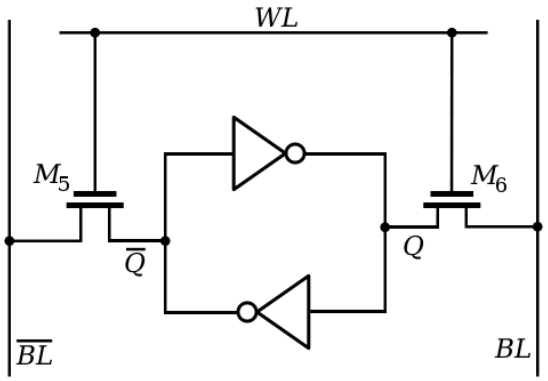
6 Transistor Static RAM Cell

In a practical circuit two pass transistors (row select) control access to one of a number of identical cells arranged in a column. Each cell can be forced into a new state by applying appropriate logic levels to the column lines and asserting row select. This circuit uses a lot of area but does not require much support circuitry.



CMOS version

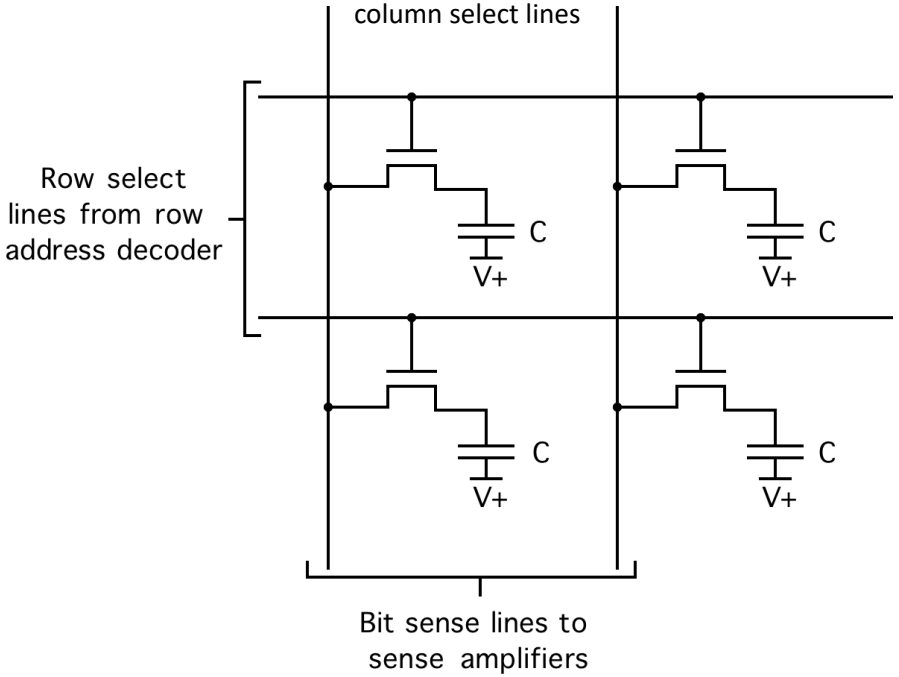




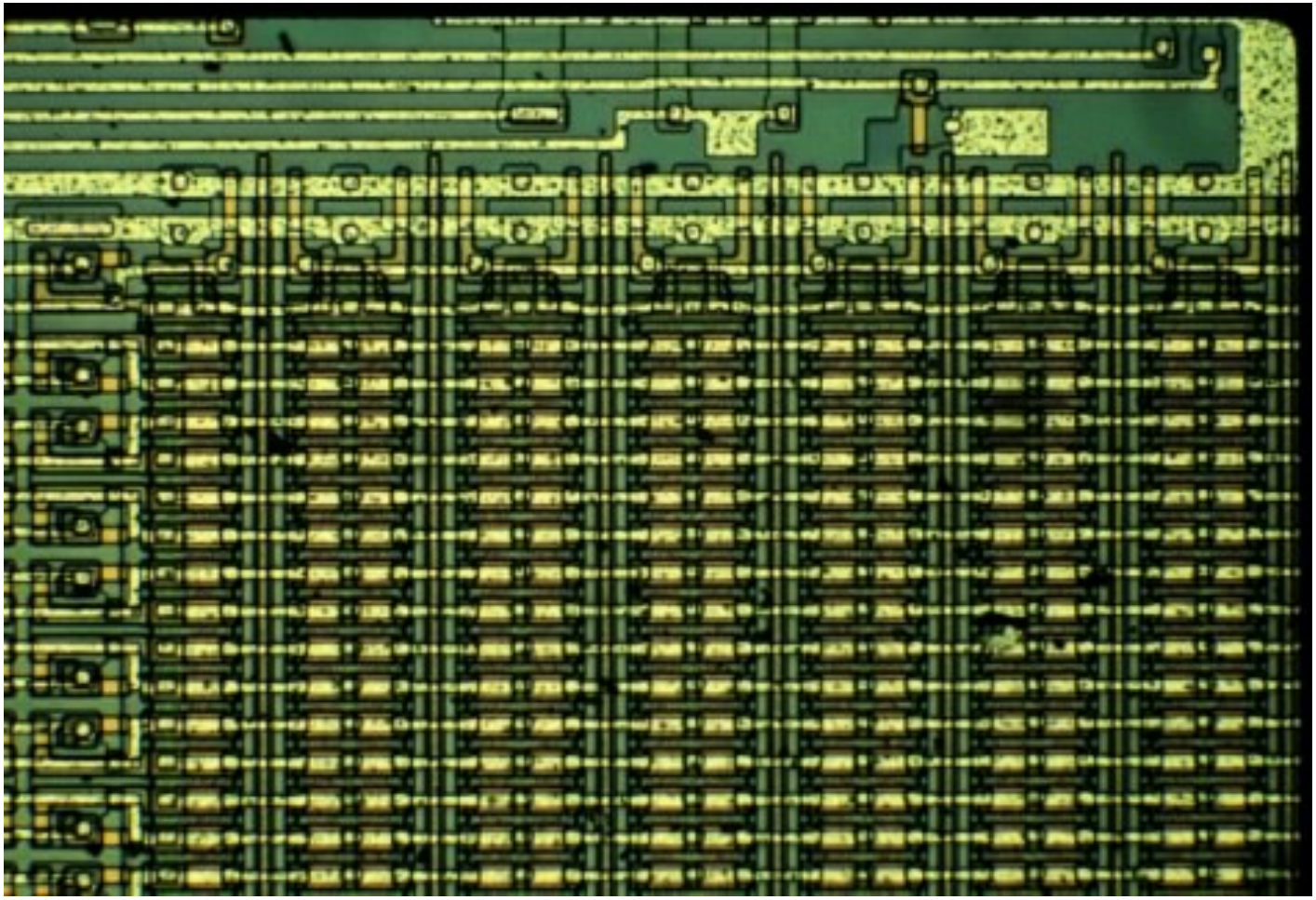
Dynamic Memory

The single transistor dynamic memory cell stores logic values as charge on a capacitor.

To charge the capacitor the logic value is placed on the column lines and the appropriate row line is asserted to switch on the pass transistor. Reading involves asserting a row line and then sensing the resulting capacitor charge which flows into the column lines. The charge is amplified and returned to the column lines to recharge the capacitors. This regenerative reading operation must be performed regularly to ensure that the capacitors do not discharge and lose the stored information.



Dynamic Memory



2116 16k by 1 bit dynamic memory

Dynamic Memory Read

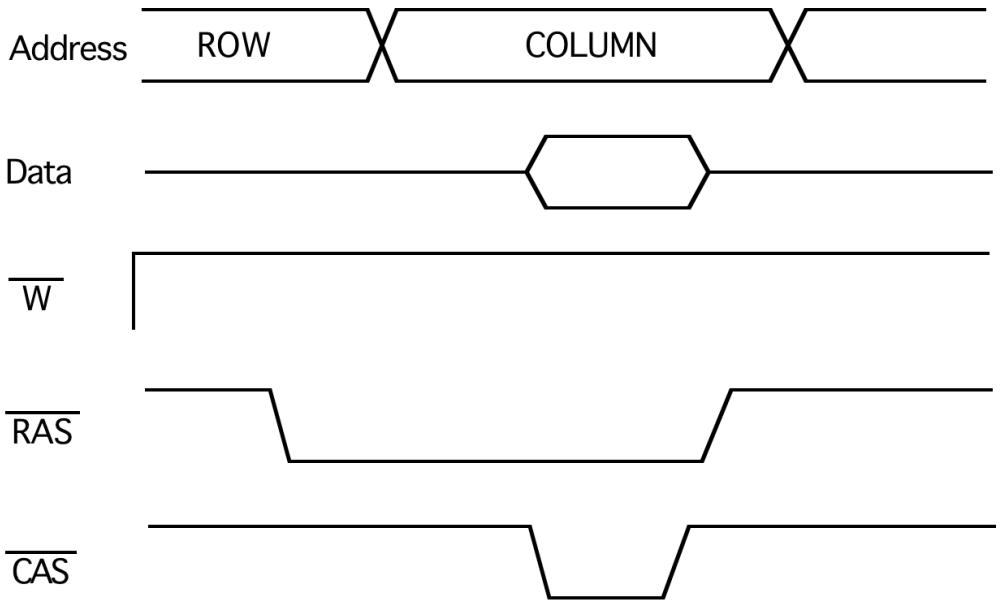
• An n-bit row address is established on the DRAM address lines.

• Row Address Strobe (L) is asserted, causing the row address decoder to select one of 2^n row lines. The 2^n transistors connected to the selected row line are switched on and transfer charge from the associated capacitor C to the column line.

• Charge for the memory cell is generatively amplified and fed back onto the column lines to re-establish the original charge on the capacitors.

• An n-bit column address is presented on the DRAM address lines.

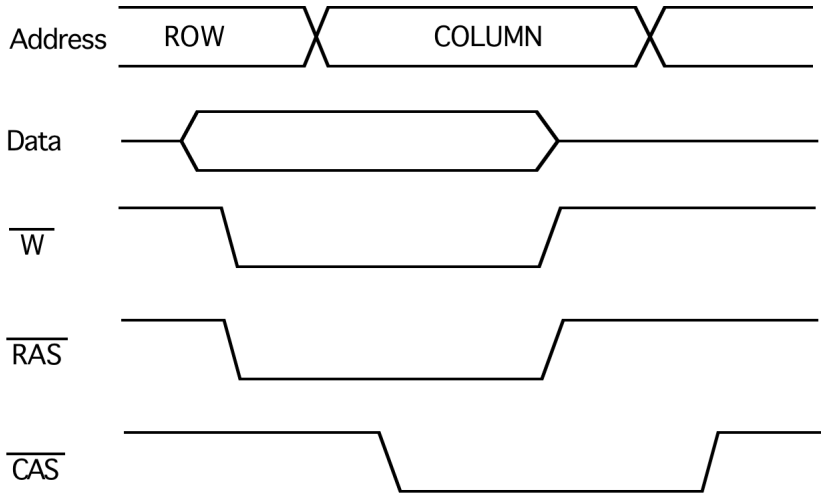
• Column Address Strobe (L) is asserted, initiating the selection of one out of 2^n column sense amplifiers and directing its output to the data out (DOUT) pin of the DRAM.



DRAM read cycle

Dynamic Memory Write

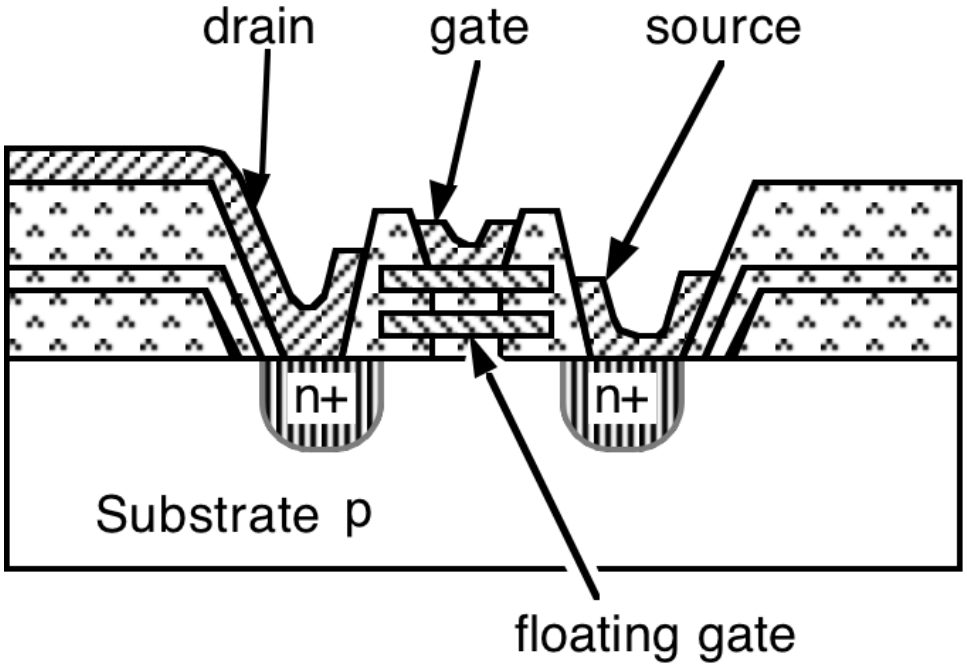
A write cycle follows the same process as the read cycle except that when the column amplifier is selected data from the data in (DIN) pin is routed to that amplifier and hence to the appropriate memory cell.



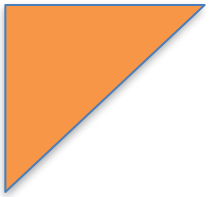
DRAM write cycle

EPROM

Most EPROMs and erasable programmable logic arrays (PLAs, EPLDs etc.) use floating gate (FAMOS) transistors as shown here.

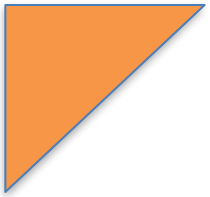


The FAMOS transistor is similar to a normal field effect transistor except that it has an additional floating (not electrically connected to anything) gate between the normal gate and transistor channel. When the floating gate is not charged up it has no effect and the transistor can be switched on by a positive voltage on the gate.



L04-3
Address Decoding

Clive Maynard



Address Decoding

In order to enable a peripheral circuit (memory, I/O or timer, etc.) logic must monitor the address and control lines.

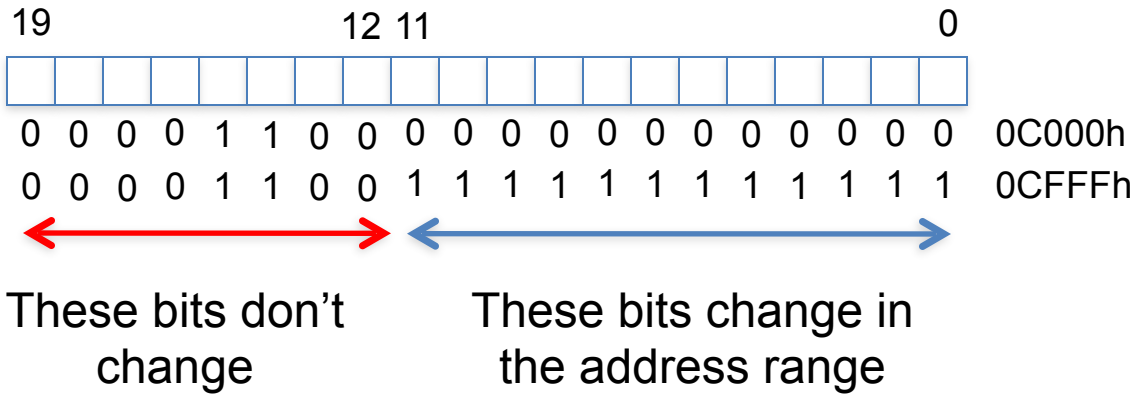
A chip select signal is generated when an address is detected in the appropriate range reserved for the peripheral circuit.

This may also be conditional on the appropriate control signals being present also.

Address decoding is performed by simple combinational logic.

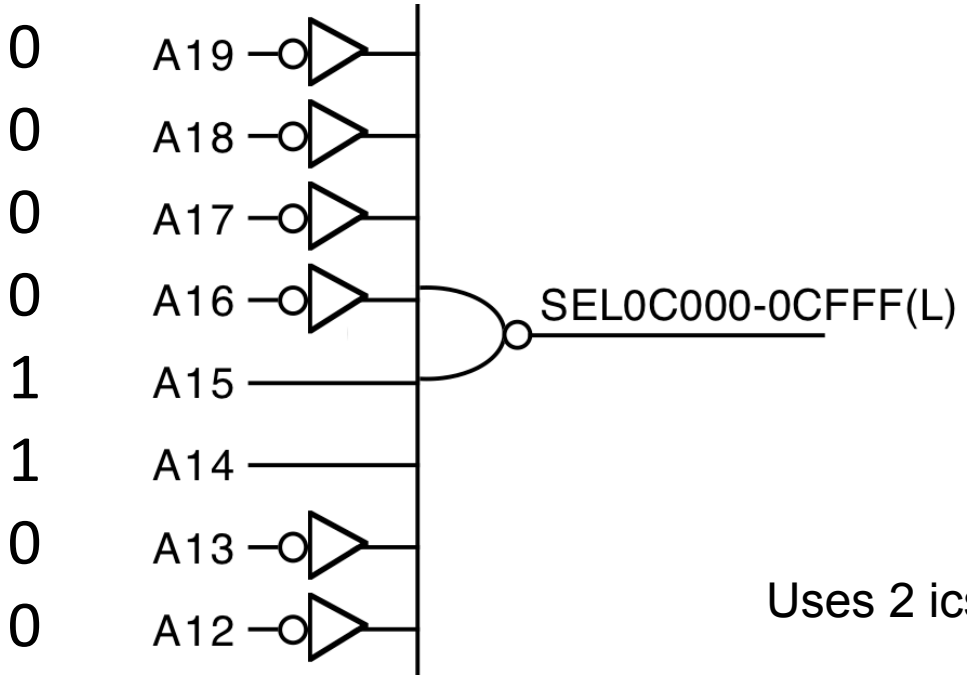
Example

Design address decoding logic which generates a chip select output asserted low when an address in the range 0C000h to 0CFFFh is detected. A 20-bit address bus is being considered and the output signal is being used to drive a memory chip which itself includes additional address decoding logic to complete the full decode of the 20 address bits and take into account the read and write control lines.



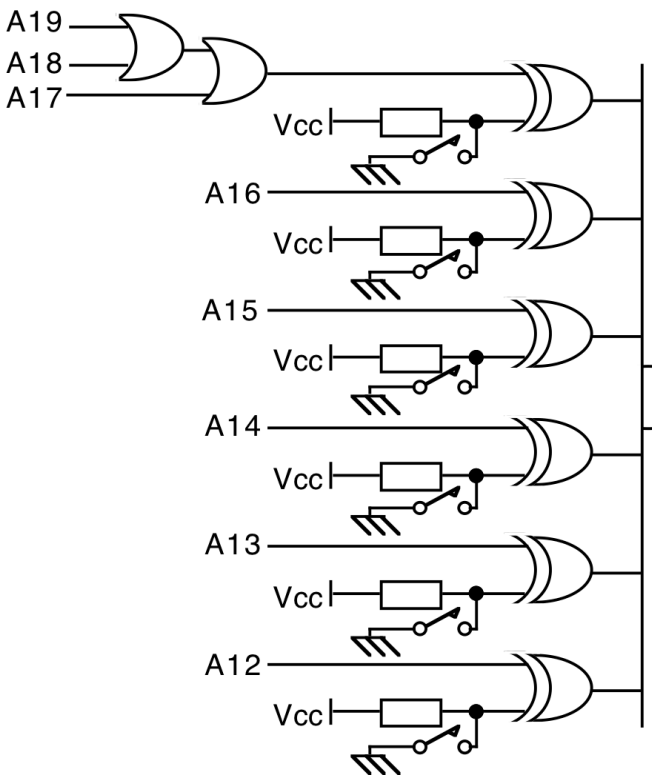
Random Logic

Bits 0 to 11 go straight to the memory chips and therefore bits 12 to 19 must be decoded to provide the chip select. In practice there are several solutions, each with advantages and disadvantages:



Switchable

This circuit uses a digital comparator to compare the upper bits of the address bus with a bit pattern set by switches (in this case). The selected address range can be readily changed by altering the switch settings:



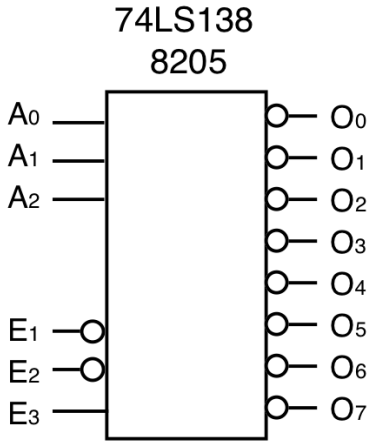
Switch values

1
1
0
0
1
1

Uses 1.5 ics + switches, etc.

Decoder

This circuit provides up to eight chip select signals to control a number of banks of memory circuits. Characteristics for the decoder are shown below:

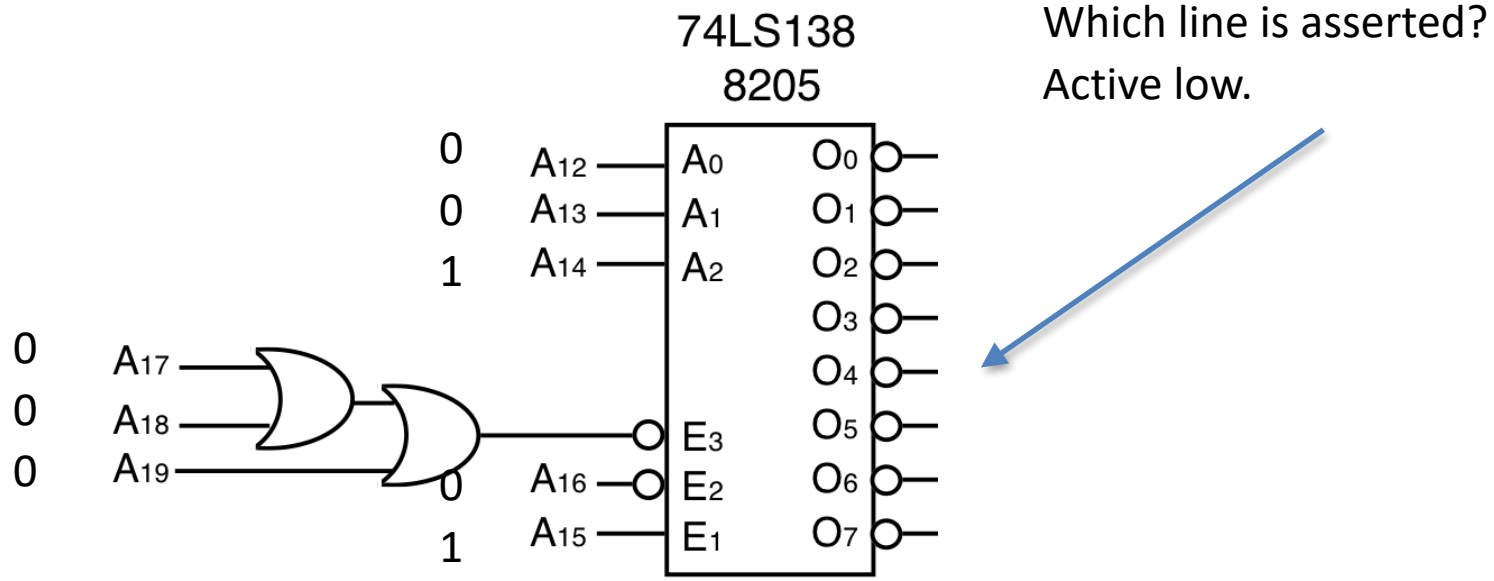


ADDR			ENABLE			OUTPUTS							
A_0	A_1	A_2	E_1	E_2	E_3	0	1	2	3	4	5	6	7
L	L	L	L	L	H	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	L	H	H	H	L	H	H	H	H	H
H	H	L	L	L	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
H	L	H	L	L	H	H	H	H	H	H	L	H	H
L	H	H	L	L	H	H	H	H	H	H	H	L	H
H	H	H	L	L	H	H	H	H	H	H	H	H	L
X	X	X	L	L	L	H	H	H	H	H	H	H	H
X	X	X	H	L	L	H	H	H	H	H	H	H	H
X	X	X	L	H	L	H	H	H	H	H	H	H	H
X	X	X	H	H	L	H	H	H	H	H	H	H	H
X	X	X	H	L	H	H	H	H	H	H	H	H	H
X	X	X	L	H	H	H	H	H	H	H	H	H	H
X	X	X	H	H	H	H	H	H	H	H	H	H	H

Uses 1.5 ics and can enable 8 banks of memory

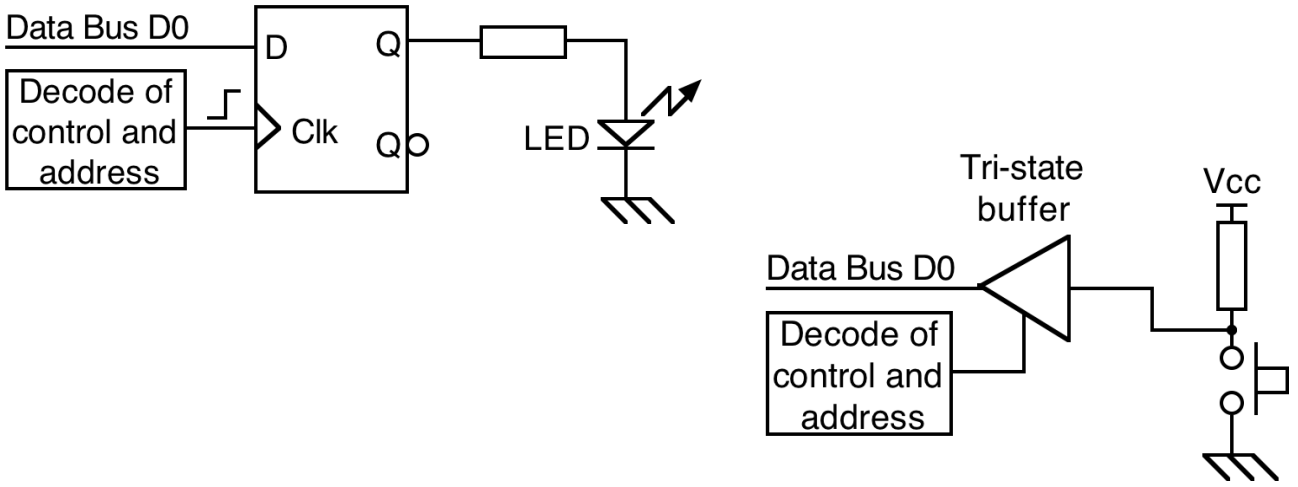
Decoder Solution

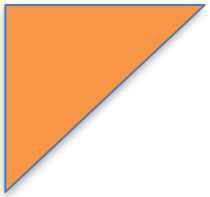
Only one output can be asserted at a time as selected by the address inputs. No output will be asserted until the chip is enabled by correctly asserting the three enable inputs.



Simple Digital I/O Again

If we did want to interface individual D flip-flops as digital outputs or tri-state buffers as digital inputs then the decoded chip select signal would have to monitor all of the microprocessor address lines and also be conditional on the appropriate write or read control signal.



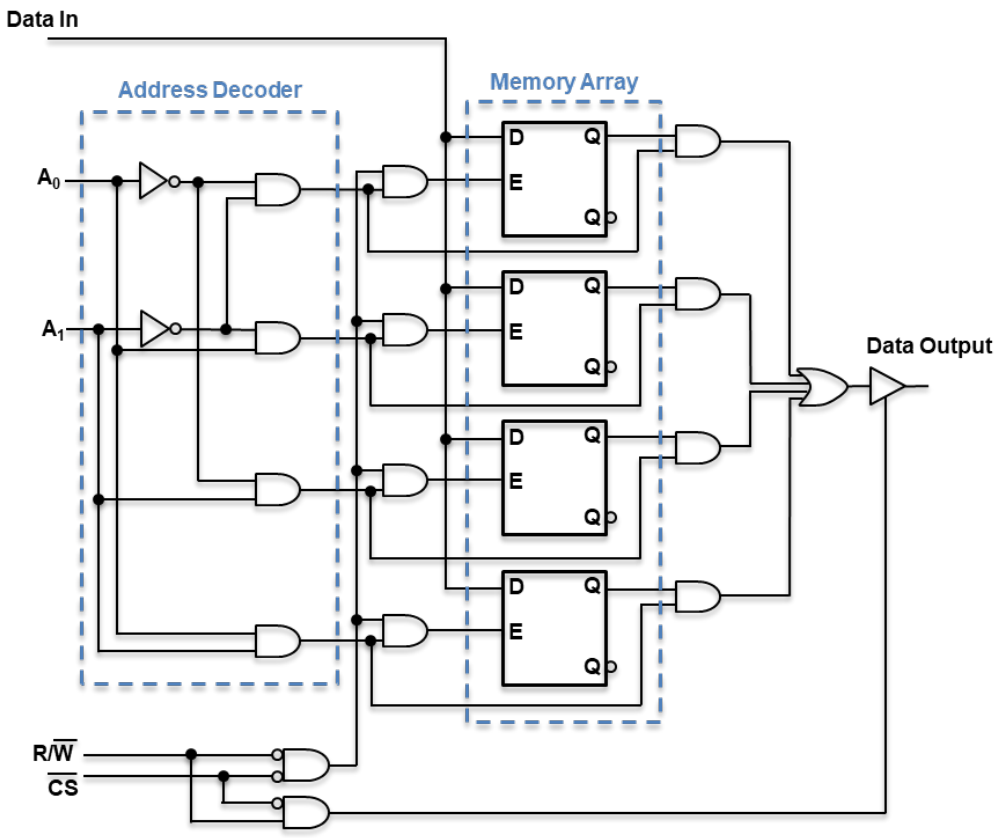


Memory Fold-over

Memory fold-over is the effect of not decoding a particular address line. The effect of this is to turn that address bit into a “don’t care”. In practice the peripheral device will be addressed twice - once when the “don’t care” address bit is low and once when it is high.

For instance, for a 20-bit address if address bit A19 is not decoded then reading/writing from/to address 0x00000, 0x00001... will have the same effect as doing the same operation with address 0x80000, 0x80001..., etc. The extra image of the addressed memory/peripheral is called a phantom. Sometimes incomplete decoding is done to save address decoding logic but care must be taken to ensure that the resulting phantoms do not clash with other memory/ peripheral devices.

Memory, An Example of Digital I/O



This diagram shows a simplified 4 by 1 memory circuit.

- Two address lines select one of the four memory cells and this logic function is performed by the address decoder.
- If the chip is selected and a write is performed then the contents of the addressed memory element is changed to the value on the Data In line.
- If a read is performed then the contents of the addressed memory element is allowed onto the data bus via a tri-state buffer (Data Output).