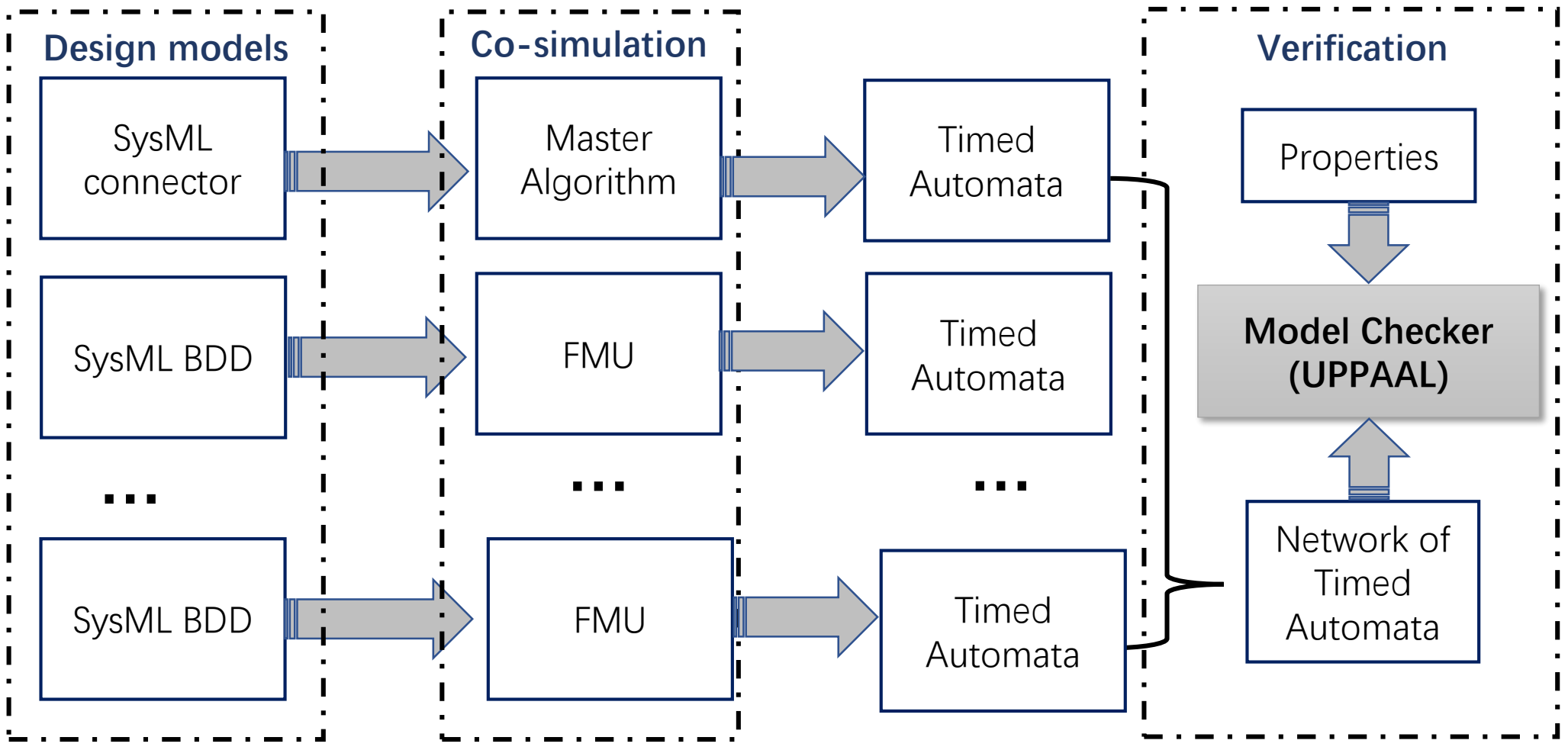
Design models
SysML connector
SysML BDD
...
SysML BDD
Co-simulation
Master Algorithm
FMU
...
FMU
Timed Automata
Timed Automata
...
Timed Automata
Verification
Properties
Model Checker (UPPAAL)
Network of Timed Automata