

# SRAM Array Structures for Energy Efficiency Enhancement

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**Abstract**—Energy efficiency is a supreme design concern in many ultralow-power applications. In such applications, static random-access memory (SRAM) plays a significant role in energy consumption due to the high density for evermore increased computing power. This brief explores and analyzes SRAM array structures for energy efficiency improvement. In contrast to the traditional practices where SRAM arrays enclose more rows than columns, this work reveals that better SRAM energy efficiencies can be achieved with a wider SRAM array structure with fewer rows than columns particularly at low supply voltage. The analysis shows that the array structure optimization can improve the energy efficiency up to 38% (64 kbit) and 10% (8 kbit) for the same SRAM bit density and the same supply voltage.

**Index Terms**—Eight-transistor (8T) static random-access memory (SRAM), energy efficiency, minimum energy, SRAM.

## I. INTRODUCTION

HIGH ENERGY efficiency is a paramount design constraint in many ultralow-power applications such as portable electronic devices, wireless sensor nodes, and implantable biomedical devices [1]. In these applications, static random-access memory (SRAM) plays a key role in energy consumption due to the high cell density for computational power improvements. One of the most popular ways of obtaining minimum energy consumption is to lower supply voltage around or below the device threshold voltage [2]–[4]. However, lowering supply voltage generates various design issues. Degradation in cell stability, noise margin, on-current-to-off-current ratio, and strong sensitivity to process–voltage–temperature variations have to be carefully handled for reliable operation [3]. Designing of SRAM in this operation region has been observed to be more challenging due to additional design constraints compared to generic digital logic, and so, various circuit techniques have been published with successful hardware measurements [2], [3]. Decoupled SRAM cells have been popularly deployed for improving cell stability [3]. Write margin issues have been tackled through several techniques using positively or negatively boosted voltage, strengthening the write access transistors utilizing channel length modulation, and collapsed supply voltage [4]–[6].

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In addition to supply voltage, SRAM array structures also influence energy consumption. Evans and Franzon [7] conducted an investigation of the array structures for optimum energy consumption. In their work, the optimum SRAM array structures for minimized energy consumption were found to be nonsquare and had more rows than columns, while the optimum array structures for minimizing the memory access time were squarer than those for the minimum energy consumption. However, this work only focused on the high-performance region where the static energy from the leakage current is insignificant compared to the dynamic energy. At ultralow supply voltage, the static energy becomes comparable to the dynamic energy [4], which requires the optimal SRAM array structure to be revisited.

In this brief, we analyze SRAM array structures for energy efficiency enhancement for ultralow-power systems. A parameter-based modeling methodology is used employing a characterization model to capture timing and parasitics extracted from the cell layout. Commercial 65-nm low-power CMOS process technology is used for simulation. In Section II, we explain voltage scaling and its effects on SRAM and eight-transistor (8T)-SRAM subarray under consideration and SRAM energy modeling. In Section III, we analytically derive optimal SRAM array structures and analyze the effects of SRAM array structural change on energy consumption. Finally, Section IV summarizes and concludes this work.

## II. 8T-SRAM ARRAY STRUCTURE AND ENERGY ESTIMATION

In this section, we will discuss the effect of voltage scaling on SRAM, the structure of 8T SRAM, and the analytical modeling of different design parameters that play a key role in determining the total energy of SRAM. We selected 8T SRAM for our energy analysis, and the following section explains the reason behind this selection.

### A. Supply Voltage ( $V_{DD}$ ) Scaling Effect on SRAM

Supply voltage is a critical parameter in minimizing the SRAM energy. SRAM for ultralow energy consumption has been explored for various recently emerging applications where performance can be mitigated for higher energy efficiency. Studies have demonstrated that subthreshold or near-threshold circuits achieve minimum energy consumption [3], [4]. Thus, SRAM design techniques for low operating voltage have been explored, generally following the traditional SRAM organizing practice of having more rows than columns [7]. Research works on optimal SRAM array structures for energy minimization have been rarely conducted. Considering the increased SRAM

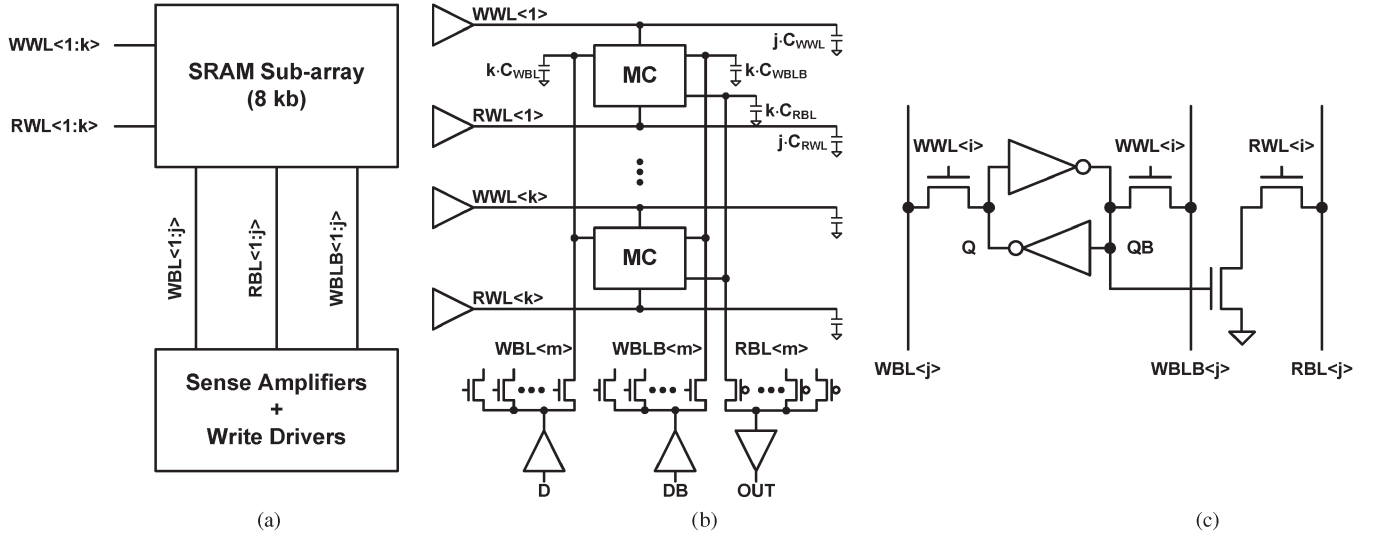


Fig. 1. (a) Eight-kilobit SRAM subarray for energy analysis. Note that  $k \times j$  is 8 kbit. (b) Bitline structure of the SRAM subarray in (a). (c) Schematic of the conventional 8T SRAM cell used in this work.

density in ultralow-energy applications, it is highly necessary to revisit SRAM array structures for better energy efficiency, as CMOS technology development is advancing the scope of voltage scaling which is a simple and widely used technique for energy efficiency enhancement. Both the dynamic energy associated with the accessed wordline and bitline and the static leakage energy are strongly affected by the supply voltage [4]. In the supply voltage region where the dynamic energy is a dominant component, lowering supply voltage decreases the total SRAM energy. However, as the supply voltage comes around or below the threshold voltage, lowering supply voltage is not much effective in the energy minimization due to the increase in the static energy. This is caused by the exponentially increased delay. Consequently, the minimum energy point is found where the supply voltage is around the device threshold voltage.

However, designing six-transistor SRAM cells operating in this region faces various challenges, one of which is the cell stability during read operation. The separated read port in the 8T SRAM cell in Fig. 1(c) overcomes the stability-related limitations of 6T SRAM cells, which makes the 8T SRAM cell a promising candidate for such low voltage levels [8]–[12]. An 8T SRAM cell is used in the subarray for our simulations since it has been widely employed for ultralow-voltage operation [8], [9], [13], [14].

### B. 8T-SRAM Subarray

An 8-kbit SRAM subarray structure for energy analysis is shown in Fig. 1(a). The number of rows ( $k$ ) and that of columns ( $j$ ) can be changed while their product remains constant. In high-performance applications, they have been mainly selected to meet the system performance requirement. However, in the SRAMs for ultralow-power applications, the array structures are limited by additional design parameter such as cell stability, read bitline sensing margin, and leakage current. A bitline structure employing the conventional 8T SRAM cell [Fig. 1(c)] and including related parameters in the wordlines and the bitlines is illustrated in Fig. 1(b).

### C. SRAM Energy Model

In this section, we will model the energy components in the SRAM subarray structure in Fig. 1. Using the parameters in Fig. 1(b), the read energy ( $E_{\text{total\_read}}$ ) and the write energy ( $E_{\text{total\_write}}$ ) of the SRAM subarray can be written as

$$E_{\text{total\_read}} = j \times k \times I_{l\_cell} \times t \times V_{DD} + (j \times C_{RWL} \times V_{DD}^2 + k \times 0.5 C_{RBL} \times V_{DD}^2) \quad (1)$$

$$E_{\text{total\_write}} = j \times k \times I_{l\_cell} \times t \times V_{DD} + (j \times C_{WWL} \times V_{DD}^2 + k \times C_{WBL} \times V_{DD}^2) \quad (2)$$

Here,  $k$  is the number of rows,  $j$  is the number of columns,  $I_{l\_cell}$  is the leakage current in an SRAM cell,  $t$  is the cycle time ( $T_{\text{cyc}}$ ) of the SRAM,  $C_{RWL}$  is the read wordline capacitance per cell,  $C_{RBL}$  is the read bitline capacitance per cell,  $C_{WWL}$  is the write wordline capacitance per cell,  $C_{WBL}$  is the write bitline capacitance per cell, and  $V_{DD}$  is the supply voltage. In the read energy equation, it is assumed that the probabilities of data “1” and those of data “0” are equal and are 0.5. The dynamic energy component is mainly determined by the wordline capacitance and the bitline capacitance, while the static energy component coming from the leakage current is determined by the memory density. The effects of the read and write operations on the leakage current of the accessed row and column are insignificant. Thus, they are neglected in the energy estimation.  $E_{\text{total\_read}}$  and  $E_{\text{total\_write}}$  can be merged into the total SRAM energy ( $E_{\text{total}}$ ) by including the probability of the read operation ( $P_r$ ) and that of the write operation ( $P_w$ ), which is given by

$$E_{\text{total}} = j \times k \times I_{l\_cell} \times t \times V_{DD} + P_r (j \times C_{RWL} \times V_{DD}^2 + k \times 0.5 C_{RBL} \times V_{DD}^2) + P_w (j \times C_{WWL} \times V_{DD}^2 + k \times C_{WBL} \times V_{DD}^2) \quad (3)$$

As shown in (3), SRAM energy is a function of multiple variables such as supply voltage, capacitance, performance, temperature, workload, and organization. SRAM energy minimization has to be conducted while considering all the aforementioned components carefully.

### III. ANALYSIS OF SRAM ARRAY STRUCTURES FOR ENERGY EFFICIENCY IMPROVEMENT

A sample SRAM subarray, as shown in Fig. 1, is used for the analysis of minimum energy-driven SRAM array structure. An SRAM subarray with the density of 8 kbit is assumed while the number of rows ( $k$ ) and that of columns ( $j$ ) vary. Due to the fixed number of input/outputs, column multiplexing ratios are automatically generated once  $k$  and  $j$  are known. The clock cycle time ( $T_{\text{cyc}}$ ) is assumed to be two times of the read delay ( $T_{\text{ltc}}$ ) including bitline precharging operation. Since each SRAM array structure will generate a different clock cycle time, each generated clock will be used for energy estimation.

#### A. Effect of SRAM Array Structure on Energy

In this section, the energy components (i.e., static energy and dynamic energy) of the SRAM are explained for determining the significance of each component on the energy minimization.

At a given supply level, changing SRAM array structures can also affect the SRAM energy. As shown in (3), dynamic energy is changed by  $j$  and  $k$ , requiring careful selection of  $j$  and  $k$ . Minimum dynamic energy is achieved with an SRAM array structure with more rows than columns, which verifies the traditional guide in [7]. However, static energy described in (3) decreases compared to dynamic energy when performance improves. Static energy minimization can be obtained with an SRAM array structure with less number of rows than columns. The optimal structure for the static energy minimization is contradictory to the dynamic energy minimization. The next section analyzes SRAM array structure for minimum energy consumption incorporating all energy components.

#### B. Analytical Derivation of Optimal SRAM Array Structures for Minimum Energy Consumption

The previous SRAM array structure guideline [7] for energy minimization is valid when the energy consumed by leakage current is negligible compared to the dynamic energy. In various recent ultralow-power applications using nanoscale CMOS technologies, energy from leakage has become much more significant. Considering this, it is strongly required to revisit SRAM array structure for many minimum-energy-driven low-voltage applications.

Assuming constant SRAM density ( $D$ ), the total SRAM energy described in (3) can be rewritten as

$$E_{\text{total}} = D \times I_{\text{L-cell}} \times t \times V_{\text{DD}} + P_r \left( j \times C_{\text{RWL}} \times V_{\text{DD}}^2 + \frac{D}{j} \times 0.5 C_{\text{RBL}} \times V_{\text{DD}}^2 \right) + P_w \left( j \times C_{\text{WWL}} \times V_{\text{DD}}^2 + \frac{D}{j} \times C_{\text{WBL}} \times V_{\text{DD}}^2 \right). \quad (4)$$

Here, SRAM array structure will determine  $j$  and  $t$ . When the supply voltage is high where the dynamic energy is dominant, the optimal SRAM array structure for minimum energy can be derived by taking the derivative of (4), which is given in the following:

$$\frac{\partial E_{\text{total}}}{\partial j} = P_r \left( C_{\text{RWL}} \times V_{\text{DD}}^2 - \frac{D}{j^2} \times 0.5 C_{\text{RBL}} \times V_{\text{DD}}^2 \right) + P_w \left( C_{\text{WWL}} \times V_{\text{DD}}^2 - \frac{D}{j^2} \times C_{\text{WBL}} \times V_{\text{DD}}^2 \right) = 0. \quad (5)$$

The optimal SRAM array structure obtained from (5) is given as

$$j = \sqrt{D} \times \sqrt{\frac{P_r \times 0.5 C_{\text{RBL}} + P_w \times C_{\text{WBL}}}{P_r \times C_{\text{RWL}} + P_w C_{\text{WWL}}}}. \quad (6)$$

The second term in (6) represents how much the optimal SRAM array structure is deviated from the equal numbered rows and columns. In this work,  $C_{\text{RWL}}$  and  $C_{\text{WWL}}$  are larger than  $C_{\text{RBL}}$  and  $C_{\text{WBL}}$  because of the larger gate capacitance than the junction capacitance and the longer horizontal dimension than the vertical dimension. Accordingly, the optimal SRAM array structure from (6) has less number of columns ( $j$ ) than that of rows ( $k$ ). This corresponds with the results shown in [7].

Similarly, when the supply voltage is low enough to make the static energy component dominant, the optimal SRAM array structure for minimum energy can be rewritten as

$$\frac{\partial E_{\text{total}}}{\partial j} = \frac{\partial E_{\text{total}}}{\partial t} \frac{\partial t}{\partial j} = D \times I_{\text{L-cell}} \times V_{\text{DD}} \frac{\partial t}{\partial j}. \quad (7)$$

Since the bitline discharging speed is the main performance limiting factor, the array structure with fewer rows than columns is to be selected for better energy efficiencies.

#### C. Analysis of SRAM Array Structures for Energy Minimization

Fig. 2 demonstrates the energy of an 8-kbit SRAM subarray at four different supply levels sweeping the number of rows ( $k$ ). Following the conventional guide [7], the minimum energy point is found at  $k = 128$  and  $j = 64$  (more rows than columns) at  $V_{\text{DD}} = 1.2$  and  $1.0$  V. This array structure indicates the minimum switching capacitance associated with the dynamic energy consumption. As  $V_{\text{DD}}$  decreases, the number of rows for minimum energy also decreases for the energy-efficient array structure. This is particularly true when  $V_{\text{DD}}$  is high and the dynamic energy is the prevailing component.

However, as  $V_{\text{DD}}$  becomes closer to the level of the transistor threshold voltage, the changes in  $j$  and  $k$  for minimum energy become more prominent. As shown in Fig. 2(c) and (d), the minimum energy points are found at  $k = 32$  and  $j = 256$  at  $V_{\text{DD}} = 0.4$  V and at  $k = 16$  and  $j = 512$  at  $V_{\text{DD}} = 0.3$  V. Compared to the optimal SRAM array structures at  $V_{\text{DD}} = 1.0$  V,  $j$  and  $k$  have stronger influence on energy consumption. The increased sensitivity of the SRAM performance to array structure (due to increased portion of the static energy in the total SRAM energy) produces this phenomenon. As expected, lowering supply voltage transforms the SRAM array structure for minimum energy from a tall and thin structure to a short and

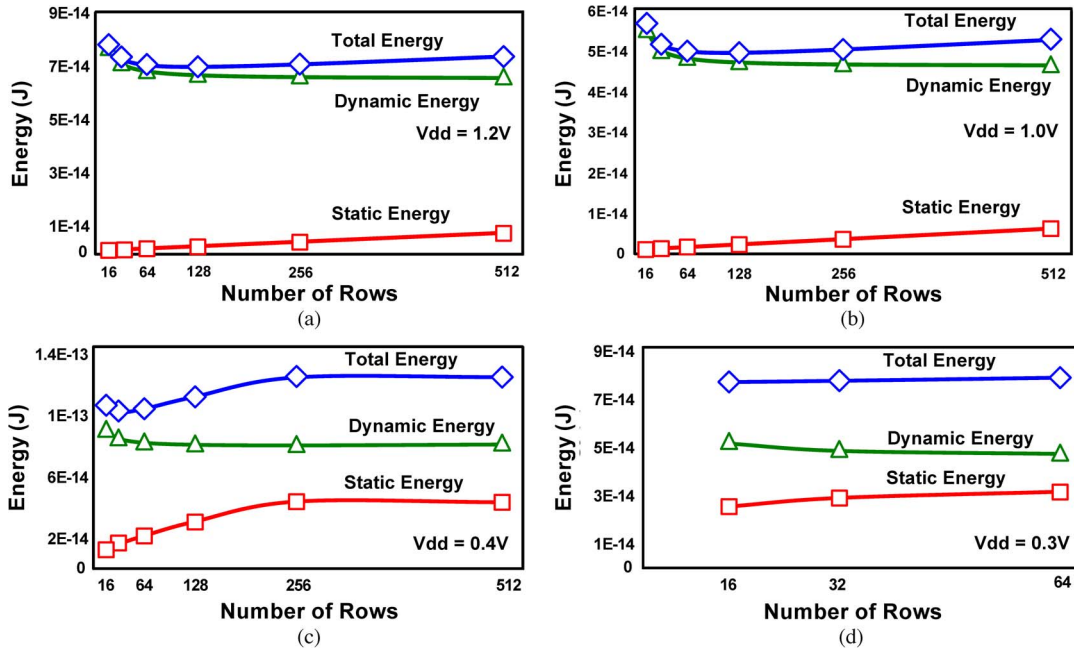


Fig. 2. Energy consumption of an 8-kbit SRAM subarray over various numbers of rows. Simulation results show that energy consumption is substantially affected by SRAM array structures. (a)  $V_{DD} = 1.2V$ , (b)  $V_{DD} = 1.0V$ , (c)  $V_{DD} = 0.4V$ , and (d)  $V_{DD} = 0.3V$ .

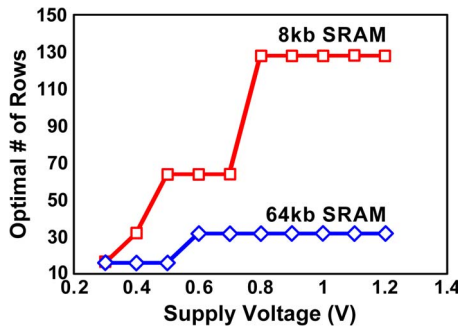


Fig. 3. Optimal numbers of rows versus supply voltage for energy-efficient array structure.

wide structure. The behavior can be explained by Fig. 2(c) and (d) where static energy plays an important role in deciding the total energy consumption in the SRAM. Also, Fig. 2(d) does not show results for array structures with rows  $> 64$  due to excessive leakage and bitline discharge failure. The simulation results shown here match the analytically derived results in Section III-B.

The optimal number of rows for minimum energy over different supply voltage levels is summarized in Fig. 3. For an array structure with a fixed density (8 kbit), the optimal number of rows for minimum energy consumption is 128 at higher supply voltages ( $> 0.7V$ ), which is larger than the number of columns ( $= 64$ ). On the other hand, the optimal number of rows decreases at lower supply voltages ( $0.3\text{--}0.7V$ ). For the SRAM array of 64 kbit (8 kbit  $\times$  8 bank architecture) where only one bank is enabled at a given time, the optimal number of rows reduces from 128 to 32. This is due to the substantial increase in the leakage energy compared to the dynamic energy in the SRAM array.

In addition, Fig. 4 depicts the percentage change in the total SRAM energy for the array structures using optimum rows and more rows than columns (taller array structure) for a fixed-

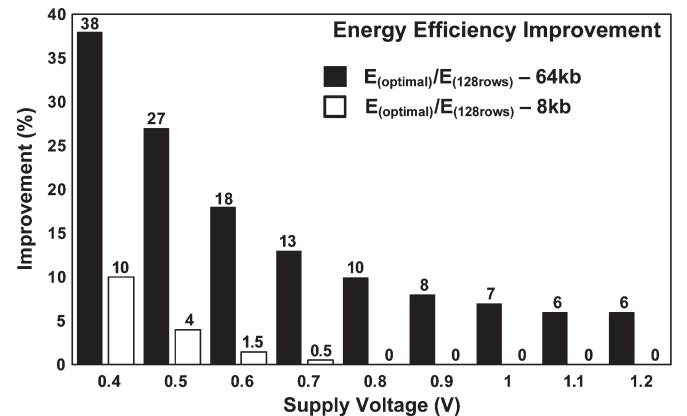


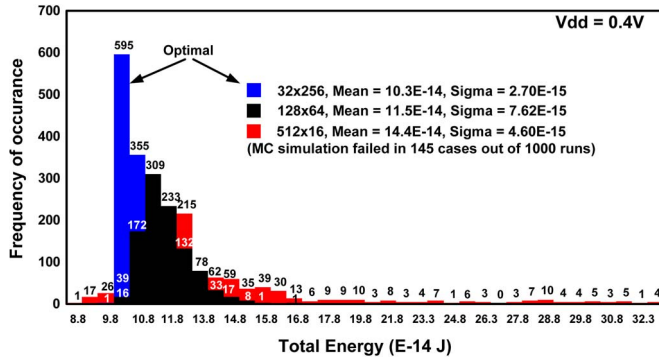
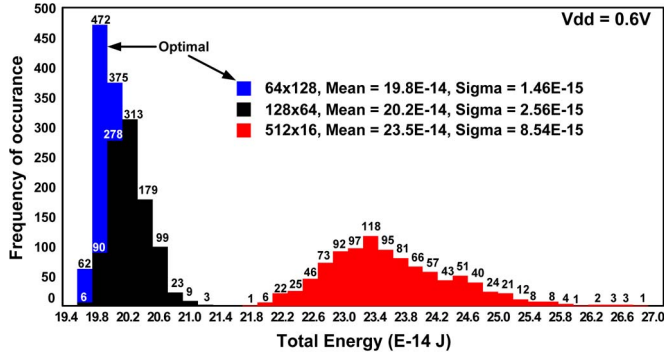
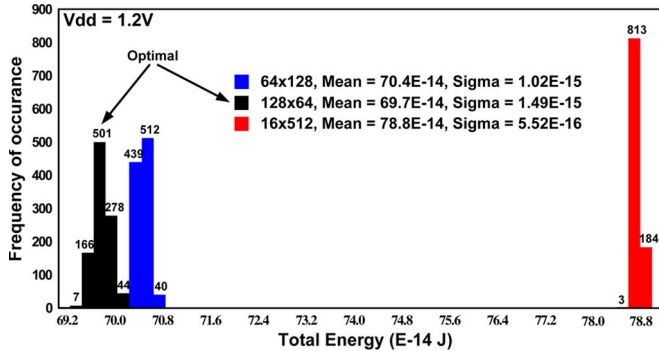
Fig. 4. Percentage change in the energy using optimal rows over 128 rows.

density SRAM. Optimum rows are the number of rows corresponding to the array structures showing minimum total energy at different supply voltages, as shown in Fig. 3. Simulation results demonstrate that the energy reduction up to 10% can be achieved using the optimal number of rows in the 8-kbit array structure operating at 0.4 V. The energy reduction is further enhanced when leakage energy becomes more significant. In the 64-kbit (8 kbit  $\times$  8 banks) SRAM array, the optimal number of rows can improve the energy efficiency up to 38% at 0.4 V when compared with the array with 128 rows. It can be inferred that, in larger SRAMs where majority of the arrays are not activated, wider array structures are more beneficial in terms of energy efficiency.

#### D. Impact of Device Variations on SRAM Array Structures for Energy Minimization

The adoption of minimum or near-minimum devices aggravates the device current deviation along with various design parameters, including energy consumption. In this section, we



Fig. 5. Statistical distribution of total energy at  $V_{DD} = 0.4$  V.Fig. 6. Statistical distribution of total energy at  $V_{DD} = 0.6$  V.Fig. 7. Statistical distribution of total energy at  $V_{DD} = 1.2$  V.

investigate the impact of device variations on the minimum-energy-driven SRAM array structures. We performed statistical simulation with 1000 sample runs for 8-kbit SRAM. Figs. 5–7 illustrate the statistical distribution of the SRAM total energy at the supply voltages of 0.4, 0.6, and 1.2 V, respectively, using the 8-kbit SRAM. To verify the effectiveness of the proposed idea, various array structures are evaluated. The numbers of rows explained in Fig. 3 are used as the optimal array structures to be compared to other array structure voltages (e.g., 32 rows at 0.4 V and 64 rows at 0.6 V). Simulation results reveal that wider array structures provide higher energy efficiencies at low supply voltage (Figs. 5 and 6), which corresponds to the results in Figs. 2 and 3. At the same time, the proposed optimal structures produce the lowest sigma values at 0.4 and 0.6 V. Note that read failures occurred at 0.4 V when 512 rows are used. At  $V_{DD} = 1.2$  V (Fig. 7), the optimal structure shows the smallest mean energy value. However, the energy variation of the structure is not the smallest. Smaller energy variations can be obtained by lowering the number of cells per bitline beyond

the optimal value, which will result in higher mean energy, as illustrated by the red graph in Fig. 7.

#### IV. CONCLUSION

Energy of various 8T-SRAM array structures over different supply levels has been analyzed. While tall array structures generate higher energy efficiency at nominal supply voltage, short and wide array structures show better energy efficiency at low-voltage operation. This change is mainly driven by the increased portion of SRAM leakage in nanoscale CMOS technology at low voltage. In this work, we have mathematically derived array structures for minimum energy consumption and verified the model with simulation. In simulation, the energy efficiency improvement of up to 10% for 8 kbit and 38% for 64 kbit was achieved by just optimizing the array structure. In addition, statistical analysis reveals that the proposed wider array structures at low voltage have less variation in energy compared to the traditional tall array structures. This result can be easily applied to energy-efficiency-driven SRAM design.

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