Design Exploration of Sensing Techniques in 2T-2R Resistive Ternary CAMs

M. Rakka, M. E. Fouda, R. Kanj, A. Eltawil and F. J. Kurdahi

***Abstract*—In-Memory Computing (IMC) is considered a great candidate to replace von-Neumann computing architecture to overcome the memory wall. Ternary content-addressable memories are the main building blocks in IMC-based architectures, such as the associative processors. In this paper, we present a juxtaposition between the capacitive and resistive sensing in 2T-2R TCAMs. A Figure of Merit, function of the dynamic range, latency, and energy, is defined to have a fair comparison between the two sensing techniques. A mathematical model for the transient behavior of both sensing schemes has been derived and verified through SPICE simulations. We studied the performance with an in-memory addition application. Results from various scenarios show that the resistive sensing outperforms the capacitive one in both theoretical and application-based contexts.**

***Index Terms*—2T-2R TCAM, In-Memory Computing, Associative Processors, Analysis, Mathematical model.**

I. Introduction

With the surge of applications that require massive parallelism, such as Machine Learning, and given that traditional computing paradigms are reaching their computational limits, a new conundrum arises: accommodating for these applications in an energy-efficient manner and with minimal overhead. Associative Processors (APs) have been proposed as in-memory platforms for handling massively parallel computations. APs carry out in-memory compute operations concurrently on multiple memory rows, thereby reducing the memory-wall problem [1]. Several AP architectures were proposed in literature [1], [2]. An AP can constitute an array of Content Addressable Memories (CAMs) that serve as storage devices and allow to search the entire memory at once in order to identify matches of a given input [3].

Ternary CAMs (TCAMs) are an extension of CAMs where partial searches are possible by enabling the 'don't care' condition on a portion of the input data. Due to the potential of TCAMs, different implementations have been introduced utilizing either SRAM or emerging devices such as resistive or phase change memories [4], [5]. SRAM-based CAMs suffer from high power consumption and low-density [4], and to address these concerns, memristor CAMs were introduced in [5]. Furthermore, several sensing schemes have been proposed to reduce the power or enhance the latency of the search operation of CAM designs [4], [6]–[9]. In conventional schemes, the match line (ML) is typically precharged high. During the evaluate phase, only the fully matched rows remain high [6]. The authors in [7] proposed a clocked self-referenced sensing scheme for 2T-2R PCM-based TCAM designs. The scheme dynamically modulates the precharge ML levels to intermediate values that enable power savings while maintaining good noise margins. A selective hit-ML precharge sensing scheme was proposed for 2T-2R TCAM in [6]. In this scheme, the ML discharges only when there is a full match while the mismatched rows remain high; hence, there is only a need to selectively precharge the fully matched MLs. At the architecture level, several solutions were also proposed to save energy. For instance, a multi-stage architecture that relies on matched rows in previous stages to selectively activate the corresponding rows in the next stages was proposed for 3T-1R TCAM in [8]. The authors in [4] proposed a capacitive sensing scheme for 2T-2R with optimal dynamic range considerations. More recently, [9] proposed an evaluate only sensing scheme suitable for nand-type SRAM-based TCAM. This scheme eliminates the precharge phase and performs search in half-cycle compared to other approaches.

In this paper, we study two sensing schemes for 2T-2R TCAM, (1) a capacitive sensing scheme with optimal dynamic range considerations, and (2) a resistive sensing scheme that eliminates the precharge phase. Particularly, the contributions of the paper are as follows. (1) We explore improvements in performance metrics in terms of dynamic sensing range, energy, and latency. (2) We develop a mathematical model for the Memristive TCAM (MTCAM) operation for both sensing schemes and validate the proposed model against SPICE simulations. (3) We study the two sensing schemes in the context of an n-bit adder application.

The rest of the paper is organized as follows. In section II, capacitive sensing and resistive sensing designs are presented. Section III presents the mathematical formulation of both designs. MATLAB and SPICE validation and simulation results are presented in section IV. Section V demonstrates an adder application. Finally, section VI concludes the work.

II. MTCAM Designs

A CAM cell can be implemented in a variety of forms. One popular implementation consists of two transistors and two memristors, which is referred to as 2T-2R [10]. A Memristor-based TCAM row consists of several of such cells, and each row is equipped with a sensing circuit to distinguish between the full match and the mismatch states as illustrated in Fig. 1. The MTCAM row either evaluates to a full match state (fm) where all of its cells are matched with the input bits or to a mismatch state otherwise. Hereon, we refer to the full mismatch/one mismatch state (fmm/1mm) as the state where all/one cell(s) are/is mismatched.

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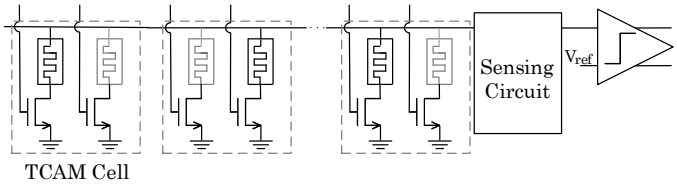

Fig. 1: 2T-2R TCAM structure.

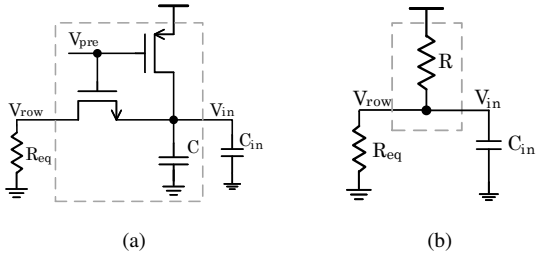

Fig. 2: Sensing techniques with the equivalent circuits of MTCAM and comparator, represented in R_{eq} and C_{in}, respectively; a) capacitive sensing circuit and b) resistive sensing circuit, shown in the dashed box.

In the capacitive sensing, a capacitor is used to distinguish between the fm, and the different mismatch states. During the precharge phase, the capacitor C is charged, and then in the evaluation phase, it discharges through a resistor equivalent to the effective resistance of the MTCAM row of cells shown in Fig. 2a. The voltage across C_{in} is used to determine evaluation into a fm or mismatch. In the case of fm, the capacitor discharges slowly, and in case of fmm, it discharges quickly to ground. Figs. 3a and 3b (in blue) show the simulated voltage and current waveforms across the capacitor of the capacitive sensing MTCAM row. Three cycles are presented corresponding to the fmm, fm, and 1mm states. Each cycle consists of a precharge phase and an evaluation phase.

Another sensing approach uses a resistor as a voltage divider for the 2T-2R CAM, as shown in Fig. 2b. Hence, the voltage that distinguishes the mismatch states from the fm state is depicted as a voltage divider across the equivalent resistor of the MTCAM cells. In this design, there is no need for a precharge phase, and only an evaluation phase is necessary to assess among the different states. Fig. 2b shows the MTCAM row based on this design during the evaluation phase. Figs. 3c and 3d (in blue) demonstrate the output voltage and current of the transient analysis carried out on the resistive sensing MTCAM row. Three cycles are considered: fmm, fm, and 1mm. In this design, each cycle consists of an evaluation phase only. Clearly, this design evaluates much faster while maintaining a good voltage drop difference between the fm and 1mm states. For more information about the setup of the transient analysis, we refer the reader to section IV.A.

III. Design Fundamental Evaluations

A. MTCAM Row Modeling

We define the equivalent resistance of a row of MTCAM cells as:

$$R_{eq}(N_{mm}) = R_{mm}//R_m//R_x \tag{1}$$

where R_{mm}, R_m and R_x represent the equivalent resistances of the mismatched, matched and 'don't care' cells within the row, respectively (see supplementary materials for detailed model). N_{mm} represents the number of mismatched cells. For the computing applications, such as the adder, which we considered in this paper, we assume no 'don't care' scenarios.

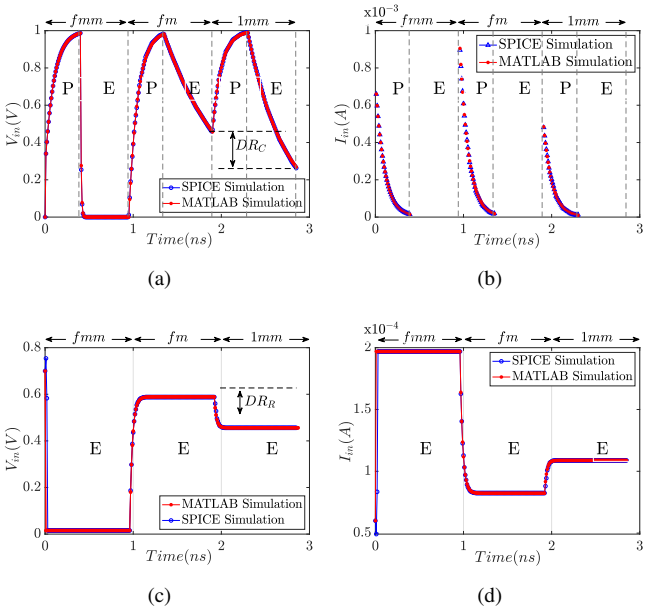

Fig. 3: SPICE/MATLAB validation of a TCAM row voltage and current for the fmm, fm, and 1mm states. For the capacitive sensing waveforms (a) and (b), P and E represent the precharge and evaluate phases, respectively. Resistive sensing waveforms, noticeably transitioning faster, are presented over the same time scale for illustration purposes in (c) and (d).

B. Figure of Merit

In order to have a fair comparison between the two sensing techniques, we define a Figure of Merit (FOM), which is a function of the following three important metrics.

- Sensing Dynamic Range, DR, which is the voltage range between the match voltage and the closest mismatch voltage (i.e., one mismatch state). It is defined as follows.

$$DR(t) = V_{fm}(t) - V_{1mm}(t) \tag{2}$$

- Latency, T_L, which is the time needed to distinguish between the fm and mismatch states to establish a maximum or desired dynamic range DR. This time determines the maximum operating frequency of the MTCAM.
- Energy Consumption, E, which is the energy consumed during the search operation by the MTCAM row.

Thus, the Figure of Merit (FOM) is defined as follows.

$$FOM = \frac{DR(T_L)}{T_L * E} \tag{3}$$

As one can inspect, the design with the higher FOM presents itself as the better design as it would be more efficient in terms of energy and time, and it would have a relatively high voltage difference suitable for sensing purposes. Generally, the energy can be defined for the circuits in Fig. 2 based on (4) and (5).

$$E = \int_{t^i}^{t^i+\Delta t} \frac{V_{dd} * (V_{dd} - V_{in})}{R_0} dt \tag{4}$$

$$V_{in}(t) = V_f + (V_{in}(t^i) - V_f)\exp(\frac{-(t-t^i)}{\tau}) \quad (5)$$

Assuming a time shift where $t > t^i$, V_f is the final voltage, τ is the corresponding time constant of the RC circuit, and R_0 is the pull-up resistance as defined in Table I. Substituting V_{in} and integrating the previous equation yields the following.

$$E = \frac{\tau V_{dd}}{R_0}\left((V_{dd} - V_f)\frac{\Delta t}{\tau} + \big(V_{in}(t^i) - V_f\big)\left(e^{\frac{-\Delta t}{\tau}} - 1\right)\right) \quad (6)$$

For the precharge phase, Δt is selected to be $n\tau$. For purposes of our simulations, we set $n = 3$ throughout the paper, which gives 95% of the steady-state value.

C. Design Specific Considerations

Three metrics were used for evaluating the performance of the two designs: T_L, Energy, and DR. We herein formulate the corresponding design specific parameters.

1) Capacitive Sensing Design:

(a) Latency: For this design, the optimal evaluation time is derived as $TE_C = (C\ln\left(\frac{R_{fm}}{R_{1mm}}\right) \times \frac{R_{fm} * R_{1mm}}{R_{fm} - R_{1mm}})$ with $R_{fm} = R_{eq}(N_{mm} = 0)$ and $R_{1mm} = R_{eq}(N_{mm} = 1)$ [4]. As such, the latency, T_{CL} can be determined by the worst-case precharge time and TE_C as follows.

$$T_{CL} = n * \tau_{CP} + TE_C \quad (7)$$

τ_{CP} is the precharge time constant defined in Table I.

(b) Energy: During the i^{th} cycle, the dissipated energy is the sum of energies dissipated during the precharge and evaluate phases: $E_C^i = E_{CE}^i + E_{CP}^i$. The energy for each phase is derived according to (4) while relying on the parameters listed in Table I. Note that the initial conditions for the precharge energy calculations in the i^{th} cycle are obtained from the outcomes of the evaluate phase of the $(i-1)^{th}$ cycle.

(c) Sensing Dynamic Range: The maximum voltage difference between the fm and 1mm states measured at the optimal time TE_C can be defined as [4]:

$$DR_C(TE_C) = V_{dd} * \theta^{\left(\frac{\theta}{1-\theta}\right)} * (1 - \theta) \quad (8)$$

with $\theta = R_{1mm}/R_{fm}$.

2) Resistive Sensing Design:

(a) Latency: This design is evaluate-based only. The latency, TE_{RL} is determined by the worst-case evaluate time as

$$TE_{RL} = n * \tau_{WC,R} \quad (9)$$

$\tau_{WC,R}$ is the worst case evaluate time constant for the fm state derived from τ_R in Table I with $R_{eq}(N_{mm} = 0)$.

(b) Energy: During the i^{th} cycle, the dissipated energy, E_R^i, is equal to the evaluate energy, E_{RE}^i, derived according to (4) while relying on the parameters listed in Table I for the resistive scheme. Specifically, for the i^{th} cycle, $V_{in}(t^i)$ is obtained from the outcomes of the previous cycle, and we expect $V_{in}(t^i + TE_{R_L})$ to reach the final voltage value, V_f, derived according to the voltage divider equation based on the corresponding cycle's N_{mm}.

(c) Sensing Dynamic Range: It can be derived from (2) as

$$DR_R(TE_{RL}) = V_{dd}\frac{R(R_{fm} - R_{1mm})}{(R + R_{fm})(R + R_{1mm})} \quad (10)$$

The maximum dynamic range can be achieved by taking the first derivative with respect to R and equating it to zero. The optimal R value is as follows.

$$R^* = \sqrt{R_{1mm}R_{fm}} \quad (11)$$

It is worth noting that R^* is optimized to maximize the dynamic range not to maximize FOM, which is a monotonically increasing function of R.

IV. Analysis and Results

A. Transient Simulations

Fig. 3 presents precharge and evaluate waveforms for the fm, fmm, and 1mm states for the following parameter combinations: $N = 128$ (number of cells per row), (R_{LRS}, R_{HRS}) = ($1k\Omega$, $\alpha * R_{LRS}$) where $\alpha = 1000$ (representing low and high memristance values), (R_{on}, R_{off}) = ($9k\Omega$, $10M\Omega$) to model the precharge transistor in Fig. 2a, and $R = 5k\Omega$. $C_{in} = 10fF$ and $C + C_{in} = 100fF$. For the capacitive scheme, a load of at least $100fF$ is needed for the comparator to properly latch V_{in} and distinguish between the fm and 1mm states due to fast discharge. The simulated SPICE voltage and current waveforms (in blue) are concurrent with the corresponding MATLAB simulated waveforms (in red) (based on (5)). Hence, the theoretical results (in IV.B) in terms of FOM and design metrics are consistent with the SPICE simulations.

As apparent in Fig. 3, the time taken by the resistive sensing design to evaluate all three states is in the order of picoseconds compared to nanoseconds for the capacitive sensing. Moreover, the corresponding energy needed for the resistive sensing design to evaluate during that time is obviously less because of the absence of the need to fully precharge which is required for the capacitive design. Note that the resistive scheme waveforms are presented over the same timescale as the capacitive one for illustration purposes only. While the dynamic range is larger in the capacitive sensing model, the resistive sensing scheme maintains a good dynamic range. This proves that the resistive sensing design has an edge when energy and latency are key concerns. The resistive sensing design is therefore ideal for inference applications where there are consecutive evaluations with no hold intervals. Particularly, the memristive array can be powered off when inference is completed, and hence no static energy will be dissipated in the resistive sensing approach.

B. Design Space Exploration: Figure of Merit Analysis

We rely on MATLAB numerical simulations to perform comparative FOM analysis for the two designs. We rely on the following design space parameter combinations to consider different memristor device values for our study [11]: $N \in \{128, 256, 512\}$, $R_{LRS} \in \{1K, 10K, 50K, 100K, 1M\}\Omega$, $R \in \{1K, 5K, 25K, 125K, 625K, 1M\}\Omega$, $R_{on} = 9K\Omega$, $R_{off} = 10M\Omega$, $V_{dd} = 1V$, $C_{in} = 10fF$, $R_{HRS} = \alpha * R_{LRS}$ where $\alpha = 1000$ and $C + C_{in} = 100fF$. We rely on these combinations to compare the two designs over different device types and ranges. In fact, some device LRS can go as low as 100Ω, and α can be as high as 1000 or more [11], [12]. While large α values may have implications on the device endurance [12], some metal Oxide RRAMs exhibit good endurance for

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TABLE I: Summary of the model parameters for the capacitive and resistive sensing circuits.

	Capacitive Sensing		Resistive Sensing
	Precharge Phase	Evaluation Phase	
τ	$\tau_{CP} = R_{on} * (C + C_{in})$	$\tau_{CE} = (R_{off} \| R_{eq}) * (C + C_{in})$	$\tau_R = (R \| R_{eq}) * C_{in}$
R_0	R_{on}	R_{off}	R
$V_{in}(t^i)$	$V_{in}(t^{i-1} + TE_{CL})$	V_{dd}	$V_{in}(t^{i-1} + TE_{RL})$
V_f	V_{dd}	0	$V_{dd}\frac{R_{eq}(N_{mm})}{R_{eq}(N_{mm})+R}$
Δt	$n\tau_{CP}$	TE_{CL}	TE_{RL}

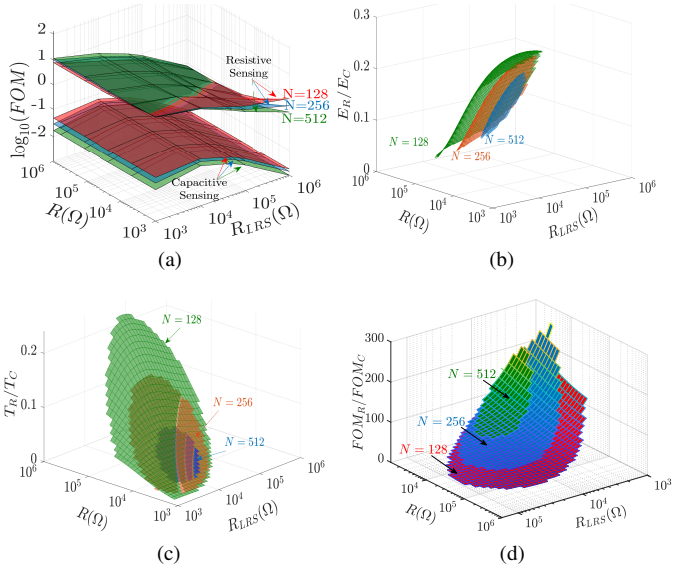


Fig. 4: (a) FOM comparison between the capacitive and resistive sensing techniques for different N values. (b) Energy ratio, (c) evaluation time ratio and (d) FOM ratio for different N values with constrained dynamic range to $DR > 75mV$.

$\alpha = 1000$ [11]. We also note that these ratios can drop due to variability [12], [13], particularly in HRS, and hence, our assumption for $\alpha = 1000$ represents a median window ratio.

Fig. 4a shows 3D plots for FOMs (when considering worst-case energy of the full mismatch case) of the two designs corresponding to the different combinations. One can see that the resistive sensing design shows higher FOM values compared to the capacitive sensing design for all LRS, R, and N values. Furthermore, the energy and latency results of the resistive sensing scheme outperform that of the capacitive sensing one over the design space. Figs. 4b, 4c and 4d present the energy, latency and FOM ratios respectively plotted with the additional constraint on the dynamic range: $DR > 75mV$ to maintain that a sense amplifier can differentiate between the fm and 1mm states. Table II lists the maximum FOM ratio along with the corresponding energy and latency measures for both designs when $DR > 75mV$. We note upto 260× FOM improvement for the resistive sensing scheme compared to the capacitive sensing scheme for $N = 256$.

While the FOM is a good overall comparator for both designs, some of the metrics may be more significant than others depending on the specific application. For example, for error-tolerant neuromorphic computing applications, energy matters most. For AP applications, with dense TCAM structures, energy as well as accuracy in terms of the DR matter, and latency could be traded-off in favor of energy and/or DR. For IP routing applications, energy is not a concern. Since the achieved search times for both the capacitive and resistive sensing schemes are fast, one may consider DR as the key metric for IP routing. If utmost search speed is under consideration, both latency and DR can be considered as key metrics for IP routing applications. As such, we present in supplementary document Table I, a summary of the preferred sensing scheme based on the performance of the desired metrics for the specific applications when $DR > 75mV$.

We further swept α values and conducted Monte Carlo simulations to mimic variability in HRS similar to the strong programming values in [13], as illustrated in supplementary document Fig. 1. We observe that the DR decreases with decreasing α for both designs, and the lower tails of the DR distributions span similar ranges in both schemes. However, the FOM ratio increases; as such, in the presence of process variations in HRS, the two schemes are mostly suited for error tolerant applications, with the resistive scheme offering energy/latency savings compared to the capacitive one.

V. In-memory Adder Example

We studied the two design alternatives in the context of n-bit adder application in a $2n \times (2n+1)$-bit TCAM array for $n \in \{16, 32, 64\}$. We implemented the LUT-based approach in [14]. At its core, the algorithm relies on four passes of 3-bit comparisons (supplementary document, Table II), operates on the different rows in parallel and consecutively computes addition from the least significant bit (LSB) to the most significant bit (MSB). The adder function pseudo-code is presented in Algorithm 1 in the supplementary document. We explored the design space to identify and compare the best resistive and capacitive sensing design points.

A. Design Space Exploration

We conducted a design space exploration with a MATLAB setup similar to that in IV.B, but with: (i) $N = 3$, (ii) $R_{LRS} \in \{500, 1K, 10K\}\Omega$. Since the adder's functionality comprises a 3-bit comparison per row, we note that one can achieve a reasonable DR_C, with a time interval that is less than the optimal TE_C. As such, (iii) we swept TE as a parameter for the capacitive sensing design over the range [0.0298-5]ns.

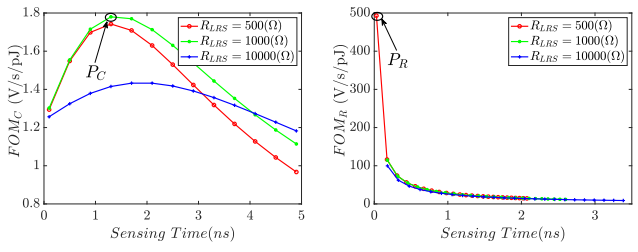
TABLE II: Energy and latency of points with the highest FOM Ratio with $DR > 75mV$ for each N.

N	Max FOM Ratio	E_R(fJ)	E_C(fJ)	TE_{RL}(ns)	T_{CL}(ns)
128	177.9	24	99	3.1E-2	3.2
256	259.7	17	99	4.7E-2	3.0
512	222.1	18	99	5.1E-2	3.1

This range is obtained based on the resistive sensing evaluate latency corresponding to the different R combinations for a given R_{LRS}. Hence for consistency, we use this TE range as our reference sensing time axis for our study. Note that for the capacitive sensing design, we still need to include the precharge time in the FOM analysis. From Fig. 5, it is evident that the resistive sensing design offers enhanced FOM values compared to the capacitive sensing design for the space under study. Despite the similarity in the range of the sensing time TE for both designs, $3\tau_{CP}$ is significant and contributes to the FOM degradation for the capacitive sensing approach. As shown in Fig. 5b, we identify the best resistive sensing design point P_R to correspond to (R_{LRS}, TE_{RL}) = (500Ω, $0.02ns$ (i.e., $R = 1K\Omega$)). Note that while R value in (11) provides the best dynamic range, it does not correspond to the best FOM. P_R yielded $DR_R = 100mV$, $TE_{RL} = 0.02ns$, $E_R = 6fJ$ and $FOM_R = 493$. For the capacitive sensing design, the best FOM was achieved at the point P_C corresponding to (R_{LRS}, TE_C) = ($1k\Omega, 1.3ns$) as shown in Fig. 5a. DR_C was around $700mV$, latency $T_{CL} = 4ns$, $E_C = 97fJ$ and $FOM_C = 1.78$ for this design point. This point offered a good trade-off between the different metrics. The FOM ratio at the best operating points is around 277.

B. Energy Saving

Herein, we focus on the energy savings at the design points P_R and P_C. For the capacitive sensing, we assumed the current evaluate will incur known energy, E_s in the following precharge, where $s \in \{fm, 1mm, 2mm, 3mm\}$. These states correspond to the full match, one, two, and full mismatch energies, respectively. For example, if the LSBs of integers A and B and the carry, $A_0B_0C = 000$, then the 1^{st} pass of the LUT-based algorithm will compare $'000'$ to $'110'$. This will result in an energy dissipation equivalent to E_{2mm} during the following precharge phase. For the resistive sensing design, on the other hand, there is no precharge phase, as indicated earlier, and the evaluation leads to a charge or discharge based on the previous state. For the j^{th} bit, the previous state is saved from either the previous pass or the last pass of $(j-1)^{th}$ bit addition. So, it depends on a number of transitional energies of interest of the form: $E_{s_1-s_2}$, where $s_{1,2} \in \{fm, 1mm, 2mm, 3mm\}$. Hence, if $A_0B_0C = 000$, the 2^{nd} pass will compare $'000'$ against $'100'$ and will dissipate an energy equal to $E_{2mm->1mm}$. In both designs, the energy for a given bit per row is computed based on the energy consumed in the four passes of the lookup table [14]. The total energy represents the sum of energies consumed due to the addition of the n-bit integers across all rows. For a word size of 16, 32, and 64 bits, we ran 1000 add operations. The resulting average energy ratios demonstrated around 14× energy savings for the resistive sensing TCAM when compared to the capacitive sensing TCAM for all n.



(a) (b)

Fig. 5: FOM versus sensing time; a) for $N = 3$ in capacitive sensing MTCAM, b) for $N = 3$ in resistive sensing MTCAM.

VI. Conclusion

In this paper, we presented a comparative study between two sensing designs of 2T-2R TCAMs. Our comparison was carried out theoretically and using SPICE simulations, where the resistive sensing MTCAM proved to have the edge over its capacitive sensing counterpart design based on the adopted Figure of Merit, which incorporates the dynamic range, latency, and energy as the design performance metrics. This is particularly true for applications where energy and latency are key concerns. In this context, resistive design showed up-to 260× FOM improvements over the capacitive design, while taking DR constraints into consideration. We also note that for $N = 128$, the resistive sensing design, which is characterized by low energy and latency, satisfies the DR constraints over a wide range of the design parameter space. Finally, we presented an adder application that maintained our theoretical and SPICE results. As such, we have demonstrated that the resistive sensing of MTCAM cell serves as an efficient building block of AP designs and their subsequent applications.

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