# Circuit Design for Beyond Von Neumann Applications Using Emerging Memory: From Nonvolatile Logics to Neuromorphic Computing

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## Abstract

Emerging memory devices enable performance improvements in memory applications and make possible chip designs using beyond von Neumann architectures. This paper explores the use of emerging memory devices in applications of nonvolatile logics and neuromorphic computing, and provides a review of several silicon examples of nonvolatile logics. This paper also discusses the challenges involved in the design of circuits for nonvolatile logics and neuromorphic computing systems based on emerging memory devices.

## Keywords

Emerging memory, ReRAM, RRAM, STT-MRAM, PCM, memristor, nonvolatile Logics, neuromorphic computing

## 1. Introduction

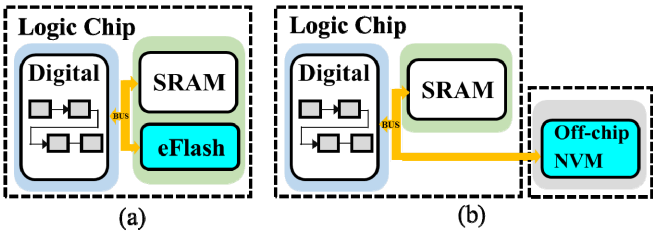



Fig. 1 Von Neumann-based structure with (a) on-chip and (b) off-chip NVM for intelligent power on-off

Many von Neumann-based energy-efficient systems (Fig. 1) employ on-chip or off-chip nonvolatile memory (NVM) in intelligent power on-off schemes (Fig. 2) aimed at reducing system standby power. This is a particularly important issue in battery-powered or energy-harvester-powered devices equipped with nanometer chips, which are particularly susceptible to current leakage. In these systems, NVM is employed for the storage of programs and critical data in power-off mode [1]-[5].

However, the serial (word-by-word) movement of data between NVM and volatile devices (SRAM, flip-flops) during power off/on operations results excessive power consumption and long access times. This underlines the need for a new circuit architecture (beyond von Neumann architecture) to accommodate intelligent power interruption schemes capable of providing fast speeds and low power consumption.

In the following sections, we discuss two emerging-memory-based approaches to the development of beyond von Neumann architectures: (1) nonvolatile logics (nvLogics) and (2) neuromorphic computing.

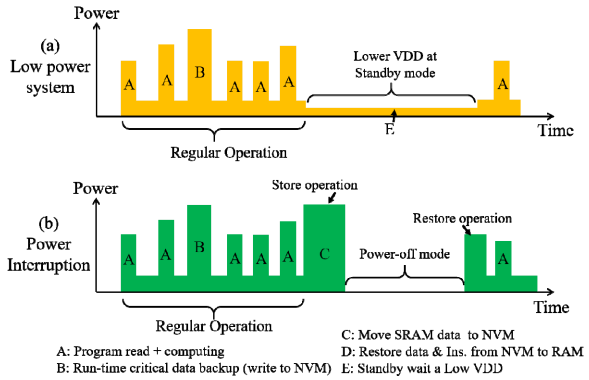



Fig. 2 Standby power reduction schemes: (a) sleep-mode with low VDD; (b) NVM-based intelligent power interruption

## 2. Recent Emerging Memory

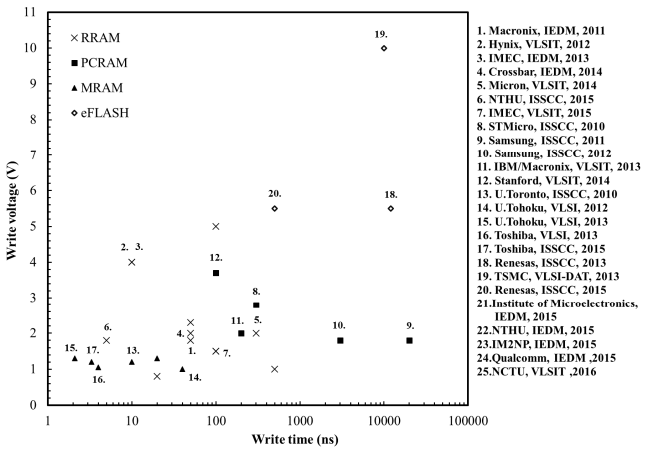



Fig. 3 Write performance of recent emerging memory devices

Fig. 3 illustrates the performance of recent emerging memory devices, including resistive RAM (ReRAM, RRAM, Memristor) [6]-[17], phase-change memory (PCM) [18]-[23], and spin-transfer-torque magnetic RAM (STT-MRAM) [24]-[28]. These memory devices have much faster write times and lower write voltages than conventional flash memory. This makes it possible for emerging memory

devices to achieve write energy far lower than that of conventional flash memory.

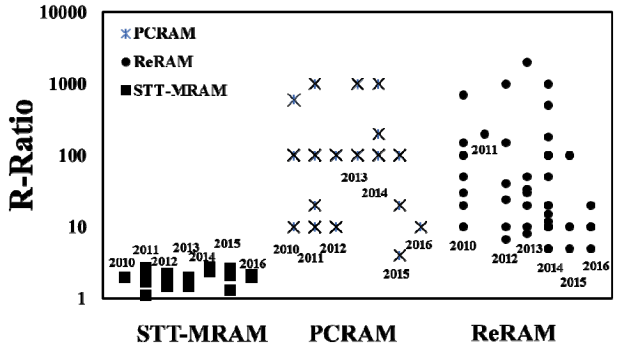



Fig. 4 R-ratio of recent emerging memory devices

Fig. 4 illustrates the resistance-ratio (R-ratio) between the two stored logic-states in recent emerging memory devices. R-ratios have been shrinking in recent years, due to lower write energy and smaller device dimensions.

Fig. 5 presents an example of write-time variations in a ReRAM device [29]. In emerging memory devices, the mean values and distribution of write times (SET and RESET operations) vary with write conditions. Due to process variations, the difference in the period for SET ($T_{SET}$) or RESET ($T_{RESET}$) operation between the fastest and slowest cells can exceed 10x or even 100x.

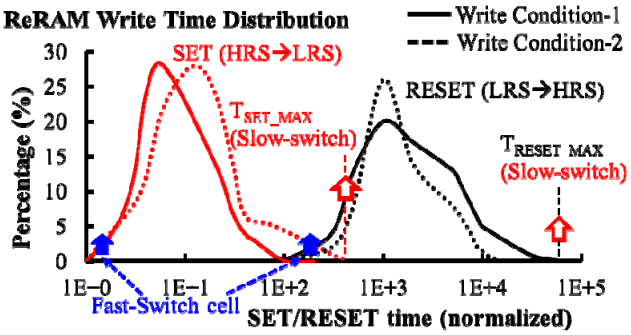



Fig. 5 Example of write-time distribution in ReRAM device

## 3. Non-Volatile Logics and Nonvolatile Processors

### 3.1. Concept of nonvolatile logics

Fig. 6 illustrates the concept of nonvolatile logic (nvLogic) and nonvolatile processors (nvProcessors). In conventional von Neumann-based SoC chips, all of the critical computing states in flip-flops (FF) and critical data in SRAM are moved to NVM macros/chips via a shared system bus during power-off operations. The word-by-word and block-by-block sequential movement of data between FF/SRAM and NVM in conjunction with the long NVM-write time of eFlash results in extended power-down latency ($T_{STORE}$) and large store (power-off) energy consumption ($E_{STORE}$). Moreover, the movement of data between FF/SRAM and NVM must be controlled by a centralized control unit or the CPU.

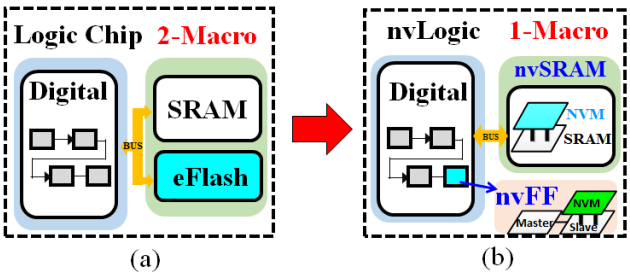



Fig. 6 Concept of nonvolatile processor and nonvolatile logics (a. modified: add a common bus between dig./SRAM/eFlash, b. remove nvTCAM)

As shown in Fig. 6(b), the placement of emerging memory devices above the CMOS devices in CMOS FF or SRAM cells allows for the movement of data between volatile CMOS circuitry and NVM devices within each nvLogic cell; i.e., without using a shared data bus in von Neumann architecture. Unlike the central control scheme in conventional von Neumann-based logic chips, the control of data movement operations is distributed among each nvFF cluster or nvSRAM macro. The parallel movement of data in nvLogic cells enables higher bandwidths, reduced power consumption, and faster store operations than conventional von Neumann-based chips/systems.

### 3.2. Examples of nvSRAMs and nvFFs

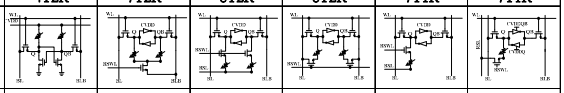
| Structure | 4T2R | 7T2R | 8T2R | 8T2R | 7T1R | 7T1R |
|---|---|---|---|---|---|---|
| Schematic |  | | | | | |
| Cell Area | 0.6x | 1x | 1.55x | 1.13x | 1.18x | 1x |
| tech. node | MTJ | ReRAM | ReRAM | ReRAM | ReRAM | ReRAM |

Fig. 7. Recent silicon-verified nvSRAM cells

Fig. 7 presents examples of recent silicon-verified nonvolatile SRAM (nvSRAM) cells [30]-[36]. Most nvSRAM devices have three operating modes: SRAM, store, and restore. SRAM mode is used for the read and write operations of high-speed or low VDDmin applications, as in regular SRAM devices. Store mode is used for data movement from the storage nodes (Q/QB) of SRAM cells to NVM devices. Restore mode is used for data movement from NVM devices to SRAM storage nodes (Q/QB).

Fig. 8 presents recent silicon-verified nonvolatile Flip-Flops (nvFFs) [37]-[40]. Most nvFFs have three operating modes: Flip-Flop, store, and restore. Flip-Flop mode is used for the regular flip-flop operations of high-speed or low VDDmin applications. Store mode is used for data movement from the storage node (Q/QB) of the slave-stage in FFs to NVM devices. Restore mode is used for data movement from the NVM device to the Q/QB in the slave-stage of FFs.

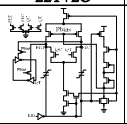
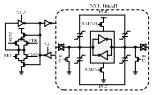
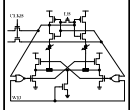
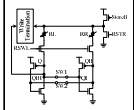
| Structure | 22T+2C | 18T+4C | 17T+2R | 15T+2R |
|---|---|---|---|---|
| Schematic |  |  |  |  |
| tech. node | 130nm | 130nm | 90nm | 65nm |
| Device | FeRAM | FeRAM | MTJ | ReRAM |

Fig. 8. Recent silicon-verified nvFF cells

### 3.3. Challenges in Circuit Design for Emerging memory-based nvLogics

The small R-ratio and wide distribution of cell resistance values in emerging memory devices results in a small difference in signals between nodes Q and QB during restore operations (power-on). This lowers the yield of data restore operations in nvFF and nvSRAM in cases where CMOS transistors are subject to significant process variation.

As illustrated in Fig. 5, nvLogics commonly employ the maximum write time ($T_W$) for NVM-write (store) operations to ensure sufficient $T_W$ for the emerging memory devices against a wide distribution in NVM write-times. However, a long $T_W$ causes (a) wasted power consumption in fast-switch cells, (b) reliability degradation due to long stress times in fast-switch cells, and (3) write failure in slow-switch cells due to power integrity degradation (lower voltage) induced by the large consumption of DC current by fast-switch cells.

## 4. Emerging Memory Based Neuromorphic Computing

### 4.1. Application of Emerging Memory in Neuromorphic Computing

As shown in Fig. 9, many recent studies have employed emerging memory (memristors) as synapses for the storage of weights in biologically inspired neural networks (NN) and neuromorphic computing [41]-[45]. As shown in Fig. 9(b), most memristor-based neuromorphic computing systems employ ReRAM and PCM devices with a high R-ratio and multi-level-cell (MLC) behavior and resistance characteristics [46]-[47]. Unlike the use of SRAM for storing weights, memristor-based synapse implementations enable energy-efficient parallel computing for matrix-vector multiplication (weight sum) using memristor arrays to accumulate a combination of input signals and synapse weightings, as shown in Fig. 9(c).

Modifications to memristor resistance (weight) during learning and training operations is achieved mainly by pulse (spike) control, such as spike-timing-dependent-plasticity (STDP) training [48]-[51].

As shown in Fig. 10, several memristor array structures [42], [52]-[54] can be used for matrix-vector multiplication operations, including (a) cross-bar structures without selectors, (b) cross-bar arrays with selectors, and (c) 1T1R arrays.

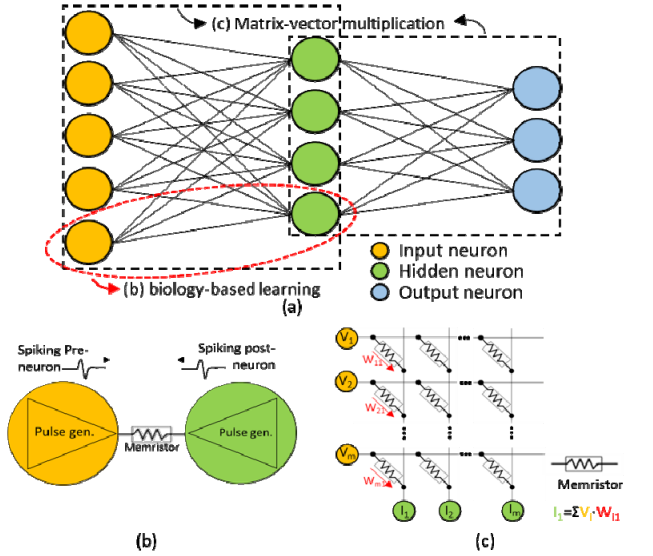



Fig. 9 (a) Simplified model of neural network (NN); (b) using a memristor as a synapse in NN; (c) using a memristor-array for matrix-vector multiplication

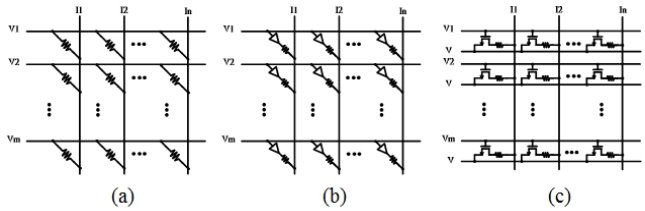



Fig. 10 Memristor array structures

### 4.2. Challenges in Circuit Designs for Emerging Memory based Neuromorphic Chips

The use of emerging memory devices as memristors for neuromorphic computing involves a number of challenges.

(1) Cell resistance behavior:

Many emerging memory devices have a small R-ratio, do not present linear behavior across a wide range of resistance values, and are limited in the number of cell resistance levels. This underlines the need to develop devices that are suitable for implementation as synapses in neuromorphic circuits. Furthermore, emerging memory devices tend to have wide distribution in cell resistance and write times. This makes it particularly difficult to develop circuits for the implementation of synapses.

(2) Area and power overhead:

The write voltage of most memristor devices is higher than the VDD of core devices. Many emerging memory devices require a larger write (SET/RESET) current to achieve a longer data-retention time. As a result, most of the circuits used for weight training require large area and power consumption.

Moreover, due to analog computing behavior, reading a memristor array requires high-accuracy sense amplifiers for analog-to-digital conversion and integrate-and-fire circuits (IFC)[55]-[56]. This results in large area overhead and high

power consumption for small-offset analog-to-digital conversion, whether using ADC or sense amplifiers.

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## 5. Summary

Low write voltage, fast cell switching, and low write power make emerging memory devices highly conducive to beyond von Neumann computing architectures. This paper explores the application of nonvolatile logics and neuromorphic computing based on emerging memory devices. The design of circuits for nvLogics and neuromorphic components involves a number of challenges associated with the characteristics of NVM devices. Novel circuit designs are required to achieve high yields, reduce area overhead, and suppress power consumption.

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