Ultra-Low-Power DLMS Adaptive Filter for Hearing Aid Applications

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***Abstract*—We present an ultra-low-power, delayed least mean square (DLMS) adaptive filter operating in the subthreshold region for hearing aid applications. Subthreshold operation was accomplished by using a parallel architecture with pseudo nMOS logic style. The parallel architecture enabled us to operate the system at a lower clock rate and reduced supply voltage while maintaining the same throughput. Pseudo nMOS logic operating in the subthreshold region (subpseudo nMOS) provided better power-delay product than subthreshold CMOS (sub-CMOS) logic. Simulation results show that the DLMS adaptive filter can operate at 22 kHz using a 400-mV supply voltage to achieve 91% improvement in power compared to a nonparallel, CMOS implementation. To validate the robust operation of subthreshold logics, a 0.35 μm, 23.1 kHz, 21.4 nW, 8×8 carry save array multiplier test chip was fabricated where an adaptive body biasing scheme is used for compensating process, supply and temperature variations. The test chip showed stable operation at a supply voltage of 0.30 V, which is even lower than the threshold voltages of the pMOS (0.82 V) and nMOS (0.67 V) transistors.**

***Index Terms*—Adaptive filter, parallel architecture, sub-pseudo nMOS, subthreshold CMOS (sub-CMOS), subthreshold operation.**

I. Introduction

CURRENT-DAY digital-signal processing (DSP) processors for hearing aid applications feature up to ten independently programmable channels with automatic gain control. Other advanced signal processing techniques such as adaptive filtering are also becoming reality in the next generation hearing aid devices [1]. Such advanced signal processing algorithms are used in hearing- aid devices to resolve the acoustic feedback problem, which happens when the amplified signal from the speaker leaks back and reenters the microphone. This leakage sound, which propagates through the human body or through the clearance between the hearing aid device and the ear canal 1) lowers the effective gain and 2) causes annoying defects such as whistling, screeching or howling that deteriorate the sound quality. Techniques for reducing the acoustic feedback in hearing aids have been investigated in the past [2]–[4]. The various methods fundamentally utilize adaptive noise cancellation to eliminate the acoustic feedback problem. Even with the sophisticated signal processing algorithms, modern hearing aid devices are compact enough to fit in the ear canal. However, due to the miniaturized battery size, completely-in-the-canal hearing aids merely have a battery life of approximately 100 h. This is troublesome because the user would have to recharge the battery every several days. Thus, obtaining the required performance within a limited power budget is the most challenging goal in custom hearing aid device designs.

Hearing aid devices are clearly one of the most suitable application areas for subthreshold logic since ultra-low-power consumption takes first priority, while the clock rate is merely in the kHz range. Digital subthreshold logic has successfully achieved ultra-low-power consumption in areas where performance is of secondary importance [5], [6]. By simply reducing the supply voltage below V_t (threshold voltage), we can operate circuits using only the minute leakage current. Although, the delay rapidly increases, ultra-low power can be achieved without major alteration of the circuit.

Not only does the magnitude of current shrink in the subthreshold region, but the behavior of transistor current also changes. In the strong inversion region, transistors provide high gain in saturation mode where $V_{\rm ds}$ (drain–source voltage) is larger than $V_{\rm gs} - V_t$ ($V_{\rm gs}$: gate–source voltage). In the subthreshold region, however, as long as $V_{\rm ds}$ is larger than approximately 3 *kT/q* ($\sim$78 mV at 300 K), transistors are in the saturation region acting like constant current sources independent of the drain voltage [7]. Due to this nature of weak inversion current, ratio-ed logic, which could only be used in limited areas in the strong inversion region, become attractive in the subthreshold region. Despite the performance benefits, ratio-ed logic (e.g., pseudo nMOS) had to be designed carefully in the strong inversion region due to issues such as degradation in noise margin and increased static power consumption. These issues arise because the V_{OL} (output low voltage) of ratio-ed logic is determined by the on-current ratio between the nMOS pull-down and the pMOS load. Since transistors act like constant current sources in the subthreshold region, simply having a supply lower than V_t can relieve the disadvantages of ratio-ed logic in the strong inversion region. V_{OL} becomes nearly zero since drain voltage has to be lower than approximately 3 *kT/q* ($\sim$78 mV at 300 K) for the drain current to fall. This is the point when the transistor in the subthreshold region fails to behave like a current source. Static power consumption of ratio-ed logic also becomes relatively low since the static current is also weak inversion current. As a result, dynamic power dissipation of ratio-ed logic in the subthreshold region

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becomes comparable to that of static CMOS. Simulations show that pseudo nMOS in subthreshold region (subpseudo nMOS) can have 27% less energy per switching than subthreshold CMOS (sub-CMOS) while providing a near-ideal voltage transfer characteristic (VTC).

In this paper, we demonstrate an ultra-low-power adaptive filter for hearing aid applications, operating in the subthreshold region. For the system to run at a supply voltage lower than V_t, a nonfolded parallel architecture using a delayed least mean square (DLMS) algorithm was realized. Exploiting parallelism, we could operate the circuit at a lower clock rate, reduce the supply voltage, and achieve ultra-low-power dissipation while maintaining the same throughput. Pseudo nMOS logic was used instead of standard CMOS logic to utilize the better power-delay product (PDP). As a result, we were able to scale down the supply voltage to 400 mV and achieve 91% improvement in power compared to a least mean square (LMS) adaptive filter implemented using a folded nonparallel architecture and standard CMOS logic style. We also show test chip measurements of an 8×8 sub-CMOS array multiplier fabricated using TSMC 0.35-μm process technology. Measurements show excellent subthreshold operation of the multiplier even when the supply voltage (0.30 V) is far below the nMOS V_t (0.67 V). Feedback control of substrate bias is also implemented in the test chip to compensate for process, voltage, and temperature (PVT) variations in subthreshold logics.

The remainder of this paper is organized as follows. In Section II, subthreshold characteristics of MOS transistors and advantages of subpseudo nMOS is discussed. Measurement results from a subthreshold logic test chip are also presented. Section III deals with various architectures of adaptive filter implementation, focusing on the advantages of the DLMS algorithm for nonfolded pipelined adaptive filter architectures. Architecture and circuit-level optimization of a DLMS adaptive filter for hearing aid applications is shown in Section IV. Comparisons showing the advantages of a nonfolded parallel architecture using subpseudo nMOS logic are presented in Section V. Conclusions are made in Section VI.

II. Subthreshold Logic

A. Static CMOS Operating in Subthreshold Region

By simply lowering the supply voltage below the transistor V_t, static CMOS circuits can operate while consuming orders of magnitude less power than in the strong inversion region. The operating frequency of subthreshold logics is much lower than regular strong inversion circuits due to the small transistor current. The low-operating frequency (<1 MHz for 0.35-μm process) and low-supply voltage reduces both dynamic power and static power, contributing to significant power savings in subthreshold logics. Both dynamic and static power in subthreshold logics are the power dissipated by the minute weak inversion current given in (1)

$$I_{\rm ds} \propto \mu_{\rm eff} C_{\rm ox} \frac{W}{L} \left(\frac{kT}{q}\right)^2 e^{\frac{(V_{\rm gs}-V_t)}{mkT/q}} \left(1 - e^{-\frac{V_{\rm ds}}{kT/q}}\right) \quad (1)$$

where

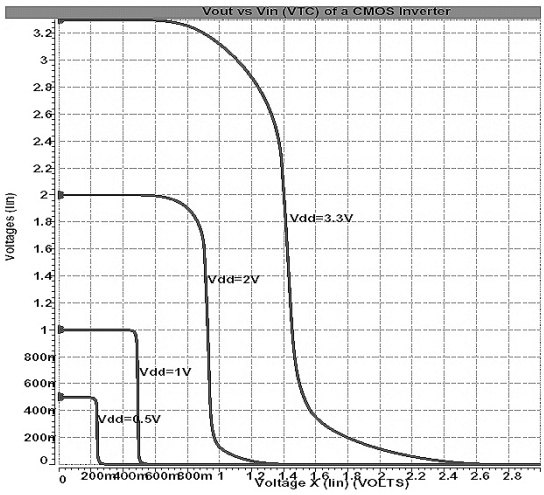

Fig. 1. VTC of a CMOS inverter for different supply voltages. VTC is closer to ideal when supply voltage is below the threshold voltage.

$\mu_{\rm eff}$	effective mobility;
$C_{\rm ox}$	oxide capacitance;
C_d	depletion capacitance;
W	transistor width;
L	transistor length;
m	$1 + C_d/C_{\rm ox}$;
kT/q	thermal voltage;
$V_{\rm gs}$	gate–source voltage;
V_t	threshold voltage;
$V_{\rm ds}$	drain–source voltage.

Characteristics of an MOS transistor in the subthreshold region are significantly different from that in the strong inversion region. The MOS saturation current, which was a quadratic function of the gate voltage (alpha power for short channel devices) in the strong inversion region, becomes an exponential function in the subthreshold region. The merits of regular CMOS logics such as excellent robustness, good noise margin, and low-power consumption are inherited in the subthreshold region. In addition, the operating current dictated by (1) provides higher transconductance ($gm = \partial I_d/\partial V_{\rm gs}$) and improved VTC compared to strong inversion CMOS. Fig. 1 shows the VTC of a static CMOS inverter for different supply voltages. As the supply voltage is lowered below the transistor V_t, the VTC becomes closer to ideal. The reason why VTC of a subthreshold CMOS inverter improves is as follows. When the input voltage of an inverter (push-pull amplifier) is close to the trip point, it has the highest dc gain since both pMOS and nMOS are in saturation region. As the input voltage part from the trip point, either the pMOS or nMOS falls into linear region. Drain current of a transistor in linear region decreases as the drain voltage reduces, lowering the gain of the push-pull amplifier. Drain–source voltage must be higher than $V_{\rm gs} - V_t$ for a strong inversion device to stay in saturation region. However, a device in subthreshold region only requires a drain voltage of 3 *kT/q* (~78 mV at 300 K) to be in saturation mode. Thereafter, the transistor acts as a current source enabling higher gain, better noise margin, and ideal VTC. This is shown in Fig. 1, where the supply voltage is 0.5 V. The poor VTC for supply voltage of 3.3 V is also shown.

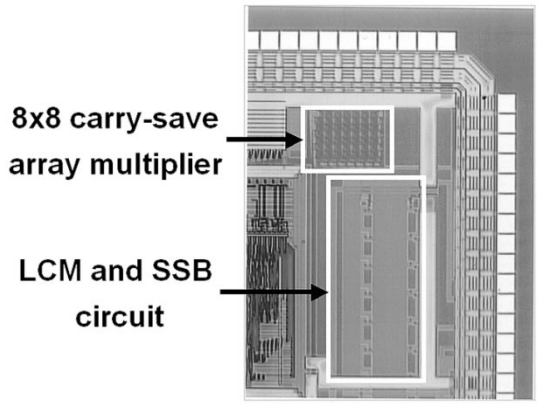

Fig. 2. Die photograph of subthreshold logic test chip with a performance regulation scheme consisting of a LCM and a SSB circuit.

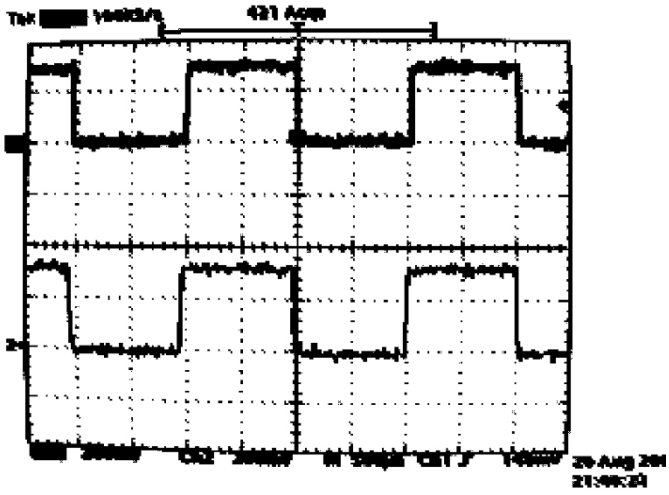

Fig. 3. LSB of the input operand (top) and MSB of the multiplier output (bottom) from the subthreshold logic test chip (200 mV/div, 500 μs/div).

Orders of magnitude lower-power consumption and better VTC are the benefits gained by operating a CMOS circuit in subthreshold region. However, performance of subthreshold logics becomes more sensitive to supply, process, and temperature variations due to the exponential dependency of weak inversion current on $V_{\rm gs}, V_t$ and temperature shown in (1). This can cause up to 4X change in operating frequency in 0.35-μm technology. For stable operation of subthreshold logics in the presence of intrinsic and environmental parameter fluctuations, it is essential to have a feedback mechanism that can regulate the transistor current and ensure robust operation.

B. Subthreshold Logic Test Chip

An 8×8 carry save array multiplier was used as a test vehicle to validate the practicality of subthreshold circuits. Fig. 2 shows the die photograph of the test chip fabricated in Taiwan semiconductor manufacturing company (TSMC) 0.35-μm process technology through MOSIS. Waveforms of the LSB of the input operand (Fig. 3, top) and the MSB of the multiplier output (Fig. 3, bottom) are shown while the test chip is operating in deep subthreshold region with $V_{DD} = 0.30$ V. Threshold voltages of the pMOS and nMOS transistors are 0.82 and 0.67 V, respectively. Power consumption of the test chip was 21.4 nW at 23.1 kHz and 39.7 nW at 40.2 kHz. Since the subthreshold transistor current depends exponentially on the $V_{\rm gs}, V_t$ and temperature, a negative feedback principle is applied to suppress the performance variations due to any changes in these parameters. The compensation scheme is based on variable threshold CMOS (VTCMOS) where a leakage current monitor (LCM) detects the PVT variations and a self-substrate biasing (SSB) circuit applies the appropriate body bias to regulate the circuit performance [8], [9].

Fig. 4 illustrates the feedback circuit consisting of the LCM and SSB. The nMOS LCM uses a turned-on nMOS with a resistor load to detect the device leakage. The resistors are sized so that the bias current gives a stable output voltage in the presence of noise while keeping the static power dissipation of the LCM low. The nMOS device is still in the subthreshold region even with $V_{\rm gs} = V_{DD}$ because the supply voltage is lower than the nMOS threshold voltage. The nMOS leakage is amplified

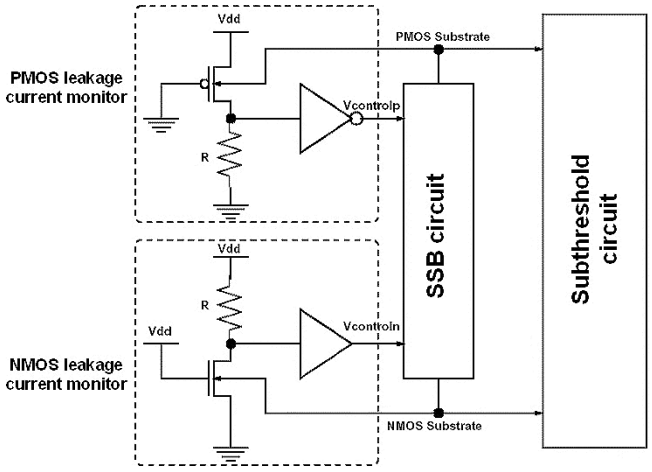

Fig. 4. LCM and SSB circuit to stabilize subthreshold logic performance.

by the $V_{\rm gs}(=V_{DD})$, enabling a fast and stable response. Substrate of the nMOS device is shared with rest of the circuit. If the nMOS device leakage increases due to process skew, supply voltage fluctuations or temperature change, the nMOS LCM activates the SSB by switching the $V_{\rm controln}$ signal. The SSB depicted in Fig. 5 is a multistage charge pump powered by two out-of-phase clock signals coming from a ring oscillator. The resolution of the charge pump is tuned by modifying the size of the pumping capacitors and the diode. As shown in Fig. 5, charge is transferred between nodes N1 and N0, and nodes N1 and N2 when $\bar{\phi}$ is high and low, respectively. When activated, the SSB lowers the nMOS substrate voltage to apply a deeper reverse body bias and reduce the leakage current. If the nMOS leakage becomes less than the leakage threshold, the LCM deactivates the SSB. Then the impact ionization leakage and junction leakage gradually charges the substrate, which in turn slowly increases the nMOS leakage. When the substrate charging continues to happen so as to trip $V_{\rm controln}$ in Fig. 4, the LCM activates the SSB and starts to apply a deeper reverse body bias. Leakage control of pMOS devices is done in the exact similar

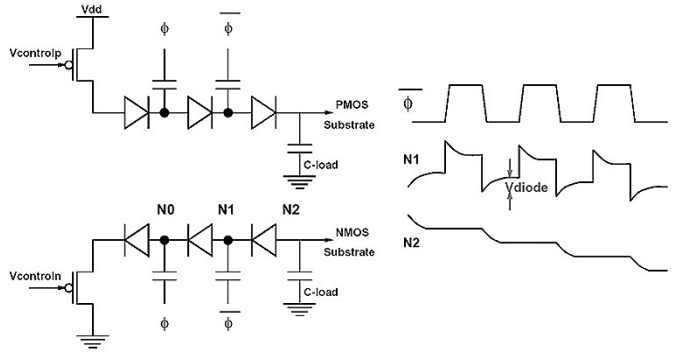

Fig. 5. SSB circuit using charge pumps to generate the reverse body bias voltage on N2.

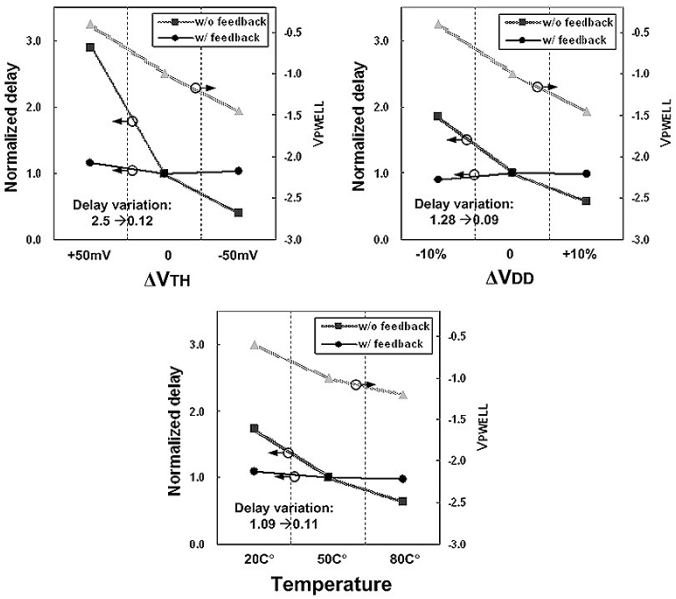

Fig. 6. Delay variation of an 8×8 multiplier with and without a compensating circuit. The optimal body bias voltage generated by the $\mathrm{LCM} + \mathrm{SSB}$ feedback circuit is also shown.

fashion. By intermittently activating the SSB as described, the die leakage can be regulated to a target value and as a result, the delay fluctuations due to PVT variations can be compensated.

Simulation results of the multiplier delay under PVT variations are shown in Fig. 6. Without a compensating scheme, delay of the multiplier in subthreshold operation can vary up to 2.5X for 50 mV V_t variations. By activating the feedback circuit, the nMOS body bias is changed from -1.0 V to -1.45 V and reduces the delay variation to 12%. Similarly for supply and temperature fluctuations, the delay variation is kept below 11% using the adaptive body biasing scheme.

The energy overhead of the regulation circuit was small such that the total power consumption including the multiplier ($V_{DD} = 0.30$ V) is still orders of magnitude less compared to when the multiplier alone is operated at a regular supply ($_{DD} = 3.3$ V). The area of the regulation circuit was three times larger than the multiplier, mostly due to the large area consumed by the poly resistor in the two leakage current monitors. However, if the regulation circuit is applied to a larger functional unit block, the relative area and energy overhead will become much smaller than what is shown for the test chip.

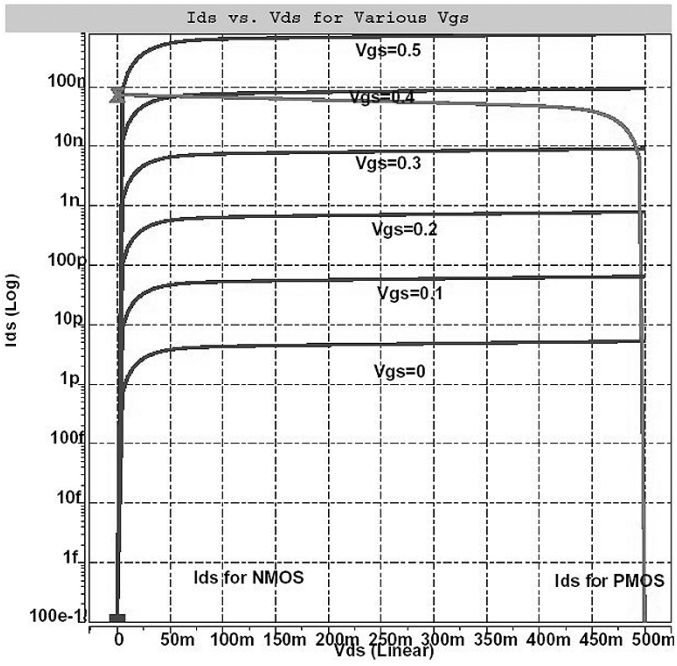

Fig. 7. I_{ds} versus V_{ds} for a subpseudo nMOS inverter ($V_{DD} = 500$ mV).

C. Subpseudo nMOS Logic

Pseudo nMOS logic is faster than static CMOS due to smaller load capacitance, shorter interconnect, and compact area [7]. However, in order to utilize pseudo nMOS logics, the drawbacks of ratio-ed logic such as large static current consumption and degradation in static noise margin should be carefully taken into account. Pseudo nMOS logic in the subthreshold region inherits the advantages it had in the strong inversion such as higher performance and smaller area. In addition to this, the drawbacks of ratio-ed logic are relieved in the subthreshold region. This is mainly because in the subthreshold region, the drain current (I_{ds}) saturates and becomes independent of the V_{ds} for $V_{\mathrm{ds}} > 3$ *kT/q* ($\sim$78 mV at 300 K). Note that a transistor in strong inversion region only enters the saturation region when $\mathrm{V_{ds}} > V_{\mathrm{gs}} - V_t$, which gives a much narrower saturation region, and thus, an undesirable VTC. Fig. 7 shows the transistor *I-V* curves of a subpseudo nMOS inverter where V_{OL} is determined by the intersection point of the pMOS I_{ds} curve and nMOS I_{ds} curve when $V_{\mathrm{gs}} = 0.5$ V. The vertical (horizontal) axis for current (voltage) is in log (linear) scale. Since the nMOS I_{ds} curve ($V_{\mathrm{gs}} = 0.5$ V) only starts to drop when V_{ds} falls below 3 *kT/q* ($\sim$78 mV at 300 K), V_{OL} is also determined to be lower than this voltage ($\sim$78 mV at 300 K). This was not the case in the strong inversion region where V_{OL} had to be fairly high for the linear region current of the nMOS to match the pMOS load current. Consequently, the output voltage of pseudo nMOS in subthreshold region swings for almost rail-to-rail, and thus provides a high noise margin. Fig. 8 shows the VTC of a pseudo nMOS inverter in both strong inversion region and subthreshold region. Increasing the width of the pMOS load causes the V_{OL} to rise and lowers the static noise margin in the strong inversion region. However, VTC of subpseudo-nMOS logic (Fig. 8, right) resembles that of standard CMOS having an ideal V_{OL} which is close to zero.

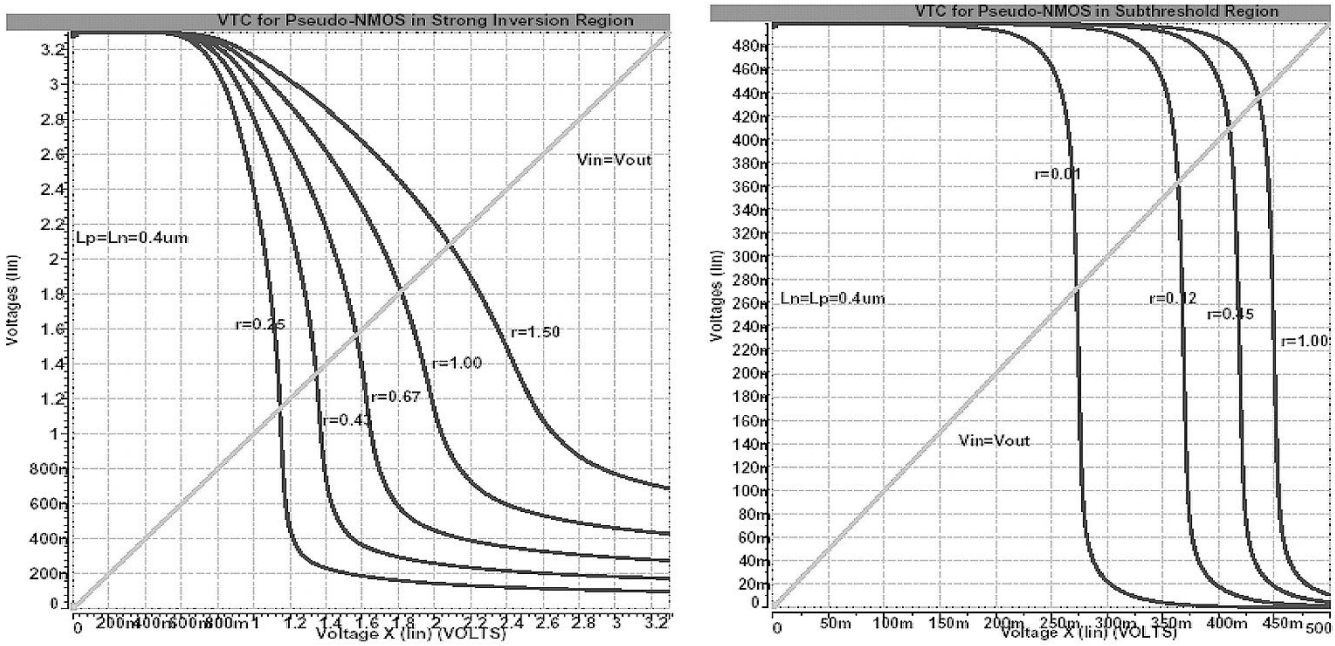

Fig. 8. VTC of a pseudo nMOS inverter in the strong inversion region (left) and in the subthreshold region (right) for different $r\,(=W/L)$ ratios. VTC of a pseudo nMOS inverter becomes similar to that of a CMOS inverter in the subthreshold region.

TABLE I
POWER AND DELAY COMPARISONS OF SUB-CMOS LOGIC AND SUBPSEUDO nMOS LOGIC

	V_{DD}	CMOS			Pseudo NMOS		
		Power	Delay	PDP	Power	Delay	PDP
INV	0.5 V	29 nW	68 ns	1.98 fJ	31 nW	45 ns	1.40 fJ
	3.3 V	0.16 mW	95 ps	15.2 fJ	0.61 mW	71 ps	43.3 fJ
NAND	0.5 V	33 nW	124 ns	4.13 fJ	25 nW	77 ns	1.97 fJ
	3.3 V	0.25 mW	109 ps	27.3 fJ	0.48 mW	78 ps	37.4 fJ
NOR	0.5 V	36 nW	133 ns	4.78 fJ	46 nW	44 ns	2.01 fJ
	3.3 V	0.16 mW	117 ps	18.7 fJ	0.42 mW	65 ps	27.3 fJ

Subpseudo nMOS is also more efficient than sub-CMOS in terms of PDP. Simulation results of pseudo nMOS gates and CMOS gates are compared in Table I for both regular ($V_{DD} = 3.3$ V) and subthreshold ($V_{DD} = 0.5$ V) operation. Even though pseudo nMOS has better performance than CMOS, PDP is much worse because of the large static power dissipation when operated at a regular 3.3 V supply voltage. We observe that in the subthreshold region, pseudo nMOS gives more than 30% improvement in PDP compared to CMOS for each logic gate. The reason behind the lower PDP in subpseudo nMOS is the smaller delay and the relatively small short circuit current in the subthreshold region. In the strong inversion region, the static power consumption was due to the transistor on-current, which is orders of magnitude larger than the off-current. In the subthreshold region, however, the short circuit current is also weak inversion current which is relatively much less significant.

As described, PDP of subpseudo nMOS logics is better than sub-CMOS during active mode since the dynamic power dominates the total power consumption. However, the static power dissipation that is still large compared to sub-CMOS causes the PDP of subpseudo nMOS to be worse than sub-CMOS during standby mode or low-data activity periods. This is because in these periods, the static power dominates the total power consumption. The regulation circuit having adaptive body bias control can be used to further reduce the static power dissipation during standby mode or low data activity periods.

III. DELAYED LMS ALGORITHM FOR PIPELINED ARCHITECTURE

Adaptive filters are successfully applied in a wide variety of areas such as channel equalization, echo cancellation, and adaptive control. LMS algorithm is generally the most popular adaptation technique because of its simplicity and ease of computation [11], [12]. Different architectures of LMS adaptive filters can be considered depending on whether the primary design constraint is area, power or performance.

A. Folded LMS Architecture

First, we consider a folded architecture shown in Fig. 9. This is similar to a general purpose DSP processor core where a single functional unit is used for every computation. Table II describes the LMS and DLMS algorithm, which are widely used in adaptive filters. The equations for the LMS algorithm are given

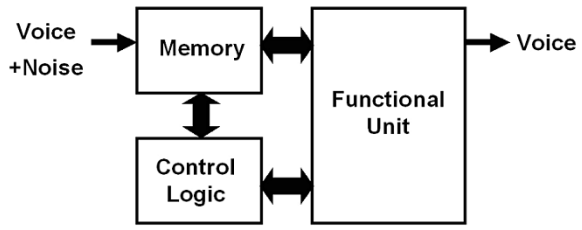

Fig. 9. Folded architecture of an LMS adaptive filter having a single functional unit.

in the lower left section of Table II. It consists of the filter coefficient update operation and FIR filter operation. When the filter length is *N*, the coefficient update operation requires *N* multiplications for deriving $e(n) \times U(n)$, and *N* additions for adding the multiplied results to $W(n)$. Similarly, the finite-impulse response (FIR) filter operation given in Table II requires another *N* multiplications and *N* additions. Hence, the total delay for processing 1 data sample using a folded architecture is $(2N + 1)t_m + 2Nt_a$, where t_m is the multiplier delay and t_a is the adder delay [13]. As the filter length *N* increases, the folded architecture suffers from a large delay since the total delay is proportional to the filter length.

Fig. 9 also shows a static memory array that stores output data from the functional unit. *N* entries are used to save the coefficient vector $W(n)$, and *N* entries are used to save the sample data vector $U(n)$. A control logic that reconfigures the functional unit and provides the correct memory address for the inputs and outputs of the functional unit is also required. The folded architecture has the advantage of small area but requires multiple clock cycles to process 1-data sample. In order to process data at a certain rate, the clock frequency of the nonfolded architecture has to be much higher since a single functional unit is responsible for both, the coefficient update operation and FIR filtering operation. The supply voltage cannot be lowered aggressively since the circuit has to run at a high frequency and, hence, the folded architecture is not a good candidate when power is the primary constraint.

B. Nonfolded DLMS Architecture

A nonfolded parallel architecture having multiple functional units and pipeline stages can be considered for single-cycle execution. Adaptive filter operation can be completed in a single clock cycle, but still the critical path delay is proportional to the filter length. This is due to the time for computing the LMS feedback error $e(n)$ (lower left equation in Table II) which cannot be done in parallel. The filter coefficients can only be updated after the feedback error is ready [14]. Accordingly, the conventional LMS algorithm shown in Table II (left column) cannot be realized in a pipelined fashion even with a nonfolded architecture having multiple functional units and pipeline flip-flops.

The serial LMS algorithm show in Table II (left column) can be transformed using relaxed look-ahead algorithms to achieve single-cycle operation via a parallel architecture with localized coefficient update blocks [15]. Recent studies show that a modified LMS algorithm with a fixed delay inserted into the coefficient update and FIR filtering operation can enable a nonfolded architecture having single cycle operation [16]. The modified LMS algorithm referred to as the delayed LMS (DLMS) algorithm is shown in Table II (right column). This is nothing other than the conventional LMS algorithm using a delayed version of the feedback error and input data for the filter coefficient update operation. The DLMS uses a delay of *N*, which is equal to the filter length. By distributing this delay throughout the nonfolded systolic architecture using retiming techniques, the critical delay can be reduced to from $(2N + 1)t_m + 2Nt_a$ to $2t_m + t_a$. The critical path delay becomes independent of the filter length for the DLMS adaptive filter [16]. The DLMS filter architecture provides a significant improvement in performance by enabling single cycle operation through parallel computation. The DLMS algorithm has drawbacks such as longer convergence time, larger minimum mean square error and longer latency compared to the conventional LMS filter. However, the convergence characteristics can be recovered by having more number of filter taps.

Initially, DLMS algorithm was introduced as a high-performance scheme. However, exploiting parallelism, it can also be used to reduce the active power dissipation for low-power applications. By using a nonfolded architecture instead of a folded architecture, we can obtain the same throughput at a lower-clock frequency. The supply voltage can be further reduced since the operating frequency is low. The area of the nonfolded architecture increases because of the multiple functional units and this slightly increases the static power consumption. However, significant improvement in active power consumption can be achieved through this area-power tradeoff. By utilizing this parallel architecture in hearing aid application, we can scale the supply voltage down to the subthreshold region and achieve ultra-low-power consumption while maintaining the same throughput.

IV. System Implementation

The prototype adaptive filter for hearing aid applications is shown in Fig. 10. An A/D converter samples acoustic data and the sampled data $s[n]$ enters the adaptive filter. After some iterations of the adaptive filter, $y[n]$ only contains the unwanted noise component in $s[n]$. Subtracting $y[n]$ from $s[n]$ leaves only the pure signal component of interest and this is amplified and delivered to the speaker of the hearing aid device. The adaptive filter for hearing aid applications has a few features, which differ from traditional adaptive filters. First, a gain normally up 20 dB is inserted in the loop to amplify the acoustic signal. Secondly, the delayed error output of the filter $x[n]$ is fed back as the reference signal instead of an external reference signal coming in. And last, a delay Δ_X is inserted to compensate for the acoustic feedback delay [1]. This delay element ensures that only the delayed component of the previous filter output gets filtered from the incoming data samples [2].

For our prototype filter design, a filter length of 12 and a compensation delay (Δ_X) of 22 cycles was used. Word length of each data signal was 8 b and the amplifying gain was set to 1. Implementation of the adaptive filter was completed for both folded and nonfolded architectures to understand the power, performance, and area tradeoffs. Each block of the folded architecture shown in Fig. 9 was described using VHDL. In our design

TABLE II
COMPARISON OF LMS AND DLMS ALGORITHM

	LMS (Least mean square)	DLMS (Delayed least mean square)
# of FU	1	N
Critical path delay	$(2N+1)t_m + 2N t_a$	$2 t_m + t_a$
Algorithm	$W(n+1) = W(n) + \mu e(n)U(n)$ $e(n) = d(n) - W^T(n)U(n)$	$W(n+1) = W(n) + \mu e(n-N)U(n-N)$ $e(n-N) = d(n-N) - W^T(n-N)U(n-N)$

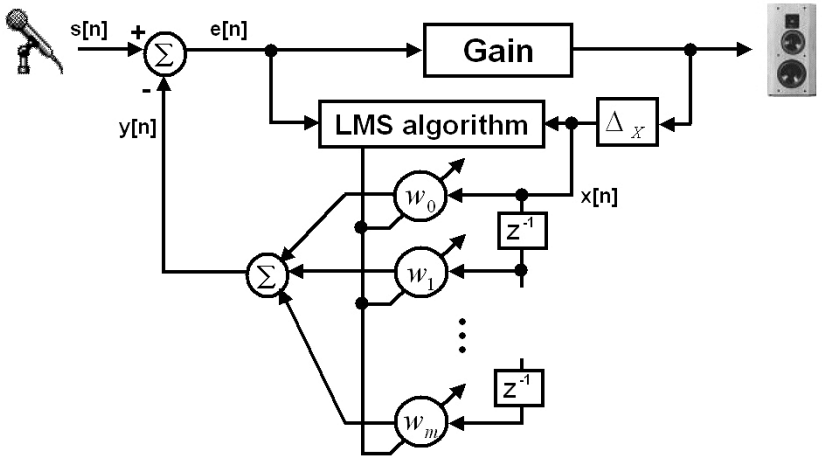

Fig. 10. Block diagram of adaptive filter for hearing aid applications.

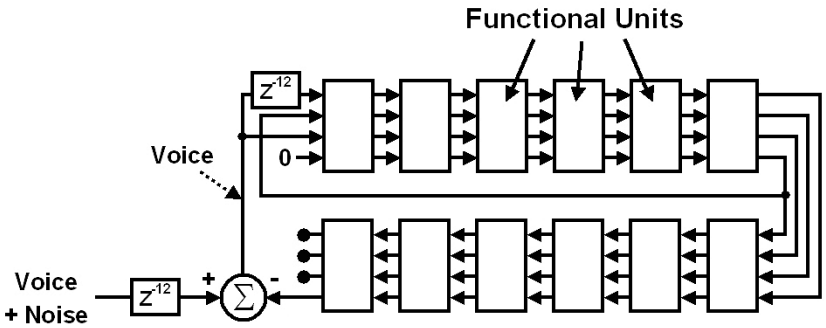

Fig. 11. Nonfolded architecture of a DLMS adaptive filter having multiple function units. The functional unit module shown in Fig. 10 is cascaded to implement the 12 tap DLMS adaptive filter.

where a filter length of 12 is used, it turned out that 34 clock cycles are needed for a single data sample to be processed. Logic synthesis was done using CMUs standard CMOS library. HP 0.35 μm bulk CMOS technology was used for extracting the layout and running HSPICE simulations. The nonfolded DLMS architecture is shown in Fig. 11, where a basic functional unit module is cascaded for the full DLMS operation. The functional unit module shown in Fig. 12 contains three 8-bit multipliers and two 8-bit adders and is dedicated for the filter coefficient update and FIR filtering operation for each filter tap. For simplicity, the multiplier in Fig. 12 with μm (learning factor) as one of its inputs, is implemented using a shifter. Conventional master-slave flip-flops are used for the delay elements in the signal flow graph. Since the filter has 12 coefficients, 12 modules were cascaded to achieve the complete DLMS filtering operation. Similar to the implementation of the folded architecture, the functional unit module of the nonfolded design was described in VHDL. The maximum throughput of the nonfolded DLMS filter is dictated by the critical path delay of the functional unit module. From the signal flow graph of the module shown in Fig. 12, the critical path contains two multipliers and one adder giving a total throughput of $1/(2t_m + t_a)$ for the DLMS adaptive filter.

To verify the merits of subpseudo nMOS, both pseudo nMOS and standard CMOS logic styles were implemented. For the pseudo nMOS implementation, we designed a new pseudo nMOS cell library by substituting a grounded pMOS device for the whole pull-up network in the layouts of the CMU standard

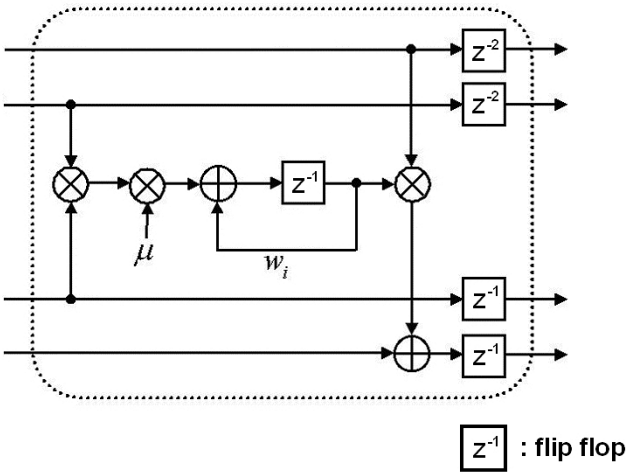

Fig. 12. Functional unit module for the nonfolded pipelined DLMS adaptive filter. This module is a dedicated processing unit for the filter coefficient update and FIR filtering operation of a single filter tap.

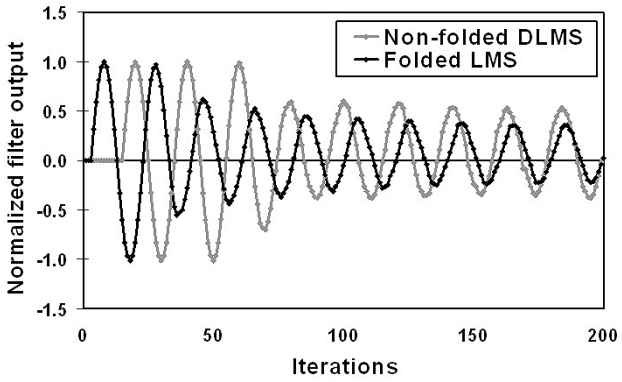

Fig. 13. Normalized filter outputs of the folded and nonfolded adaptive filter architectures.

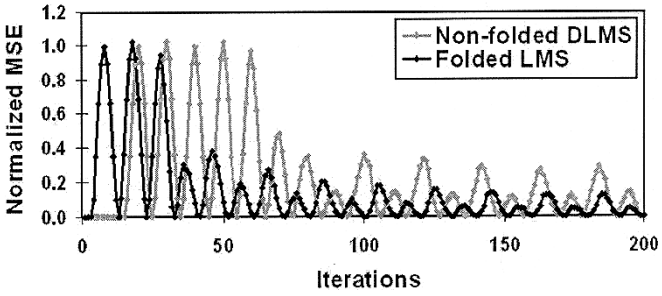

Fig. 14. Normalized mean square error (MSE) of the folded and nonfolded adaptive filter architectures.

library cells. Transistor sizing of pseudo nMOS was done in an aggressive fashion geared toward higher performance. The W/L ratio between pMOS and nMOS of the pseudo nMOS cell library was 1.0. Although this is inappropriate in the strong inversion region due to the low static noise margin, the subthreshold characteristics in Fig. 8 show excellent static noise margins for pseudo nMOS even for heavily skewed P/N ratios. Namely, this strategy is possible for pseudo nMOS in subthreshold region since the static noise margin is less sensitive to sizing than in the strong inversion region.

V. Simulation Results

The normalized output waveforms of the folded LMS architecture and nonfolded DLMS architecture are shown in Fig. 13. The input data was a 1.0 kHz sinusoidal signal and the sampling frequency was 22 kHz. The folded LMS filter shows a faster convergence time and smaller convergence error compared to the nonfolded DLMS filter. This can also be noticed in Fig. 14, where the minimum mean square error (MSE) is shown for both filter architectures. The convergence time is longer and its convergence value is larger for the nonfolded DLMS filter. Better convergence characteristics can be achieved by having more number of filter taps for the nonfolded DLMS filter.

Table III shows the system attributes of the three different implementations having the same throughput of 22 kHz. HSPICE (BSIM3 models) was used to derive the delay and energy of the folded and nonfolded filter architectures. Due to the large number of transistors, simulations were done separately for each functional block of the nonfolded filter. Summing up the power consumption of each functional unit module gave the total filter power consumption. The input signals for each functional unit module were obtained using HDL simulations.

Since it takes one clock cycle to process one input data for the nonfolded architecture, clock frequency is the same as the input data rate (22 kHz). Whereas for the folded architecture, it requires a clock frequency of 748 kHz ($=34 \times 22$ kHz) since 34 clock cycles are needed for the LMS operation of each input data using a single functional unit. The supply voltage of the folded architecture was 44% higher than the nonfolded architecture so that it can run at a higher clock rate. The number of transistors increased by a factor of 3.6 for the nonfolded architecture due to the multiple functional units. This caused the static leakage to increase from 0.19–0.48 nJ. However, the low supply voltage and slow clock frequency of the nonfolded architecture attributed to 87% savings in total active power consumption.

The table also shows the comparison between nonfolded architecture using different logic styles: sub-CMOS and subpseudo nMOS. The sub-CMOS implementation could operate at a supply voltage of 450 mV, which is below the V_t. Energy efficiency was 2.80 nJ/operation where 17% is static power. By using subpseudo nMOS logic, we could further lower the supply voltage down to 400 mV and achieve 27% improvement in energy consumption per operation compared to sub-CMOS logic. The better performance of subpseudo nMOS enabled the circuit to meet the target frequency of 22 kHz at a lower-supply voltage. Dynamic power of the subpseudo nMOS implementation was less than half of sub-CMOS due to less load capacitance and lower supply voltage. The static power consumption of subpseudo nMOS was more than twice of the sub-CMOS implementation. The energy results in Table III are when the clock period is equal to the critical path delay. In case, the clock period is longer and the data activity is low, PDP of the subpseudo nMOS becomes larger than that of sub-CMOS due to the large static power. Leakage reduction schemes such as body biasing or power gating can be used to suppress the static power during standby mode.

TABLE III
SIMULATION RESULTS FOR THREE ADAPTIVE FILTER IMPLEMENTATIONS

	Clock frequency	V_{DD}	Energy per operation				Transistor count
			dynamic	static	clock	total	
Folded standard CMOS (LMS)	748 kHz	650 mV	18.89 nJ	0.19 nJ	2.81 nJ	21.71 nJ	31k
Non-folded Sub-CMOS (DLMS)	22 kHz	450 mV	1.98 nJ	0.48 nJ	0.34 nJ	2.80 nJ	111k
Non-folded Sub-Pseudo NMOS (DLMS)	22 kHz	400 mV	0.79 nJ	0.99 nJ	0.29 nJ	2.05 nJ	86k

VI. CONCLUSION

As modern hearing aid devices are miniaturized, acoustic signals must be processed within a small power budget due to the reduced battery size. At the same time, sophisticated signal-processing algorithms such as subband filtering or adaptive noise cancellation are required for better quality of sound. In this paper, we introduced different architectures and logic styles for ultra-low-power adaptive filters in hearing aid applications. A nonfolded architecture with multiple functional units was proposed to achieve ultra-low-power consumption by operating the circuit at a supply voltage even lower than V_t. We were able to maintain the same throughput with less power dissipation by reducing both the clock rate and supply voltage. Comparisons between the folded and nonfolded filter architectures show that 87% active power reduction can be achieved by trading off area for power. Though the number of transistors increased around 3.6 times, this unrolling strategy could enable subthreshold operation of the chip for ultra-low-power dissipation. We also explored the suitability of subpseudo nMOS. Due to the nature of transistor current in the subthreshold region, subpseudo nMOS proved to be comparable to CMOS in terms of robustness, noise margin and power consumption. At the same time, pseudo nMOS logic inherits all the advantages it had in the normal strong inversion region, such as better performance, less area, and reduced routing. As a result, subpseudo nMOS showed 27% higher energy efficiency than sub-CMOS in our prototype implementation. By applying architecture and circuit level optimization techniques, the nonfolded DLMS filter using subpseudo nMOS logic was capable of operating in the subthreshold region consuming ultra-low power with a desired performance.

When a lower drain voltage is applied to short channel devices, the drain induced barrier lowering (DIBL) causes the V_t to rise. Hence, subthreshold logics become more power efficient for scaled technologies since lowering the supply voltage can also reduce the leakage power dissipation. However, regulation of subthreshold logic performance becomes more challenging since channel length variations and doping density fluctuations worsen for sub-90 nm technology nodes. Solving these issues can be future research areas.

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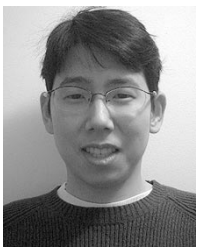

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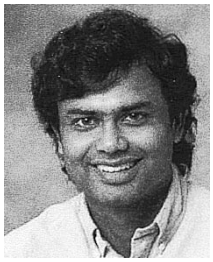

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