深 圳 市 金 逸 晨 电 子 有 限 公 司

LCD MODULE

MODULE NO. :

0.96-8pin13p_ips

Customer:
Approved By(核准) :

深圳市金逸晨电子有限公司		
Approved By(核准) :	Checked By(审核) :	Prepared By(编写) :

RECORDS OF REVISION

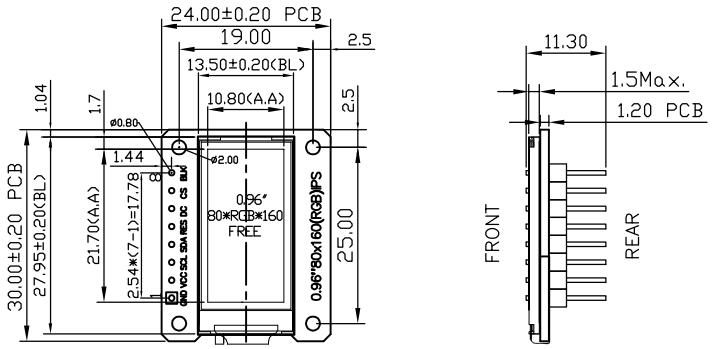
(修订记录)

Part Number (产品型号)	Revision (版本)	Revision Content (修订内容)	Revised on (修订日期)
0.96-8PIN13P_IPS	V1.0	第一次发行	2019-11-18

CONTENTS

VER.	REVISED RECORD	DATA
V1.0	第一次发行	2020-01-03

1.外形图



2.功能&特性

2-1. 分辨率: 80*RGB*160
2-2. 面板类型:IPS
2-3. 颜色：全彩262K
2-4. 显示模式：普通黑色
2-5. LCM工作电压(VCC_IN): 2.5~3.3V
屏工作电压(Vddio):1.65~3.3V
2-6. 背光1白LED,Vbl=2.8~3.0V,If=15mA(20mAmax.)
2-7. 工作温度: -20℃~70℃
2-8. 储存温度: -30℃~80℃
2-9. 连接方式/驱动IC:COG/ST7735S
13P间距0.7mm 焊接;
2-10. 接口：4线SPI
2-11. 视角方向：全视角

3.机械规格

3-1. 模块尺寸: 10.8mm(L)*21.7mm(W)*11.3mmMAX(H)
3-2. 有效区域(A/A): 10.8mm(L)*21.7mm(W)
3-3. 点距离: 0.135mm(L)*0.1356mm(W)

NO.	Symbol
1	GND
2	VCC
3	SCL
4	SDA
5	RES
6	DC
7	CS
8	BLK

SHEET: 1 of 1

APPROVALS		DATE
DWN	ZJP	2020-01-03
CHK		
APP		

金逸晨电子有限公司

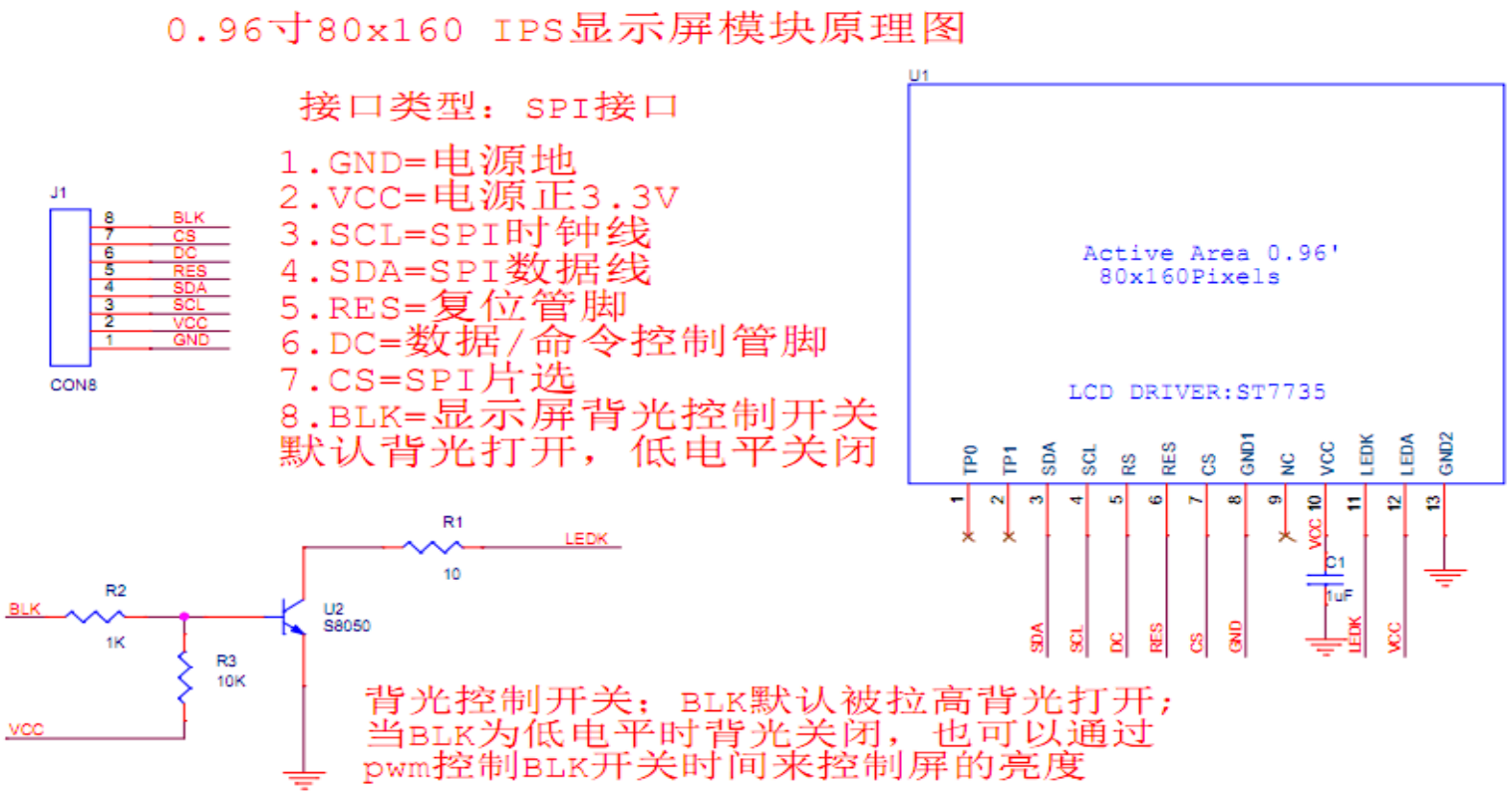
MODEL NUMBER : 0.96-8pin13p_ips_LCM

SCALE: Unspecified TOL: 0.1

UNITS: MM

DO NOT SCALE THIS DRAWING.

4. 原理图：



注意：电路及元件值仅作参考

5. 引脚说明：

Pin no.	Symbol	Function
1	BLK	背光控制开关，默认拉高背光打
2	CS	片选
3	DC	命令/数据
4	RES	复位
5	SDA	数据
6	SCL	时钟
7	VCC	电源正极
8	GND	电源负极

6. 电气特性

6-1 DC电气特性

6-1.1: **Absolute Maximum Ratings**（绝对最大额定值）

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage (I/O)	VDD	-0.3	4.6	V	
Analog Supply Voltage	VDDIO	-0.3	4.6	V	
Logic Input Voltage	VIN	-0.3	VDD+0.3	V	
Operation Temperature	Top	-20	70	℃	
Storage Temperature	Tst	-30	80	℃	

6-1.2: **Model Characteristics**（模块特性）

Parameter	Symbol	Min	TYP	MAX	Unit	Notes
Voltage for LED backlight	V_{bL}	2.8	--	3.0	V	
Supply Voltage for Logic	VDD	2.5	2.8	3.3	V	
Interface Operation Voltage	VDDIO	1.65	1.8	3.3	V	
Gate Driver High Voltage	VGH	10	-	15	*V*	
Gate *Driver Low* Voltage	VGL	-13	-	-7.5	V	
Operating Current for V_{DD}	I_{DD}	--	2	3	mA	
Current for LED backlight	I_{bL}	15	-	20	mA	1 LED
Brightness	L_{br}	250	300	--	cd/m^2	
Sleep In Mode VDD	I_{dd}	--	15	30	uA	
Sleep In Mode VDDIO	I_{ddio}	--	5	10	uA	

6-2 AC电气特性

6-2.1、 Serial Interface Timing Characteristics: (4-wire SPI)

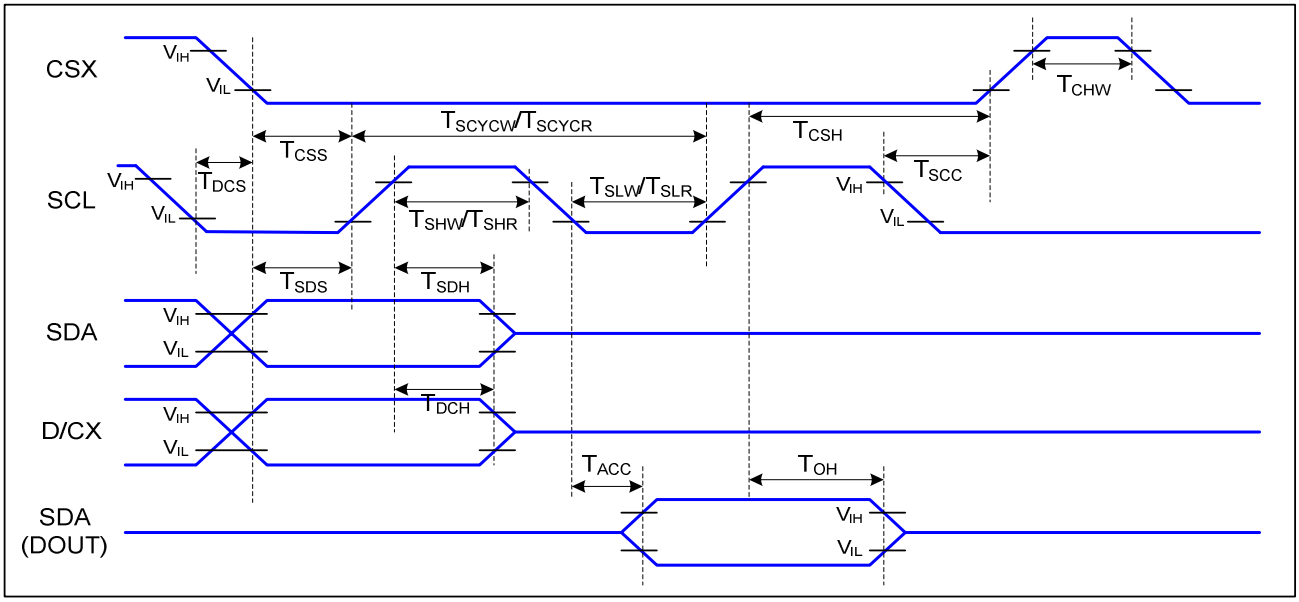


Figure 7 4-line Serial Interface Timing

Ta=25 ℃, VDDI=1.65~3.7V, VDD=2.5~4.8V

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	TCSS	Chip Select Setup Time (Write)	45		ns	
	TCSH	Chip Select Hold Time (Write)	45		ns	
	TCSS	Chip Select Setup Time (Read)	60		ns	
	TSCC	Chip Select Hold Time (Read)	65		ns	
	TCHW	Chip Select “H” Pulse Width	40		ns	
SCL	TSCYCW	Serial Clock Cycle (Write)	66		ns	-Write Command & Data Ram
	TSHW	SCL “H” Pulse Width (Write)	15		ns	
	TSLW	SCL “L” Pulse Width (Write)	15		ns	
	TSCYCR	Serial Clock Cycle (Read)	150		ns	-Read Command & Data Ram
	TSHR	SCL “H” Pulse Width (Read)	60		ns	
	TSLR	SCL “L” Pulse Width (Read)	60		ns	
D/CX	TDCS	D/CX Setup Time	10		ns	
	TDCH	D/CX Hold Time	10		ns	
SDA (DIN) (DOUT)	TSDS	Data Setup Time	10		ns	For Maximum CL=30pF For Minimum CL=8pF
	TSDH	Data Hold Time	10		ns	
	TACC	Access Time	10	50	ns	
	TOH	Output Disable Time	15	50	ns	

Table 7 4-line Serial Interface Characteristics

Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

7. 指令表

COMMAND TABLE

System Function Command List (1)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
NOP	0	0	↑	1	-	0	0	0	0	0	0	0	0	(00h)	No Operation
SWRESET	0	0	↑	1	-	0	0	0	0	0	0	0	1	(01h)	Software Reset
RDDID	0	0	↑	1	-	0	0	0	0	0	1	0	0	(04h)	Read Display ID
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
		1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		ID1 Read
		1	1	↑	-	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20		ID2 Read
		1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		ID3 Read
RDDST	0	0	↑	1	-	0	0	0	0	1	0	0	1	(09h)	Read Display Status
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
		1	1	↑	-	BSTON	MY	MX	MV	ML	RGB	MH	ST24		-
		1	1	↑	-	ST23	IFPF2	IFPF1	IFPF0	IDMON	PTLON	SLOUT	NORON		-
		1	1	↑	-	VSSON	ST14	INVON	ST12	ST11	DISON	TEON	GCS2		-
		1	1	↑	-	GCS1	GCS0	TEM	ST4	ST3	ST2	ST1	ST0		-
RDDPM	0	0	↑	1	-	0	0	0	0	1	0	1	0	(0Ah)	Read Display Power Mode
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
		1	1	↑	-	BSTON	IDMON	PTLON	SLPOUT	NORON	DISON	-	-		-
RDD MADCTL	0	0	↑	1	-	0	0	0	0	1	0	1	1	(0Bh)	Read Display MADCTL
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
		1	1	↑	-	MY	MX	MV	ML	RGB	MH	-	-		-
RDD COLMOD	0	0	↑	1	-	0	0	0	0	1	1	0	0	(0Ch)	Read Display Pixel Format
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
		1	1	↑	-	0	0	0	0	-	IFPF2	IFPF1	IFPF0		-
RDDIM	0	0	↑	1	-	0	0	0	0	1	1	0	1	(0Dh)	Read Display Image Mode
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
		1	1	↑	-	VSSON	D6	INVON	-	-	GCS2	GCS1	GCS0		-
RDDSM	0	0	↑	1	-	0	0	0	0	1	1	1	0	(0Eh)	Read Display Signal Mode
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
		1	1	↑	-	TEON	TEM	-	-	-	-	-	-		-
RDDSDR	0	0	↑	1	-	0	0	0	0	1	1	1	1	(0Fh)	Read Display Self-diagnostic result
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
		1	1	↑	-	RELD	FUND	ATTD	BRD	-	-	-	-		-

"-": Don't care

System Function Command List (2)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
SLPIN	0	0	↑	1	-	0	0	0	1	0	0	0	0	(10h)	Sleep In & Booster Off
SLPOUT	0	0	↑	1	-	0	0	0	1	0	0	0	1	(11h)	Sleep Out & Booster On
PTLON	0	0	↑	1	-	0	0	0	1	0	0	1	0	(12h)	Partial Mode On
NORON	0	0	↑	1	-	0	0	0	1	0	0	1	1	(13h)	Partial Off (Normal)
INVOFF	0	0	↑	1	-	0	0	1	0	0	0	0	0	(20h)	Display Inversion Off (Normal)
INVON	0	0	↑	1	-	0	0	1	0	0	0	0	1	(21h)	Display Inversion On
GAMSET	0	0	↑	1	-	0	0	1	0	0	1	1	0	(26h)	Gamma Curve Select
		1	↑	1	-	-	-	-	-	GC3	GC2	GC1	GC0		-
DISPOFF	0	0	↑	1	-	0	0	1	0	1	0	0	0	(28h)	Display Off
DISPON	0	0	↑	1	-	0	0	1	0	1	0	0	1	(29h)	Display On
CASET	0	0	↑	1	-	0	0	1	0	1	0	1	0	(2Ah)	Column Address Set
		1	↑	1	-	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8		X Address Start: 0≦XS≦X
		1	↑	1	-	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0		
		1	↑	1	-	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8		X Address End: S≦XE≦X
		1	↑	1	-	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0		
RASET	0	0	↑	1	-	0	0	1	0	1	0	1	1	(2Bh)	Row Address Set
		1	↑	1	-	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8		Y Address Start: 0≦YS≦Y
		1	↑	1	-	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0		
		1	↑	1	-	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8		Y Address End:S≦YE≦Y
		1	↑	1	-	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0		
RAMWR	0	0	↑	1	-	0	0	1	0	1	1	0	0	(2Ch)	Memory Write
		1	↑	1	-	D7	D6	D5	D4	D3	D2	D1	D0		Write Data
RGBSET	0	0	↑	1	-	0	0	1	0	1	1	0	1	(2Dh)	LUT for 4k,65k,262k Color display
		1	↑	1	-	-	-	R005	R004	R003	R002	R001	R000		Red Tone 0
		1	↑	1	-	-	-	:	:	:	:	:	:		:
		1	↑	1	-	-	-	Ra5	Ra4	Ra3	Ra2	Ra1	Ra0		Red Tone “a”
		1	↑	1	-	-	-	G005	G004	G003	G002	G001	G000		Green Tone 0
		1	↑	1	-	-	-	:	:	:	:	:	:		:
		1	↑	1	-	-	-	Gb5	Gb4	Gb3	Gb2	Gb1	Gb0		Green Tone “b”
		1	↑	1	-	-	-	B005	B004	B003	B002	B001	B000		Blue Tone 0
		1	↑	1	-	-	-	:	:	:	:	:	:		:
		1	↑	1	-	-	-	Bc5	Bc4	Bc3	Bc2	Bc1	Bc0		Blue Tone “c”
RAMRD	0	0	↑	1	-	0	0	1	0	1	1	1	0	(2Eh)	Memory Read
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
		1	1	↑	-	D7	D6	D5	D4	D3	D2	D1	D0		Read Data

“-“: Don’t care

System Function command List (3)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
PTLAR	10.1.25	0	↑	1	-	0	0	1	1	0	0	0	0	(30h)	Partial Start/End Address Set
		1	↑	1	-	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8		Partial Start Address (0,1,2, ..P)
		1	↑	1	-	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0		
		1	↑	1	-	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8		Partial End Address (0,1,2, .., P)
		1	↑	1	-	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0		
SCRLAR	10.1.26	0	↑	1	-	0	0	1	1	0	0	1	1	(33h)	Scroll area set
		1	↑	1	-	-	-	-	-	-	-	-	-		Top fixed area (0,1, 2, .., 161)
		1	↑	1	-	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0		
		1	↑	1	-	-	-	-	-	-	-	-	-		Vertical scroll area (0,1, 2, .., 161)
		1	↑	1	-	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0		
		1	↑	1	-	-	-	-	-	-	-	-	-		Bottom fixed area (0,1, 2, .., 161)
		1	↑	1	-	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0		
TEOFF	10.1.27	0	↑	1	-	0	0	1	1	0	1	0	0	(34h)	Tearing effect line off
TEON	10.1.28	0	↑	1	-	0	0	1	1	0	1	0	1	(35h)	Tearing Effect Mode Set & on
		1	↑	1	-	-	-	-	-	-	-	-	TEM		Mode1: TEM="0" Mode2: TEM="1"
MADCTL	10.1.29	0	↑	1	-	0	0	1	1	0	1	1	0	(36h)	Memory Data Access Control
		1	↑	1	-	MY	MX	MV	ML	RGB	MH	-	-		-
VSCSAD	10.1.30	0	↑	1	-	0	0	1	1	0	1	1	1	(37h)	Scroll Start Address of RAM
		1	1	1	-	-	-	-	-	-	-	-			SSA=0,1,2,…,161
		1	1	1	-	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0		
IDMOFF	10.1.31	0	↑	1	-	0	0	1	1	1	0	0	0	(38h)	Idle Mode Off
IDMON	10.1.32	0	↑	1	-	0	0	1	1	1	0	0	1	(39h)	Idle Mode On
COLMOD	10.1.33	0	↑	1	-	0	0	1	1	1	0	1	0	(3Ah)	Interface Pixel Format
		1	↑	1	-	-	-	-	-	-	IFPF2	IFPF1	IFPF0		Interface Format
RDID1	10.1.34	0	↑	1	-	1	1	0	1	1	0	1	0	(DAh)	Read ID1
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
		1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		Read Parameter
RDID2	10.1.35	0	↑	1	-	1	1	0	1	1	0	1	1	(DBh)	Read ID2
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
		1	1	↑	-	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20		Read Parameter
RDID3	10.1.36	0	↑	1	-	1	1	0	1	1	1	0	0	(DCh)	Read ID3
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
		1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		Read Parameter

"-": Don't care

Note 1: After the H/W reset by RESX pin or S/W reset by SWRESET command, each internal register becomes default state (Refer "RESET TABLE" section)

Note 2: Undefined commands are treated as NOP (00 h) command.

Note 3: B0 to D9 and DA to F are for factory use of driver supplier.

Note 4: Commands 10h, 12h, 13h, 20h, 21h, 26h, 28h, 29h, 30h, 33h, 36h (ML parameter only), 37h, 38h and 39h are updated during V-sync when Module is in Sleep Out Mode to avoid abnormal visual effects. During Sleep In mode, these commands are updated immediately. Read status (09h), Read Display Power Mode (0Ah), Read Display MADCTL (0Bh), Read Display Pixel Format (0Ch), Read Display Image Mode (0Dh), Read Display Signal Mode (0Eh).

更详细具全的指令说明可参阅芯片ST7735S规格书。