1. Description

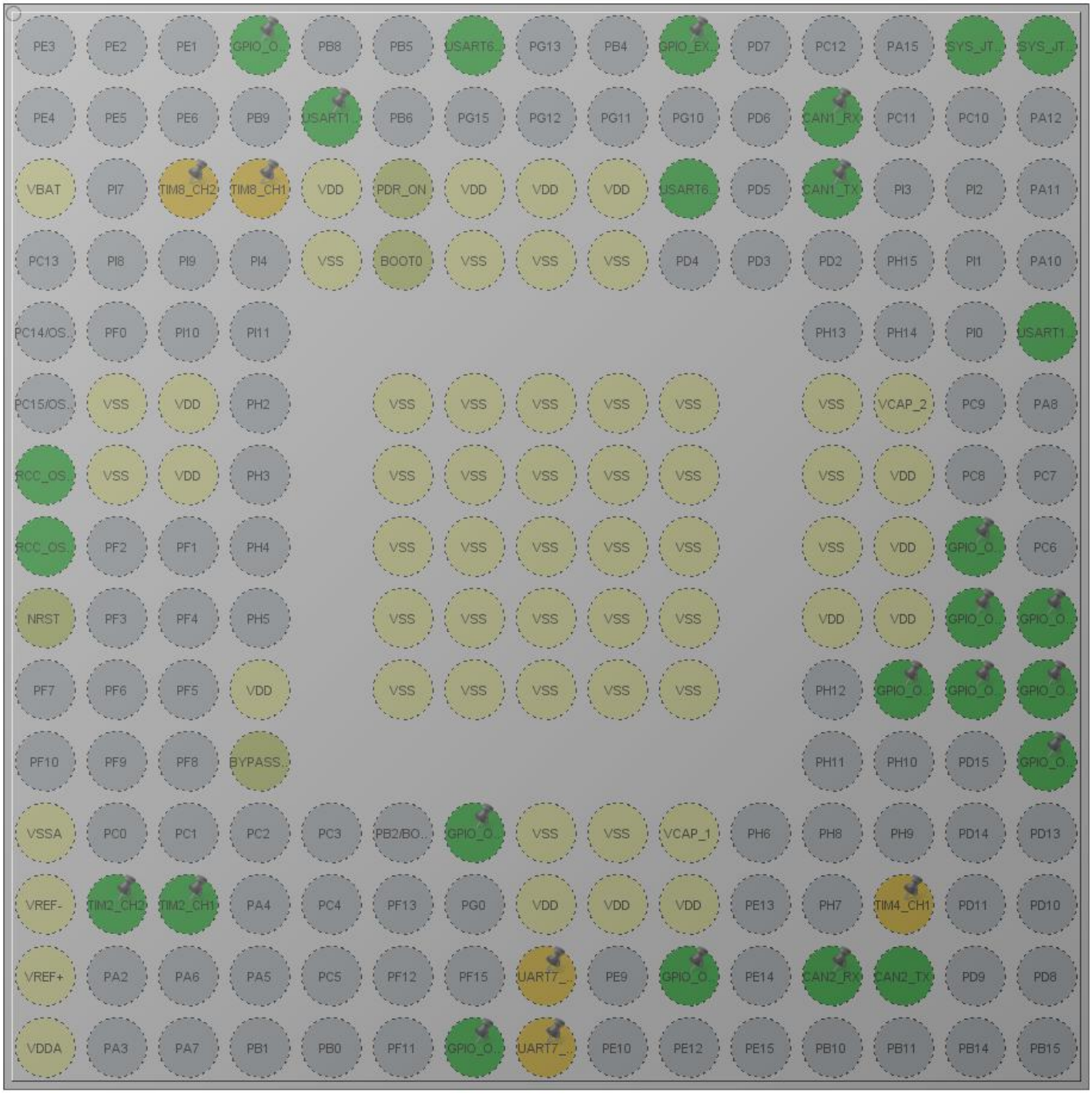
1.1. Project

Project Name	2019RC_MR1
Board Name	custom
Generated with:	STM32CubeMX 5.0.1
Date	02/16/2019

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F427/437
MCU name	STM32F427IIHx
MCU Package	UFBGA176
MCU Pin number	201

2. Pinout Configuration



UFBGA176 +25 (Top view)

3. Pins Configuration

Pin Number UFBGA176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
A4	PE0 *	I/O	GPIO_Output	
A7	PG14	I/O	USART6_TX	
A10	PB3	I/O	GPIO_EXTI3	
A14	PA14	I/O	SYS_JTCK-SWCLK	
A15	PA13	I/O	SYS_JTMS-SWDIO	
B5	PB7	I/O	USART1_RX	
B12	PD0	I/O	CAN1_RX	
C1	VBAT	Power		
C3	PI6 **	I/O	TIM8_CH2	
C4	PI5 **	I/O	TIM8_CH1	
C5	VDD	Power		
C6	PDR_ON	Reset		
C7	VDD	Power		
C8	VDD	Power		
C9	VDD	Power		
C10	PG9	I/O	USART6_RX	
C12	PD1	I/O	CAN1_TX	
D5	VSS	Power		
D6	BOOT0	Boot		
D7	VSS	Power		
D8	VSS	Power		
D9	VSS	Power		
E15	PA9	I/O	USART1_TX	
F2	VSS	Power		
F3	VDD	Power		
F6	VSS	Power		
F7	VSS	Power		
F8	VSS	Power		
F9	VSS	Power		
F10	VSS	Power		
F12	VSS	Power		
F13	VCAP_2	Power		
G1	PH0/OSC_IN	I/O	RCC_OSC_IN	
G2	VSS	Power		
G3	VDD	Power		
G6	VSS	Power		

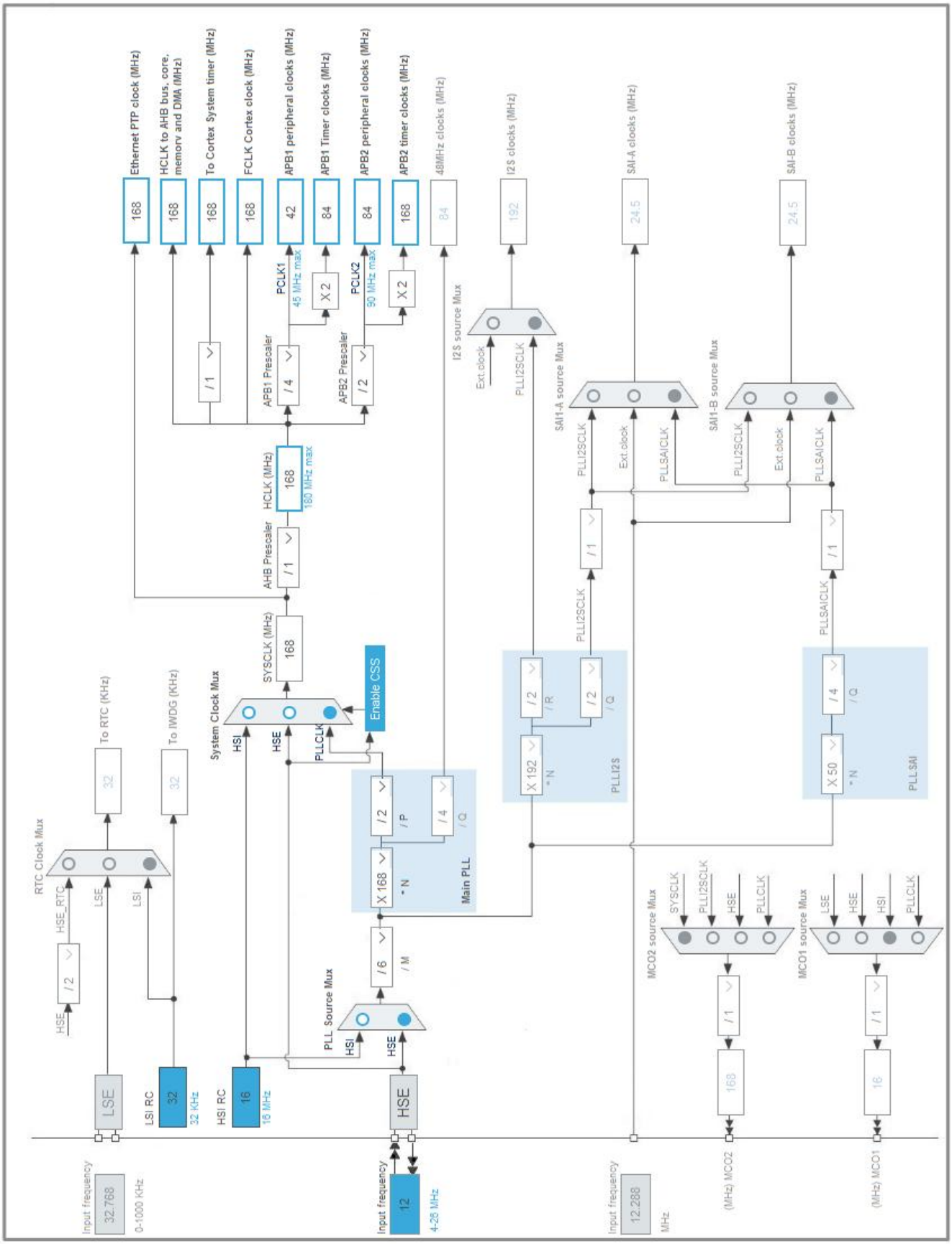
Pin Number UFBGA176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
G7	VSS	Power		
G8	VSS	Power		
G9	VSS	Power		
G10	VSS	Power		
G12	VSS	Power		
G13	VDD	Power		
H1	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
H6	VSS	Power		
H7	VSS	Power		
H8	VSS	Power		
H9	VSS	Power		
H10	VSS	Power		
H12	VSS	Power		
H13	VDD	Power		
H14	PG8 *	I/O	GPIO_Output	
J1	NRST	Reset		
J6	VSS	Power		
J7	VSS	Power		
J8	VSS	Power		
J9	VSS	Power		
J10	VSS	Power		
J12	VDD	Power		
J13	VDD	Power		
J14	PG7 *	I/O	GPIO_Output	
J15	PG6 *	I/O	GPIO_Output	
K4	VDD	Power		
K6	VSS	Power		
K7	VSS	Power		
K8	VSS	Power		
K9	VSS	Power		
K10	VSS	Power		
K13	PG5 *	I/O	GPIO_Output	
K14	PG4 *	I/O	GPIO_Output	
K15	PG3 *	I/O	GPIO_Output	
L4	BYPASS_REG	Reset		
L15	PG2 *	I/O	GPIO_Output	
M1	VSSA	Power		
M7	PG1 *	I/O	GPIO_Output	
M8	VSS	Power		

Pin Number UFBGA176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
M9	VSS	Power		
M10	VCAP_1	Power		
N1	VREF-	Power		
N2	PA1	I/O	TIM2_CH2	
N3	PA0/WKUP	I/O	TIM2_CH1	
N8	VDD	Power		
N9	VDD	Power		
N10	VDD	Power		
N13	PD12 **	I/O	TIM4_CH1	
P1	VREF+	Power		
P8	PE8 **	I/O	UART7_TX	
P10	PE11 *	I/O	GPIO_Output	
P12	PB12	I/O	CAN2_RX	
P13	PB13	I/O	CAN2_TX	
R1	VDDA	Power		
R7	PF14 *	I/O	GPIO_Output	
R8	PE7 **	I/O	UART7_RX	

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	2019RC_MR1
Project Folder	C:\Users\1234567\Desktop\MR1-v6.0
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F4 V1.23.0

5.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F427/437
MCU	STM32F427IIHx
Datasheet	024030_Rev9

6.2. Parameter Selection

Temperature	25
Vdd	null

7. IPs and Middleware Configuration

7.1. CAN1

mode: Mode

7.1.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum)	**3 ***
Time Quantum	**71.42857142857143 ***
Time Quanta in Bit Segment 1	**9 Times ***
Time Quanta in Bit Segment 2	**4 Times ***
ReSynchronization Jump Width	1 Time

Basic Parameters:

Time Triggered Communication Mode	Disable
Automatic Bus-Off Management	Disable
Automatic Wake-Up Mode	Disable
No-Automatic Retransmission	Disable
Receive Fifo Locked Mode	Disable
Transmit Fifo Priority	Disable

Advanced Parameters:

Operating Mode	Normal

7.2. CAN2

mode: Mode

7.2.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum)	**3 ***
Time Quantum	**71.42857142857143 ***
Time Quanta in Bit Segment 1	**9 Times ***
Time Quanta in Bit Segment 2	**4 Times ***
ReSynchronization Jump Width	1 Time

Basic Parameters:

Time Triggered Communication Mode	Disable
Automatic Bus-Off Management	Disable
Automatic Wake-Up Mode	Disable
No-Automatic Retransmission	Disable

Receive Fifo Locked Mode	Disable
Transmit Fifo Priority	Disable

Advanced Parameters:

Operating Mode	Normal

7.3. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.3.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1
Power Over Drive	Disabled

7.4. SYS

Debug: Serial Wire

Timebase Source: TIM7

7.5. TIM2

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

7.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**84 ***
Counter Mode	Up

Counter Period (AutoReload Register - 32 bits value)	**19999 ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (32 bits value)	**1000 ***
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (32 bits value)	**1000 ***
Fast Mode	Disable
CH Polarity	High

7.6. USART1

Mode: Asynchronous

7.6.1. Parameter Settings:

Basic Parameters:

Baud Rate	**100000 ***
Word Length	8 Bits (including Parity)
Parity	**Even ***
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.7. USART6

Mode: Asynchronous

7.7.1. Parameter Settings:

Basic Parameters:

Baud Rate	**9600 ***
Word Length	8 Bits (including Parity)

Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.8. FREERTOS

mode: Enabled

7.8.1. Config parameters:

Versions:

FreeRTOS version	9.0.0
CMSIS-RTOS version	1.02

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	Disabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled

Memory management settings:

Memory Allocation	Dynamic
TOTAL_HEAP_SIZE	**30000 ***
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled

USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Disabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	**Enabled ***
TIMER_TASK_PRIORITY	**3 ***
TIMER_QUEUE_LENGTH	10
TIMER_TASK_STACK_DEPTH	256

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

7.8.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Disabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
CAN1	PD0	CAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PD1	CAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
CAN2	PB12	CAN2_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB13	CAN2_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
RCC	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
TIM2	PA1	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA0/WKUP	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART1	PB7	USART1_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
	PA9	USART1_TX	Alternate Function Push Pull	Pull-up	**Very High ***	
USART6	PG14	USART6_TX	Alternate Function Push Pull	Pull-up	**Very High ***	
	PG9	USART6_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
Single Mapped Signals	PI6	TIM8_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI5	TIM8_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE8	UART7_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PE7	UART7_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
GPIO	PE0	GPIO_Output	Output Push Pull	**Pull-up ***	**High ***	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PB3	GPIO_EXTI3	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	**n/a**	
	PG8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PG7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PG6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PG5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PG4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PG3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PG2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PG1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PF14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

8.2. DMA configuration

DMA request	Stream	Direction	Priority
USART1_RX	DMA2_Stream2	Peripheral To Memory	Low
USART6_RX	DMA2_Stream1	Peripheral To Memory	Low

USART1_RX: DMA2_Stream2 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART6_RX: DMA2_Stream1 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
EXTI line3 interrupt	true	5	0
CAN1 RX0 interrupts	true	5	0
TIM7 global interrupt	true	0	0
DMA2 stream1 global interrupt	true	5	0
DMA2 stream2 global interrupt	true	5	0
CAN2 RX0 interrupts	true	5	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
CAN1 TX interrupts	unused		
CAN1 RX1 interrupt	unused		
CAN1 SCE interrupt	unused		
TIM2 global interrupt	unused		
USART1 global interrupt	unused		
CAN2 TX interrupts	unused		
CAN2 RX1 interrupt	unused		
CAN2 SCE interrupt	unused		
USART6 global interrupt	unused		
FPU global interrupt	unused		

*** User modified value**

9. Software Pack Report