Experiment 3: Combinational Logic and Sequential Logic Circuit Design

16231235 李谨杰 Table number：23

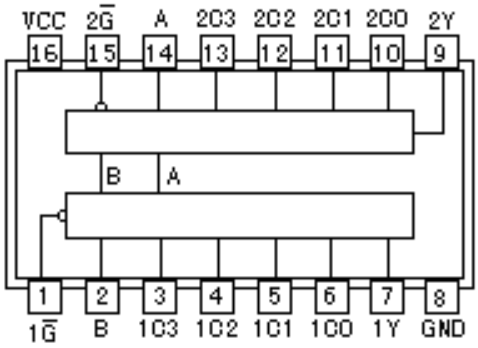
Objective

1. To familiarize and check several types of non-memory logic components.
2. To master and test the logic functions of D and JK flip-flops.
3. To learn to design and debug combinational logic circuit.
4. To realize the way to design a Mod-16 counter by flip-flops.
5. To study basic debugging ways for sequential logic circuit.

Introduction of MSI chips

74LS153 Truth Table

Data select	Enable control	Data inputs	Data output
B A	G	C_3 C_2 C_1 C_0	Y
0 0 0 0	0	X X X 0 X X X 1	0 1
0 1 0 1	0	X X 0 X X X 1 X	0 1
1 0 1 0	0	X 0 X X X 1 X X	0 1
1 1 1 1	0	0 X X X 1 X X X	0 1
X X	1	X X X X	0
Note: X stands for 0 or 1 (don't care).			

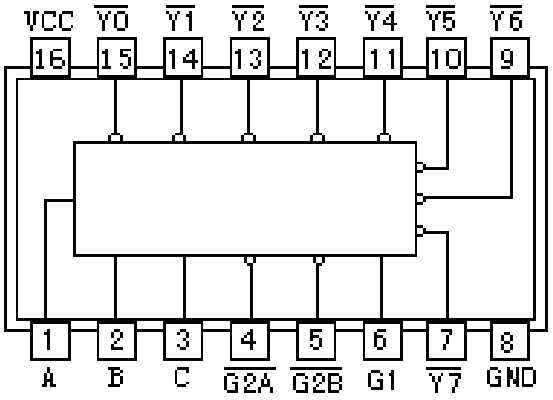


74LS153 pin diagram

Functions of 3-line-to 8-line Decoder 74LS138

Data Inputs					Data Outputs							
Enable Controls		Decoding Selection			Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
G1	G2A+G2B	C	B	A								
0	X	X	X	X	1	1	1	1	1	1	1	1
X	1	X	X	X	1	1	1	1	1	1	1	1

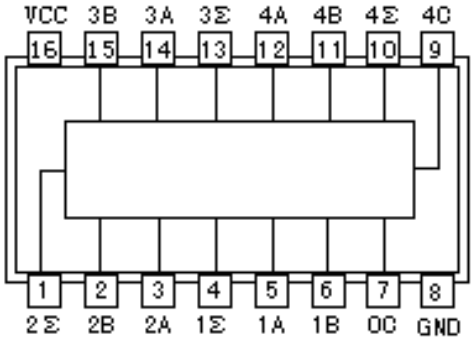
1	0	0	0	0	0	1	1	1	1	1	1	1
1	0	0	0	1	1	0	1	1	1	1	1	1
1	0	0	1	0	1	1	0	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1	1	1
1	0	1	0	0	1	1	1	1	0	1	1	1
1	0	1	0	1	1	1	1	1	1	0	1	1
1	0	1	1	0	1	1	1	1	1	1	0	1
1	0	1	1	1	1	1	1	1	1	1	1	0



Pin Diagram of 74LS138

Truth Table of 74LS283

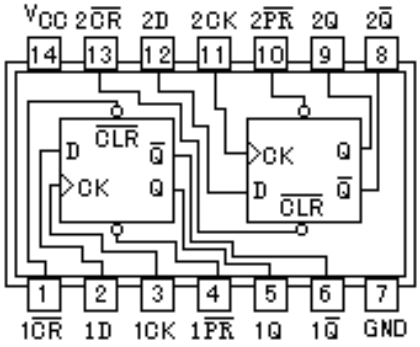
C_{n-1}	A_n	B_n	Σ_n	C_n
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



Pin-out Diagram of 74LS283

The characteristics of 74LS74

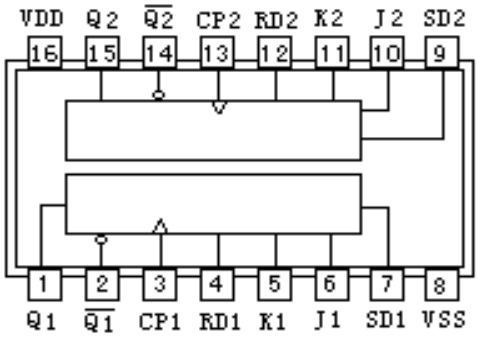
Inputs				Outputs	
		CK	D	Qn+1	
0	1	X	x	1	0
1	0	X	x	0	1
0	0	X	x	Unstable*	Unstable*
1	1	↑	1	1	0
1	1	↑	0	0	1
1	1	0	x	Qn	
* This is forbidden because the logic relation is broken.					



Pin-out Diagram of 74LS74

The characteristics of CD4027

Inputs				Outputs	
SD	RD	CP	J K	Qn+1	
0	1	X	X x	0	1
1	0	X	X x	1	0
1	1	X	X x	Unstable	Unstable
0	0	↑	0 0	Qn	
0	0	↑	0 1	0	1
0	0	↑	1 0	1	0
0	0	↑	1 1		Qn
0	0	↓	X x	Qn	



CD4027 pin diagram

Design

1. Design a combinational logic circuit called 3-person vote circuit in three ways:

   (1) Design the circuit by using only NAND gates.
   (2) Design by using 1-of-4 data selector/multiplexer 74LS153.
   (3) Design by using 3-line-to-8-line decoder 74LS138 and one NAND gate.

2. To design and verify BCD to excess-3 code converter.

3. Design a 4-bit binary synchronous up counter which can be cleared at any time using 2pcs of CD4027 and NAND gates. Draw the logic diagram indicating pin numbers.

Truth Table for 3-person voting circuit

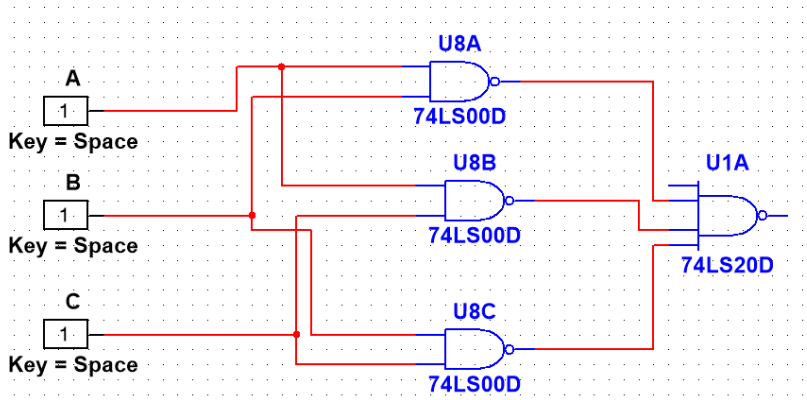
Inputs			Output
C	B	A	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

BCD to excess-3 code converter

Decimal Numbers	BCD Code DCBA	Excess-3 Code E3E2E1E0	Y
0	0000	0011	0
1	0001	0100	0
2	0010	0101	0
3	0011	0110	0
4	0100	0111	0
5	0101	1000	0
6	0110	1001	0
7	0111	1010	0
8	1000	1011	0
9	1001	1100	0
10	1010	Invalid code	1
11	1011		1
12	1100		1
13	1101		1
14	1110		1
15	1111		1

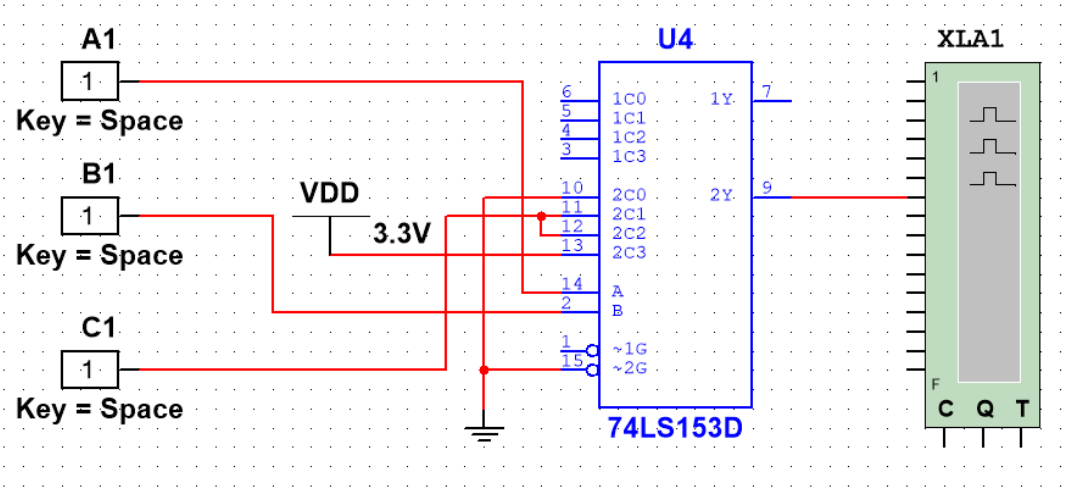
Tasks

1. Build your 3-person vote circuit by NAND gates.



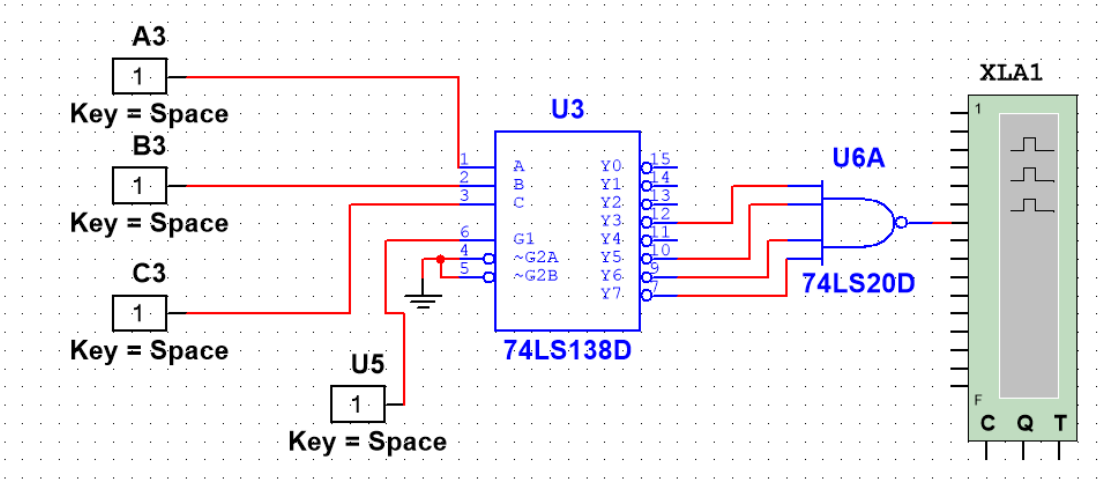
Circuit 1

2. Test the logic function of 1-of-4 data selector 74LS153, comparing it with its truth table. Build the 3-person voting circuit by 74LS153, and check if it works correctly.



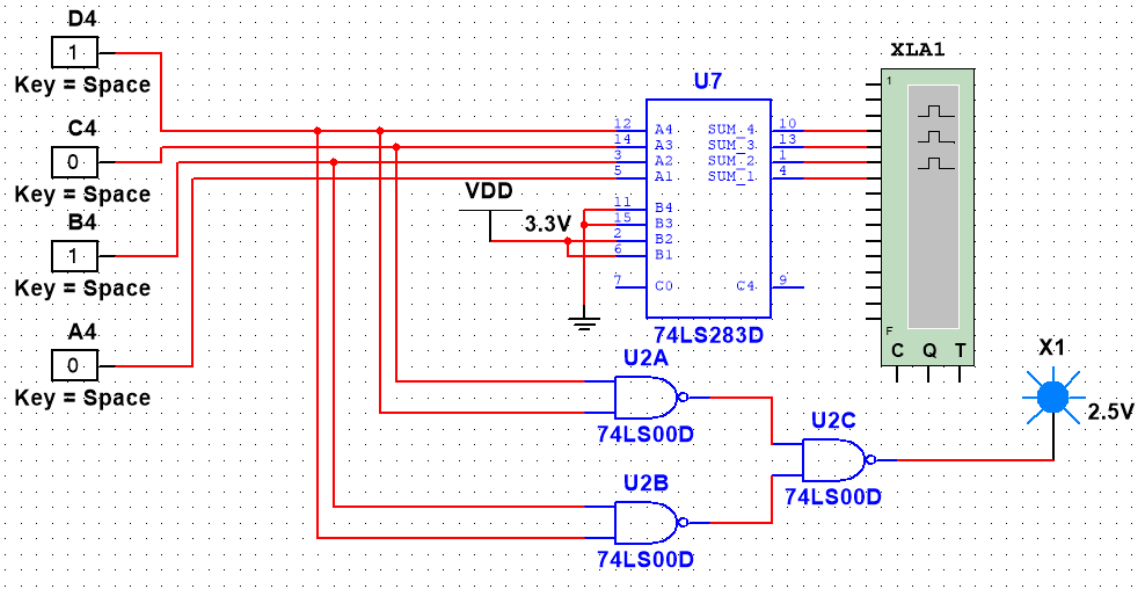
Circuit 2

3. Test the logic function of 3-line-to-8-line decoder 74LS138, comparing it with its truth table. Build the 3-person voting circuit by 74LS138, and check if it works correctly.



Circuit 3

4. Test the logic function of 74LS283. Build BCD to excess-3 code converter including the indication circuit.

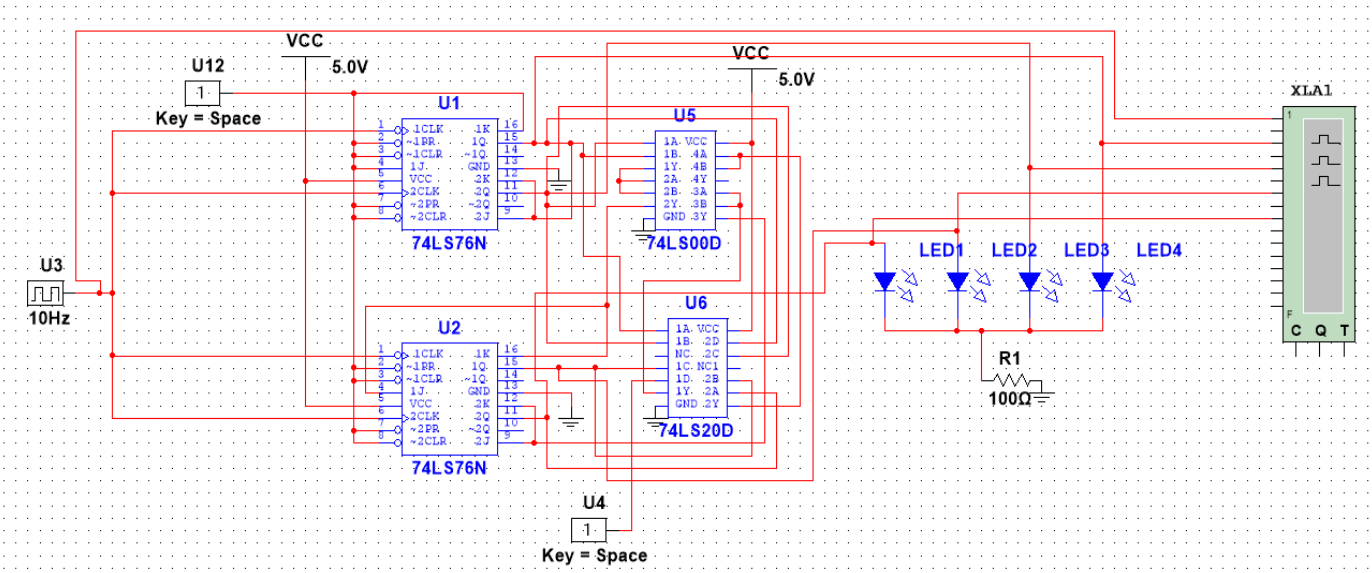


Circuit 4

5. Test the logic function of 74LS74 and CD4027, noting the SET and RESET functions, observing when it is triggered (positive or negative edge), and compare it with its truth table. List testing results.

6. Build the 4-bit binary(Mod-16) synchronous up counter with logic switch as inputs and LEDs as outputs, checking if it works correctly.

J0=K0=1
J1=K1=Q0
J2=K2=Q1*Q0
J3=K3=Q1*Q2*Q3



Circuit 5

7. On CRO, observe each output of flip-flops of the counter with sequent CLOCK on experiment trainer kits as CLOCK input, and draw the timing diagrams on square paper.

Data collation and analysis

Task 2：

Testament of 74LS153:

B	A	G	C3	C2	C1	C0	Y
0	0	0	x	X	X	1	1
0	0	0	x	X	X	0	0
0	1	0	x	X	1	X	1
0	1	0	x	X	0	X	0
1	0	0	x	1	X	X	1
1	0	0	x	0	X	X	0
1	1	0	1	X	X	X	1
1	1	0	0	X	X	X	0
x	x	1	x	X	X	x	0

My design of 3-person voting circuit works well.

Task 3:

Testament of 74LS138:

Data Inputs					Data Outputs							
Enable Controls		Decoding Selection			Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
G1	G2A+G2B	C	B	A								
0	X	X	X	X	1	1	1	1	1	1	1	1
X	1	X	X	X	1	1	1	1	1	1	1	1
1	0	0	0	0	0	1	1	1	1	1	1	1
1	0	0	0	1	1	0	1	1	1	1	1	1
1	0	0	1	0	1	1	0	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1	1	1
1	0	1	0	0	1	1	1	1	0	1	1	1
1	0	1	0	1	1	1	1	1	1	0	1	1
1	0	1	1	0	1	1	1	1	1	1	0	1
1	0	1	1	1	1	1	1	1	1	1	1	0

My design of 3-person voting circuit works well.

Task 4:

Testament of 74LS283:

C_{n-1}	A_n	B_n	Σ_n	C_n
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

My design of BCD to excess-3 code converter works well.

Task5

Testament of 74LS74:

PR	CR	CK	D	Q_{n+1}	$\overline{Q_{n+1}}$
0	1	X	X	1	0
1	0	X	X	0	1
1	1	↑	1	1	0
1	1	↑	0	0	1
1	1	0	X	Qn	$\overline{Q_n}$
0	0	↑	X	1	1

Testament of CD4027:

SD	RD	CP	J	K	Qn+1	$\overline{Q_{n+1}}$
0	1	X	X	X	0	1
1	0	X	X	X	1	0
1	1	X	X	X	Unstable	Unstable
0	0	↑	0	0	Qn	$\overline{Q_n}$
0	0	↑	0	1	0	1
0	0	↑	1	0	1	0
0	0	↑	1	1	$\overline{Q_n}$	Qn
0	0	↓	X	X	Qn	$\overline{Q_n}$

Task 6 and Task 7

I haven't present right waveform on oscilloscope, but I get right input and output when giving single pulse.

Clear	Clk	Dn	Cn	Bn	An	Dn+1	Cn+1	Bn+1	An+1
↑	x	x	x	x	x	0	0	0	0
0	↑	0	0	0	0	0	0	0	1
0	↑	0	0	0	1	0	0	1	0
0	↑	0	0	1	0	0	0	1	1
0	↑	0	0	1	1	0	1	0	0
0	↑	0	1	0	0	0	1	0	1

0	↑	0	1	0	1	0	1	1	0
0	↑	0	1	1	0	0	1	1	1
0	↑	0	1	1	1	1	0	0	0
0	↑	1	0	0	0	1	0	0	1
0	↑	1	0	0	1	1	0	1	0
0	↑	1	0	1	0	1	0	1	1
0	↑	1	0	1	1	1	1	0	0
0	↑	1	1	0	0	1	1	0	1
0	↑	1	1	0	1	1	1	1	0
0	↑	1	1	1	0	1	1	1	1
0	↑	1	1	1	1	0	0	0	0

Summary

I have learned a lot about simulation. When I preview task 6, I do the simulation, but forget to connect enable sockets. As the result, I can't figure out right answer for a long time.

So when I connect digital circuit, I should make sure every input of IC in a clear state. Otherwise the IC can't work under normal conditions.