Experiment4　Simple Digital Cymometer

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1. Purpose

1) Know digital testing principle of signal frequency and period, and know the basic constitution and work principle of digital cymometers.
2) Learn and master the ways to get pulse waveform generators by active crystal oscillator, passive crystal oscillator, resistors, capacitors and inverters.
3) Study to use MSI of counters and frequency demultiplier.
4) Learn to assemble a simple digital cymometer, and study commonly used testing methods.

2. Experiment Principle

1) Principle of digital testing frequency

Figure 4.1 shows the principle block diagram of a simple digital cymometer. It comprises following four basic parts:

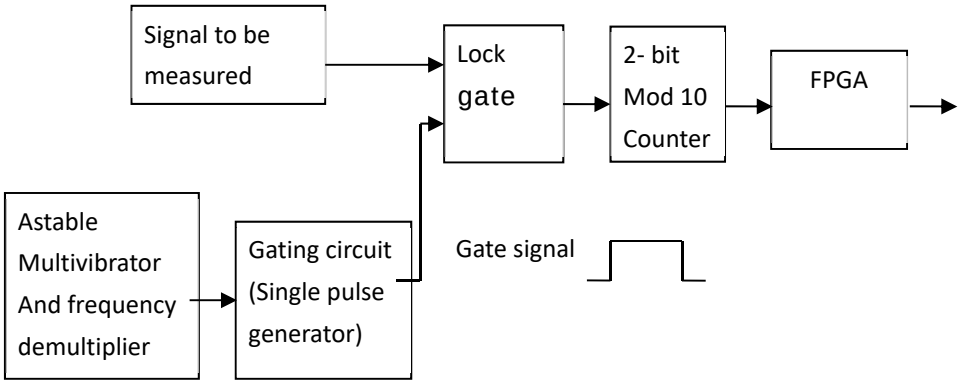


Figure 4.1 Principle Block Diagram of a Digital Cymometer

a) Lock gate

Lock gate consists of gate circuits with the pulses to be countered as one input and gate signal as another input, and the gate signal controls it to open or close.

b) Astable multivibrator

Normally, crystal oscillator and frequency demultiplier can be used to get frequency known and steady oscillation whilst the latter dividing the signal frequency to change the width of gate signal. Here a ring oscillator with RC circuit is used.

c) Gating control circuit

It is used to change the periodic signal from frequency demultiplier into single pulse signal called gate signal.

d) Counter and displaying circuit

It counts the pulses from lock gate, and then display in decimal form via decoding.

Frequency defines as the cycle number of a periodic signal in 1 second. If the circulation number is N in 1 second, the frequency f = N.

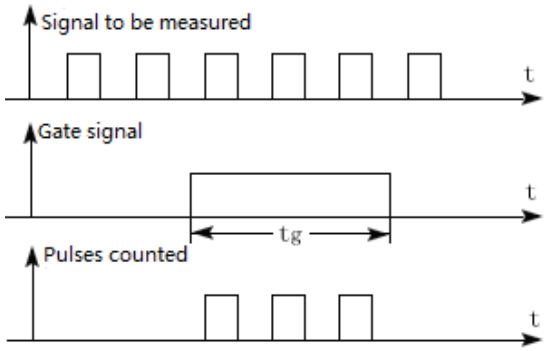


Figure 4.2 Sketch Map of Measuring Frequency Principle

Figure 4.2 illustrates the principle of measuring frequency. Only when gate signal is HIGH can the measured signal passes lock gate and count by the counter. When gate signal is LOW, the lock gate closes and counting stops. If time width of gate signal is known as t_g, the frequency to be measured is

$$f = \frac{N}{t_g}$$

Therein, N is the number counted by the counter.

In order to improve measuring accuracy, it is required that the number of counted pulses is enough. If the frequency of measured signal is low, and the width of gate signal t_g is not wide enough, a error will be big. In this situation, the signal period can be measured.

2) Ring astable multivibrator (oscillator) with RC circuit

BY utilizing transmission time of gate circuits, odd NAND gates each connecting together from the beginning to the end constitute an oscillator, commonly called ring astable multivibrator. Due to the transmission time of gate circuits being several scores of nanoseconds ,the oscillation frequency is very high, and can not be adjusted. If RC delay circuit is added into the ring circuits, delay time can increase, and oscillation frequency can be changed by changing TC parameter, which is ring asable multivibrator with RC circuit shown in Figure 4.3. The inputs and outputs voltage waves are shown in Figure 4.4.

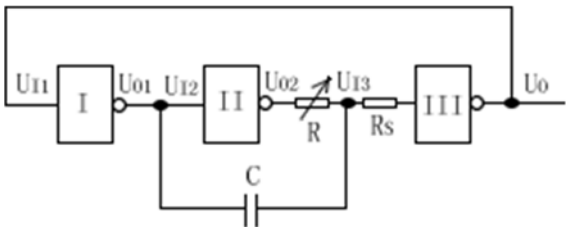


Figure 4.3 Ring Astable Multivibrator

It is obvious that U_O, U_{I1} and U_{O1}, U_{I2} are NOT logic, so is U_{I2} and U_{O2}. The voltage of capacitor can not jump due to the existence of RC, so U_{I3} jumps following U_{O2}. With capacitor charging and discharging, when U_{I3} reaches threshold voltage U_T, NOT gate III will turn over.

The period of the circuit is $T \approx 2.2RC$. For TTL NAND gates, the value of R should be no more than 2KΩ. Normally RS is 100Ω around.

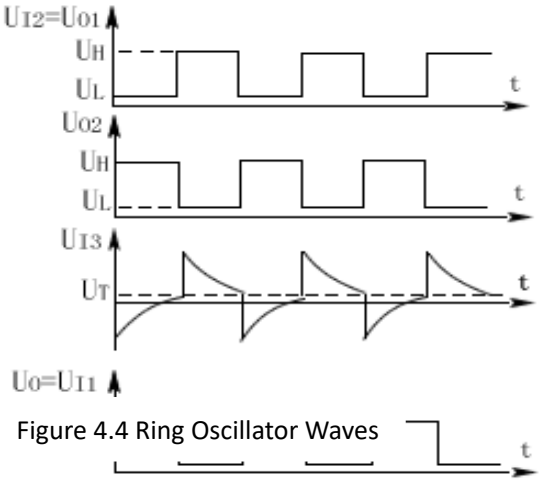


Figure 4.4 Ring Oscillator Waves

3) Singal Pulse Generator

In order to get gate signal of single pulse, single pulse generator whose input is periodic pulses is utilized. K is a control switch. A single pulse with a fixed width will give out with each push. The pulse width has nothing to do with push time but decided by the period of input pulse. Figure 4.5 are single pulse generator circuit and waves.

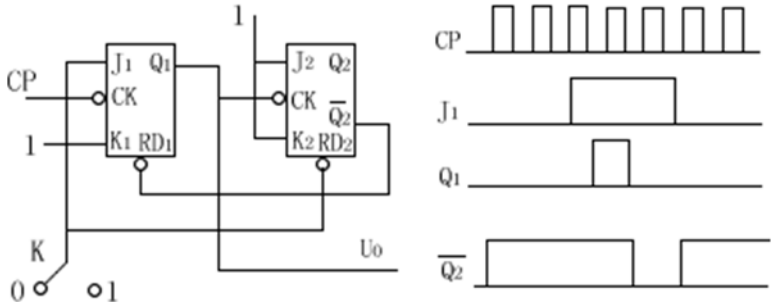


Figure 4.5 Single Pulse Generator Circuit and Waves

The work procedure is as following: switch K is at terminal “0” normally. When power on, Q_2=0, $\overline{Q_2}=1$ due to the RESET pin of the second flip-flop R_{D2}=0. The first flip-flop J_1=0, K_1=1, then Q_1=0. When switch K is pressed to terminal “1”, then J_1=K_1=1 and R_{D1}=1. Under the motivation of pulse CP, the first flip-flop will be in toggle mode which makes Q_1 change to “1” state from “0” state, and change back to state “0” from state “1”. The falling edge of Q_1 leads the second flip-flop turnover since the conditions have been ready: R_{D2}=1 , J_2=K_2=1. Q_2 changes to state “1” from state“0”, $\overline{Q_2}$ changes to state “0” from state“1”. Because $\overline{Q_2}$ works at terminal R_{D1} of the first flip-flop, R_{D1}=0 which RESET the first flip-flop to “0”. A you can see from Figure 4.5, when switch K is pressed (J_1=1), the output Q_1 of the first flip-flop is a single pulse whose width is the period of CLOCK pulse CP.

4) Mod-10 Counter 74LS90

74LS90 is a medium size scale integrated asynchronous counter.

Pin A and B are counting pulse input with negative edge-triggered. $R_0(1)$ and $R_0(2)$ are RESET terminals with HIGH active. $R_9(1)$ and $R_9(2)$ are SET 9 terminals with HIGH active. When pin A acts as CLOCK pulse input and Q_A as output, 74LS90 works as a binary counter. When pin B acts as CLOCK pulse and $Q_DQ_CQ_B$ as outputs, 74LS90 can realize modulus-5 counting. When Q_A is connected to pin B and pin A acts as CLOCK pulse input, 74LS90 can realize BCD counting. When Q_D is connected to pin A and pin B acts as CLOCK pulse input, 74LS90 can realize biquinary counting (5421 code). The truth tables are shown in table 4-3 and table 4-4. By using feedback SET 9, 74LS90 can realize septenary counting. Figure 4.6 shows the sketch map of binary code decimal 8421 wire connection. When the tenth pulse comes after the counter counts 1001, the counter SET 0 immediately, and gives out a carry pulse to upper bit.

Table 4-3 74LS90 BCD Count Sequence

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

Table 4-4 74LS90 Bi-quinary Count

Count	Outputs			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

5) Medium Scale Integrated Circuit Frequency Demultiplier (Oscillator)---- CD4060

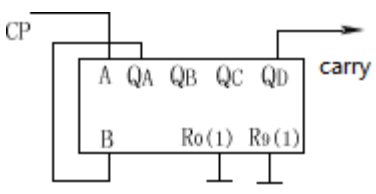


Figure 4.6 8421 Code Wire Connection Sketch Map

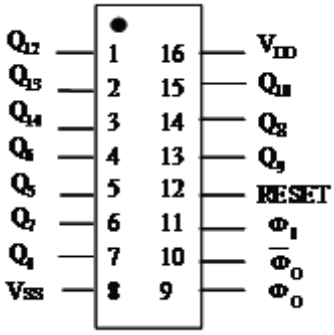


Figure 4.7 CD4060 Pin-out Diagram

CD4060 function is summarized in table 4-5.

Table 4-5 CD4060 Functions

Inputs		**Outputs**		
RESET	ØI	Øo	/Øo	Q divider

H	X	L	L	L
L	CK	Ck	/CK	**Q4～10，12 ～14**

3. Experiment Contents

1) Build the astable oscillator by NOT gate, resistors and capacitors. Frequency can be adjusted between 100Hz—1000Hz.
2) Construct the single pulse generator by J-K flip-flops 74LS73.
3) Build 2-bit Mod-10 counter by 74LS90 with RESET function.
4) Get frequency dividing signals 214, 213, 212, 210, 29, 28, 27, 26, 25, 24 and basic positive and negative clock signals from the output of frequency dividing circuit consisting of 4MHz active crystal oscillator and CD4060 frequency demultiplier. Make these output signals as the signals to be measured of your digital cymometer.

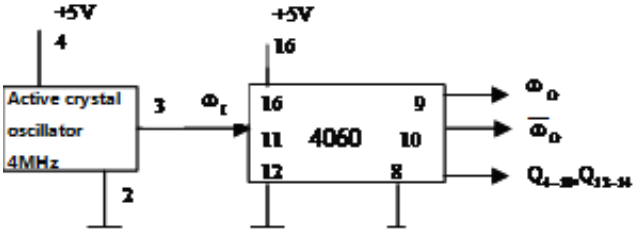


Figure 4-9 Oscillator and Frequency Demultiplier

5) Assemble above four steps and Lock gate together to make a whole digital cymometer. Test the cymometer, comparing the results with actual frequencies (tested by CRO).
6) Make a waveform generator by 11.0592MHz passive crystal oscillator, NOT gate, resistors and capacitors. Obverse signal wave on CRO and draw down.

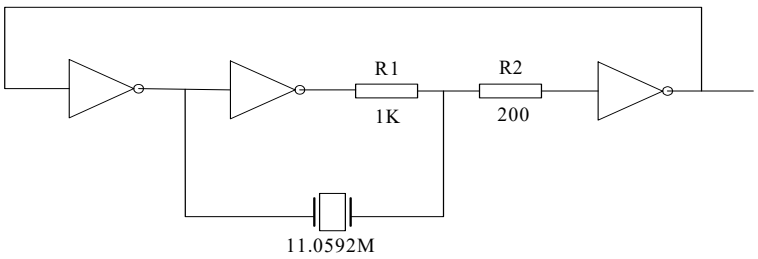


Figure 4-10 Waveform Generator

7) Design and test a 60-frequency-divider circuit.
8) Design oscillators with certain frequency by CD4060, crystal oscillator or resistors and capacitors.

4. IC's Supplied

74LS90	2 pieces
74LS73	1 piece
74LS00	1 piece
74LS04	1 piece
CD4060	1 piece

Potentiometer 2KΩ 1W	1 piece
Resistor 100Ω	1piece
Capacitor 10uF	1 piece
Active crystal oscillator	1 piece
Passive crystal oscillator	1 piece

5. Experiment circuits

1) The astable oscillator

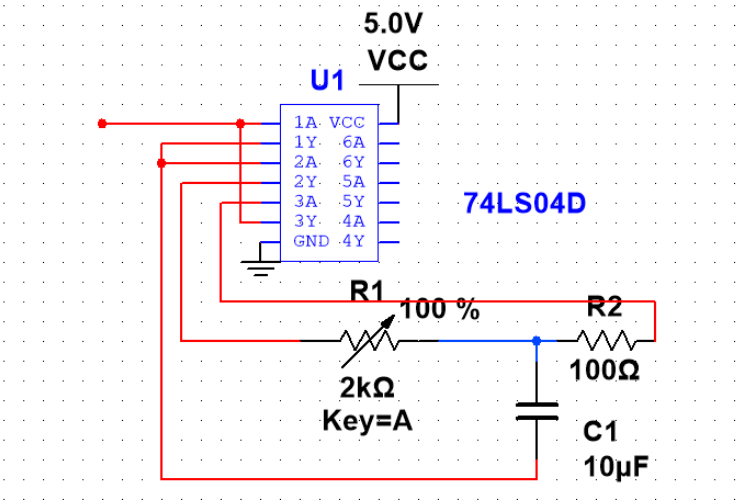


Figure 1

2) The single pulse generator

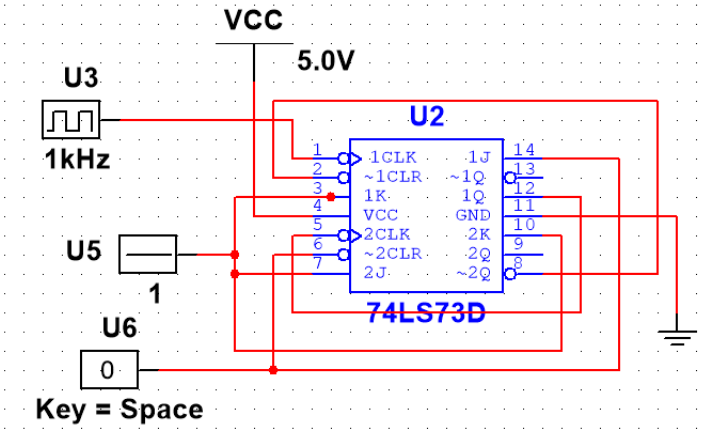


Figure 2

3) 2-bit Mod-10 counter

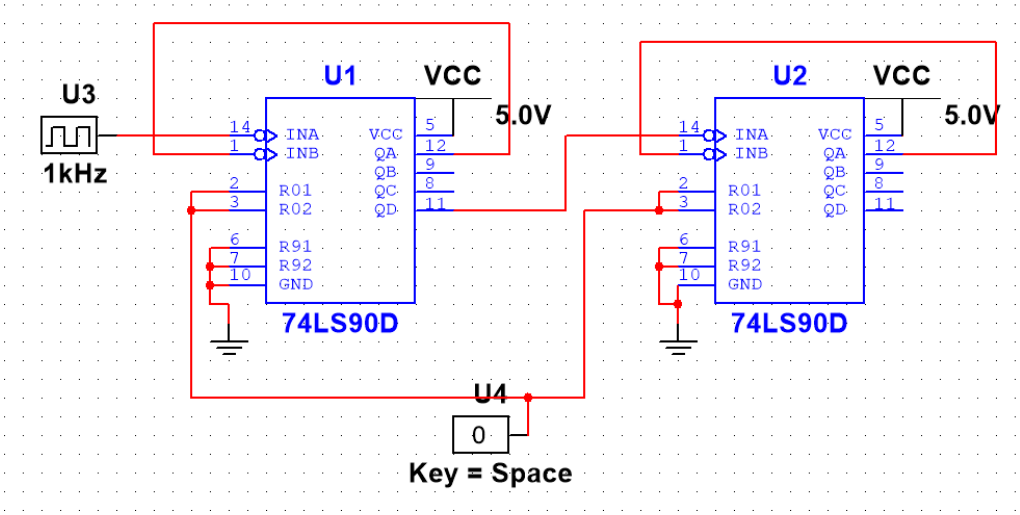


Figure 3

4) Oscillator and Frequency Demultiplier

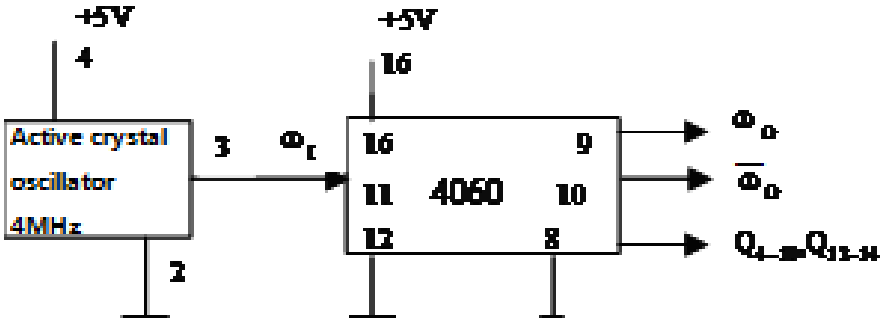


Figure 4

5) Waveform generator by 11.0592MHz passive crystal oscillator

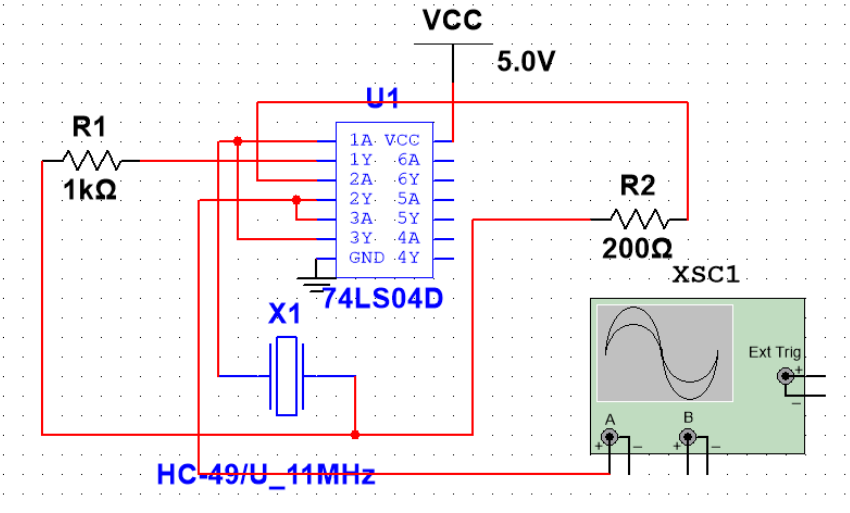


Figure 5

6) 60-frequency-divider

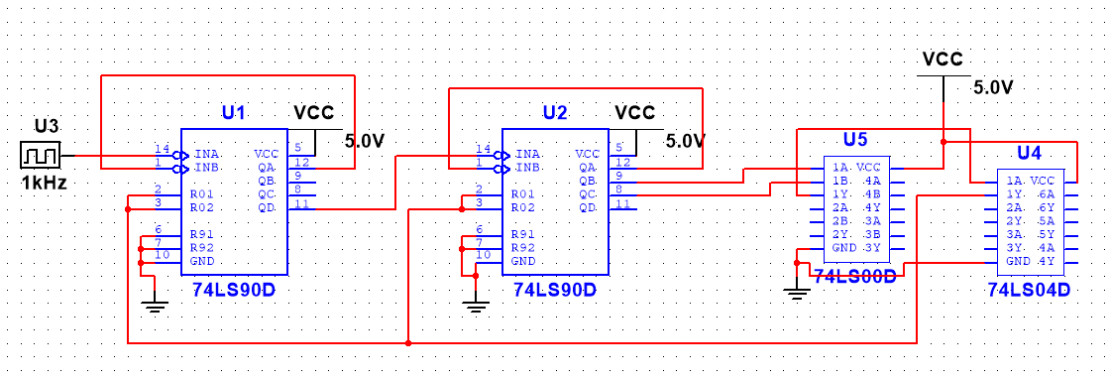
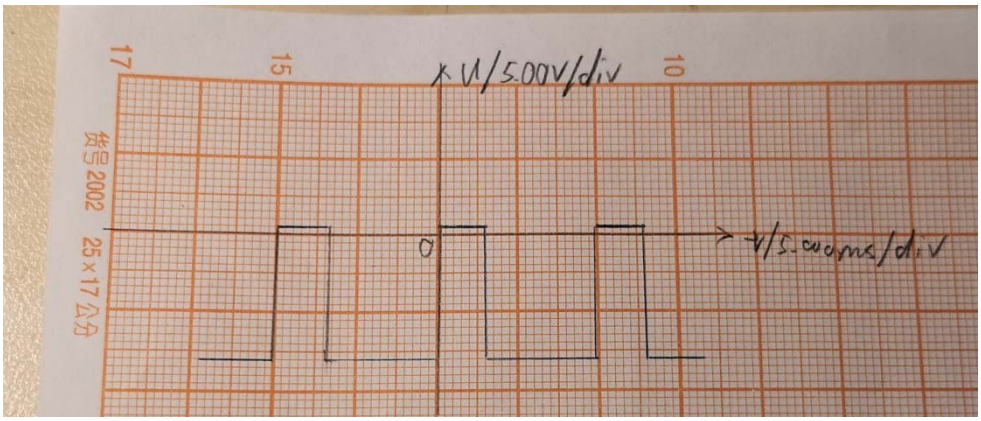


Figure 6

6. Conclusion

1) The astable oscillator

The U waveforms are as follows. It can be seen that after wave filtering， the waveform is very closed to square waveform.



2) The single pulse generator

It is hard to describe the experiment phenomenon by stable picture. When I touch pad, figure on the screen would rise for a period, depending on clock signal.

3) 2-bit Mod-10 counter

When I connect input wire to 1Hz clock signal, the digital tube would count number from 00 to 99, then go back to 00.

In addition, there is an interesting phenomenon: at first, numbers showed always jumped from 59 to 79, but other function worked normally. When I changed ten bit and one bit, the whole circuit works very good incredibly!

4) Oscillator and Frequency Demultiplier

$$f = \frac{4 \times 10^6}{2^n} \text{Hz}$$

Pin	3	2	1	15	13	14	6	4	5	7
Diving signals	2^{14}	2^{13}	2^{12}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4
ft/HZ	250	500	1k	4k	8k	16k	32k	64k	128k	256k

I test pin 1, and get right result.

5) The digital cymometer

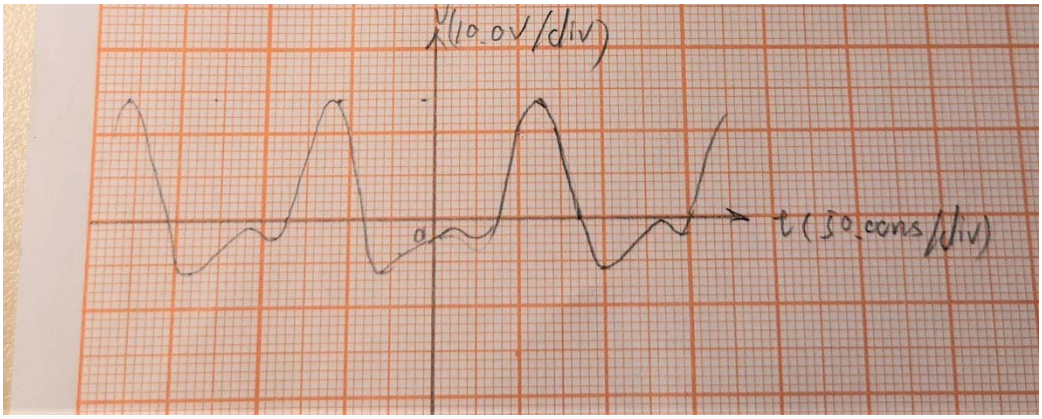
After the circuit is connected, the data is measured as follows. It can be seen that

the digital cymometer works normally.

	1	2	3	4	5	6	7	8	9	10	$f = \frac{N}{t_g}$
1K	10	20	31	41	51	62	72	82	92	02	1.02k

From this result, this simple digital cymometer can get precise frequency of clock signal.

6) I draw the waveform as follow:



7) I design a 60-frequency-divider circuit as figure 6.

Only if make sure every part of the circuit works well, then the whole circuit is possible to success.