Experiment 6 Digitalized Signal Generator

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1. Purpose

Make an analog signal generator by D/A converter and memory. The data to produce signals are regulated by DC stabilized voltage power supply and converted by A/D, and then stored in memory.

1) Learn to use D/A and A/D converters.
2) Study and learn the usage of RAM.
3) Understand the function of bus three--state buffer.

2. Experiment Explanations

Figure 6.1 is the block diagram of digitalized signal generator. The instantaneous values of the wave to be produced are already stored in RAM according to priority. The address forming net output addressing signal under timing clock. The data in corresponding address is read out from RAM and input to D/A converter making it output analog signal value.

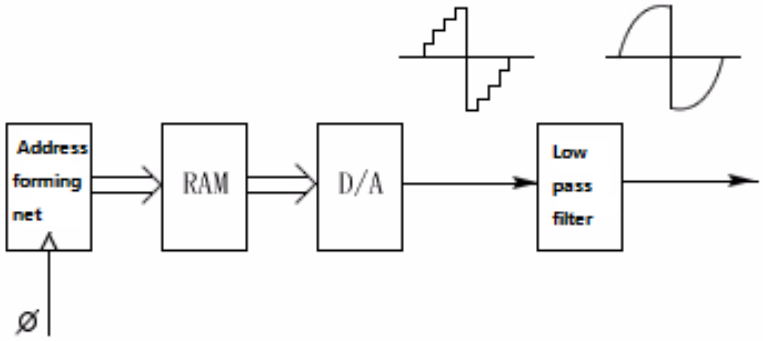


Figure 6.1 Basic block diagram of digitalized signal generator

In order to process signals using digital techniques, the incoming analog signal must be converted into digital form. Figure 6.2 shows how to store instantaneous values at different time of the wave to be produced in RAM. The wave sampling time should be identical to clock period. A new address is formed under each clock period, and the corresponding wave instantaneous value is stored in it after A/D conversion. If the voltage value input to A/D converter is different, data written to RAM is different, and relative wave produced is different.

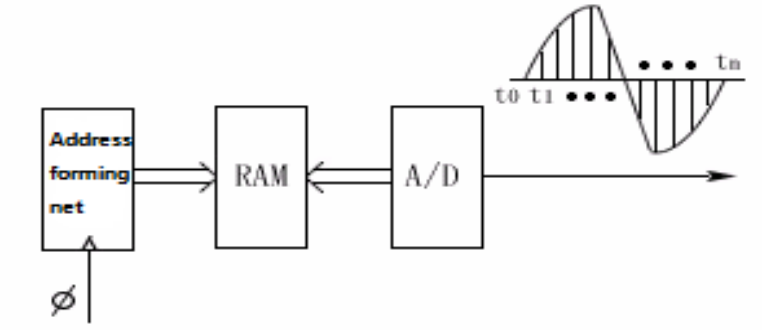


Figure 6.1 Sketch of wave data sampling

Several ICs used in this experiment are introduced here.

1) IC 2114 Static Random-Access Memory (RAM)

The RAM used in this experiment is 2114 whose pin-out diagram and framework is shown in figure 6.3. There are 1024 memory cells, and 4-bit binary code can be stored in one cell.

	Address inputs
$\overline{WE}$	Write allow
$\overline{CS}$	Chip select
I/01−I/04	Data input/output
V_{CC}	source（+5V）
GND	Ground

(a) Illustration of pin-out symbols

(b) pin-out diagram

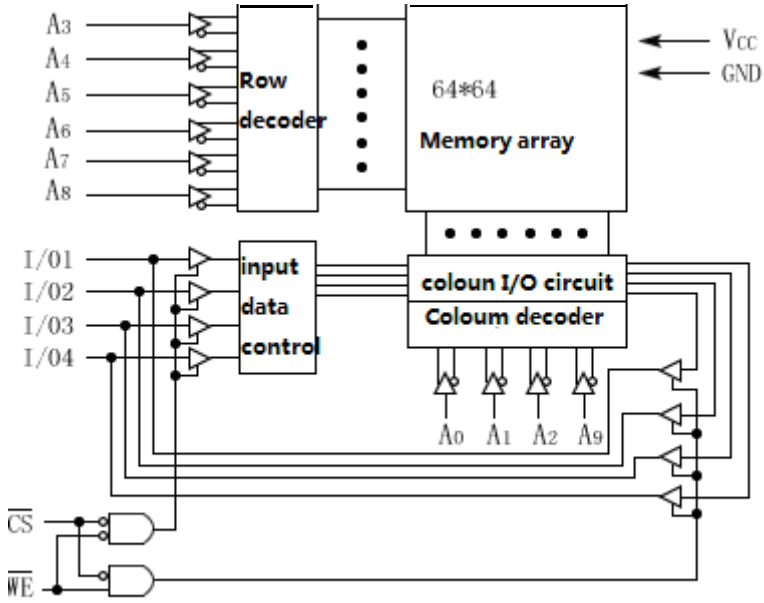


Figure6.3 Constitution block diagram

The memory cells in a SRAM are organized in rows and columns. A_0～A_9 are address inputs. Any one of 1024 memory cells can be visited by selecting different address codes A_0～A_9, reading out or writing into a 4-bit binary code D_3～D_0 which is output (when read out) or input (when write into) from I/04～I/01 separately. READ or WRITE is selected by the voltage on $\overline{WE}$. When $\overline{WE}$ is LOW, WRITE is selected, the code input from I/04～I/01 is stored in one cell. Otherwise, when $\overline{WE}$ is HIGH, READ is selected, and the code in one cell is output through I/04～I/01 while the code still keeping in it.

Table 6-1 Read/write control

$\overline{CS}$	$\overline{WE}$	Mode
0	0	WRITE
0	1	READ

1	X	unselected

$\overline{CS}$ is chip selection. When it is LOW, the chip is selected, READ or WRITE can operate. When it is HIGH, the chip is not selected and will not operate, see table 6-1.In addition, pin GND to the ground, U_{CC} to +5V source.

When using this kind of IC, at least one of $\overline{CS}$ and $\overline{WE}$ should be in HIGH voltage during address change. Otherwise chip is in WRITE operation refreshing the code stored in cells. When $\overline{WE}$ is LOW, the voltage of address lines and data lines are must be stable.

2) DA converter DAC0832

Digital-to-analog conversion is an important part of a digital processing system. Once the digital data has been processed, it is converted back to analog form. Pin-out diagram of DAC0832 is shown in figure 6.4. It has 8 digital input terminals DI_7～DI_0 through which 8-bit binary code can be input. I_{out1} and I_{out2} are analog output terminals. When digital input is the maximum value, the output current from I_{out1} is the maximum. When input digital is zero, output current is the minimum. The two terminals can be connected to external operational amplifier. There is a feedback resistor inside the chip, which can act as the feedback resistor of the operational amplifier, and output by pin 9 (R_{fb}). The functions of other terminals are as following:

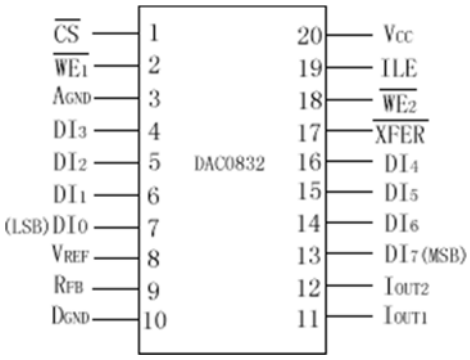


Figure 6.4 DAC0832 D/A converter

U_{CC}: to power supply, from +5～+15V, +15V is priority.

V_{REF}: to standard voltage source. It is connected with D/A conversion net inside chip, from +10V～-10V.

DGND: digital ground

There are also 5 control terminals:

(1) $\overline{CS}$: chip selection, LOW active

(2) ILE: input latch permit, HIGH active

(3) $\overline{WR_1}$: WRITE signal 1. When ILE is HIGH, $\overline{CS}$ is LOW, $\overline{WR_1}$ is LOW, the input digital quantity can be latched in input register.

(4) $\overline{XFER}$: control transmission signal, Low active.

(5) $\overline{WR2}$: WRITE signal 2. When $\overline{XFER}$ is LOW, $\overline{WR2}$ is LOW, it can transfer and latch the digital quantity latched in input register to DAC register.

These terminals can be used in the system with several DAC0832 to control several digital quantity conversions and output. In this experiment, ILE is HIGH, $\overline{XFER}$ and $\overline{WR2}$ to ground, $\overline{CS}$ and $\overline{WR_1}$ to ground.

Figure 6.5 shows the connection of DAC0832 and operational amplifier.

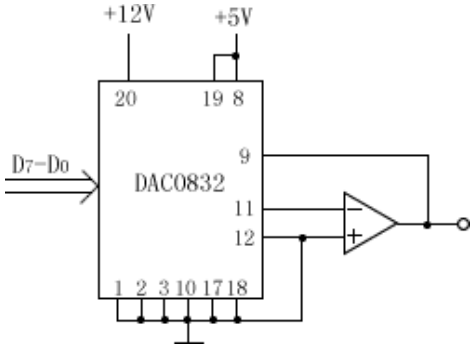


Figure 6.5 Current/voltage conversion circuit

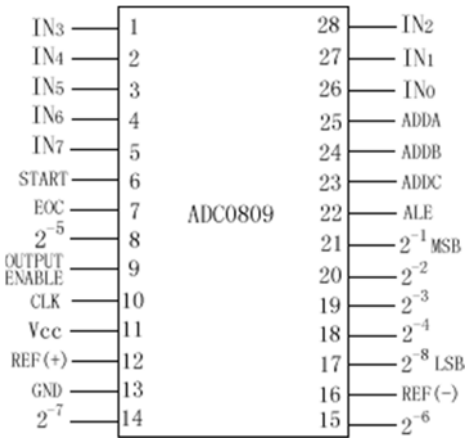


Figure 6.6 ADC0809 A/D converter

3) A/D converter ADC0809

Analog to digital conversion is the process by which an analog quantity is converted to digital form. Figure 6.6 is pin out diagram of ADC0809 A/D converter. It is an 8-bit analog to digital converter with 8 channels, and can convert 8 routes analog quantity inputs which input through IN_0～IN_7 and selected by the 3-bit binary code on ADDA, ADDB and ADDC. For example, in this experiment, only 1 signal needs conversion. If the signal goes to IN_0, the voltages input on ADDA, ADDB and ADDC all should be LOW. If the signal goes to IN_1, ADDA should be HIGH, and so on.

For this chip, U_{CC} on +5V, REF (+) and REF (-) are reference voltage inputs with the former normally on +5V, and the latter to ground. Analog voltage input ranges from 0～5V. The 8 digital quantity output terminals 2^{-1}, 2^{-2},……. 2^{-8}, are relative to reference voltage. Other control terminals are as following:

CLK: timing clock input signal.

START: start conversion signal, HIGH active. Conversion process is going on when it goes from high to low.

ALE: address input permit. Chose input analog quantity route, permitting address input, and HIGH active.

EOC: conversion finished signal. It is a output signal, and HIGH active.

OUTPUT ENABLE (OE): output permit signal. HIGH active. When it is LOW, ADC0809 output is in high-resistance state.

Figure 6.7 shows the ADC0809 conversion timing diagram.

4) 4-bus-buffer (three-state output) 74LS125

There are four buffers inside one chip, and three-state output. See appendix for its pin-out diagram. Therein, A is input, Y is output, and C is control terminal. When C is LOW, Y = A; When C is HIGH, output is disconnected and in high-resistance state.

5) 4-bit binary synchronous counter 74LS163

74LS163 is medium scale integration circuit chip. See appendix for its pin-out diagram. The function table is shown in table 6-2.

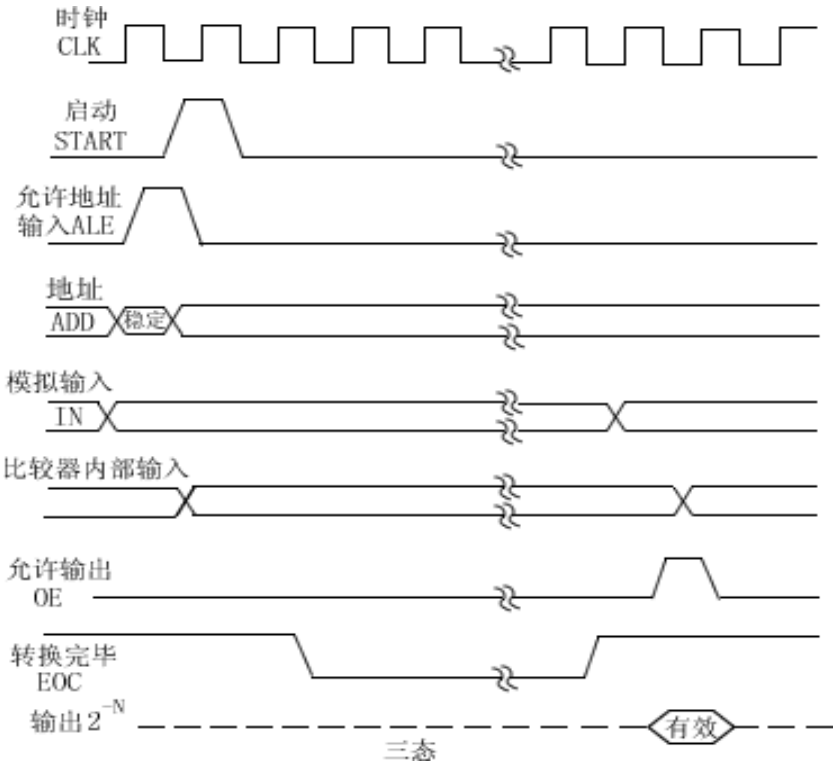


Figure 6.7 ADC0809 conversion timing diagram

From the table, it is seen that when reset CLR = 1, set LOAD = 1, and count permit P=T=1, it works at count state, and pin 15 output carry out pulse.

This chip can realize programmable counter, in which each output can be set as any voltage. When LOAD=0, outputs are identical to inputs under the next pulse. Reset of this counter is synchronous, which means reset can realize only when CLR=0 and a clock pulse coming.

Table6-2 74LS163 function table

Inputs									Outputs			
CP	CLR	LOAD	P	T	A	B	C	D	Q_A	Q_B	Q_C	Q_D
↑	0	×	×	×	×	×	×	×	0	0	0	0
↑	1	0	×	×	A	B	C	D	A	B	C	D
×	1	1	0	×	×	×	×	×	keep			
×	1	1	×	0	×	×	×	×	keep			
↑	1	1	1	1	×	×	×	×	Count			

3. Preparation Requirements

1) Design a circuit by ADC0809, 2114, 74LS125 and 4-bit binary counter 74LS163 which can convert the voltage from DC stabilized voltage source 0 ～5V to 4-bit digital quantities and store them in RAM, and check whether these voltage digital quantities stored are correct by LEDs. As the maximum number of address that 74LS163 can decode is 16, 16 voltage quantities are enough.
2) Study out a circuit by 73LS163 to test D/A converter DAC0832.
3) Design a waveform generator by 74LS163, ADC0809, DAC0832, 74LS125 and 2114 whose period of the wave produced is T, and instantaneous value is more

than zero permanently. Requirements are as following:

(1) The instantaneous values of the wave to be produced come from DC stabilized voltage source, and then ADC0809 converts them into 4-bit digital quantities and store them in 2114 in sequence. The instantaneous value can be taken in equal time interval T/15 in a whole period T.

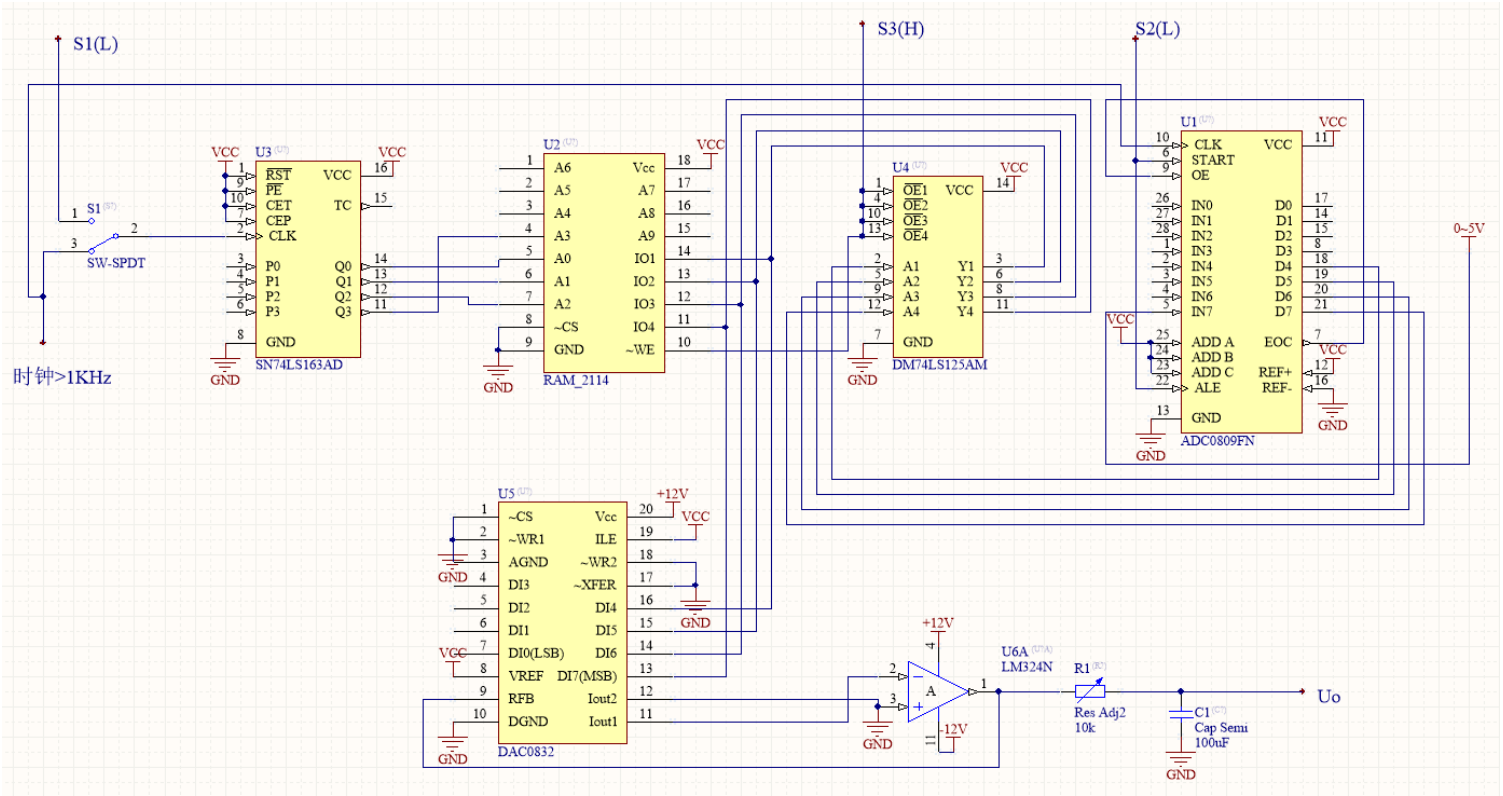
(2) DAC0832 converts the stored digital quantities of voltage into smooth periodic analog voltage.

If you feel difficult, you can have a reference to the reference scheme at the back.

4. Experiment Contents

1) Build the A/D circuit. Convert analogue signal from DC power supply to digital quantity and store into RAM2114. Check the function of buffer 74LS125. Switch off the power and remain the circuit for further use.
2) Build the circuit for testing D/A converter DAC0832 by 74LS163. Off the power.
3) Based on steps 1 and 2, join OP-amp and filter circuit to make the circuit to produce periodic waves. Observe the “stairsteps” wave and smooth wave on CRO.
4) Selection: Produce a waveform you want to realize.
   Consideration: Whether or not a piece of 74LS163 can store/take 32 numbers?

5. Experiment Scheme



I design this circuit based on given ICs and reference scheme. After I finish wiring, first, ADC0809 transfers analog signal (voltage) to digital signal, at the same time 74LS163 choose the right address. Then, S3 turns to high level, and data from ADC can be stored in RAM_2114. After making all data stored (16 in total), connect CLK of 163 to 1KHz, and numbers stored are transferred to DAC0832. Then I observe step in stairs

waveform on the oscilloscope.

The relationship of output and voltage is listed as follow:

$U_{IN} = 5 \times \left(\frac{1}{2}D_7 + \frac{1}{4}D_6 + \frac{1}{8}D_5 + \frac{1}{16}D_4\right)$			
State of output	Voltage(V)	State of output	Voltage(V)
0000	0	1000	2.5000
0001	0.3125	1001	2.8125
0010	0.6250	1010	3.1250
0011	0.9375	1011	3.4375
0100	1.2500	1100	3.7500
0101	1.5625	1101	4.0625
0110	1.8750	1110	4.3750
0111	2.1875	1111	4.6875

Table 1 Correspondence from digital signal to voltage

6. Conclusions and analysis

1) Design principle and logic diagram have been displayed above.

Figure 1 photo of waveform

I draw the waveform as follow:

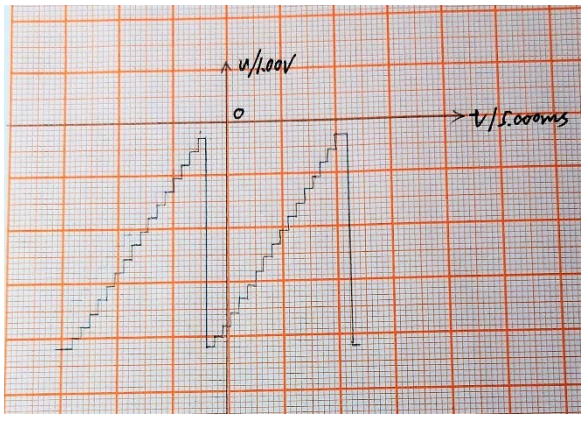


Figure2 waveform from LM324

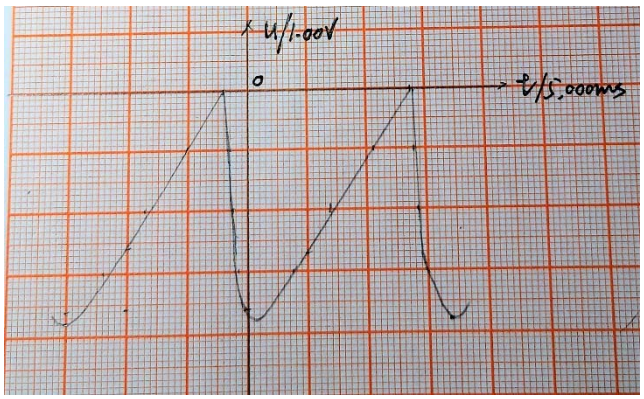


Figure3 waveform from filter

2) Figure2 is the waveform without filtering, it has obviously “stair steps”. When I adjust the potentiometer to increase resistance, the curve becomes more and more smooth, just like figure3.
3) From figure1, it seems that my waveform receives some interference. The reasons might be various. To figure out, I connect 74LS163 to DAC0832, and get figure 4.

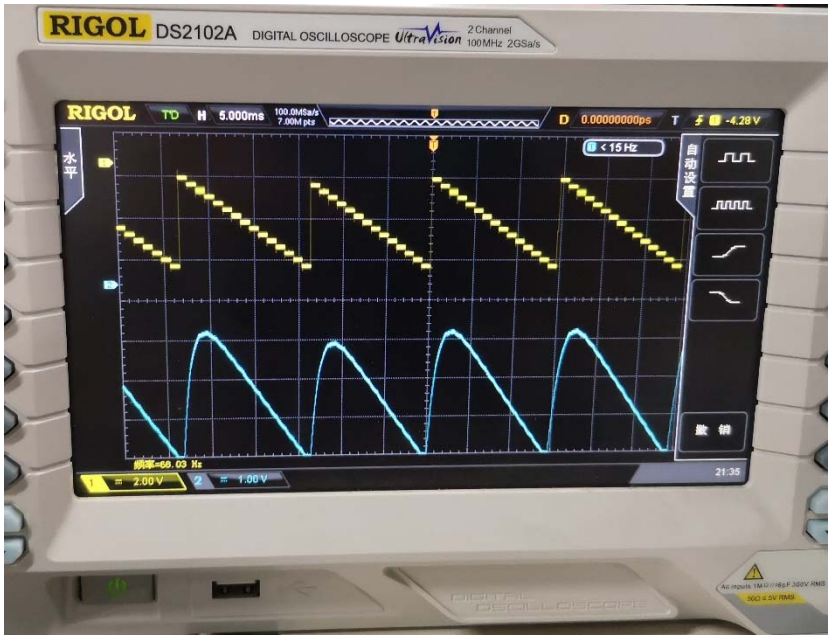


Figure 4 Waveform when 163 is connected to DAC0832

The waveform on the screen is very good, indicate that the problem might be IC 2114, wires or ground. At first, my wires are not long enough, so I connect 2 lines into one, and this connection may cause signal attenuation. And if one connection from one pin to ground is poor, interference also comes. Now I finally understand the importance of copper plating when designing a PCB board.

7. Summary

From now on, I have finished every experiment this semester. Luckily, although I missed first two experiments, I finished them in the end by my own. And I finish every experiment of digital circuit, no fail! The secret of success is easy: connect the ICs into circuit only after testing them and be patient. After a long period of wiring, analysis, the feeling of accomplishment always brings me power to start the next. Thanks for Ms. Huang and Mr. Li, I really learn a lot this semester.