

AMD Zynq™ UltraScale+™ MPSoCs

	CG Devices	EG Devices	EV Devices
Application Processor	Dual -core Arm® Cortex®-A53 MPCore™ up to 1.3 GHz	Quad-core Arm Cortex-A53 MPCore up to 1.5 GHz	Quad-core Arm Cortex-A53 MPCore up to 1.5 GHz
Real-Time Processor	Dual-core Arm Cortex-R5F MPCore up to 533 MHz	Dual-core Arm Cortex-R5F MPCore up to 600 MHz	Dual-core Arm Cortex-R5F MPCore up to 600 MHz
Graphics Processor		Mali™-400 MP2	Mali™-400 MP2
Video Codec			H.264 / H.265
Programmable Logic	81K–600K System Logic Cells	81K–1143K System Logic Cells	192K–504K System Logic Cells
Applications	 Sensor Processing & Fusion Motor Control Low-cost Ultrasound Traffic Engineering 	 Flight Navigation Missile & Munitions Military Construction Secure Solutions Networking Cloud Computing Security Data Center Machine Vision Medical Endoscopy 	 Situational Awareness Surveillance/Reconnaissance Smart Vision Image Manipulation Graphic Overlay Human Machine Interface Automotive ADAS Video Processing Interactive Display

AMD Zynq™ UltraScale+™ MPSoCs: CG Devices

4																
		Device Name ⁽¹⁾	ZU1CG	ZU2CG	ZU3CG	ZU3TCG	ZU4CG	ZU5CG	ZU6CG	ZU7CG	ZU9CG					
	Application	Processor Core		Dual-core Arm® Cortex®-A53 MPCore™ up to 1.3 GHz												
	Processor Unit	Memory w/ECC	L1 Cache 32 KB I / D per core, L2 Cache 1 MB, on-chip Memory 256 KB													
(PS)	Real-Time	Processor Core				Dual-core Arm	Cortex-R5F MPCor	e up to 533 MHz								
E S	Processor Unit	Memory w/ECC			L1 Cach	ne 32 KB I / D per c	ore, Tightly Coupled	d Memory 128 KB p	er core							
ste	External	Dynamic Memory Interface			x16: DDR	4 w/o ECC; x32/x64	1: DDR4, LPDDR4, D	DR3, DDR3L, LPDDR	3 w/ ECC							
Sy	Memory	Static Memory Interfaces					NAND, 2x Quad-SP									
ing	Campagativity	High-Speed Connectivity			PCle® Gen2	x4, 2x USB3.0, SAT	A 3.1, DisplayPort™	[™] , 4x Tri-mode Gigal	oit Ethernet							
ess	Connectivity	General Connectivity			2xUSB 2.0	0, 2x SD/SDIO, 2x l	JART, 2x CAN 2.0B,	2x I2C, 2x SPI, 4x 3	32b GPIO							
6	Integrated	Power Management				Full / Low	/ PL / Battery Powe	er Domains								
Ь	Block	Security					RSA, AES, and SHA									
	Functionality	AMS - System Monitor				10-bit, 1 MSPS -	- Temperature and	Voltage Monitor								
PS	to PL Interface						12 x 32/64/1	28b AXI Ports								
	D	System Logic Cells (K)	81	103	154	157	192	256	469	504	600					
	Programmable	CLB Flip-Flops (K)	74	94	141	144	176	234	429	461	548					
	Functionality	CLB LUTs (K)	37	47	71	72	88	117	215	230	274					
		Distributed RAM (Mb)	1.0	1.2	1.8	2.1	2.6	3.5	6.9	6.2	8.8					
Ľ.	Memory	Total Block RAM (Mb)	3.8	5.3	7.6	5.1	4.5	5.1	25.1	11.0	32.1					
gic (PL)		UltraRAM (Mb)	-	-	-	14.0	13.5	18.0	-	27.0	-					
ogi	Clocking	Clock Management Tiles (CMTs)	3	3	3	1	4	4	4	8	4					
e Ľ		DSP Slices	216	240	360	576	728	1,248	1,973	1,728	2,520					
Programmable Lo	Integrated ID	PCI Express®	-	-	-	1x Gen3x8	2x Gen3x8 ⁽²⁾	2x Gen3x8 ⁽²⁾	-	1x Gen3x16 & 1x Gen3x8	-					
an	Integrated IP	150G Interlaken	-	-	-	-	-	-	-	-	-					
ogr		100G Ethernet MAC/PCS w/RS-FEC	-	-	-	-	-	-	-	-	-					
Pr		AMS - System Monitor	1	1	1	1	1	1	1	1	1					
	Transceivers	GTH Transceivers ⁽³⁾	-	-	-	8	16	16	24	24	24					
	Transceivers	GTY Transceivers	-	-	-	-	-	-	-	-	-					
	Speed Grades	Extended ⁽⁴⁾		-1 -2	2 -2L				-1 -2 -2L -3							
	Speed Grades	Industrial	-1 -1L -2													

^{1.} For full part number details, see the Ordering Information section in DS891, Zyng UltraScale+ MPSoC Overview.

^{2.} ZU4 and ZU5 also support 1x Gen3x16 based on available GTH.

^{3.}GTH data rates are package dependent:

a) Maximum 12.5 Gb/s in SFVC784, SFVD784, and SFVE784

b) Maximum 16.3 Gb/s in all other packages

AMD Zynq™ UltraScale+™ MPSoCs: EG Devices

		J														
		Device Name ⁽¹⁾	ZU1EG	ZU2EG	ZU3EG	ZU3TEG	ZU4EG	ZU5EG	ZU6EG	ZU7EG	ZU9EG	ZU11EG	ZU15EG	ZU17EG	ZU19EG	
	Application	Processor Core		Quad-core Arm® Cortex®-A53 MPCore™ up to 1.5 GHz												
	Processor Unit	Memory w/ECC		L1 Cache 32 KB I / D per core, L2 Cache 1 MB, on-chip Memory 256 KB												
ווייי	Real-Time	Processor Core	Dual-core Arm Cortex-R5F MPCore™ up to 600 MHz													
	Processor Unit	Memory w/ECC		L1 Cache 32 KB I / D per core, Tightly Coupled Memory 128 KB per core												
•	Graphic & Video	Graphics Processing Unit							00 MP2 up t							
yst	Acceleration	Memory							L2 Cache 64	КВ						
g Sy	External	Dynamic Memory Interface				x16:	DDR4 w/o E0	CC; x32/x64: I	DDR4, LPDDF	R4, DDR3, DD	R3L, LPDDR3	B w/ ECC				
sin	Memory	Static Memory Interfaces						N.	AND, 2x Qua	d-SPI						
ces	Connectivity	High-Speed Connectivity PCIe® Gen2 x4, 2x USB3.0, SATA 3.1, DisplayPort™, 4x Tri-mode Gigabit Ethernet														
Pro	Confidential	General Connectivity	2xUSB 2.0, 2x SD/SDIO, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO													
<u>-</u>	Integrated Block – Functionality	Power Management Full / Low / PL / Battery Power Domains														
		Security	RSA, AES, and SHA													
	<u> </u>	AMS - System Monitor		10-bit, 1 MSPS – Temperature and Voltage Monitor												
PS t	to PL Interface									128b AXI Por						
	Programmable Functionality	System Logic Cells (K)	81	103	154	157	192	256	469	504	600	653	747	926	1,143	
		CLB Flip-Flops (K)	74	94	141	144	176	234	429	461	548	597	682	847	1,045	
		CLB LUTs (K)	37	47	71	72	88	117	215	230	274	299	341	423	523	
•		Max. Distributed RAM (Mb)	1.0	1.2	1.8	2.1	2.6	3.5	6.9	6.2	8.8	9.1	11.3	8.0	9.8	
(PL	Memory	Total Block RAM (Mb)	3.8	5.3	7.6	5.1	4.5	5.1	25.1	11.0	32.1	21.1	26.2	28.0	34.6	
gic		UltraRAM (Mb)	-	-	-	14.0	13.5	18.0	-	27.0	-	22.5	31.5	28.7	36.0	
ρ̈	Clocking	Clock Management Tiles (CMTs)	3	3	3	1	4	4	4	8	4	8	4	11	11	
ole		DSP Slices	216	240	360	576	728	1,248	1,973	1,728	2,520	2,928	3,528	1,590	1,968	
mal		PCI Express®	-	-	-	1x Gen3x8	2x Gen3x8 ⁽²⁾	2x Gen3x8 ⁽²⁾	-	1x Gen3x16 & 1x Gen3x8 ⁽³⁾	-	2x Gen3x16 & 2x Gen3x8 ⁽³⁾	-	3x Gen3x16 & 1x Gen3x8 ⁽³⁾	3x Gen3x16 & 2x Gen3x8 ⁽³⁾	
[ב	Integrated IP	150G Interlaken	-	-	-	-	-	-	-	-	-	1	-	2	4	
Programmable Logic (PL)		100G Ethernet MAC/PCS w/RS-FEC	-	-	-	-	-	-	-	-	-	2	-	2	4	
		AMS - System Monitor	1	1	1	1	1	1	1	1	1	1	1	1	1	
	Transceivers	GTH Transceivers ⁽⁴⁾	-	-	-	8	16	16	24	24	24	32	24	44	44	
	Hanstelvers	GTY Transceivers	-	-	-	-	-	-	-	-	-	16	-	28	28	
	Speed Grades	Extended ⁽⁵⁾		-1 -	2 -2L			-1 -2	-2L -3				-1 -2 -2L -3	<u> </u>		

^{1.} For full part number details, see the Ordering Information section in DS891, Zyng UltraScale+ MPSoC Overview.

Industrial



-1 -1L -2

^{2.} ZU4 and ZU5 also support 1x Gen3x16 based on available GTH.

^{3.} PCle block configuration dependent on available transceivers.

^{4.} GTH data rates are package dependent:

a) Maximum 12.5 Gb/s in SFVC784, SFVD784, and SFVE784

b) Maximum 16.3 Gb/s in all other packages

AMD Zynq™ UltraScale+™ MPSoCs: EV Devices

	<i>-</i> — <i>-</i>	<u> </u>	00001 =									
		Device Name ⁽¹⁾	ZU4EV	ZU5EV	ZU7EV							
	Application Processor Unit	Processor Core	Qı	Quad-core Arm® Cortex®-A53 MPCore™ up to 1.5 GHz								
	Application Processor Offic	Memory w/ECC		ory 256 KB								
(5	Real-Time Processor Unit	Processor Core		Dual-core Arm Cortex-R5F MPCore [™] up to 600 MF	łz							
(PS)		Memory w/ECC	L1 Cache	KB per core								
ma	Graphic & Video	Graphics Processing Unit		Mali™-400 MP2 up to 667 MHz								
ste	Acceleration	Memory		L2 Cache 64 KB								
Sy	External Memory	Dynamic Memory Interface	x16: DDR4 v	v/o ECC; x32/x64: DDR4, LPDDR4, DDR3, DDR3L, LP	DDR3 w/ ECC							
ing	external Memory	Static Memory Interfaces		NAND, 2x Quad-SPI								
ess		High-Speed Connectivity	PCIe® Gen2 x4	PCIe® Gen2 x4, 2x USB3.0, SATA 3.1, DisplayPort™, 4x Tri-mode Gigabit Ethernet								
٥٥.	Connectivity	General Connectivity	2xUSB 2.0, 2	2x SD/SDIO, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI,	4x 32b GPIO							
P		Power Management		Full / Low / PL / Battery Power Domains								
	Integrated Block	Security		RSA, AES, and SHA								
	Functionality	AMS - System Monitor		10-bit, 1 MSPS – Temperature and Voltage Monitor								
PS to	o PL Interface			12 x 32/64/128b AXI Ports								
		System Logic Cells (K)	192	256	504							
	Programmable Functionality	CLB Flip-Flops (K)	176	234	461							
		CLB LUTs (K)	88	117	230							
		Max. Distributed RAM (Mb)	2.6	3.5	6.2							
()	Memory	Total Block RAM (Mb)	4.5	5.1	11.0							
(P		UltraRAM (Mb)	13.5	18.0	27.0							
gic	Clocking	Clock Management Tiles (CMTs)	4	4	8							
e Logic (PL)		DSP Slices	728	1,248	1,728							
ple		Video Codec Unit (VCU)	1	1	1							
Programmabl		PCI Express® Gen 3x16	2x Gen3x8 ⁽²⁾	2x Gen3x8 ⁽²⁾	1x Gen3x16 &							
E	Integrated IP	•			1x Gen3x8 ⁽³⁾							
gra		150G Interlaken	<u>-</u>	-	-							
ro		100G Ethernet MAC/PCS w/RS-FEC	<u>-</u>	-	-							
		AMS - System Monitor	1	1	1							
	Transceivers	GTH Transceivers ⁽⁴⁾	16	16	24							
		GTY Transceivers	<u>-</u>	-	<u>-</u>							
	Speed Grades	Extended ⁽⁵⁾		-1 -2 -2L -3								
		Industrial	Industrial -1 -1L -2									

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1. For full part number details, see the Ordering Information section in DS891, Zynq UltraScale+ MPSoC Overview. 2.ZU4 and ZU5 also support 1x Gen3x16 based on available GTH.

3.PCle block configuration dependent on available transceivers.

-2LE (Tj = 0°C to 110°C). For more details, see the Ordering Information section in DS891, Zyng UltraScale+ MPSoC Overview.



GTH data rates are package dependent:
 All data rates are package dependent:
 All data rates are package dependent:

a) Maximum 12.5 Gb/s in SFVC784 and SFVE784

b) Maximum 16.3 Gb/s in all other packages

C1760

D1760

E1924

42.5x42.5

42.5x42.5

45x45

1.0

1.0

1.0

AMD Zynq™ UltraScale+™ MPSoCs

			<u> </u>				_								
			ZU1	ZU2	ZU3	ZU3T	ZU4	ZU5	ZU6	ZU7	ZU9	ZU11	ZU15	ZU17	ZU19
Pkg Footprint ^(2,3)	Dimensions (mm)	Ball Pitch (mm)							3V HD I/O, 1. H 16.3 Gb/s,	8V HP I/Os GTY 32.75 Gb/s					
4494	9.5x15	0.5	170, 24, 58 4, 0, 0												
\530	9.5x16	0.5		170, 24, 58 4, 0, 0	170, 24, 58 4, 0, 0										
484	19x19	0.8	170, 24, 58 4, 0, 0	170, 24, 58 4, 0, 0	170, 24, 58 4, 0, 0										
625	21x21	0.8	170, 24, 156 4, 0, 0	170, 24, 156 4, 0, 0	170, 24, 156 4, 0, 0										
C784 ⁽⁴⁾	23x23	0.8	214, 24, 156, 4, 0, 0	214, 96, 156 4, 0, 0	214, 96, 156 4, 0, 0	214, 72, 52 4, 4, 0	214, 96, 156 4, 4, 0	214, 96, 156 4, 4, 0							
784 ^(4,5)	23x23	0.8				214, 72, 52 4, 8, 0									
784 ^(4,5)	23x23	0.8					214, 72, 58 4, 8, 0	214, 72, 58 4, 8, 0							
900	31x31	1.0					214, 48, 156 4, 16, 0	214, 48, 156 4, 16, 0		214, 48, 156 4, 16, 0					
900	31x31	1.0							214, 48, 156 4, 16, 0		4, 48, 156 4, 16, 0		214, 48, 156 4, 16, 0		
1156	35x35	1.0							214, 120, 208 4, 24, 0		1, 120, 208 4, 24, 0	2	214, 120, 208 4, 24, 0		
1156	35x35	1.0								214, 48, 312 4, 20, 0		214, 48, 312 4, 20, 0			
1517	40x40	1.0										214, 72, 416 4, 16, 0		214, 72, 572 4, 16, 0	214, 72, 572 4, 16, 0
1517	40x40	1.0								214, 48, 416 4, 24, 0		214, 48, 416 4, 32, 0			

4, 32, 0 214, 96, 416

4, 32, 16

214, 96, 416

4, 32, 16

214, 48, 260

4, 44, 28

214, 96, 572

4, 44, 0

214, 96, 416

4, 32, 16

214, 48, 260

4, 44, 28

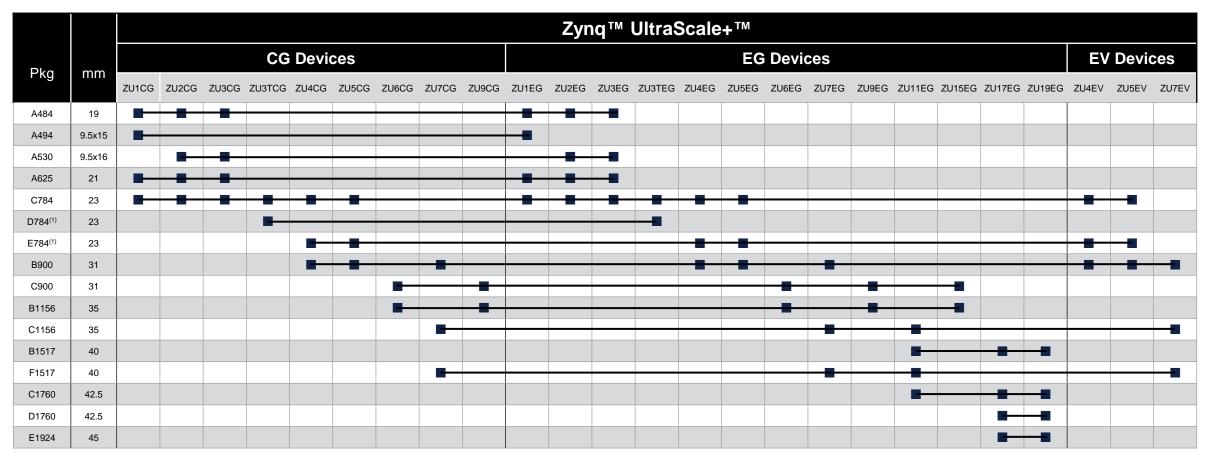
214, 96, 572

4, 44, 0

XMP104 (v2.8)

AMD Zynq™ UltraScale+™ MPSoC Device Migration Table

The Zynq UltraScale+ family provides footprint compatibility to enable users to migrate designs from one device to another. Any two packages with the same footprint identifier code (last letter and number sequence) are footprint compatible.

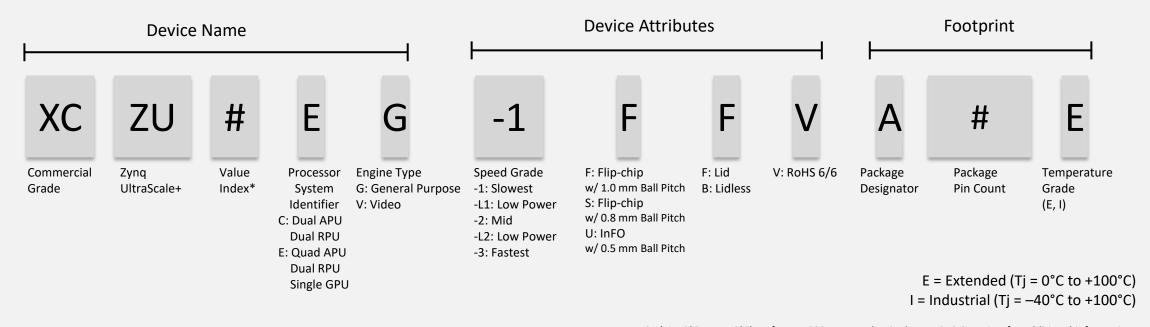


Notes



^{1.} Migration between D784 and E784 is supported. See UG1075, Zyng UltraScale+ Device Packaging and Pinouts Product Specification.

AMD Zynq™ UltraScale+™ MPSoC Ordering Information



Note: -L2E (Tj = 0°C to +110°C). Refer to DS891, Zynq UltraScale+ MPSoC Overview for additional information.

*T in ZU3T value index denotes increase in resources and transceivers vs. ZU3.



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