NATIONAL UNIVERSITY OF SINGAPORE

SCHOOL OF COMPUTING

SEMESTER II AY2018/2019

MIDTERM ASSESSMENT FOR
CG1112: ENGINEERING PRINCIPLES AND PRACTICE II

9th March 2019 Time Allowed: 1 Hour

INSTRUCTIONS TO CANDIDATES:

1. Use **2B Pencil** to shade the **OCR form**. Ensure your student number is shaded properly.

2. This assessment paper consists of **EIGHTEEN (18)** questions.

3. This assessment paper comprises **ELEVEN (11) printed pages** including this front page.

4. Each MCQ carries 1 mark. No penalty for wrong answer. Total marks for the paper is **18**.

5. This is a **close book assessment** with **one A4 reference sheet** allowed.

6. Submit only the **OCR** form at the end of the assessment.

Question 1 and 2 uses the following context:

Alex implemented function **`print_power_table(B, E)`** to print out a table of exponentials. The value at row $\mathbf{B_x}$ and column $\mathbf{E_y}$ is $\mathbf{B_x}^{E_y}$, where rows and columns both start counting from 1, e.g. **`print_power_table( 3, 4 )`** give the following output:

1	1	1	1
2	4	8	16
3	9	27	81

```
void print_power_table( int B, int E )
{
    int row, col;

    for (row = 1; row <= B; row++)
        for (col = 1; col <= E; col++)
            printf("%d ", pow(row, col) );
    printf("\n");
}
```

1. ***Ignoring*** the cost of the **pow()** function, the ***tightest complexity*** for the code above is:
   a. O(N^2)
   b. O(B)
   c. O(E)
   d. O(B x E)
   e. O(B^2 x E^2)

Commented [ys1]: Ans. (a) is incorrect as "N" is not defined in this question + inaccurate. This code depends on both the number of column and row.

2. If the **`pow()`** function is implemented as follow:

```
void pow( int base, int exp )
{
    if (exp == 0)
        return 1;
    return base * pow(base, exp-1);
}
```

The updated tightest complexity of **`print_power_table()`** with **`pow()`** function included is:
   a. O(N^2 x E)
   b. O(B^2)
   c. O(E^2)
   d. O(B x E^2)
   e. O(B^3 x E^2)

Commented [ys2]: Ans. pow() takes O(E), as it is a recursive function with O(E) invocation and each takes O(1) time.
So, considered together with q1, you get O(B x E x E).

3. If we are told that algorithm A is of complexity O(f(N)) with a constant **N_0 and K** that satisfy the Big-O definition. Give the correct pair of words that completes the following statements for algorithm A:
   i. Given a $N_1 > N_0$ and keeping the same K, it ___________ satisfy the O(f(N)) definition.
   ii. Given a K' < K and keeping the same N_0, it _____________ satisfy the O(f(N)) definition.

	i	*ii*
a.	must	must
b.	**must**	**may**
c.	may	must
d.	may	may
e.	None of the above.	

Commented [ys3]: Ans. The second statement is about the multiple possibilities of N0 and K. The original K can a constant that is higher than absolutely necessary, which allows a few K' to satisfy the definition. However, this not true **in general,** e.g. K' can be 0 ➔ no way that O(f(n)) can now be satisfied.

4. Which of the following statements regarding Pi and Arduino Uno is/are TRUE?
   i. The SD Card on the Pi plays the role of "hard disk" of a normal PC.
   ii. Pi requires a keyboard and mouse to boot up properly.
   iii. Raspbian (the OS used on Pi) is a variant of the Windows 7 operating system.

   a. (i) only.
   b. (i) and (ii) only.
   c. (ii) and (iii) only.
   d. (i), (ii) and (iii).
   e. None of the above.

Commented [ys4]: (ii) is wrong as you can have headless pi setup.
(iii) Raspbian is Linux distribution.

5. Which of the following statements regarding **Git Remote Repository** is/are TRUE?
   i. It is essentially a git repository placed on a remotely accessible location.
   ii. A "Git Fetch" operation download the latest version of the repository from remote and merge with local content.
   iii. When using a web base repository hosting service (e.g. GitHub), there is no way for us to restrict user access to the remote repository, i.e. it is accessible by everyone.

   a. (i) only.
   b. (i) and (ii) only.
   c. (ii) and (iii) only.
   d. (i), (ii) and (iii).
   e. None of the above.

Commented [SYJ5]: Ans.
(ii) is false as you still need a separate "Git Merge" operation for merging, i.e. "Fetch" only download latest version. (iii) is false, e.g. can use private repo and control the collaborator

6. Suppose our good friends Uno and Duo are working on the file EasyMidterm.c under the same Git remote repository. Suppose Duo see the following content after an attempted merge:

```
The midterm is supposed to be
<<<<<<< HEAD
easy.
=======
hard.
>>>>>>>
Something is
<<<<<<< HEAD
right.
=======
very wrong.
>>>>>
```

Which of the following statement(s) is / are **TRUE**?

i.	Duo wrote the line "**easy.**".
ii.	Duo must be the one who wrote "**Something is**".
iii.	Uno wrote the line "**right.**".

a. (i) only.
b. (i) and (ii) only.
c. (ii) and (iii) only.
d. (i), (ii) and (iii).
e. None of the above.

Commented [ys6]: Ans.

(ii) is unknown, i.e. the line can be written by either Uno or Duo in earlier versions.

7. You decide to operate the AT328p using the Internal 128KHz RC Oscillator. When operating Timer0 in Phase-Correct PWM mode, what is the largest period of the PWM signal using only the internal pre-scaler.

The list of prescalers available within the microcontroller are 1, 8, 64, 256 and 1024.

a. 4.08 s
b. 0.245 s
c. 7.8 us
d. 8 ms
e. 10 ms

Commented [RS7]: f = (128k) / 1024 * 510) = 0.245Hz
T = 1/f = 4.08s

8. Two switches are connected to PORTB pins 0 and 5. The switch connected to Pin 0, is operating in Active-High mode (a logic ‘1’ is read when the switch is pressed, ‘0’ otherwise). The switch connected to Pin 5 is operating in Active-Low mode (a logic ‘0’ is read when the switch is pressed, ‘1’ otherwise). An Active-Low LED is connected to PORTD Pin 7 (a logic ‘0’ turns it ON and a logic ‘1’ turns it OFF).

   Given the following definitions:

```
#define MASK_BIT_7 0b10000000
#define MASK_BIT_5 0b00100000
#define MASK_BIT_0 0b00000001
```

   Which configuration below is correct?

a.	DDRB = (MASK_BIT_5) | (MASK_BIT_0) ;
	DDRD = (MASK_BIT_7);

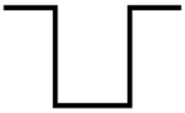
b.	**DDRB &= ~((MASK_BIT_5) | (MASK_BIT_0)) ;** **DDRD |= (MASK_BIT_7);**
c.	DDRB &= ((MASK_BIT_5) | (MASK_BIT_0)) ; DDRD |= ~(MASK_BIT_7);

d.	DDRB = ((MASK_BIT_5) & (MASK_BIT_0)) ;
	DDRD = (MASK_BIT_7) & 0x00;

e.	DDRB &= (MASK_BIT_7); DDRD |= ~((MASK_BIT_5) | (MASK_BIT_0)) ;

Commented [RS8]: (b) This is the setting that sets PortB 5,0 to input (0) and PortD7 (1) to output.

9. The figure below shows the pulse received from a motor encoder every time it rotates



   What are the possible Interrupts that can be used to capture this encoder pulse?

   a) INT0
   b) INT1
   c) Timer0
   d) Timer2
   e) All of the above

Commented [RS9]: All are possible options.

10. Both Timer0 and Timer2 are configured to automatically generate a Phase-Correct PWM at the output OC0A and OC2A pins. The Output Compare Match Interrupts are also enabled and Nested Interrupts are allowed. Both OCR0A and OCR2A are initialized with the same value.

    Examine the following statements:

    1) Due to pre-emption of lower priority interrupts by higher-priority interrupts, the PWM duty-cycle and/or period can be affected.
    2) The duty-cycle and/or period of the PWM signals will not be affected by nested interrupts.
    3) Only the Timer0 interrupt can affect the duty cycle and/or period of the PWM signals.
    4) Only the Timer2 interrupt can affect the duty cycle and/or period of the PWM signals.

    Which of the above statements are TRUE?

    a. Only Statements 3 and 4
    b. Only Statement 2
    c. Only Statement 1
    d. Only Statements 1 and 3
    e. Only Statements 1 and 4

Commented [RS10]: Sinec the PWM outputs are generated automatically by the HW, the ISR does not play a part.

11. Timer0 and Timer2 are configured as per the earlier question (Question 10). The prescaler for Timer0 is 8 and the prescaler for Timer2 is 1024. Which of the following statements is correct?

    a. Timer0 PWM and Timer2 PWM will have the same period.
    b. Timer2 PWM will have a shorter period that Timer0 PWM.
    c. Both Timer0 and Timer2 will have the same PWM duty-cycle.
    d. Timer0 PWM will have a smaller duty-cycle than Timer2 PWM.
    e. Timer2 PWM will have a smaller duty-cycle than Timer0 PWM.

Commented [RS11]: Since the OCR0 registers have the same value, the Duty-Cycle will be the same.

12. An LED is connected to PORTB Bit 4 in Active-Low configuration, with the DDRB register already configured accordingly. Examine the following code snippet to control the LED. Note that the initial value of variable ‘x’ is not yet decided.

```
char x = <to be decided>;
x = (((x & 0x80) >> 4) | ((x & 0x01) << 4));
if(x & 0x08)
    PORTB &= 0xEF;
else
    PORTB = 0xFF;
```

Which option has all possible values of ‘x’ that will **ALWAYS** turn **ON** the LED.

a. 0xC1, 0x1A, 0x21
b. 0x11, 0xD1, 0x9A
c. 0xFF, 0xAA, 0x88
d. 0xA1, 0x11, 0x1C
e. None of the above

Commented [RS12]: The code is checking for the MSB to be set.
Only this combination has all three values with the MSB set to '1'.

13. In the context of soldering, what does rosin flux do?

a. Helps conduct heat better to make better joints.
b. Cleans the joints to help solder flow and set better.
c. Produces smoke to make what you do look impressive.
d. Protects the components from heat damage.
e. Reduces electromagnetic interference from the soldering iron.

Commented [SYJ13]: **This is the main purpose for flux – clean the joints especially of oxides.**

14. Bob is a very environmentally minded engineer and would like to build products that minimize impact on the environment. Which of the following steps can he take?

i. Deactivate parts of the Atmega328P that are not being used at the moment.
ii. Use leaded solder because it takes less energy to solder components.
iii. Increase the clock frequency of the Atmega328P.
iv. Use conventional alkaline batteries instead of rechargeable batteries.

a. i. and iv. ONLY are correct.
b. ii. and iv. ONLY are correct.
c. i. ONLY is correct.
d. ii. and iii. ONLY are correct.
e. iv. ONLY is correct.

Commented [SYJ14]: **ii. pollutes the world with leaded solder when the circuit is discarded, iii increases energy consumption, iv. increases waste.**

15. We have an Arduino with a clock rate of 16 MHz that is polling a device that sends a 4-byte reading once every 10 milliseconds. Which of the following statements is TRUE?

   a. Decreasing the clock rate of the Arduino to 4 MHz will increase the number of instructions wasted in polling because the Arduino will now execute more instructions each second.
   b. Increasing the clock rate to 20 MHz will decrease the number of instructions wasted in polling by letting us read the device faster.
   c. Increasing the clock rate to 20 MHz will increase the number of instructions wasted in polling because the device will now produce the data more slowly.
   d. Decreasing the clock rate of the Arduino to 4 MHz will reduce the number of instructions wasted in polling because the hardware because the device will now produce the data more quickly.
   e. Increasing the clock rate to 20 MHz will increase the number of instructions wasted in polling because the Arduino is now able to execute more instructions per second.

Commented [SYJ15]: The key idea here is that the device operates independently of the MCU, and hence will always send 4 bytes every 10 ms regardless of the MCU's clock speed. If they understand slide 11 of the notes they will realize that the MCU operates at one instruction per clock cycle, and increasing to 20 MHz means more instructions being executed in one second, hence more wastage.

16. We have an Atmega328P with a clock frequency of 8 MHz. Suppose we use Timer 0 in CTC mode with a prescalar of 64, with a suitable compare value loaded into OCR0A to trigger a TIMER0_COMPA_vect interrupt once every millisecond. How many clock cycles are there in between each triggering of this interrupt?

   a. 8,000
   b. 16,000
   c. 64,000
   d. 125,000
   e. 250,000

Commented [SYJ16]: This is a trick question; there will always be 8000 clock cycles in each millisecond regardless of the prescalar.

17. We now use interrupts instead of polling on a 16 MHz Arduino, where the device triggers an interrupt each time it has data to be read (again each reading is 4 bytes, every 10 ms). Executing the ISR takes 128 microseconds. Which ONE of the following statements is true?

   a. The amount of data transferred per second increases if we increase the Arduino's clock rate to 20 MHz.
   b. Increasing the Arduino's clock rate to 20 MHz allows the ISR to retrieve the data from the device faster.
   c. Increasing the Arduino's clock rate to 20 MHz does not affect how fast the ISR retrieves the data from the device.
   d. Decreasing the Arduino's clock rate to 4 MHz reduces the amount of data transferred per second.
   e. None of the options a. to d. above are true.

Commented [SYJ17]: The device only triggers an interrupt when its data is ready to be read immediately, so the ISR can read it without any delay. ISRs are made up of machine instructions, and increasing the clock rate will make these instructions run faster, and hence, since the ISR can read the data without delay, the ISR is executed faster than on 16 MHz.

Note: The amount of data transferred per second is and will always be 400 bytes per second (100 pieces of data /sec x 4 bytes), but this is irrelevant here.

18. Suppose we increased the clock frequency of the Atmega328P in Question 5 to 20 MHz. What is the best prescalar value that we can use for Timer 0, given that we want to trigger the TIMER0_COMPA_vect interrupt once every millisecond, in CTC mode?

    a. 1
    b. 8
    c. 64
    d. 256
    e. 1024

    The table shows the resolution for each prescalar and the corresponding OCR0A value. None of the possible values are integers, but choosing the closest value minimizes deviation from our 1ms target since the interrupt triggering interval is given by OCR0A x resolution where resolution = 20000000 / P

Prescalar	Resolution	V Value	OCR0A	Actual Interval
1	0.05 us	20000	-	-
8	0.4 us	2500	-	-
64	3.2 us	312.5	-	-
256	12.8 us	78.125	77	998.4 us (1.6 us error)
1024	51.2 us	19.53	19	1024 us (24 us error)

**~~~ End of Questions ~~~**

Commented [SYJ18]: Ans.
The table shows the resolution for each prescalar and the corresponding OCR0A value. None of the possible values are integers, but choosing the closest value minimizes deviation from our 1ms target since the interrupt triggering interval is given by OCR0A x resolution where resolution = 20000000 / P

Prescalar

...

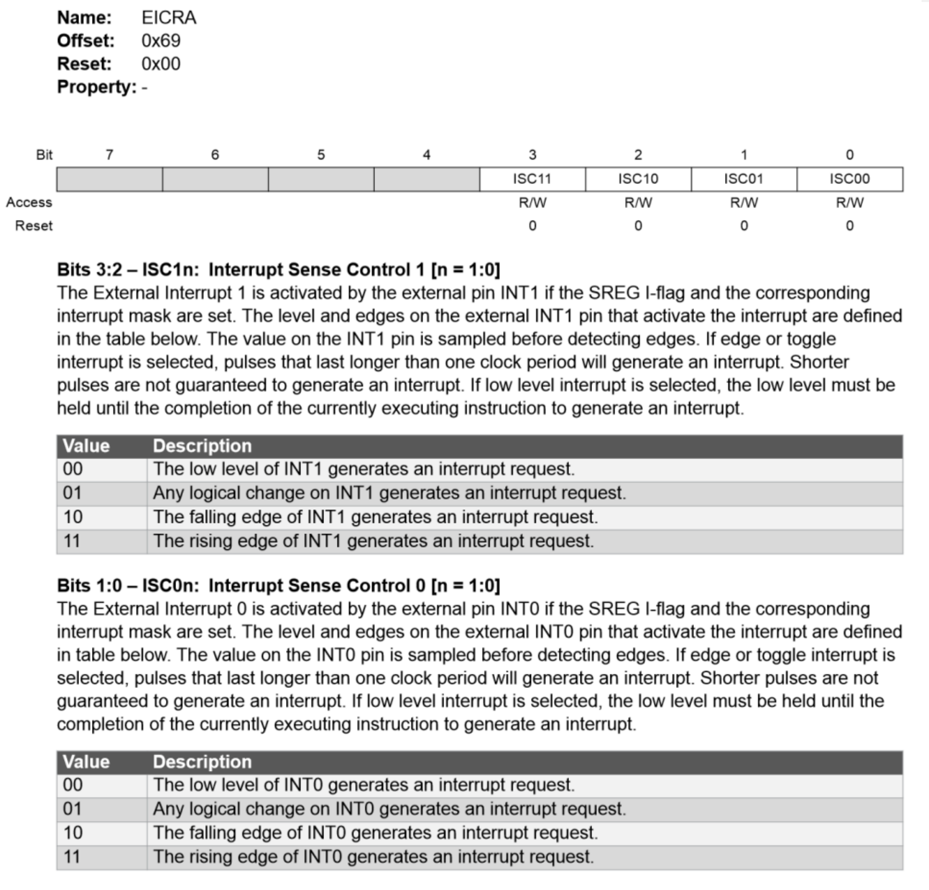
Commented [TKYC19R18]:

Commented [TKYC20R18]:

Commented [TKYC21R18]:

APPENDIX

EICRA and EIMSK layout



Name: EICRA
Offset: 0x69
Reset: 0x00
Property: -

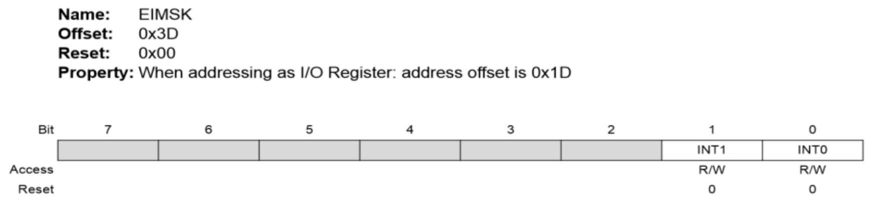
Bit	7	6	5	4	3	2	1	0
					ISC11	ISC10	ISC01	ISC00
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 3:2 – ISC1n: Interrupt Sense Control 1 [n = 1:0]
The External Interrupt 1 is activated by the external pin INT1 if the SREG I-flag and the corresponding interrupt mask are set. The level and edges on the external INT1 pin that activate the interrupt are defined in the table below. The value on the INT1 pin is sampled before detecting edges. If edge or toggle interrupt is selected, pulses that last longer than one clock period will generate an interrupt. Shorter pulses are not guaranteed to generate an interrupt. If low level interrupt is selected, the low level must be held until the completion of the currently executing instruction to generate an interrupt.

Value	Description
00	The low level of INT1 generates an interrupt request.
01	Any logical change on INT1 generates an interrupt request.
10	The falling edge of INT1 generates an interrupt request.
11	The rising edge of INT1 generates an interrupt request.

Bits 1:0 – ISC0n: Interrupt Sense Control 0 [n = 1:0]
The External Interrupt 0 is activated by the external pin INT0 if the SREG I-flag and the corresponding interrupt mask are set. The level and edges on the external INT0 pin that activate the interrupt are defined in table below. The value on the INT0 pin is sampled before detecting edges. If edge or toggle interrupt is selected, pulses that last longer than one clock period will generate an interrupt. Shorter pulses are not guaranteed to generate an interrupt. If low level interrupt is selected, the low level must be held until the completion of the currently executing instruction to generate an interrupt.

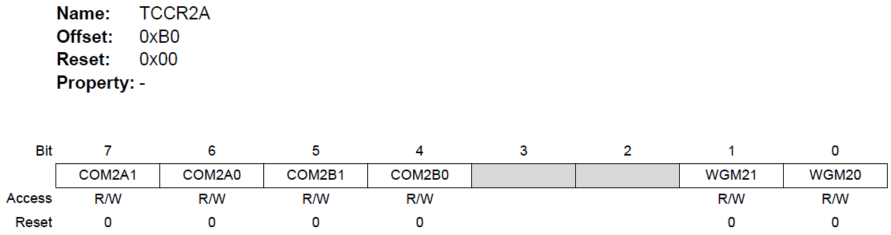
Value	Description
00	The low level of INT0 generates an interrupt request.
01	Any logical change on INT0 generates an interrupt request.
10	The falling edge of INT0 generates an interrupt request.
11	The rising edge of INT0 generates an interrupt request.



Name: EIMSK
Offset: 0x3D
Reset: 0x00
Property: When addressing as I/O Register: address offset is 0x1D

Bit	7	6	5	4	3	2	1	0
							INT1	INT0
Access							R/W	R/W
Reset							0	0

Configuration registers for Timer 2.



Name: TCCR2A
Offset: 0xB0
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	COM2A1	COM2A0	COM2B1	COM2B0			WGM21	WGM20
Access	R/W	R/W	R/W	R/W			R/W	R/W
Reset	0	0	0	0			0	0

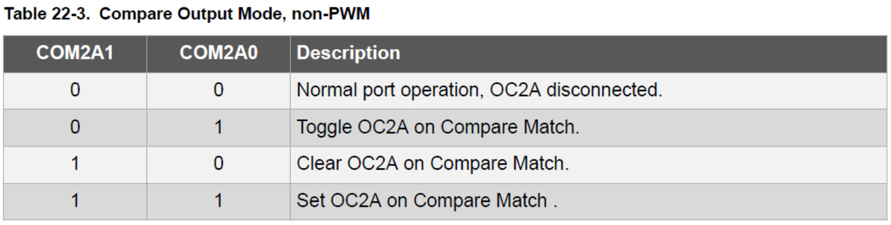


Table 22-3. Compare Output Mode, non-PWM

COM2A1	COM2A0	Description
0	0	Normal port operation, OC2A disconnected.
0	1	Toggle OC2A on Compare Match.
1	0	Clear OC2A on Compare Match.
1	1	Set OC2A on Compare Match .

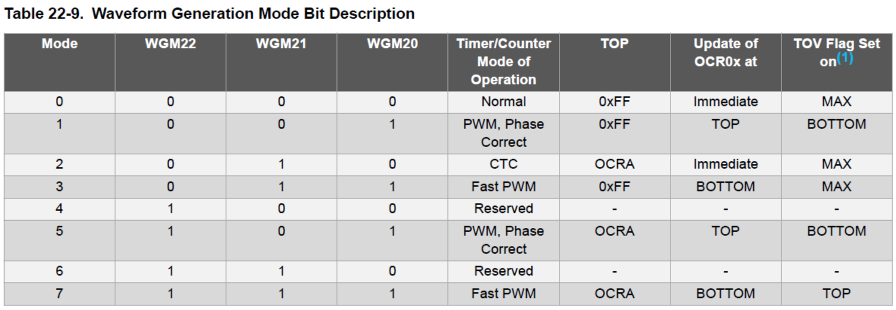
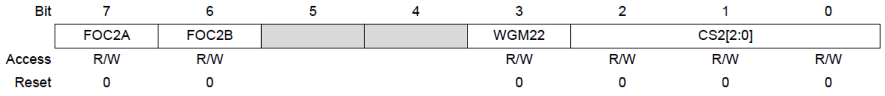
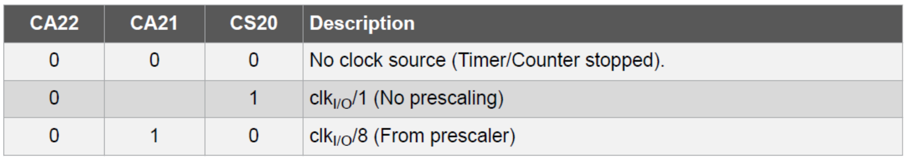


Table 22-9. Waveform Generation Mode Bit Description

Mode	WGM22	WGM21	WGM20	Timer/Counter Mode of Operation	TOP	Update of OCR0x at	TOV Flag Set on[1]
0	0	0	0	Normal	0xFF	Immediate	MAX
1	0	0	1	PWM, Phase Correct	0xFF	TOP	BOTTOM
2	0	1	0	CTC	OCRA	Immediate	MAX
3	0	1	1	Fast PWM	0xFF	BOTTOM	MAX
4	1	0	0	Reserved	-	-	-
5	1	0	1	PWM, Phase Correct	OCRA	TOP	BOTTOM
6	1	1	0	Reserved	-	-	-
7	1	1	1	Fast PWM	OCRA	BOTTOM	TOP



Bit	7	6	5	4	3	2	1	0
	FOC2A	FOC2B			WGM22	CS2[2:0]		
Access	R/W	R/W			R/W	R/W	R/W	R/W
Reset	0	0			0	0	0	0



CA22	CA21	CS20	Description
0	0	0	No clock source (Timer/Counter stopped).
0		1	$clk_{I/O}/1$ (No prescaling)
0	1	0	$clk_{I/O}/8$ (From prescaler)