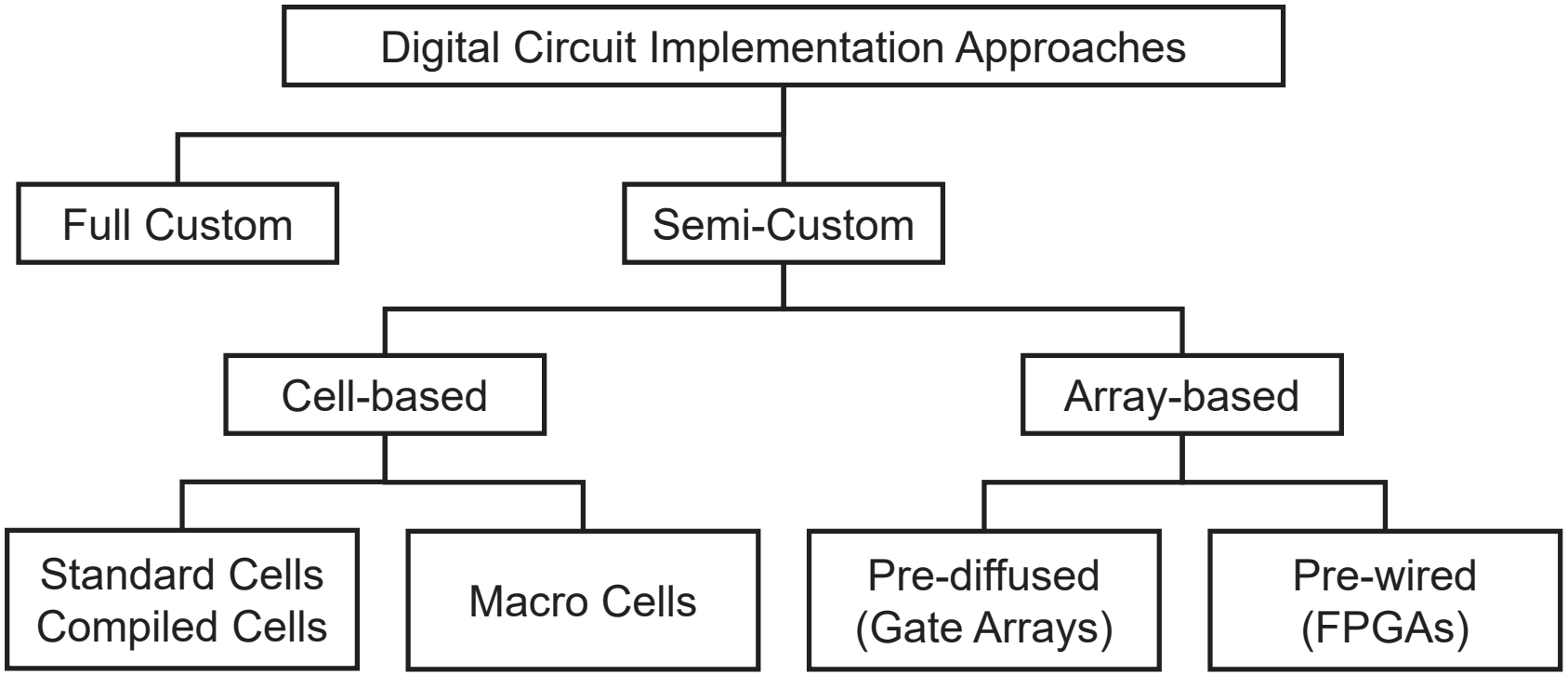
Week 2-1

The Standard Cell Methodology

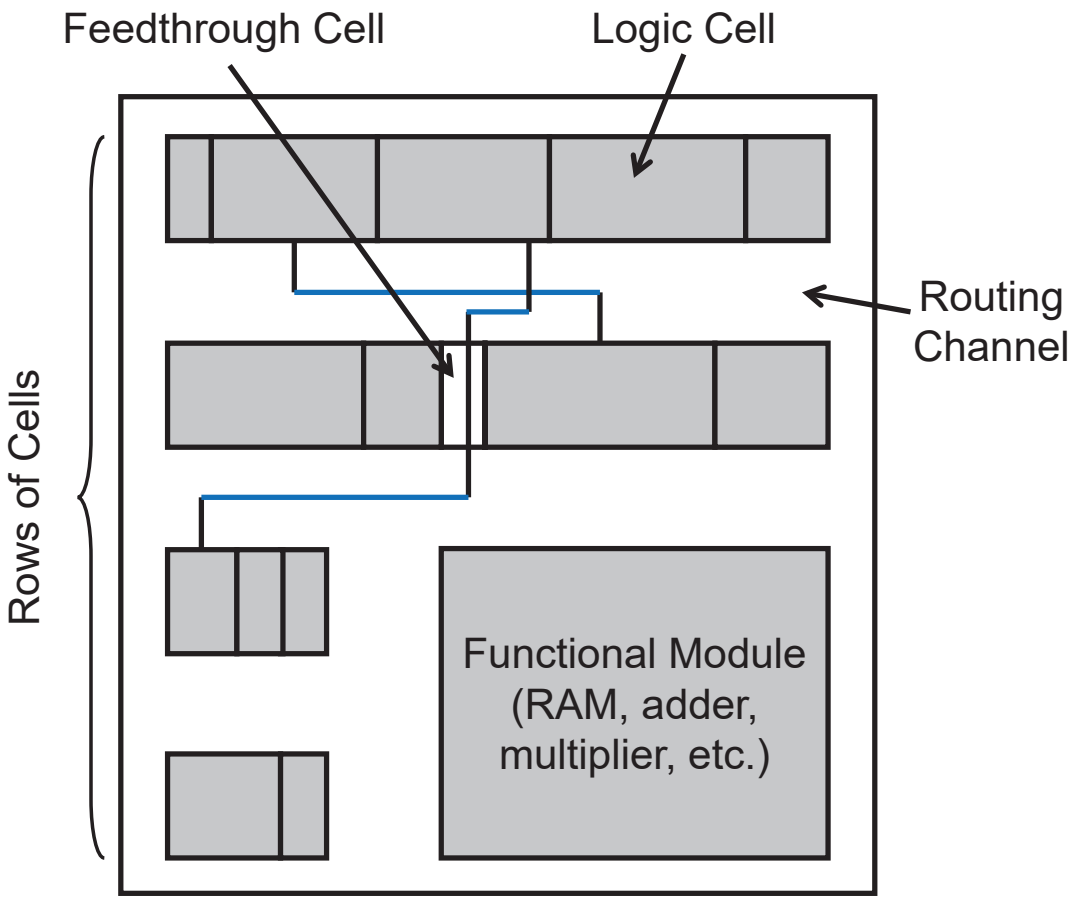
Implementation Choices



Approach taken depends on desired tradeoffs between time-to-market, cost, design complexity, aggressiveness of design specifications

Design for fast time-to-market: design automation techniques
Design for high performance/high density: handcrafted full custom design

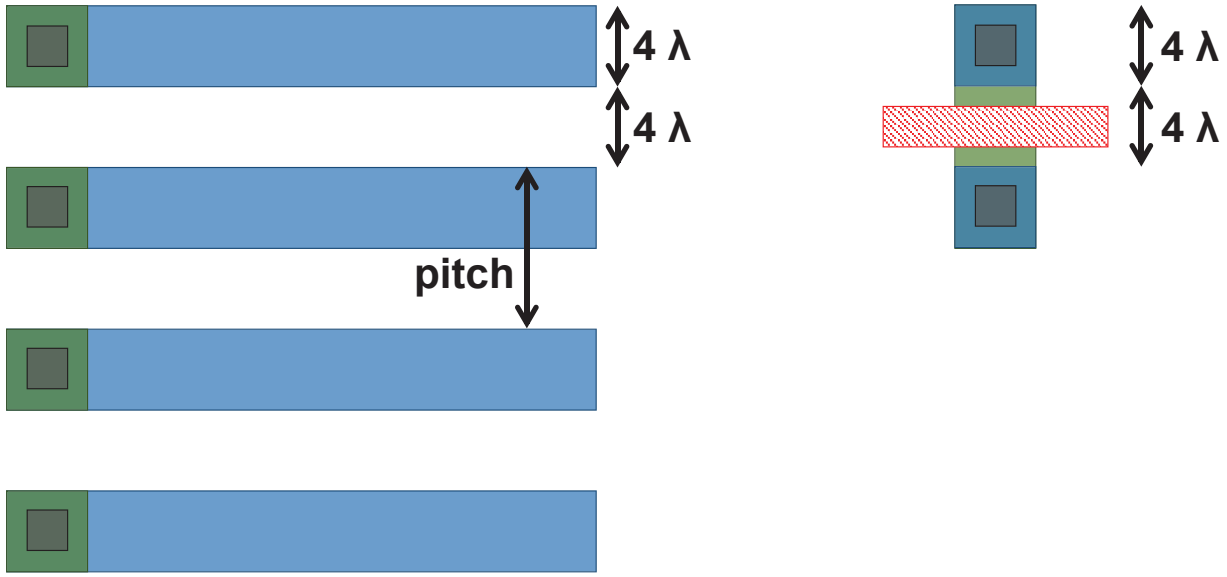
The Cell-based Approach (Standard Cell)



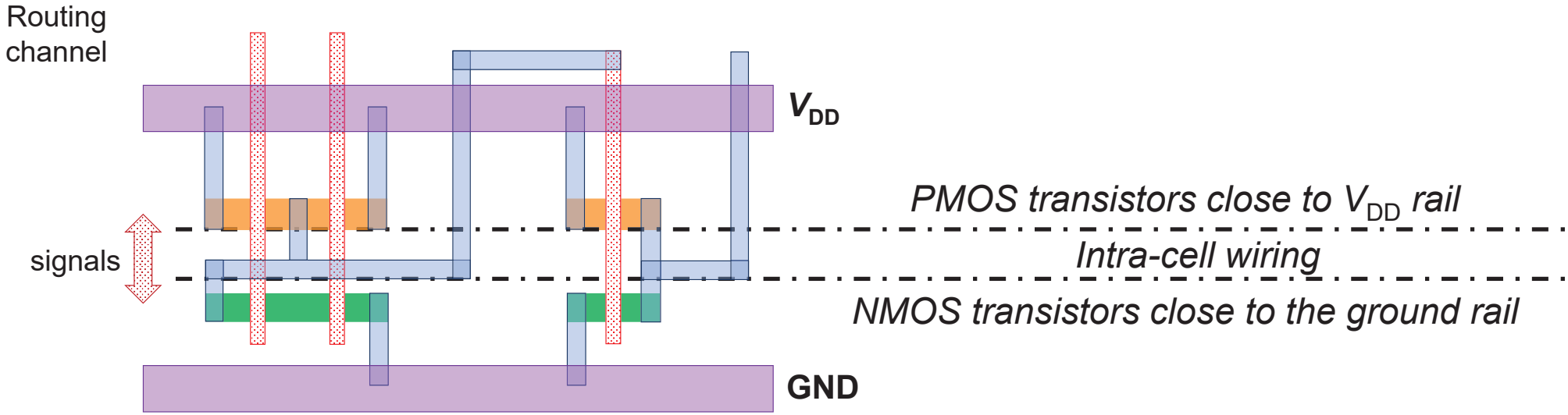
- **Routing channel requirements are reduced by presence of more interconnect (metal) layers**
- **Except for the first one or two metal layers, wires in each layer run in one direction (allow for denser packing)**
  - **Wires in consecutive layers run orthogonal to each other, and are shorted using vias**
- **Library of cells designed for:**
  - **Different Boolean functions**
  - **Different drive strengths**
- **Width and height of all cells are defined by rules**
  - **Height defined by number of M1 signal wires (tracks) that can run horizontally**
  - **Width is multiple of a common factor**
  - **Wire endpoints defined on same grid coordinates (enables automated routing)**
  - **Allow placement to be defined by grid coordinates, (*x*, *y*), thus enabling automated placement**

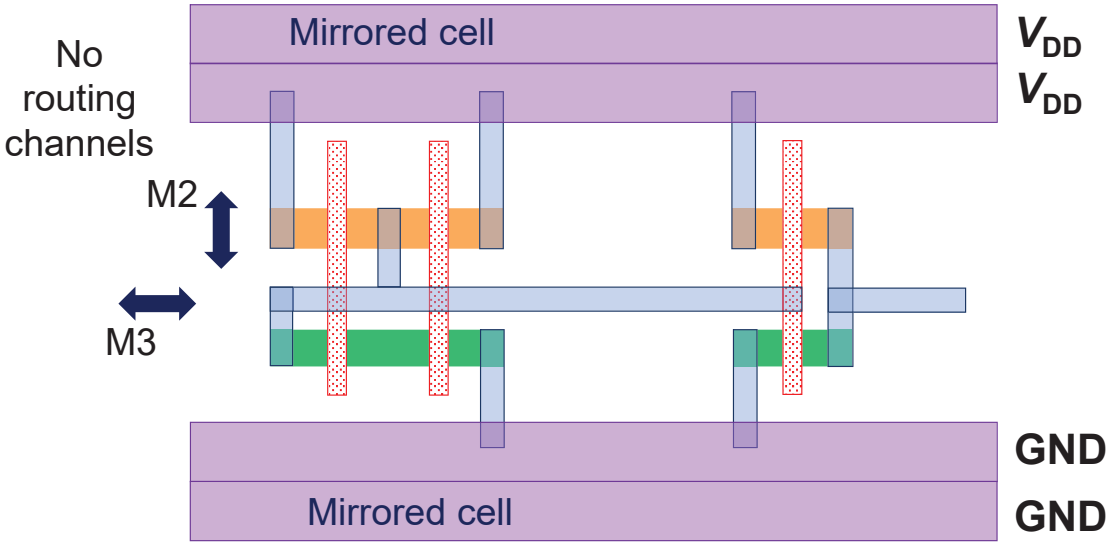
Design Rules – Wire Tracks

- **The feature size, *f*, is the minimum spacing between the drain and source (min. dimension of gate structure between drain and source)**
- **Scalable design rules are expressed in terms of λ = *f*/2**
- **A *wiring track* is the space required for a wire**
  - **e.g., 4 λ width, 4 λ spacing from neighbor = 8 λ pitch**
- **This rule applies to transistors as well**



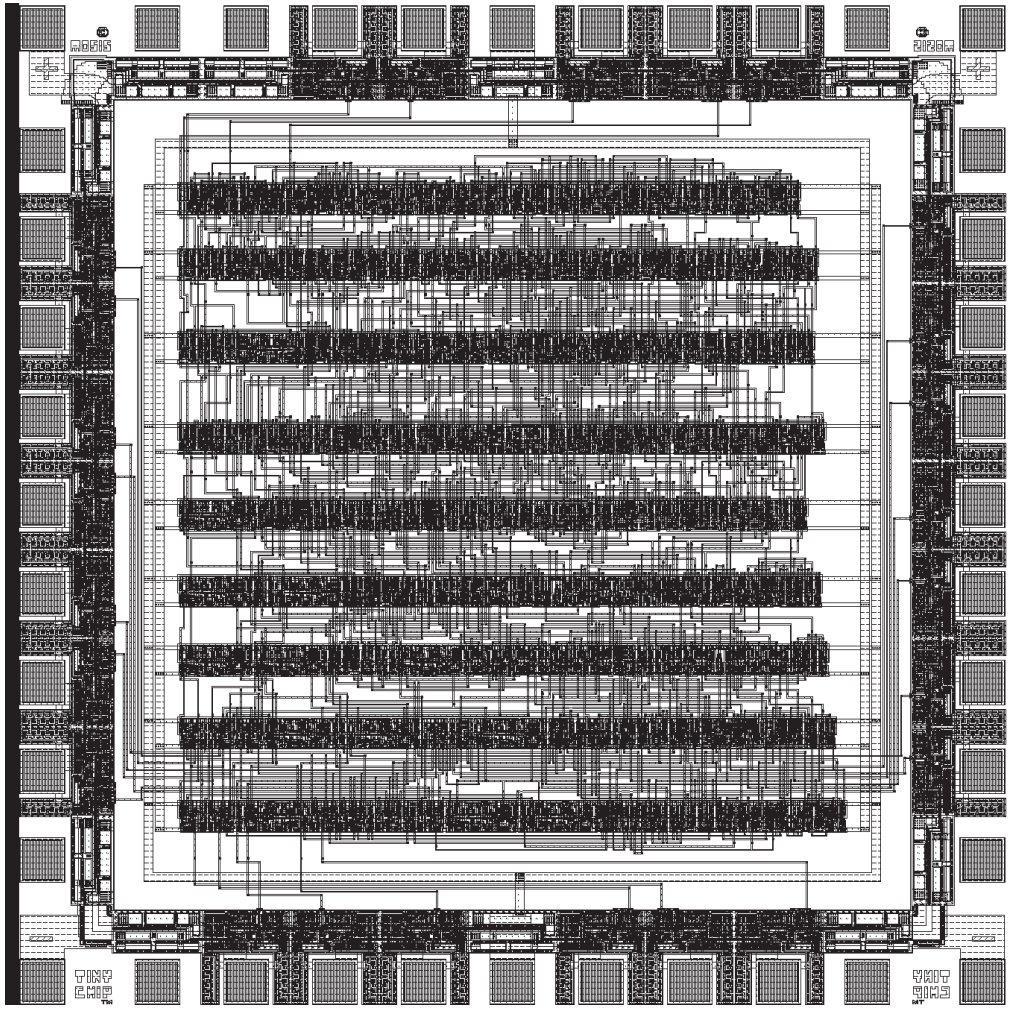
Structure of a Row of Standard Cells





Cell mirroring enables sharing of power and ground rails

Standard Cell – Early Example



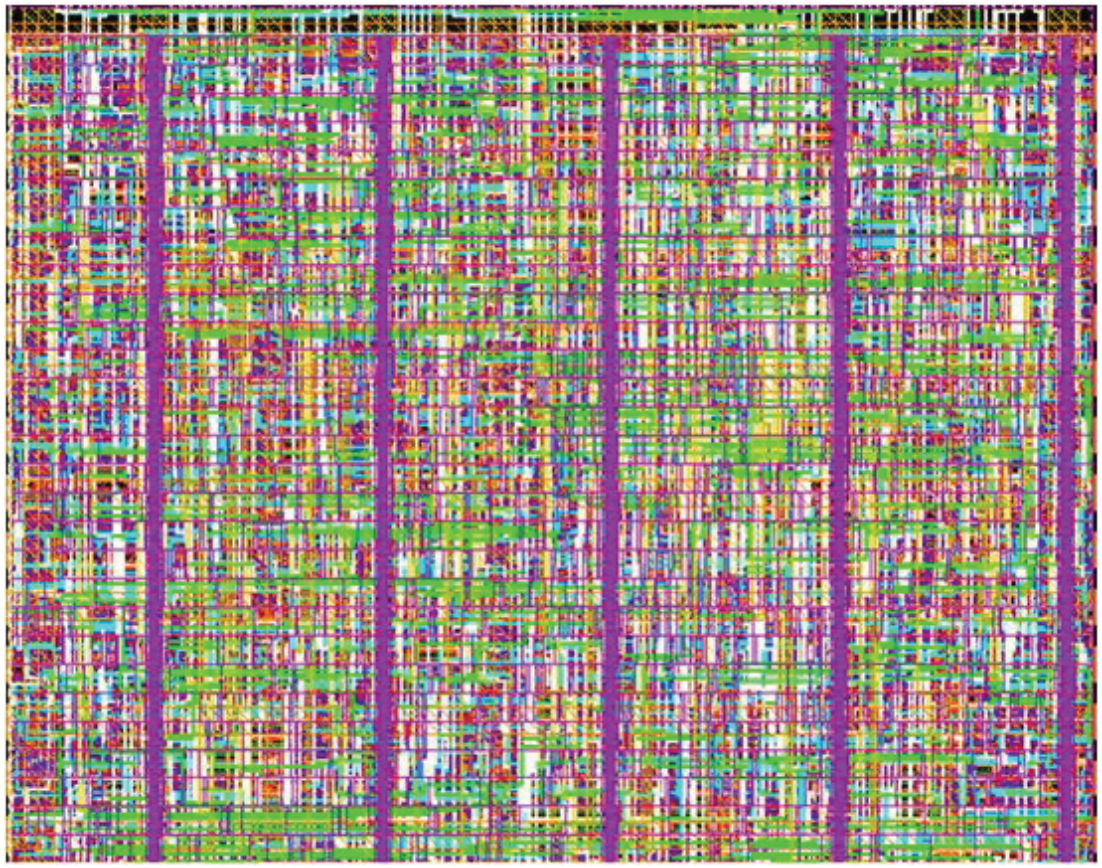
- **Large area overhead for the interconnects**
  - **Feedthrough cells**
  - **Large routing channels**

- **Adding more metal layers**
  - **Less requirements on routing channels**

[Brodersen92]

Standard Cell – The New Generation

Design in a 7 metal layers technology



- **Cell structure hidden under interconnect layers**
  - **Density: 90%**
  - **Small area overhead for interconnects**

Standard Cells

Designing a standard cell library is time consuming, although amortized among a large number of designs

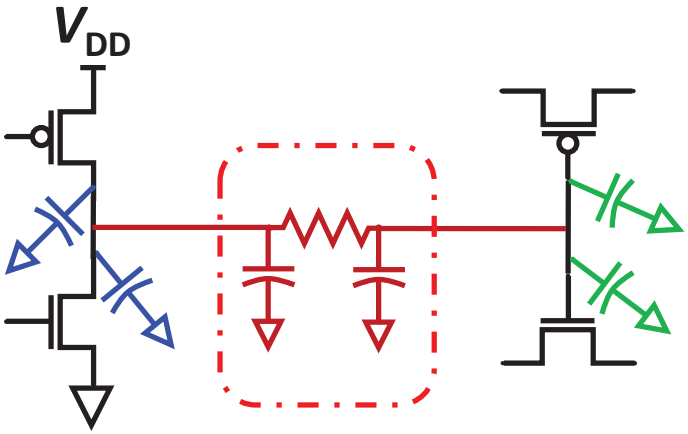
- **Today it is common practice to have several cell versions**
  - **Number of inputs**
  - **Transistor sizing for different capacitative loads (*driving strength*)**
  - **Pull-up/pull-down ratios**
  - **Technology: V_{TH}, V_{DD}, technology corner cases**
- **Non-trivial choice of the mix of logic cells**
  - **Small library with most cells having limited fan-ins?**
  - **Large library with many versions of the same cell?**
  - **Conservative large driving capabilities lead to power/area overhead**
- **Technology libraries are broadly differentiated based on the target design goal (low-power vs high-performance)**

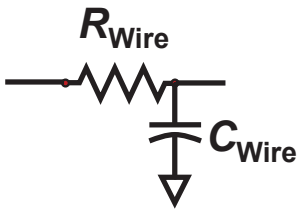
Synthesis tools choose the correct cell version in the library based on the speed/area/power constraints

Week 2-2

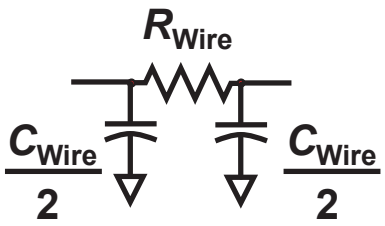
Interconnects

Load Estimation

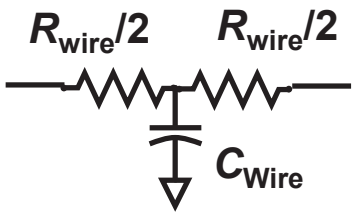




L-model
(lumped model)



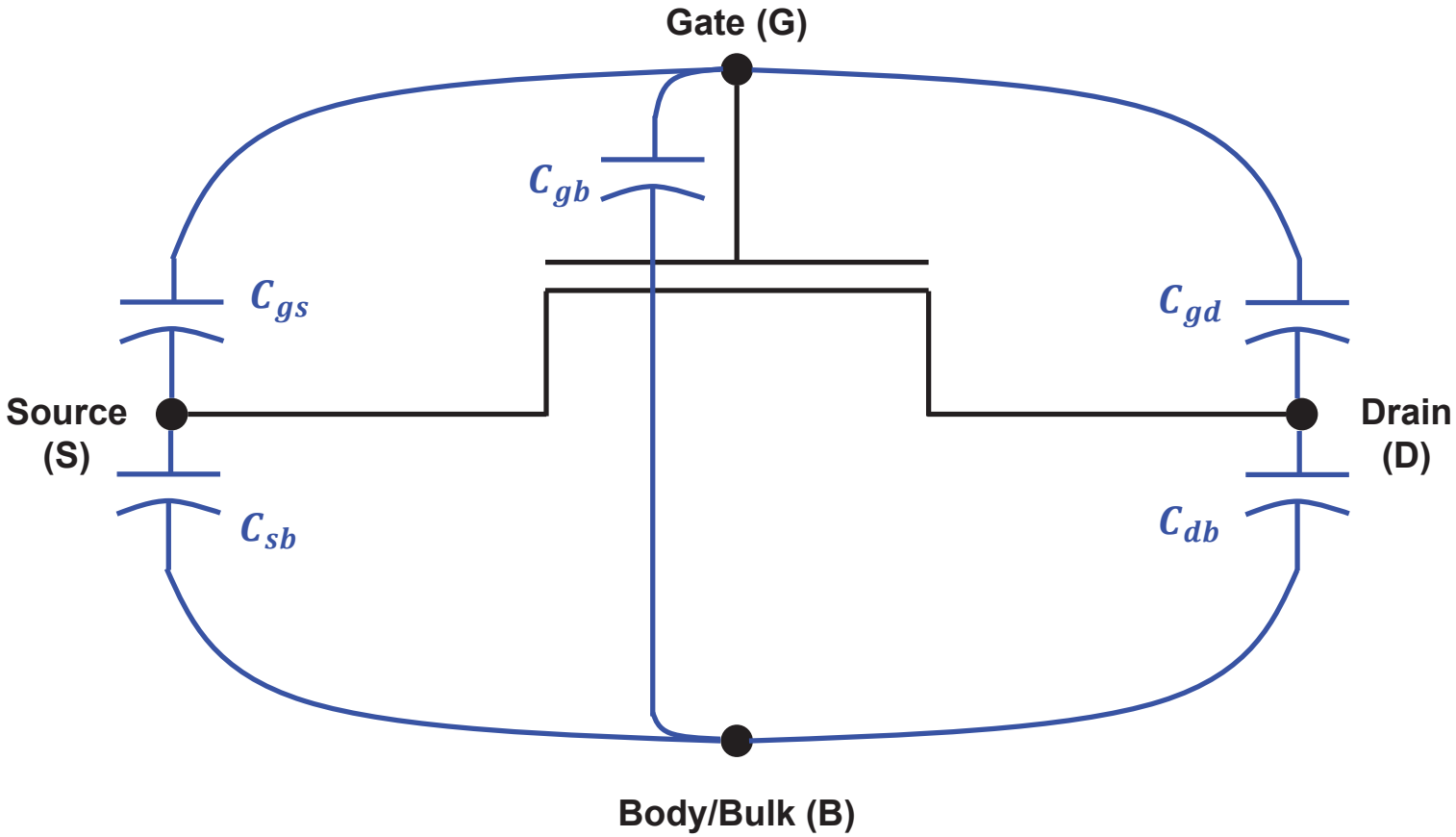
π-model



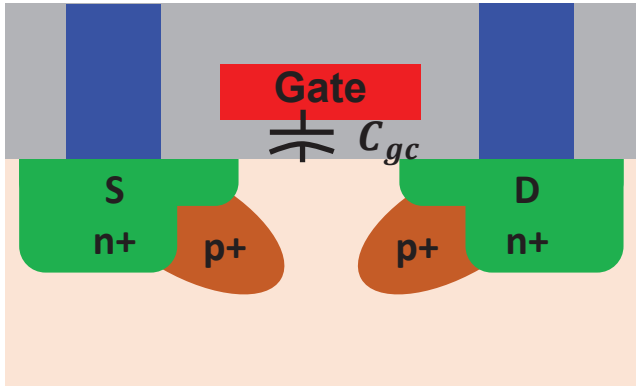
T-model

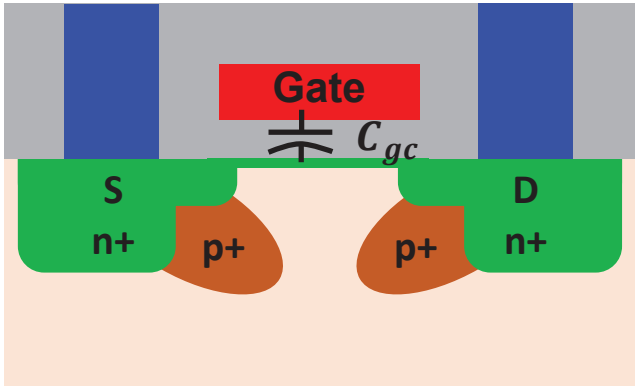
- Parasitics model the effect of the physical implementation of the circuit on the electrical behavior of the circuit. There are contributions from:
  1. Gate capacitance of MOSFETs
  2. Junction capacitances of MOSFETs
  3. Capacitance and resistance of the interconnect (metal wires for signal routing)

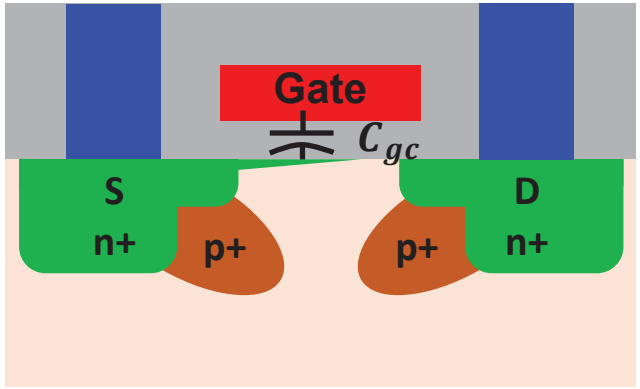
Capacitor Model for the MOSFET



Intrinsic Gate Capacitances

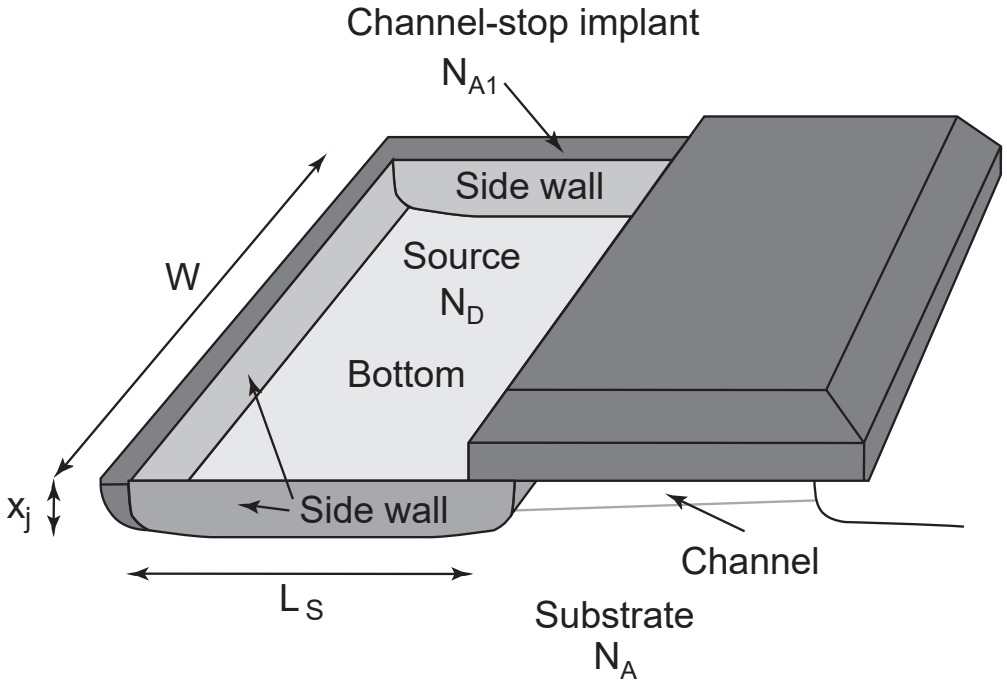






Operating Region	C_{gb}	C_{gs}	C_{gd}
Cutoff	$C_{OX}WL_{EFF}$	0	0
Linear/Triode	0	$\frac{C_{OX}WL_{EFF}}{2}$	$\frac{C_{OX}WL_{EFF}}{2}$
Saturation	0	$\frac{2}{3}C_{OX}WL_{EFF}$	0

Junction Capacitances



C_{ja0}: zero voltage junction cap. per unit area
C_{jp0}: zero voltage junction cap. per unit peri.

V_j: voltage across the junction (+ve: forward-bias, -ve: reverse-bias)

ϕ: built-in potential of junction (0.6 ~ 0.9 V)

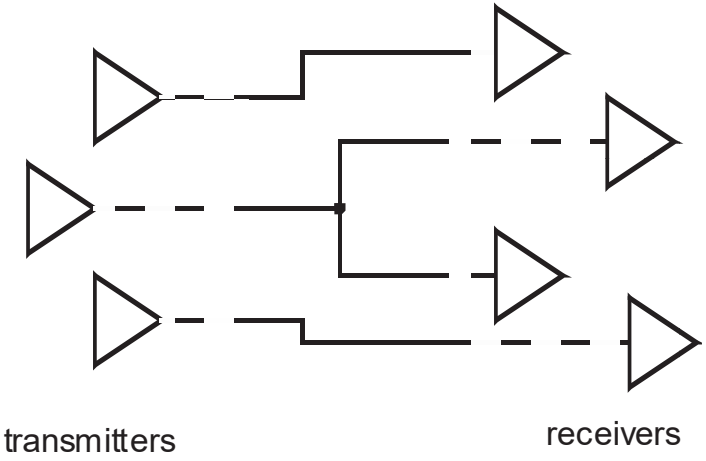
ma, mp: grading coefficients (0.3 ~ 0.5)

$$C_{diff} = C_{bottom} + C_{sw} = C_j \times AREA + C_{jsw} \times PERIMETER$$
$$= C_j L_S W + C_{jsw}(2L_S + W)$$

$$C_j = C_{ja0}\left(1 - \frac{V_j}{\phi}\right)^{-ma} \qquad C_{jsw} = C_{jp0}\left(1 - \frac{V_j}{\phi}\right)^{-mp}$$

Parameter	n-diffusion	p-diffusion
C_{ja0}	0.1 fF / μm^2	0.1 fF / μm^2
C_{jp0}	0.9 fF / μm	0.8 fF / μm

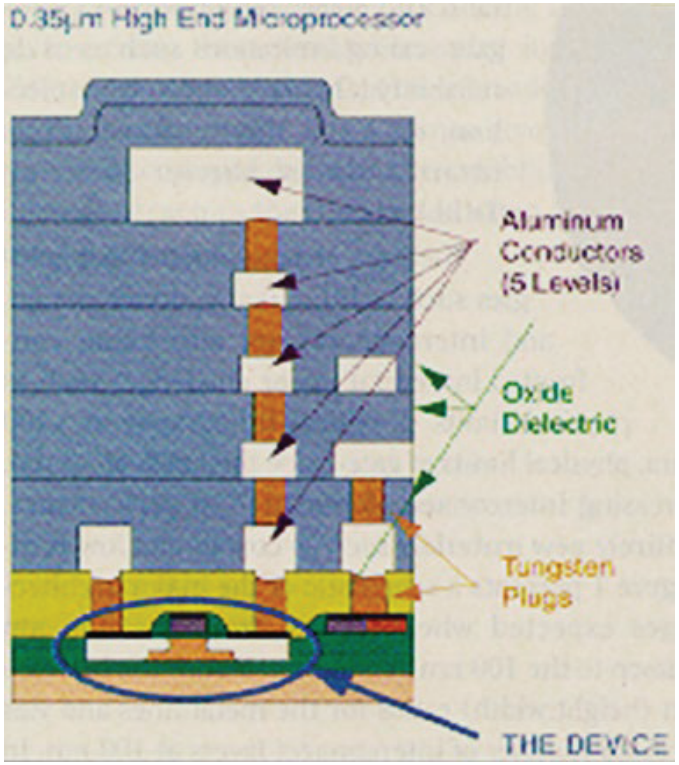
Interconnects (Signal Routing Wires)



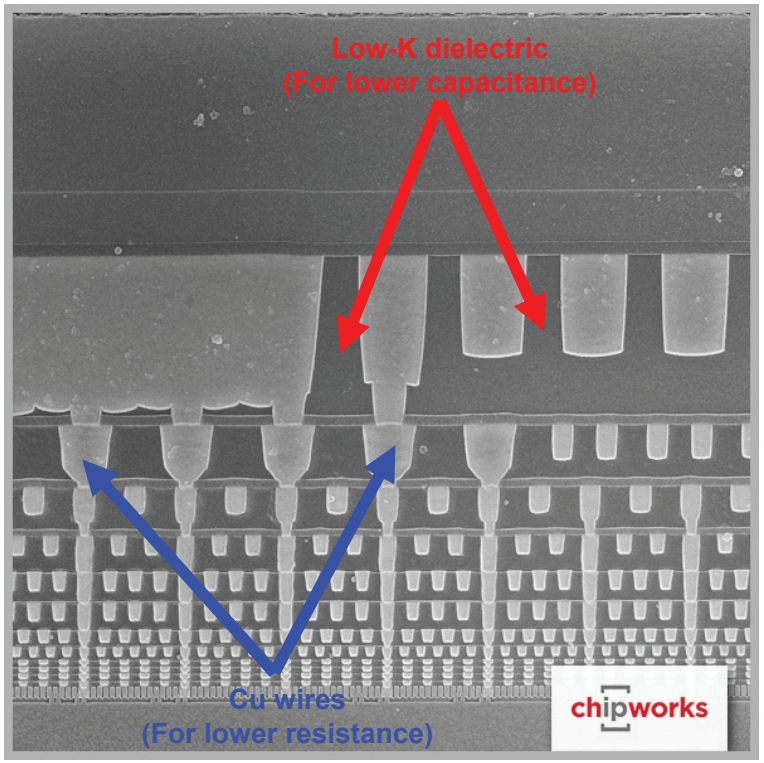
Schematics

Physical

Interconnects in Real Chips



0.35um 5M layers



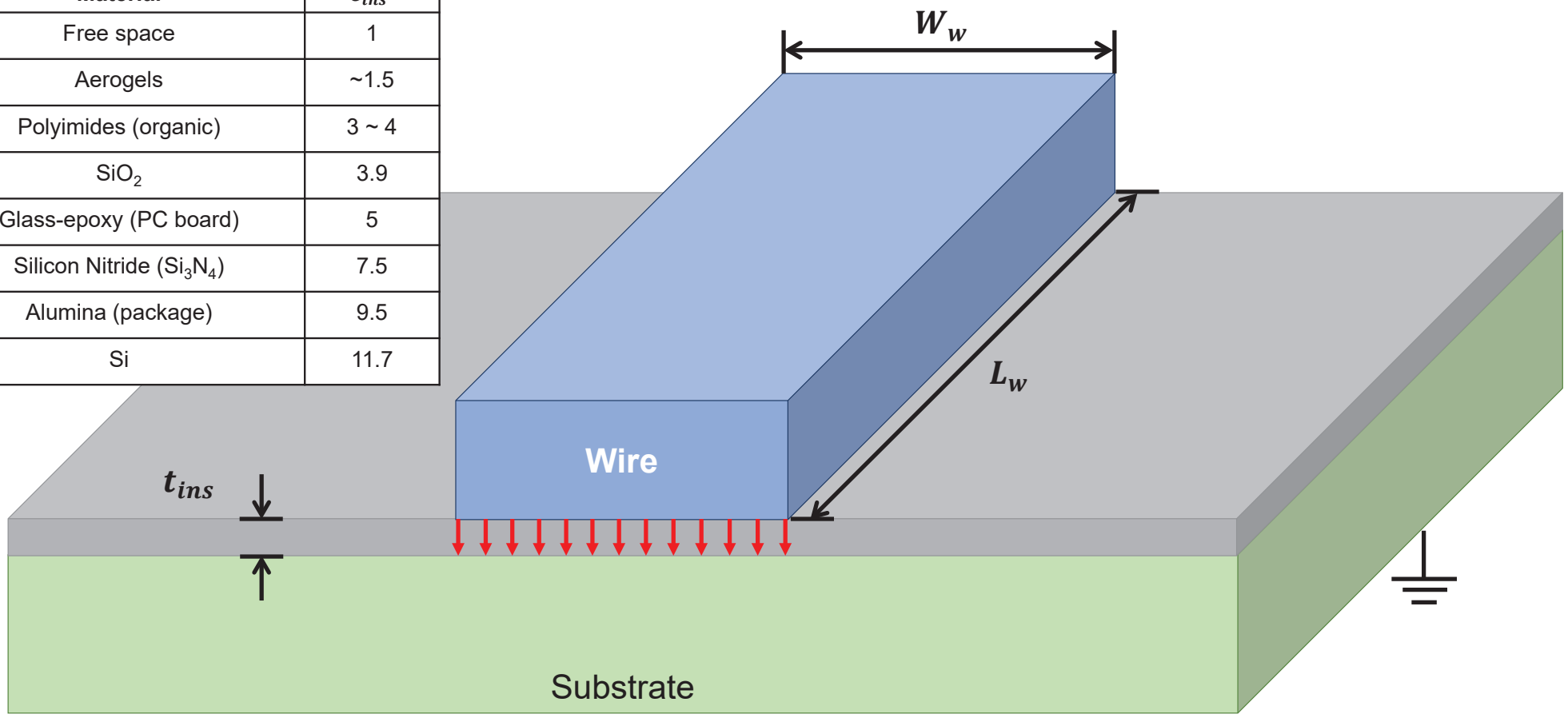
14 nm (Intel's Broadwell / i7 6800k)

e.g. GlobalFoundries and TSMC's 28nm ➔ 10 layers of Metal

Interconnect Capacitance - I

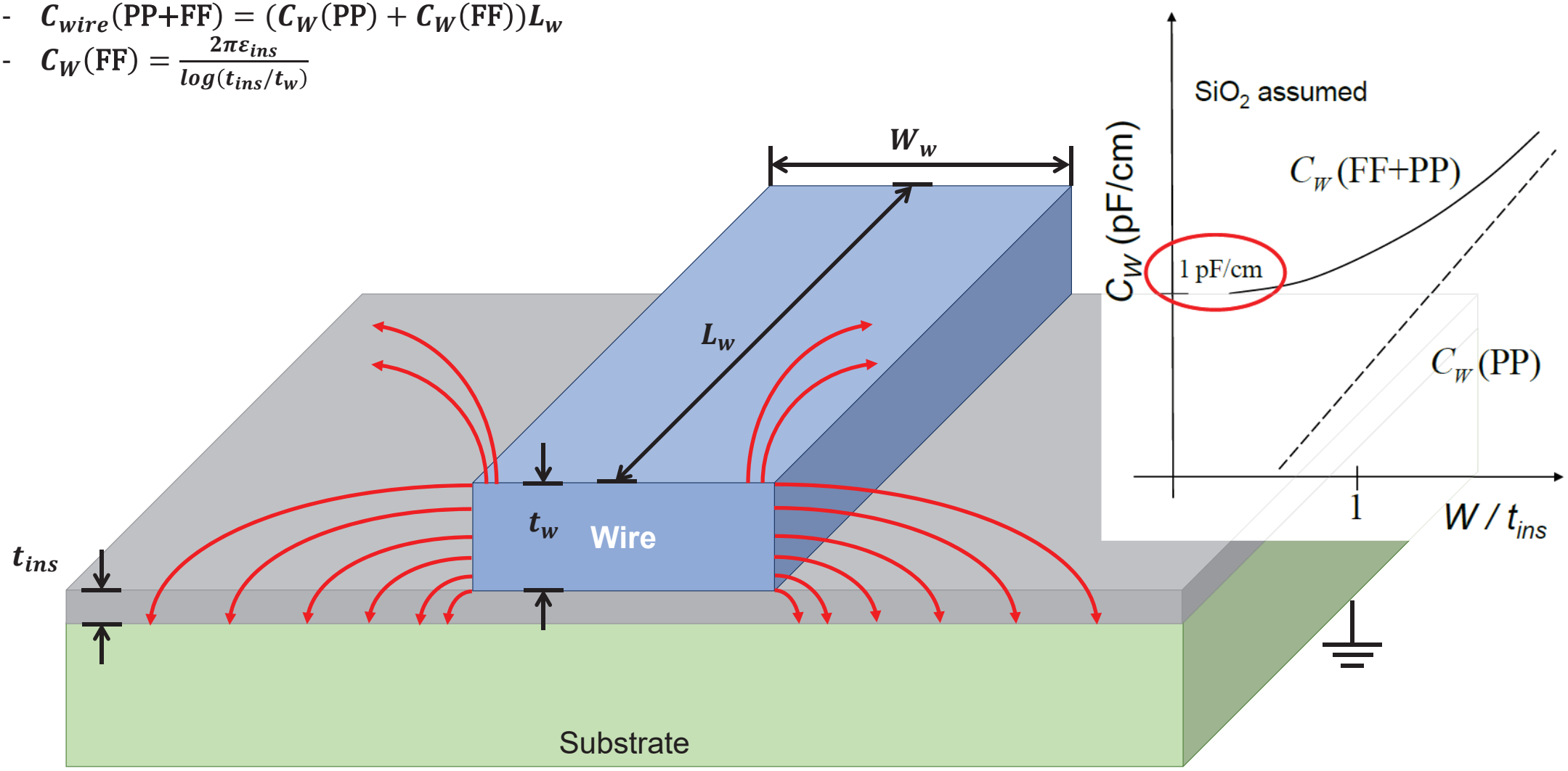
- $C_{wire}(\text{PP}) = C_{ins} W_w L_w$ $\quad C_{ins} = \varepsilon_{ins}/t_{ins}$
- $C_{wire}(\text{PP}) = (C_{ins} W_w) L_w = C_W(\text{PP}) L_w$

Material	ε_{ins}
Free space	1
Aerogels	~1.5
Polyimides (organic)	3 ~ 4
SiO_2	3.9
Glass-epoxy (PC board)	5
Silicon Nitride (Si_3N_4)	7.5
Alumina (package)	9.5
Si	11.7

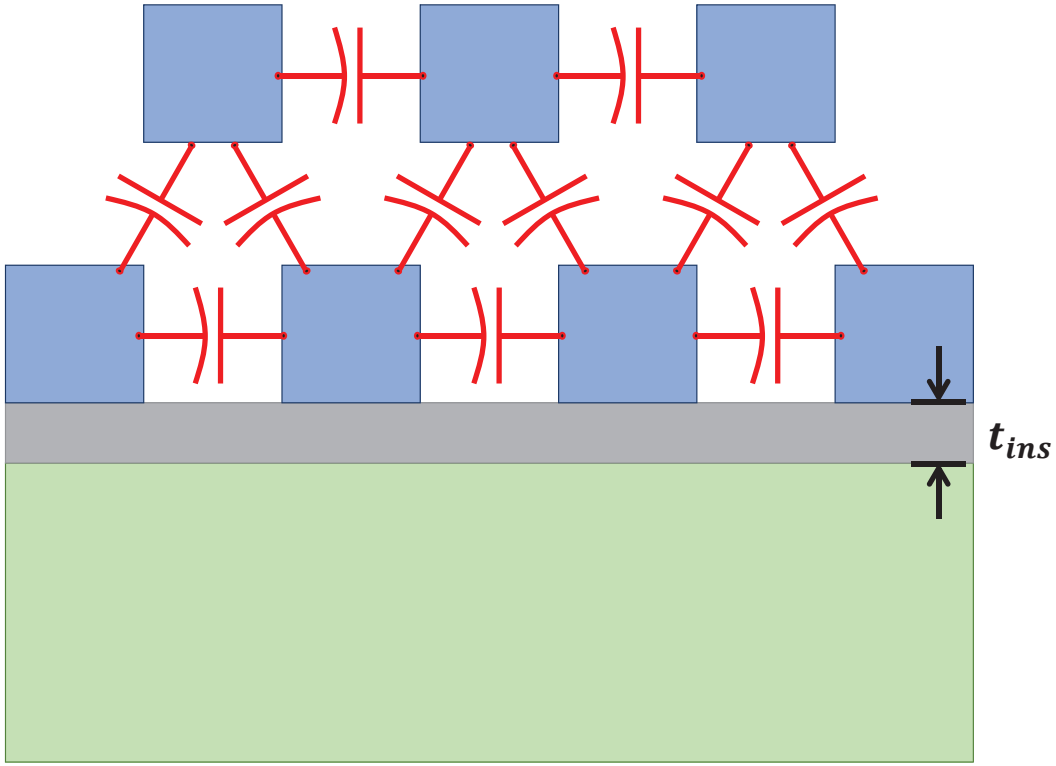


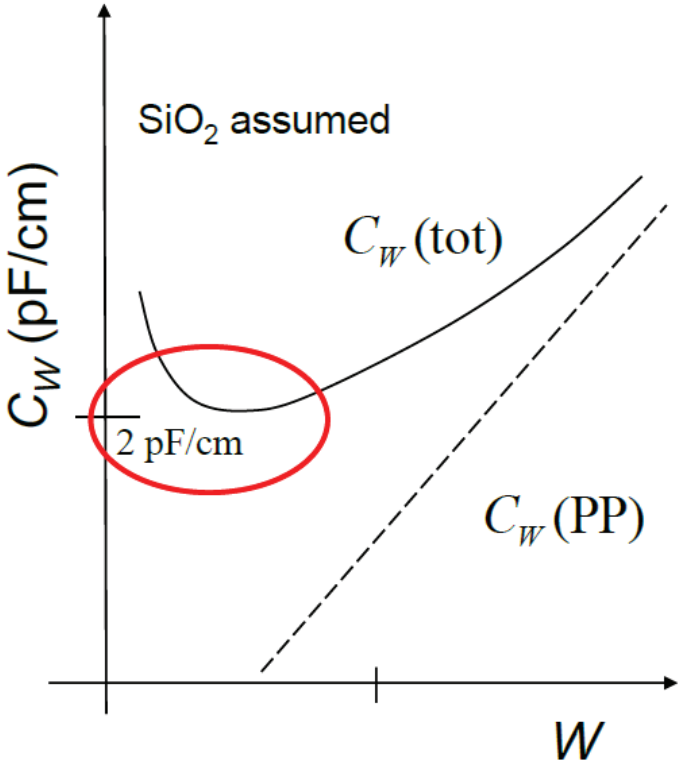
Interconnect Capacitance - III

- $C_{wire}(\text{PP+FF}) = (C_W(\text{PP}) + C_W(\text{FF}))L_w$
- $C_W(\text{FF}) = \frac{2\pi\varepsilon_{ins}}{log(t_{ins}/t_w)}$



Wire-wire Capacitance





see Fig. 5.22, Taur and Ning, *Fundamentals of VLSI Devices*

$$C_{wire} = (C_W(\mathrm{PP}) + C_W(\mathrm{FF}) + C_W(\mathrm{WW}))L_w$$

Also see A. Bansal, B. C. Paul, and K. Roy, IEEE Trans. CAD vol. 25, no. 12, pp. 2765, 2006

Wiring Capacitances

CAPACITANCE PARAMETERS	N+	P+	POLY	M1	M2	M3	M4	M5	M6	D_N_W	N_W	UNITS
Area (substrate)	963	1159	110	38	19	13	8	8	3		125	aF/um^2
Area (N+active)			8556	51	21	14	11	9	8			aF/um^2
Area (P+active)			8309									aF/um^2
Area (poly)				58	17	10	7	5	4			aF/um^2
Area (metal1)					41	15	10	7	5			aF/um^2
Area (metal2)						36	14	9	7			aF/um^2
Area (metal3)							39	15	9			aF/um^2
Area (metal4)								36	14			aF/um^2
Area (metal5)									37			aF/um^2
Area (r well)	987											aF/um^2
Area (no well)	143											aF/um^2
Fringe (substrate)	248	203		13	61	55	43	24				aF/um
Fringe (poly)				64	38	29	24	20	17			aF/um
Fringe (metal1)					61	34		23	19			aF/um
Fringe (metal2)						53	36	26	22			aF/um
Fringe (metal3)							54	34	28			aF/um
Fringe (metal4)								57	35			aF/um
Fringe (metal5)									53			aF/um
Overlap (P+active)			636									aF/um

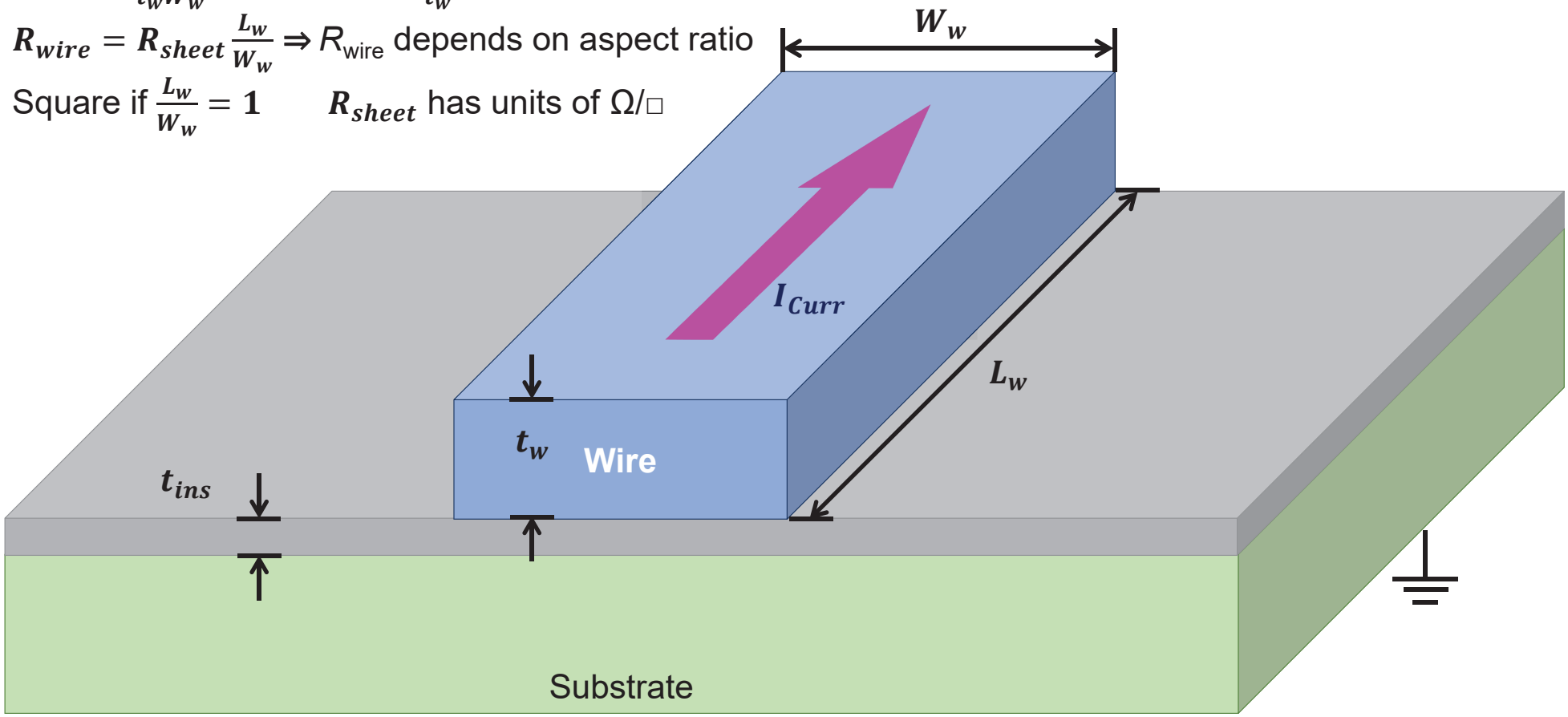
Interconnect Resistances

IR drop in wires due to interconnect resistances can severely impact signal integrity on wires with large current flow (e.g., power supply rails, clock, global and semi-global signaling lines)

$\boldsymbol{R_{wire}} = \frac{\rho L_w}{t_w W_w}$ $\boldsymbol{R_{sheet}} = \frac{\rho}{t_w}$

$\boldsymbol{R_{wire}} = \boldsymbol{R_{sheet}} \frac{L_w}{W_w} \Rightarrow R_{\text{wire}}$ depends on aspect ratio

Square if $\frac{L_w}{W_w} = \mathbf{1}$ $\boldsymbol{R_{sheet}}$ has units of Ω/□



Interconnect Materials

Material	ρ (Ω-m)
Silver (Ag)	1.6×10^{-8}
Copper (Cu)	1.7×10^{-8}
Gold (Au)	2.2×10^{-8}
Aluminum (Al)	2.7×10^{-8}
Tungsten (W)	5.5×10^{-8}

Material	Sheet Resistance (Ω/❑)
n- or p-well diffusion	1000 – 1500
n^+, p^+ diffusion	50 – 150
n^+, p^+ diffusion with silicide	3 – 5
n^+, p^+ polysilicon	150 – 200
n^+, p^+ polysilicon with silicide	4 – 5
Aluminum	0.05 – 0.1

PROCESS PARAMETERS	N+	P+	POLY	N+BLK	PLY+BLK	M1	M2	UNITS
Sheet Resistance	6.6	7.6	7.7	60.1	312.5	0.08	0.08	ohms/sq
Contact Resistance	10.4	10.9	9.7				4.36	ohms
Gate Oxide Thickness	40							angstrom

PROCESS PARAMETERS	M3	POLY_HRI	M4	M5	M6	N_W	UNITS
Sheet Resistance	0.08	1304.6	0.07	0.07	0.04	913	ohms/sq
Contact Resistance	9.08		13.85	19.37	22.28		ohms

∘

Tackling Interconnect Resistances

- Process Technology Solutions
  - Selective technology scaling
  - Use better interconnect materials
    - e.g. transition from aluminum to copper (introduced by IBM ~1997)
    - Future (cobalt, carbon nanotubes, ???)
  - More interconnect layers
    - Reduce average wire-length
  - New schemes
    - Optical

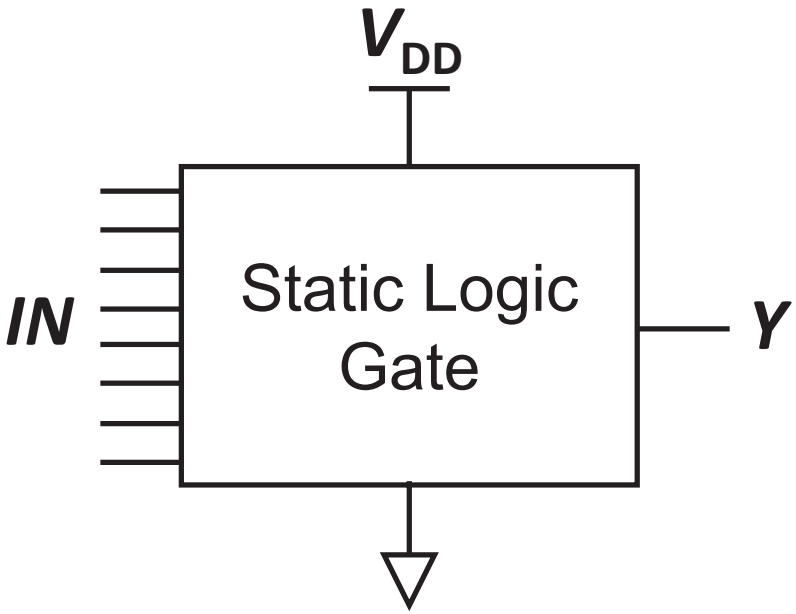
- Design Solutions (e.g. power ring design)
  - Optimize metal width
  - Choosing metal layer

Read more
https://semiengineering.com/all-about-interconnects/
https://semiengineering.com/dealing-with-resistance-in-chips/

Week 2-3

Introduction to Static CMOS Logic

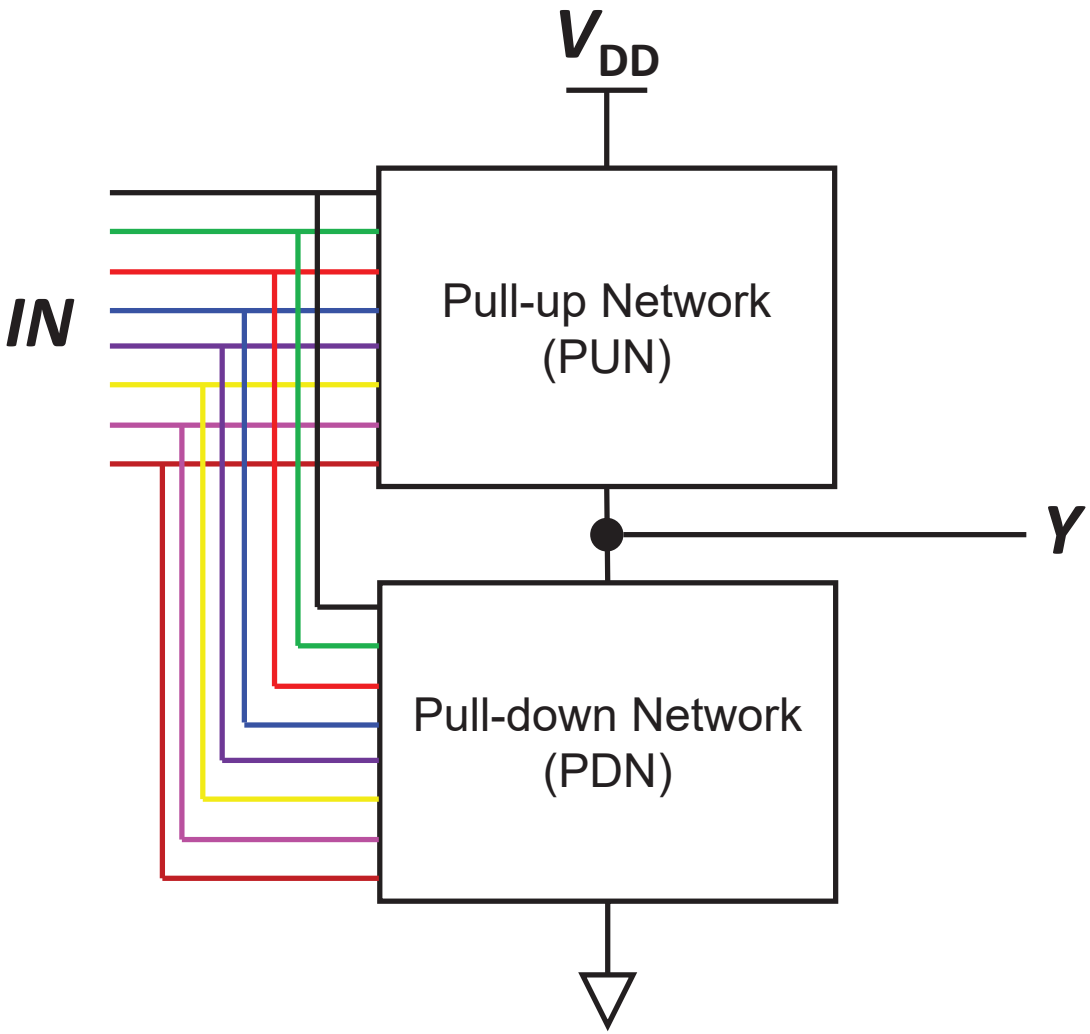
Static Complementary MOS (CMOS) Logic



Key Characteristics

- Inputs and output are analog voltages
  - Voltage level correspond to digital values
- Transfer characteristic (relationship between inputs and output)
  - Described by truth table or Boolean function
- Output responds “immediately” to changes to input signals (with some propagation delay)
- Power must be supplied to the logic gate (*i.e.*, V_{DD} is sufficiently high) for transfer characteristic to hold true
- Output is connected to either ***GND*** or V_{DD}

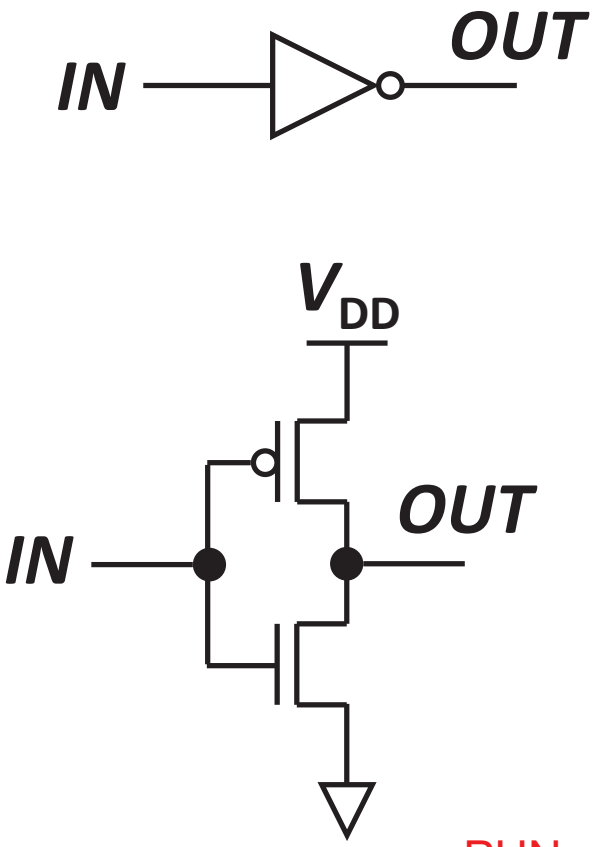
Static Complementary MOS (CMOS) Logic

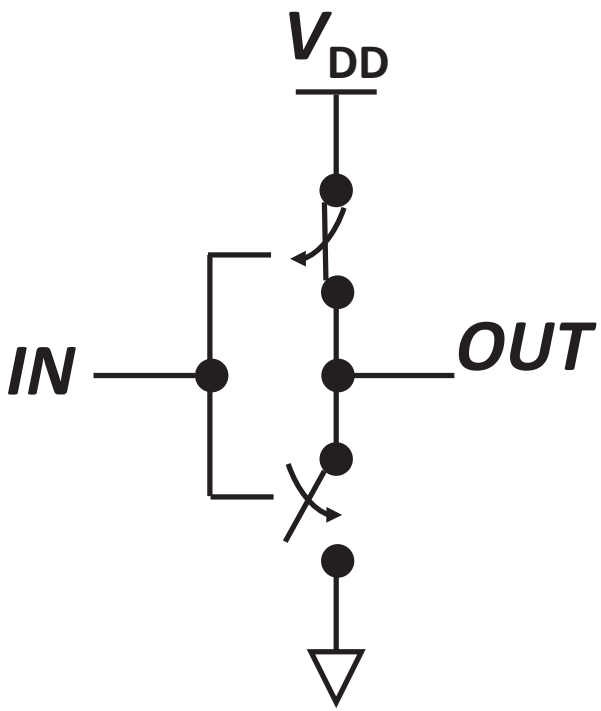


Static CMOS Logic

- Static CMOS logic gates formed using both NMOS and PMOS transistors
  - Pull-down network:
    - Consists of NMOS transistors only
    - Determines which input pattern gives *Y* = '0' (***GND***)
  - Pull-up network:
    - Consists of PMOS transistors only
    - Determines which input pattern gives Y = '1' ($\boldsymbol{V_{DD}}$)
- Every input signal is given to the gates of at least one pair of transistors
  - One PMOS and one NMOS transistor
- Fan-in: number of inputs the logic gate has
- Fan-out: number of inputs receiving the output of the logic gate

Example: The Static CMOS Inverter





Basic Idea

- NMOS and PMOS behave as complementary switches:
  - NMOS: “normally-off”
  - PMOS: “normally-on”
  - “normally”: when gate is 0
- ***IN*** = ‘0’ (***GND***):
  - NMOS: off
  - PMOS: on
  - Output: V_{DD}
- ***IN*** = ‘1’ (V_{DD}):
  - NMOS: on
  - PMOS: off
  - Output: ***GND***

Other Characteristics of Static CMOS Logic

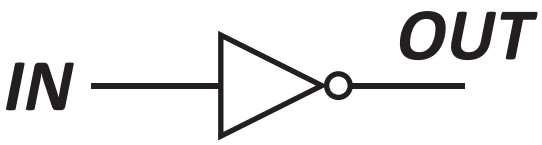
PUN and PDN never connect output to ***GND*** and V_{DD} at the same time

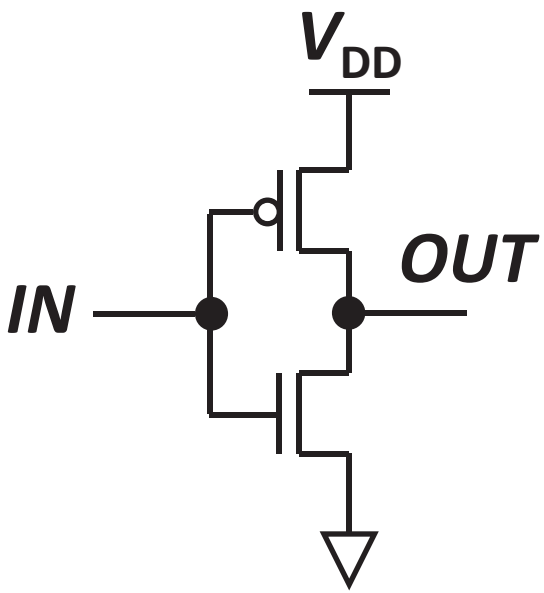
Very high input impedance; Very low output impedance

Week 2-4

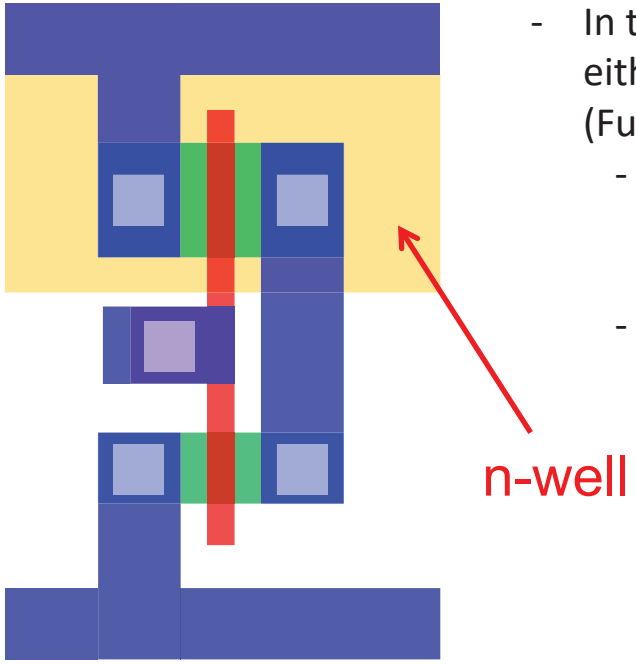
Introduction to the Static CMOS Inverter

The Static CMOS Inverter



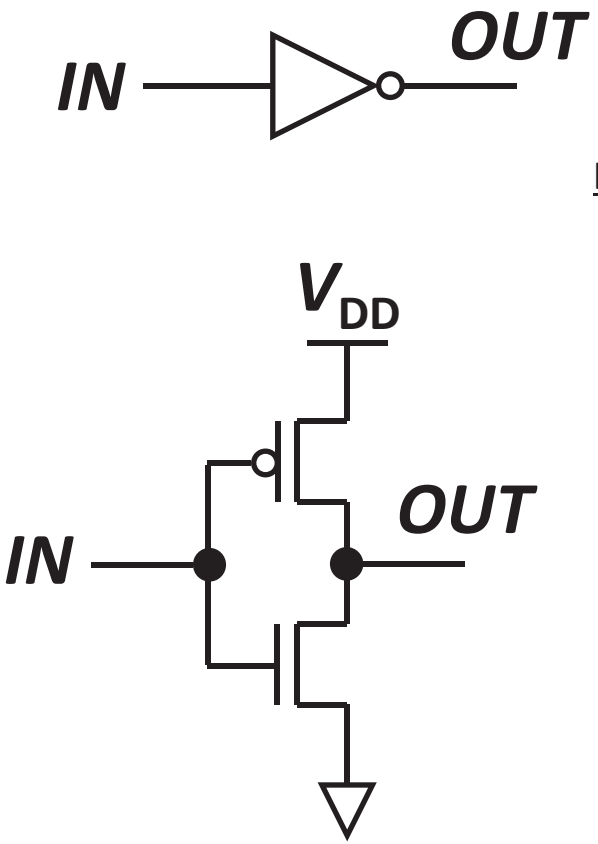


Layout View of CMOS Inverter

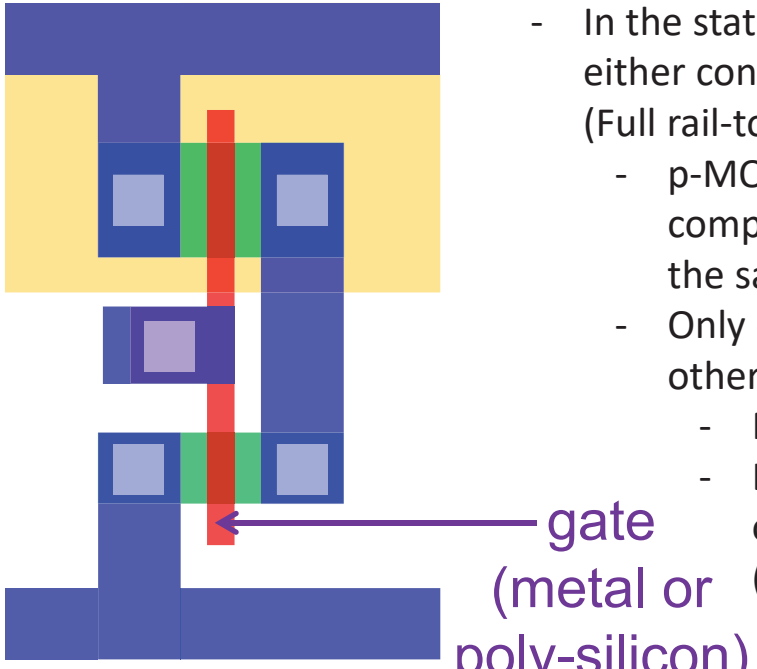


- Simplest static CMOS logic gate
  - One p-MOSFET in PUN
  - One n-MOSFETs in PDN
- Gates of MOSFETs are controlled by the same signal
  - Extremely high input impedance
- In the static state, the output node Y is either connected to **GND** or to $\boldsymbol{V_{DD}}$ (Full rail-to-rail output swing)
  - p-MOSFET and n-MOSFET are complementary switches controlled by the same signal
  - Only one of the MOSFETs is on. The other is off
    - No static power consumption
    - Low output impedance from output to $\boldsymbol{V_{DD}}$ (PMOS is on) or **GND** (NMOS is on) in steady state

The Static CMOS Inverter

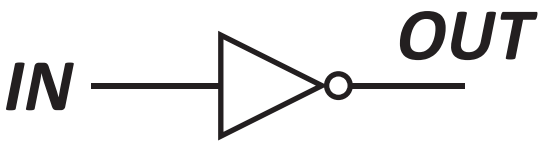


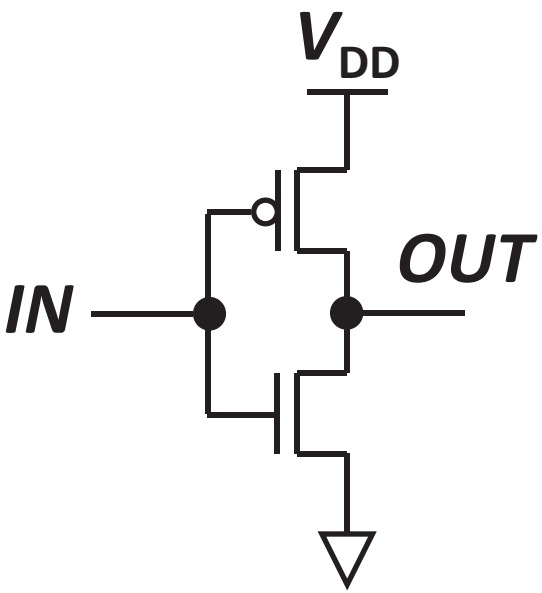
Layout View of CMOS Inverter



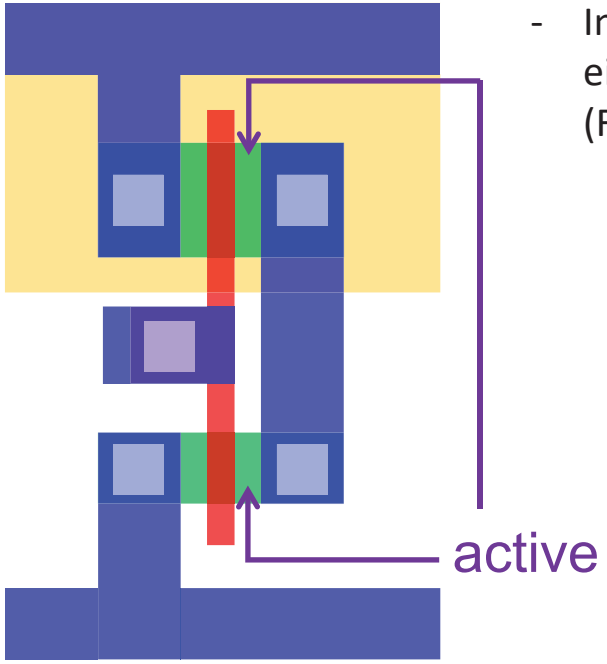
- Simplest static CMOS logic gate
  - One p-MOSFET in PUN
  - One n-MOSFETs in PDN
- Gates of MOSFETs are controlled by the same signal
  - Extremely high input impedance
- In the static state, the output node Y is either connected to **GND** or to $\boldsymbol{V_{DD}}$ (Full rail-to-rail output swing)
  - p-MOSFET and n-MOSFET are complementary switches controlled by the same signal
  - Only one of the MOSFETs is on. The other is off
    - No static power consumption
    - Low output impedance from output to $\boldsymbol{V_{DD}}$ (PMOS is on) or **GND** (NMOS is on) in steady state

The Static CMOS Inverter



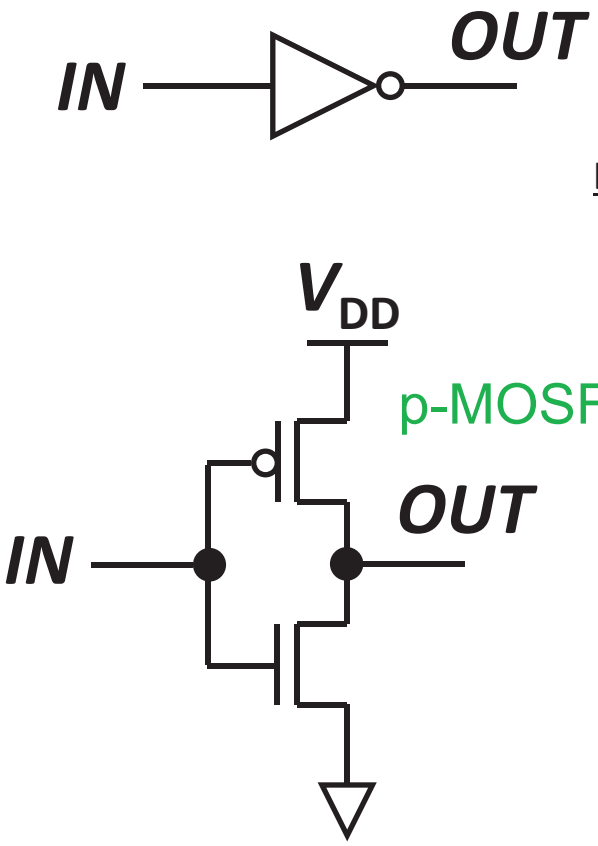


Layout View of CMOS Inverter

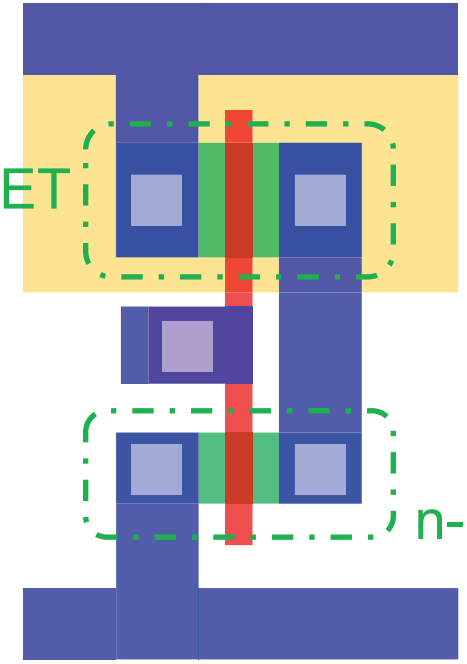


- Simplest static CMOS logic gate
  - One p-MOSFET in PUN
  - One n-MOSFETs in PDN
- Gates of MOSFETs are controlled by the same signal
  - Extremely high input impedance
- In the static state, the output node Y is either connected to **GND** or to $\boldsymbol{V_{DD}}$ (Full rail-to-rail output swing)
  - p-MOSFET and n-MOSFET are complementary switches controlled by the same signal
  - Only one of the MOSFETs is on. The other is off
    - No static power consumption
    - Low output impedance from output to $\boldsymbol{V_{DD}}$ (PMOS is on) or **GND** (NMOS is on) in steady state

The Static CMOS Inverter

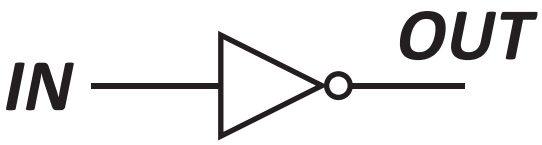


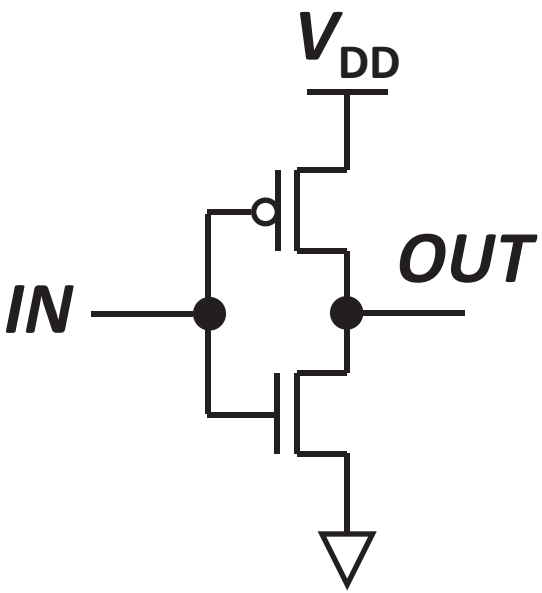
Layout View of CMOS Inverter



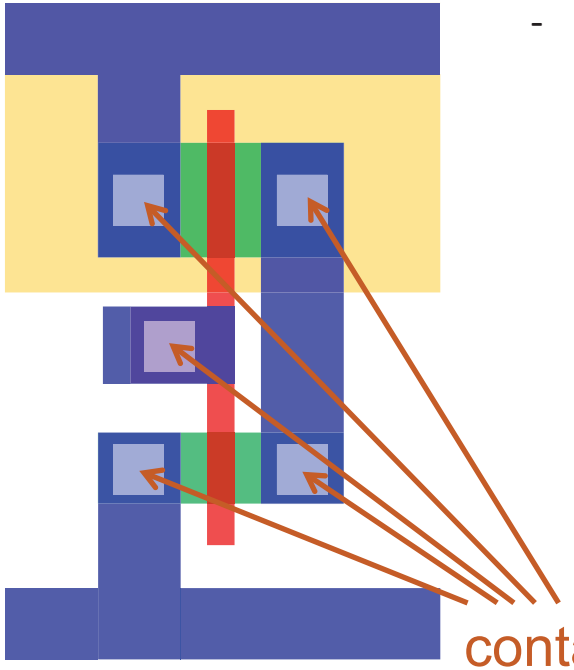
- Simplest static CMOS logic gate
  - One p-MOSFET in PUN
  - One n-MOSFETs in PDN
- Gates of MOSFETs are controlled by the same signal
  - Extremely high input impedance
- In the static state, the output node Y is either connected to **GND** or to $\boldsymbol{V_{DD}}$ (Full rail-to-rail output swing)
  - p-MOSFET and n-MOSFET are complementary switches controlled by the same signal
  - Only one of the MOSFETs is on. The other is off
    - No static power consumption
    - Low output impedance from output to $\boldsymbol{V_{DD}}$ (PMOS is on) or **GND** (NMOS is on) in steady state

The Static CMOS Inverter



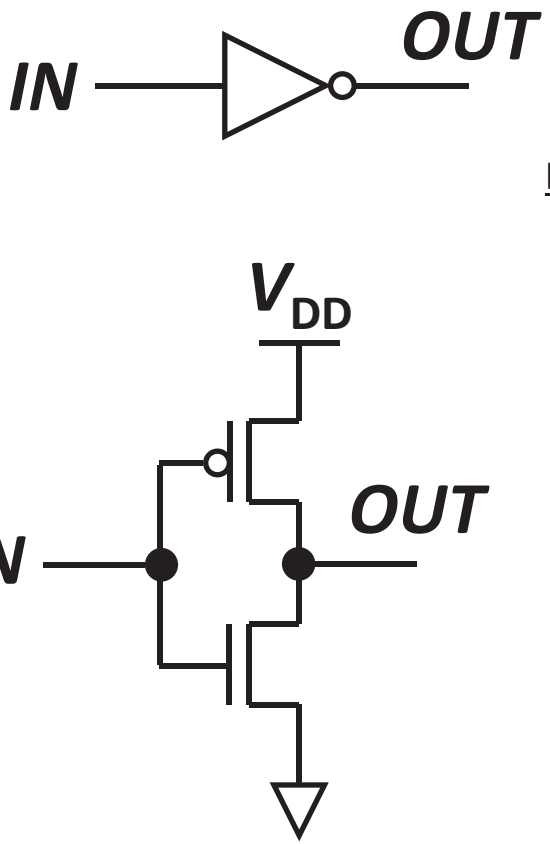


Layout View of CMOS Inverter

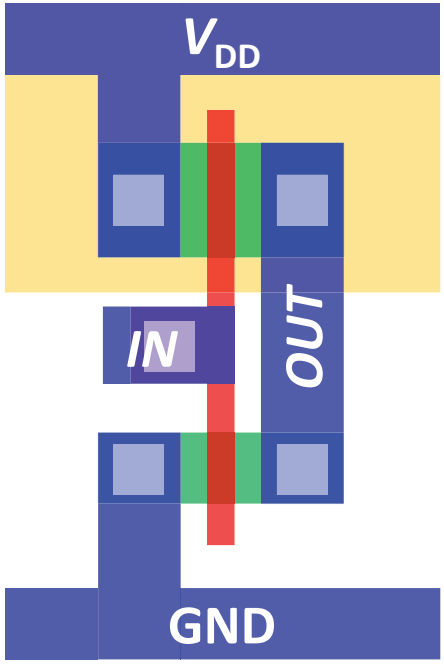


- Simplest static CMOS logic gate
  - One p-MOSFET in PUN
  - One n-MOSFETs in PDN
- Gates of MOSFETs are controlled by the same signal
  - Extremely high input impedance
- In the static state, the output node Y is either connected to **GND** or to $\boldsymbol{V_{DD}}$ (Full rail-to-rail output swing)
  - p-MOSFET and n-MOSFET are complementary switches controlled by the same signal
  - Only one of the MOSFETs is on. The other is off
    - No static power consumption
    - Low output impedance from output to $\boldsymbol{V_{DD}}$ (PMOS is on) or **GND** (NMOS is on) in steady state

The Static CMOS Inverter

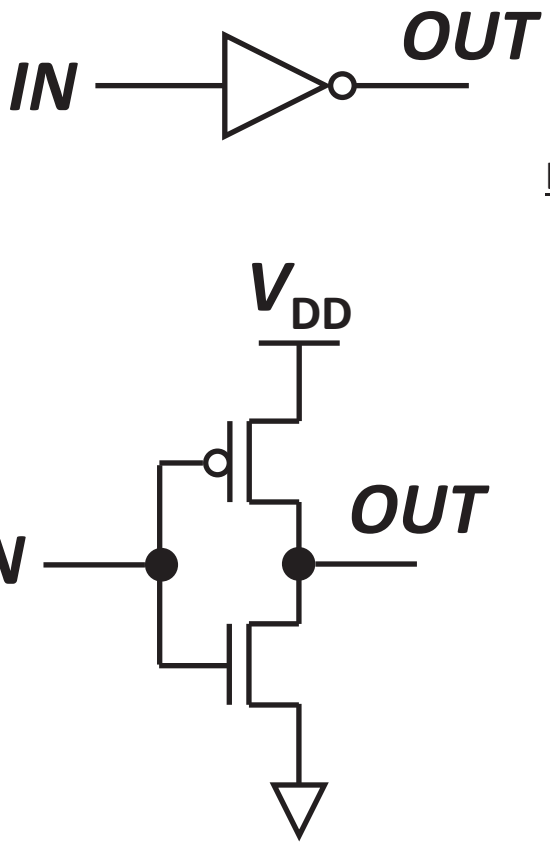


Layout View of CMOS Inverter

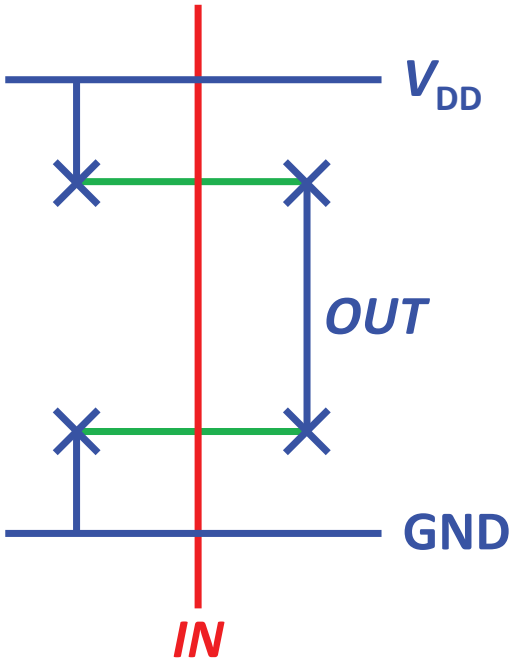


- Simplest static CMOS logic gate
  - One p-MOSFET in PUN
  - One n-MOSFETs in PDN
- Gates of MOSFETs are controlled by the same signal
  - Extremely high input impedance
- In the static state, the output node Y is either connected to **GND** or to $\boldsymbol{V_{DD}}$ (Full rail-to-rail output swing)
  - p-MOSFET and n-MOSFET are complementary switches controlled by the same signal
  - Only one of the MOSFETs is on. The other is off
    - No static power consumption
    - Low output impedance from output to $\boldsymbol{V_{DD}}$ (PMOS is on) or **GND** (NMOS is on) in steady state

The Static CMOS Inverter



Layout View of CMOS Inverter (Stick Diagram)

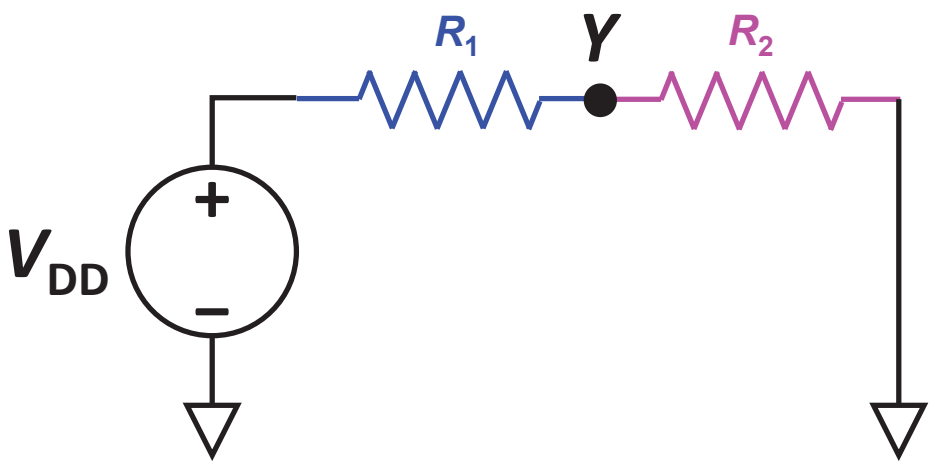


- Simplest static CMOS logic gate
  - One p-MOSFET in PUN
  - One n-MOSFETs in PDN
- Gates of MOSFETs are controlled by the same signal
  - Extremely high input impedance
- In the static state, the output node Y is either connected to **GND** or to $\boldsymbol{V_{DD}}$ (Full rail-to-rail output swing)
  - p-MOSFET and n-MOSFET are complementary switches controlled by the same signal
  - Only one of the MOSFETs is on. The other is off
    - No static power consumption
    - Low output impedance from output to $\boldsymbol{V_{DD}}$ (PMOS is on) or **GND** (NMOS is on) in steady state

Week 2-5

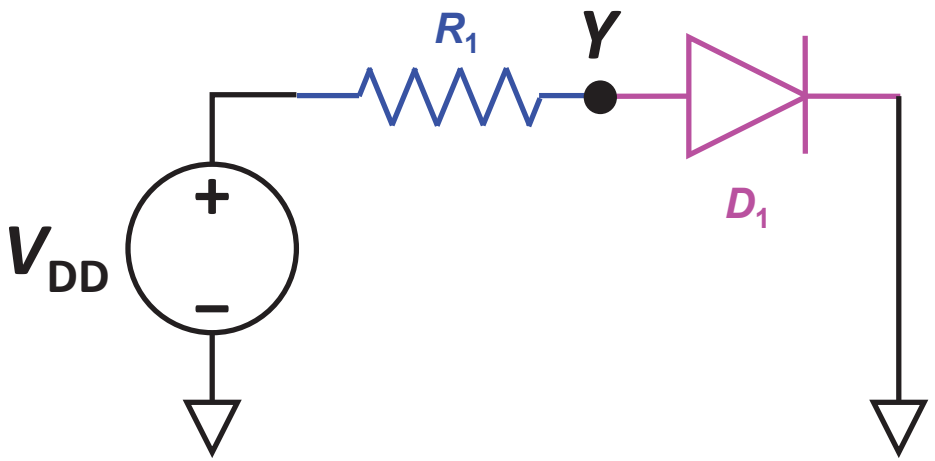
Introduction to Load Line Analysis

Solving for DC Solution to Non-linear Circuits



- Given this circuit, determine the stead state voltage of the node ***Y***
  - $V_Y/V_{DD} = (R_2)/(R_1+R_2)$
  - Simple problem
- What if R_2 is a non-linear element such as a diode?

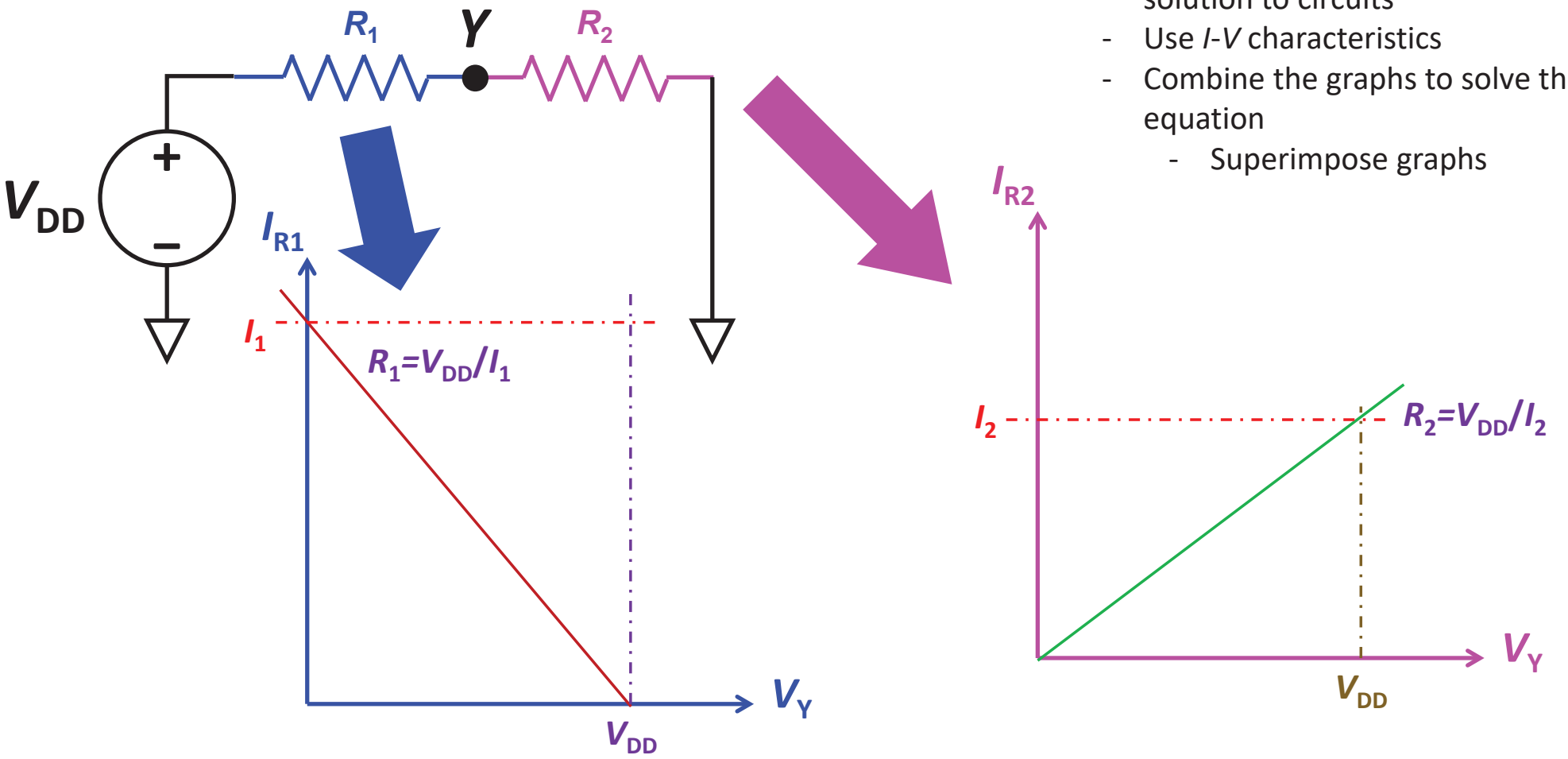
Solving for DC Solution to Non-linear Circuits



- Given this circuit, determine the stead state voltage of the node ***Y***
  - $V_Y/V_{DD} = (R_2)/(R_1+R_2)$
  - Simple problem
- What if R_2 is a non-linear element such as a diode?
  - $I_D = I_{D0}\exp(-V_Y/nV_T)$
  - $I_D = (V_{DD}-V_Y)/R_1$
  - $(V_{DD}-V_Y)/R_1 = I_{D0}\exp(-V_Y/nV_T)$
- Not trivial to solve!

Load Line Analysis

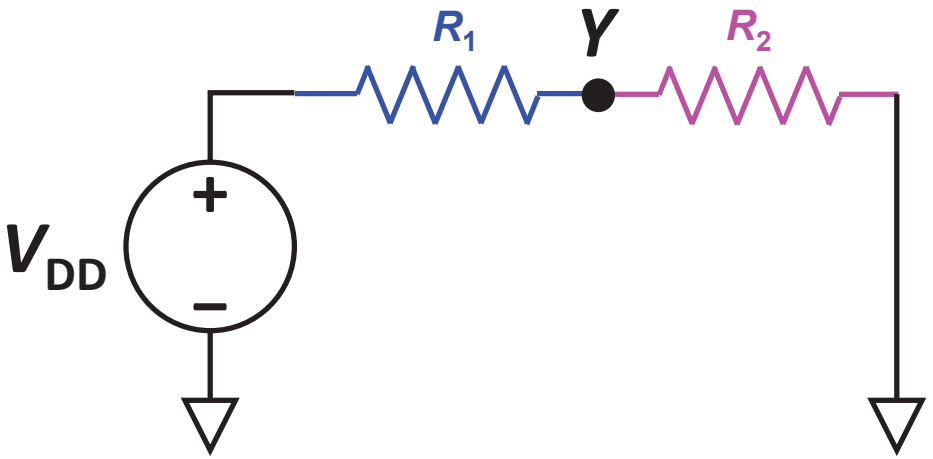
$I_{R1} = I_{R2} \rightarrow (V_{DD}-V_Y)/R_1 = V_Y/R_2$



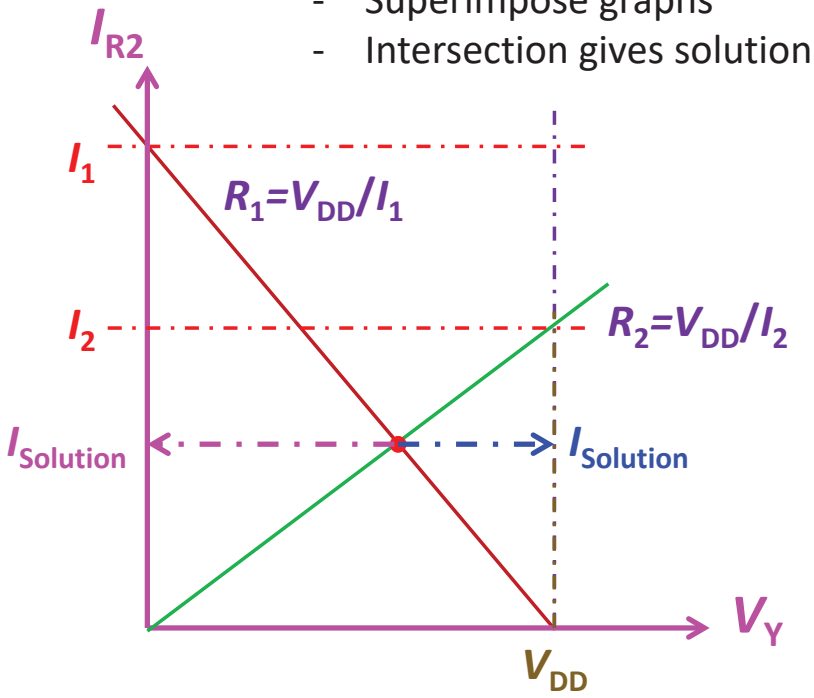
- Graphical method to solve for DC solution to circuits
- Use *I-V* characteristics
- Combine the graphs to solve the equation
  - Superimpose graphs

Load Line Analysis

$I_{R1} = I_{R2} \rightarrow (V_{DD}-V_Y)/R_1 = V_Y/R_2$

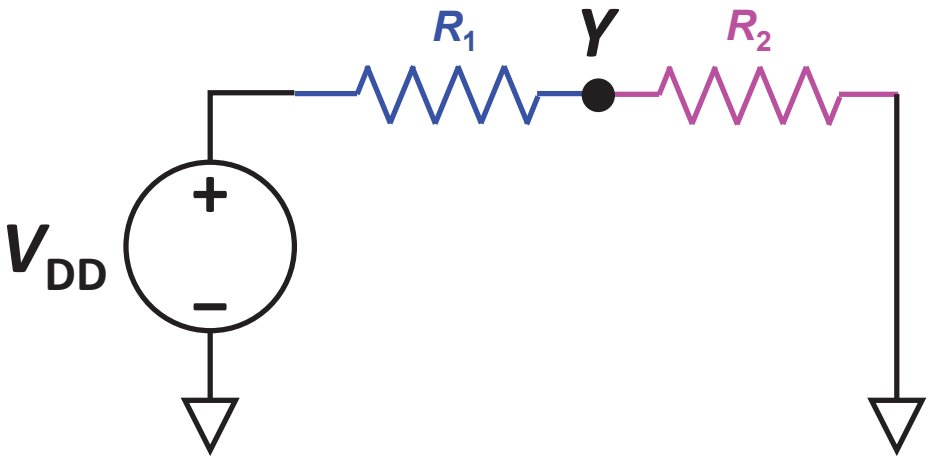


- Graphical method to solve for DC solution to circuits
- Use *I-V* characteristics
- Combine the graphs to solve the equation
  - Superimpose graphs
  - Intersection gives solution

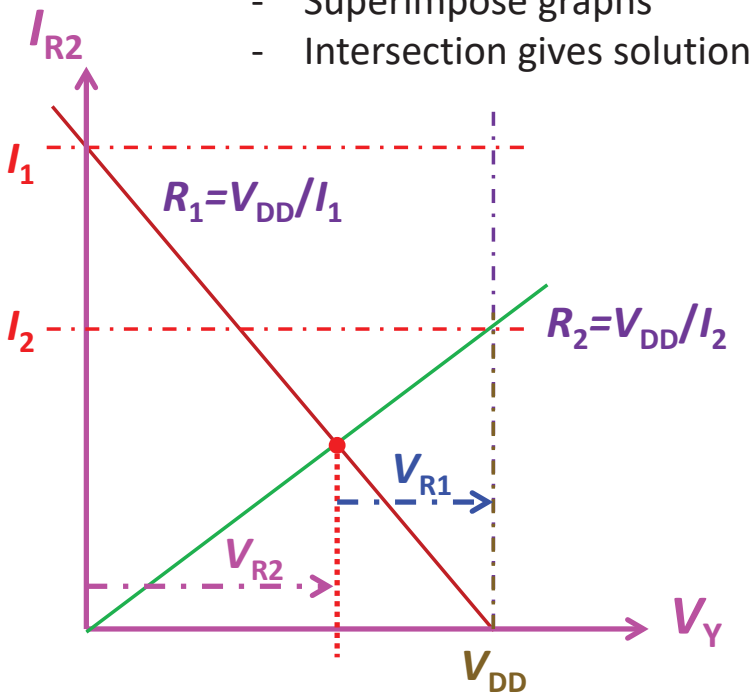


Load Line Analysis

$I_{R1} = I_{R2} \rightarrow (V_{DD}-V_Y)/R_1 = V_Y/R_2$

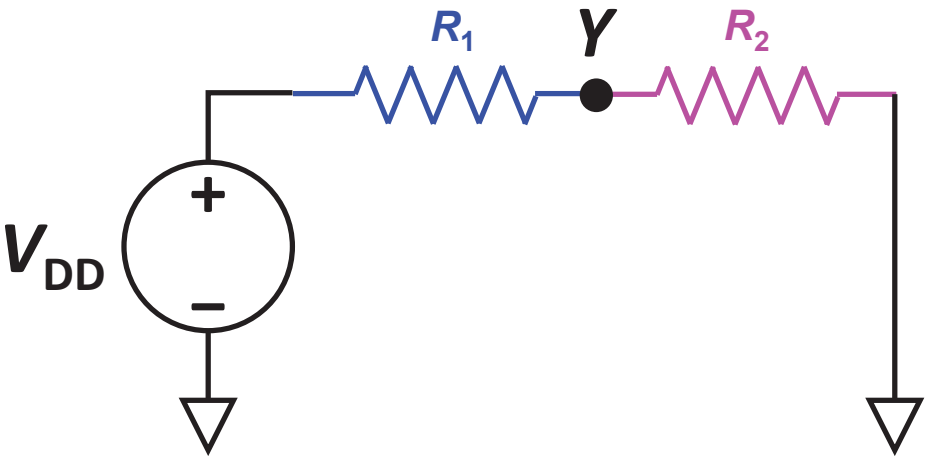


- Graphical method to solve for DC solution to circuits
- Use *I-V* characteristics
- Combine the graphs to solve the equation
  - Superimpose graphs
  - Intersection gives solution

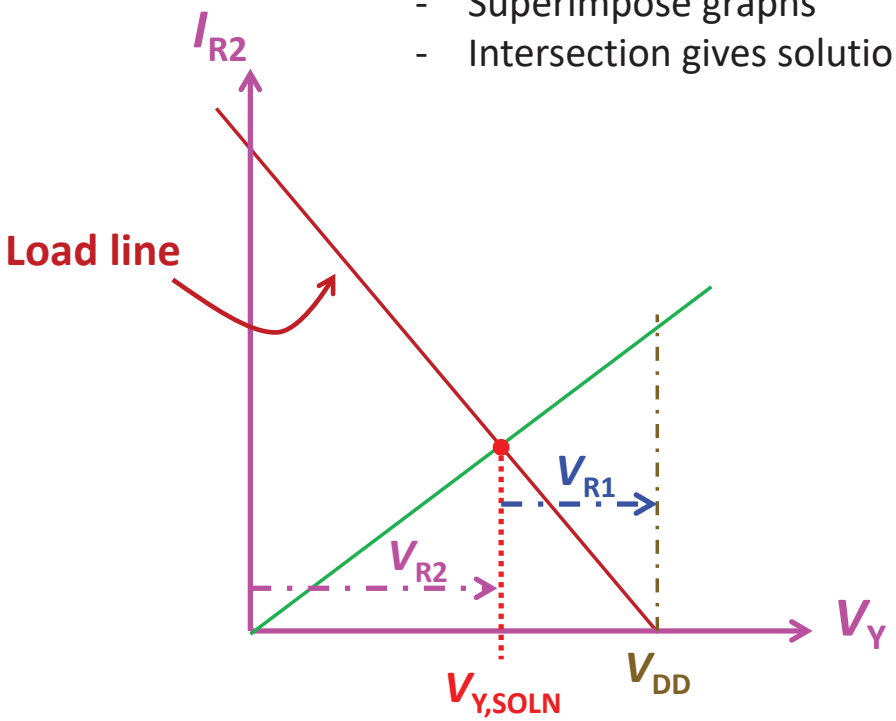


Load Line Analysis

$I_{R1} = I_{R2} \rightarrow (V_{DD}-V_Y)/R_1 = V_Y/R_2$



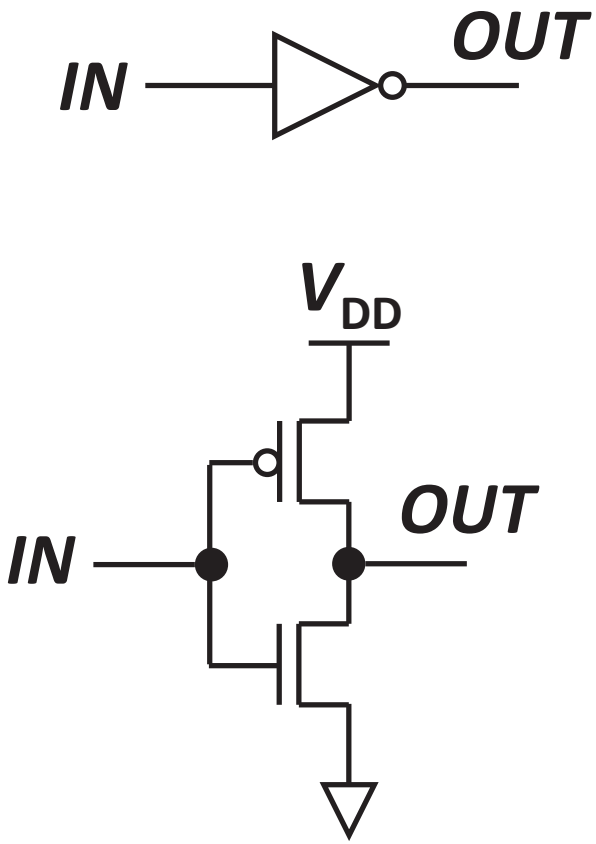
- Graphical method to solve for DC solution to circuits
- Use *I-V* characteristics
- Combine the graphs to solve the equation
  - Superimpose graphs
  - Intersection gives solution



Week 2-6

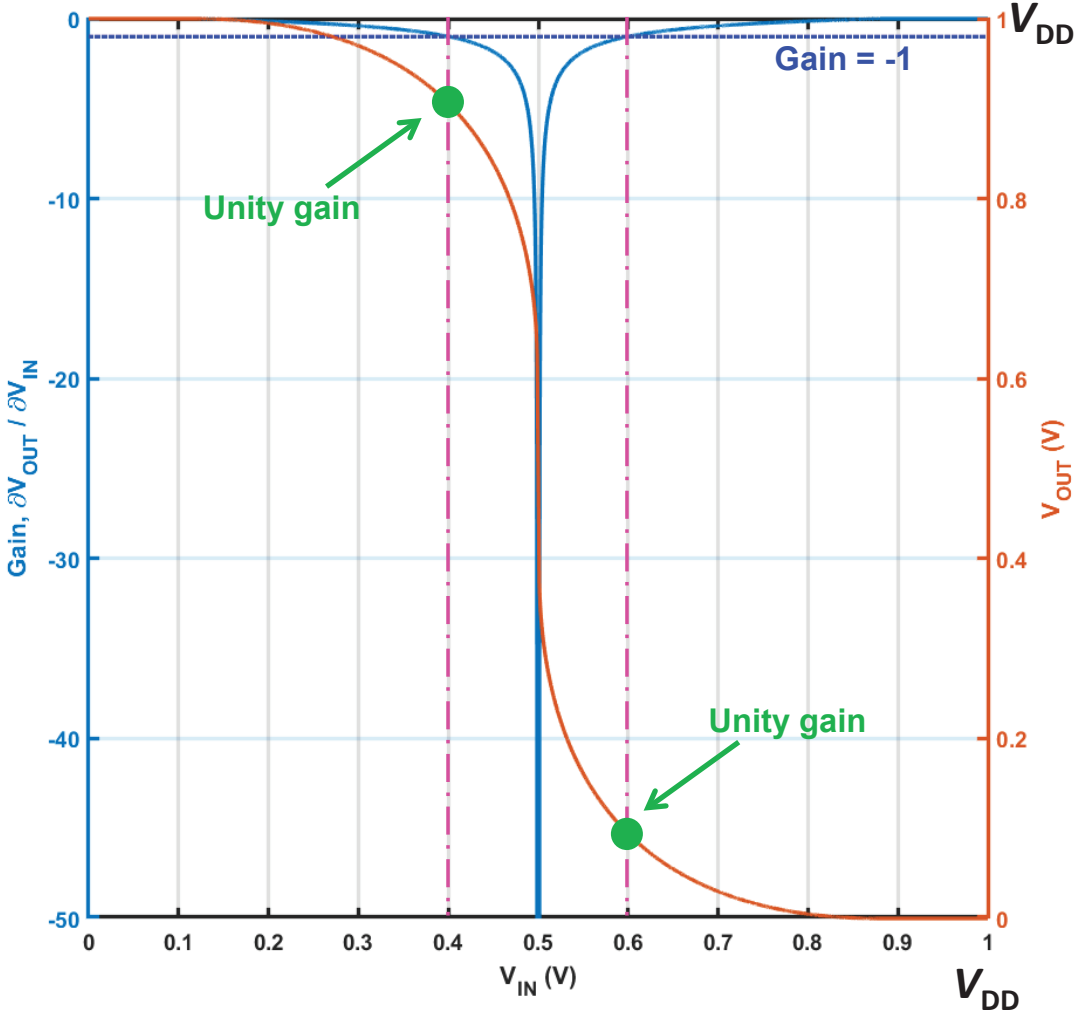
Static Response of the Static CMOS Inverter

Static Response of the Static CMOS Inverter



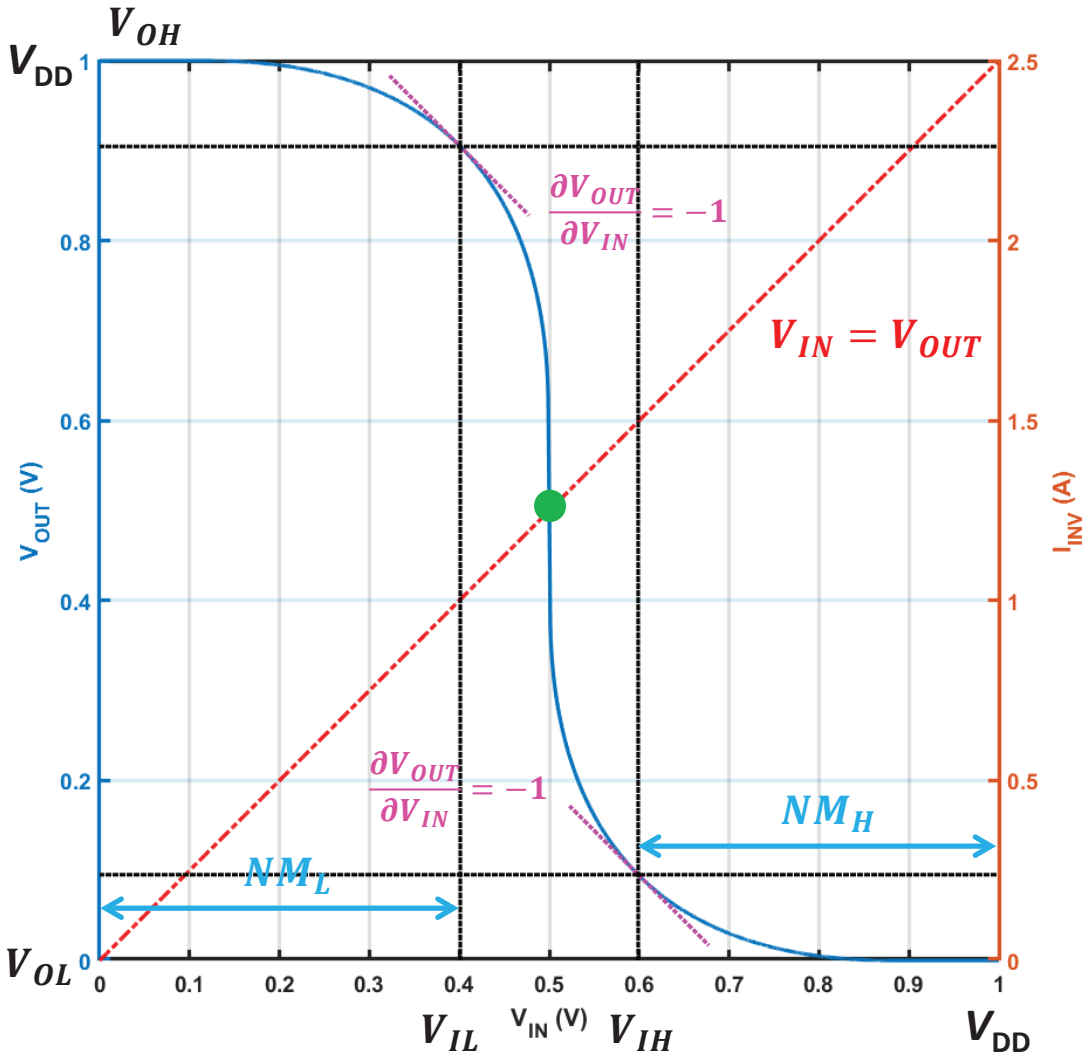
- What is the output voltage, V_{OUT}, as we vary the analog input voltage V_{IN}?
  - Expectation for V_{IN} = 0 V:
    - n-MOSFET in cut-off
      - $R_{PDN} = R_{OFF}$
    - p-MOSFET is on
      - $R_{PUN} = R_{ON}$
    - $R_{OFF} >> R_{ON}$
    - $V_{OUT} \approx V_{DD}$
  - Expectation for $V_{IN} = V_{DD}$:
    - n-MOSFET is on
      - $R_{PDN} = R_{ON}$
    - p-MOSFET is in cut-off
      - $R_{PUN} = R_{OFF}$
    - $R_{ON} << R_{OFF}$
    - $V_{OUT} \approx$ 0 V
  - What if V_{IN} is a voltage in the range $0 < V_{IN} < V_{DD}$?

The Voltage Transfer Characteristic (VTC)



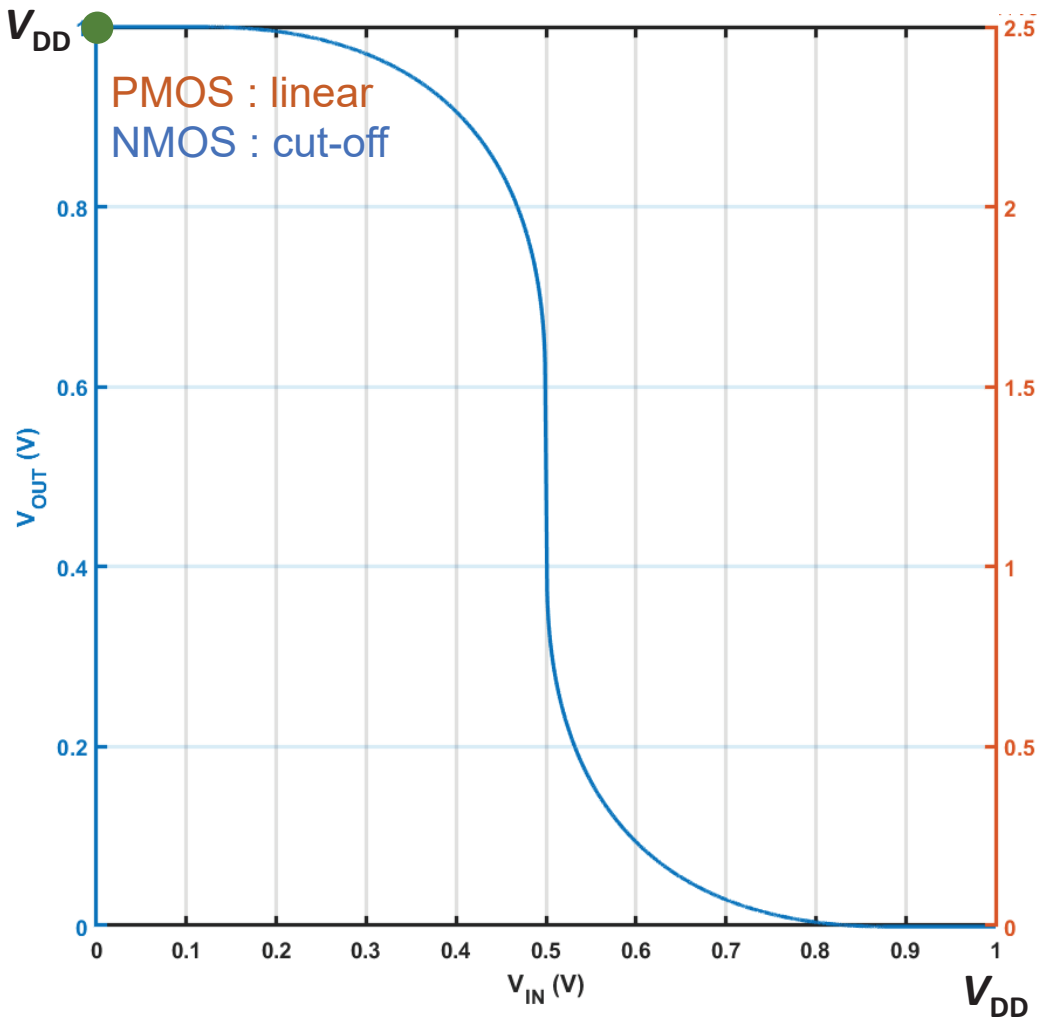
- What is the output voltage, V_{OUT}, as we vary the analog input voltage V_{IN} in the range $0\ V < V_{IN} < V_{DD}$?

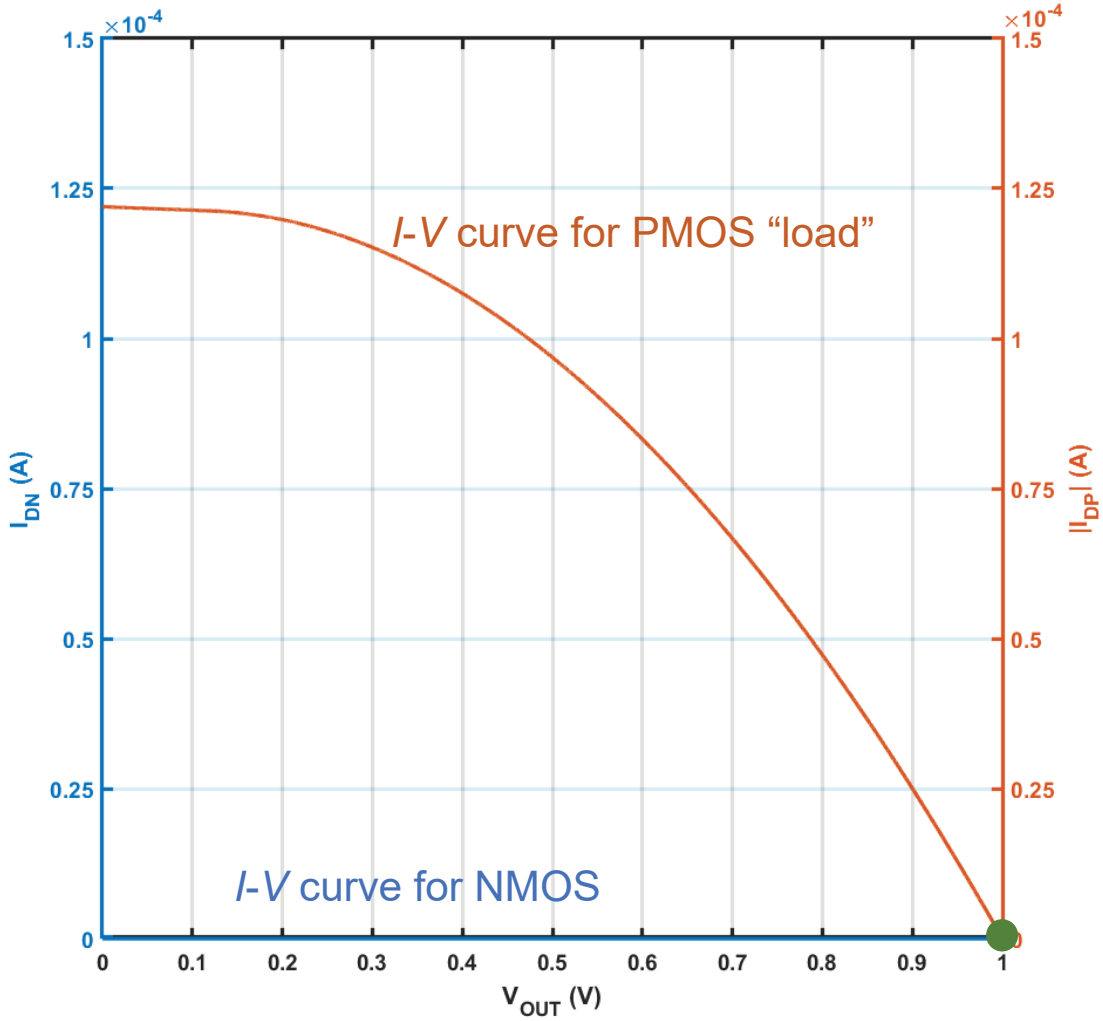
The Voltage Transfer Characteristic (VTC)



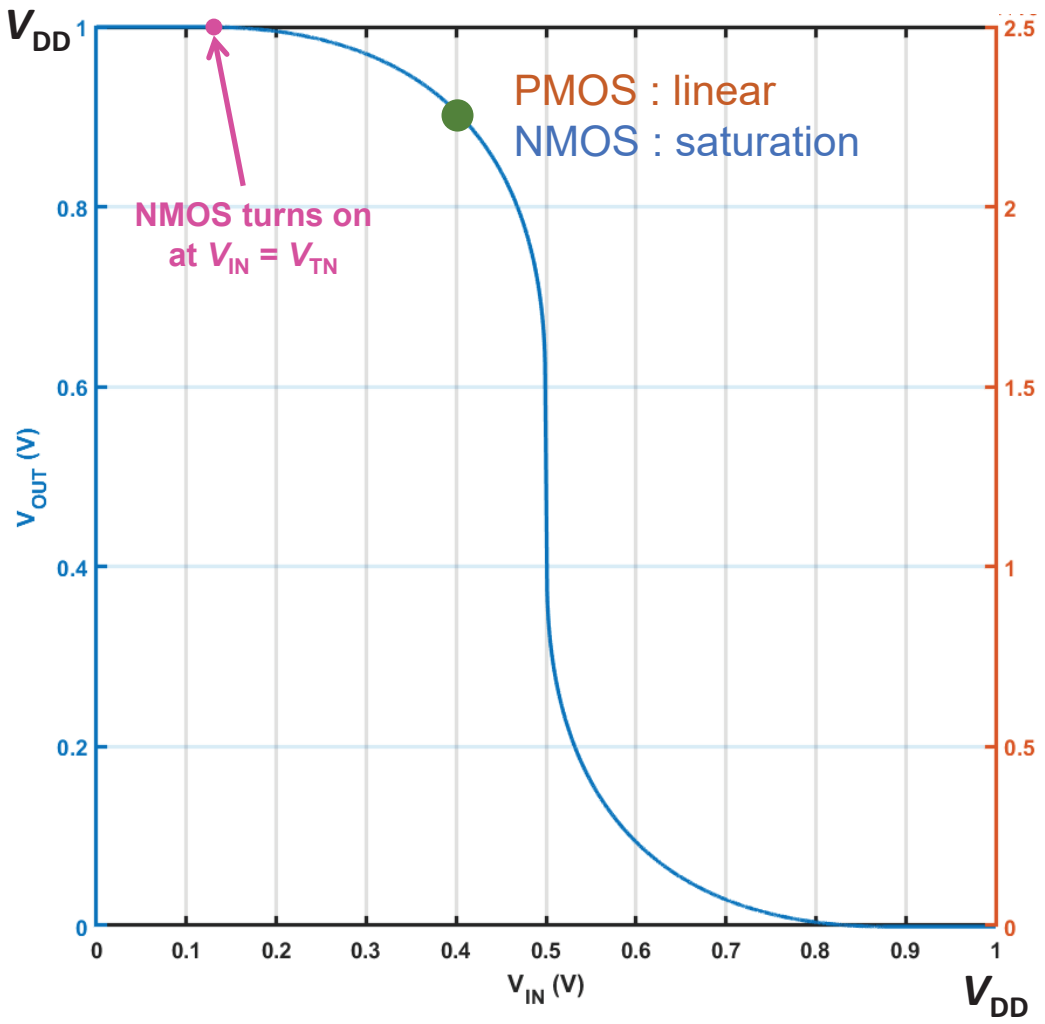
- What is the output voltage, V_{OUT}, as we vary the analog input voltage V_{IN} in the range $0\ V < V_{IN} < V_{DD}$?
  - Mid-point (trip point): $V_M = V_{IN} = V_{OUT}$
  - Gain = $\frac{\partial V_{OUT}}{\partial V_{IN}}$
  - Output High Voltage (ideal input): V_{OH}
  - Input Low Voltage: V_{IL}
  - Noise Margin (Low): NM_L
  - Output Low Voltage (ideal input): V_{OL}
  - Input High Voltage: V_{IH}
  - Noise Margin (High): NM_H
- How to get the VTC?

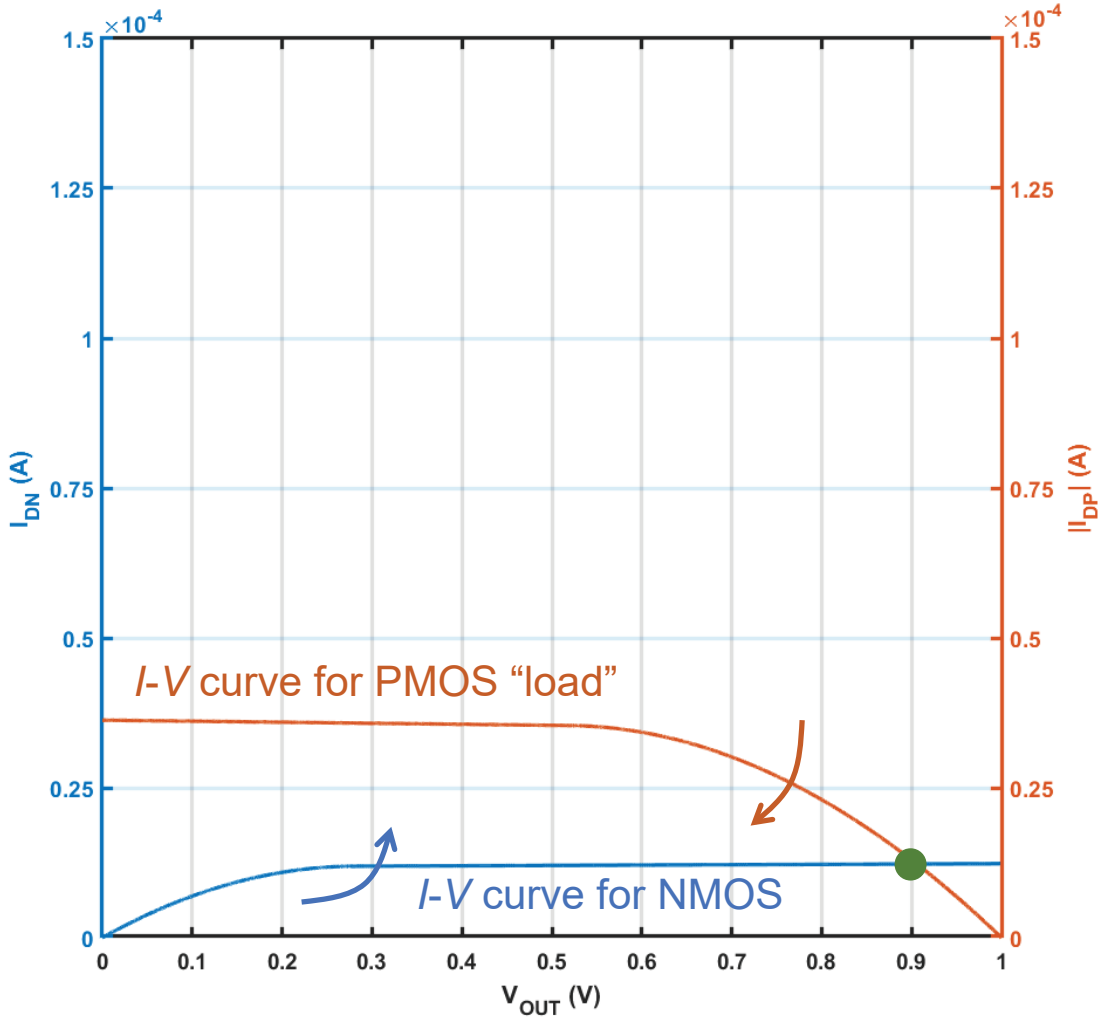
Load Line Analysis for Static CMOS Inverter



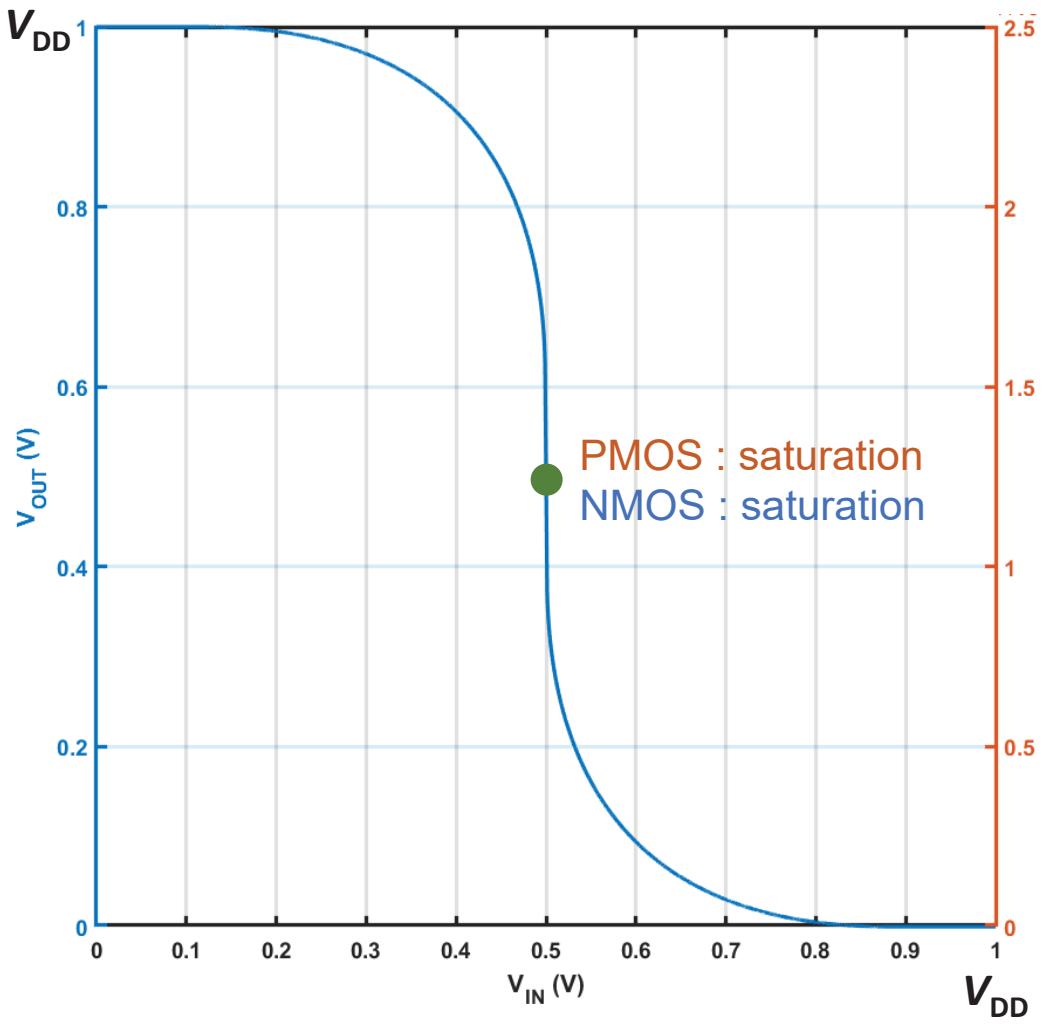


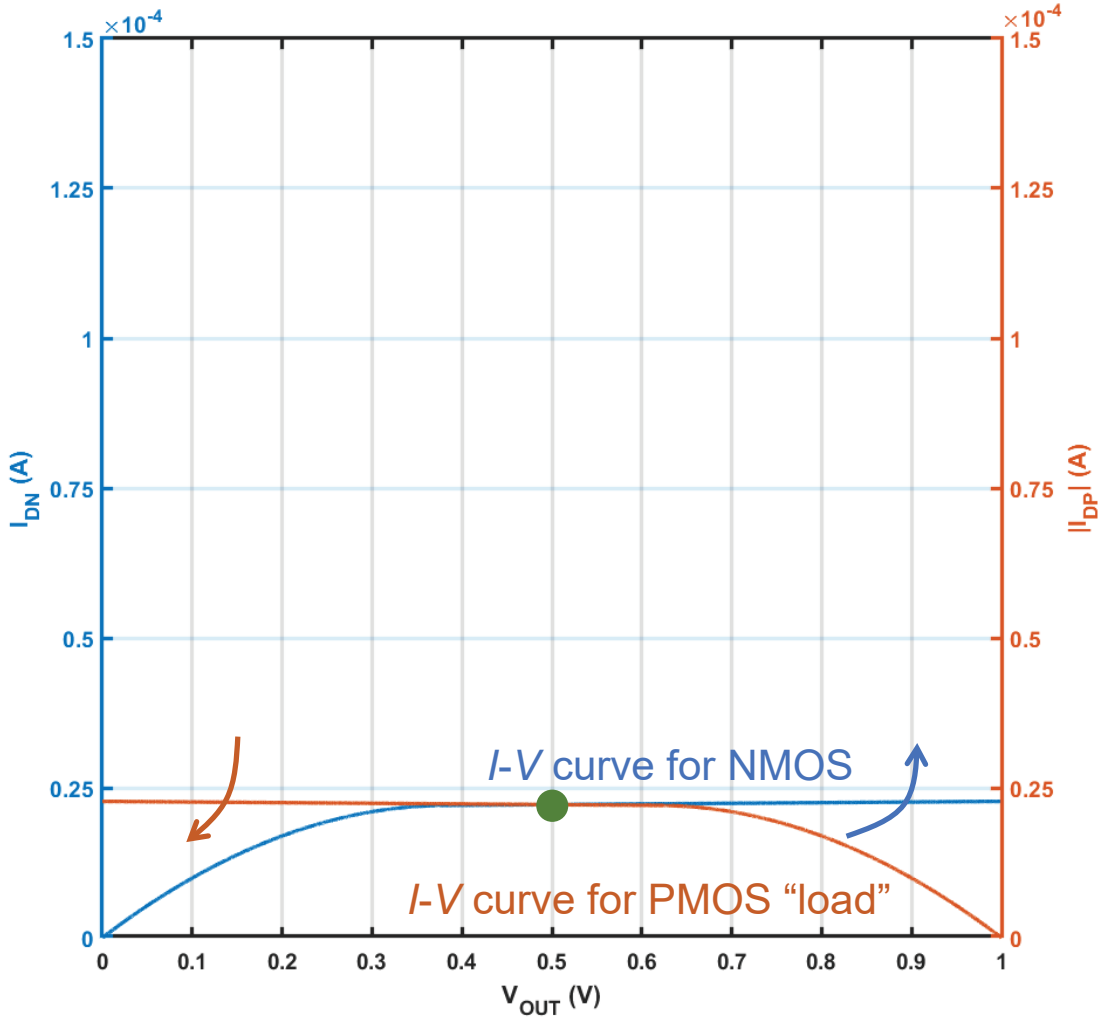
Load Line Analysis for Static CMOS Inverter



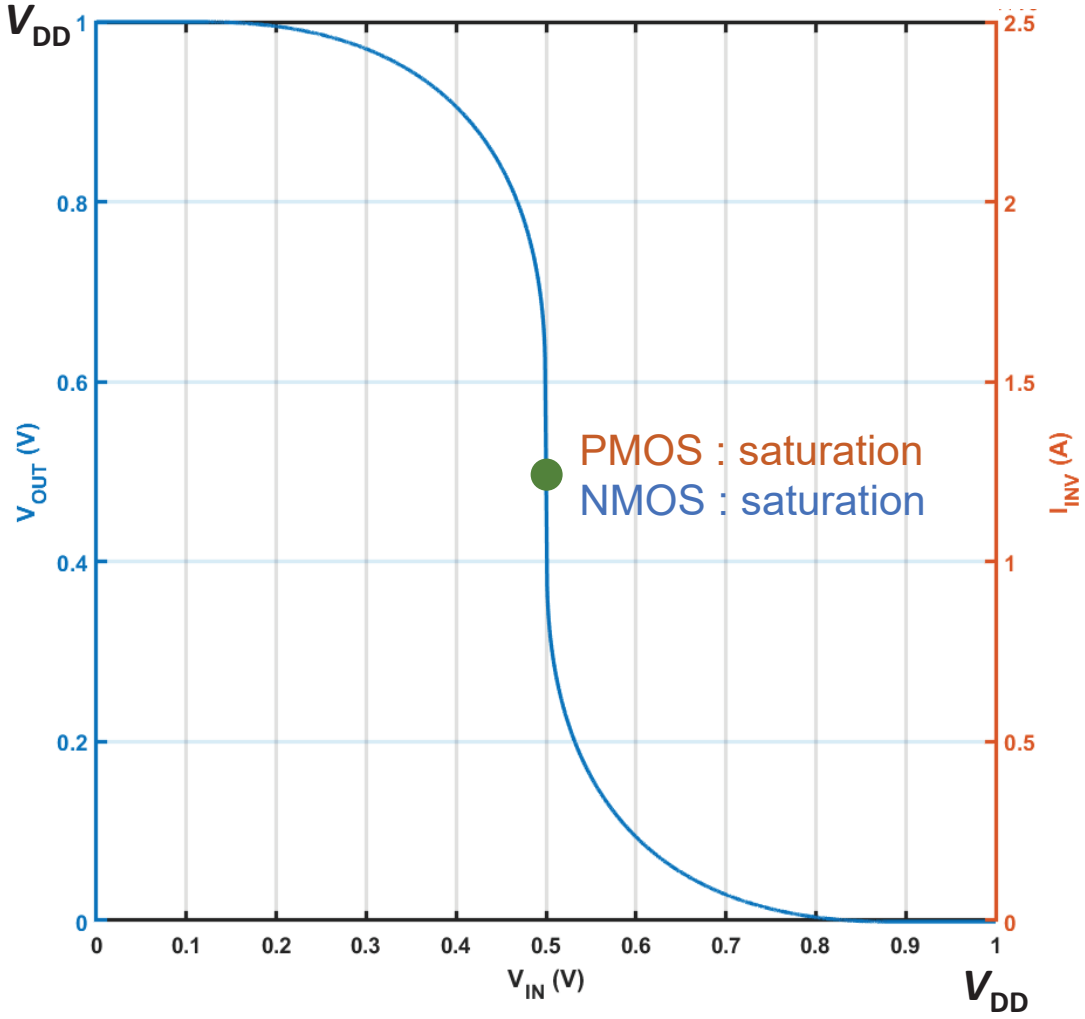


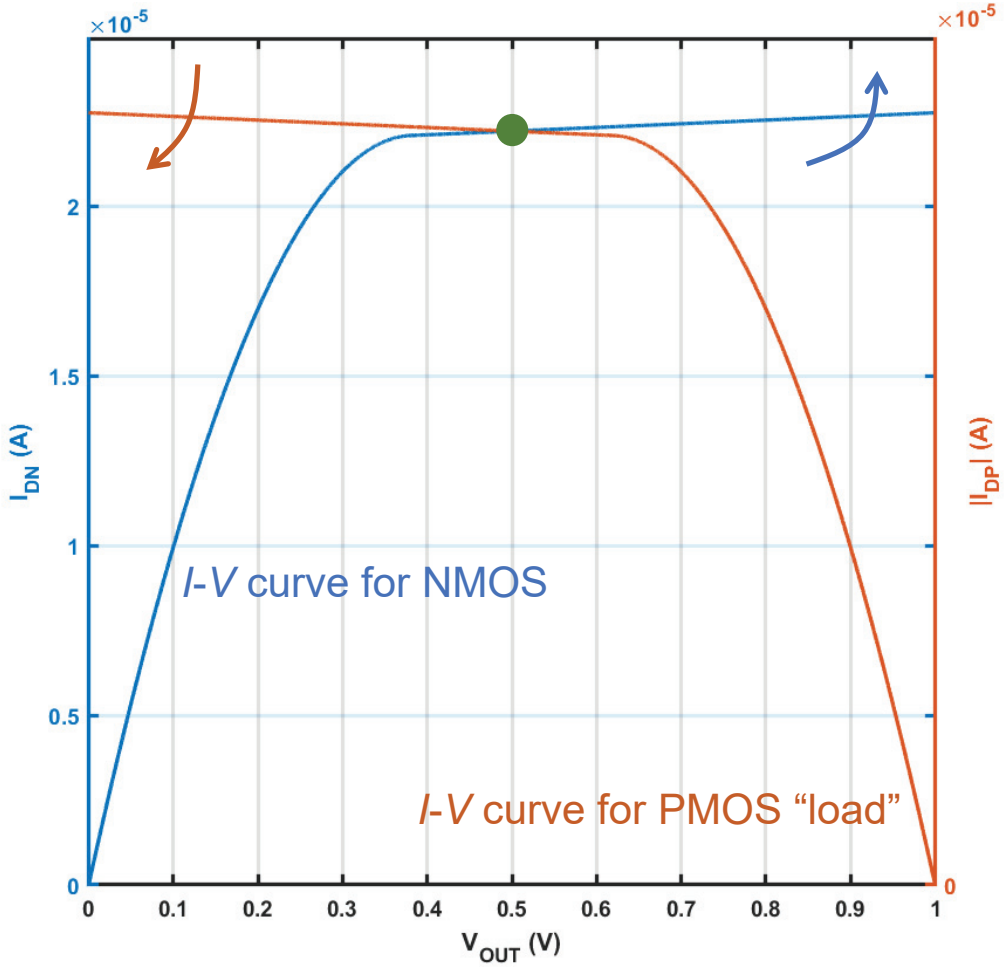
Load Line Analysis for Static CMOS Inverter



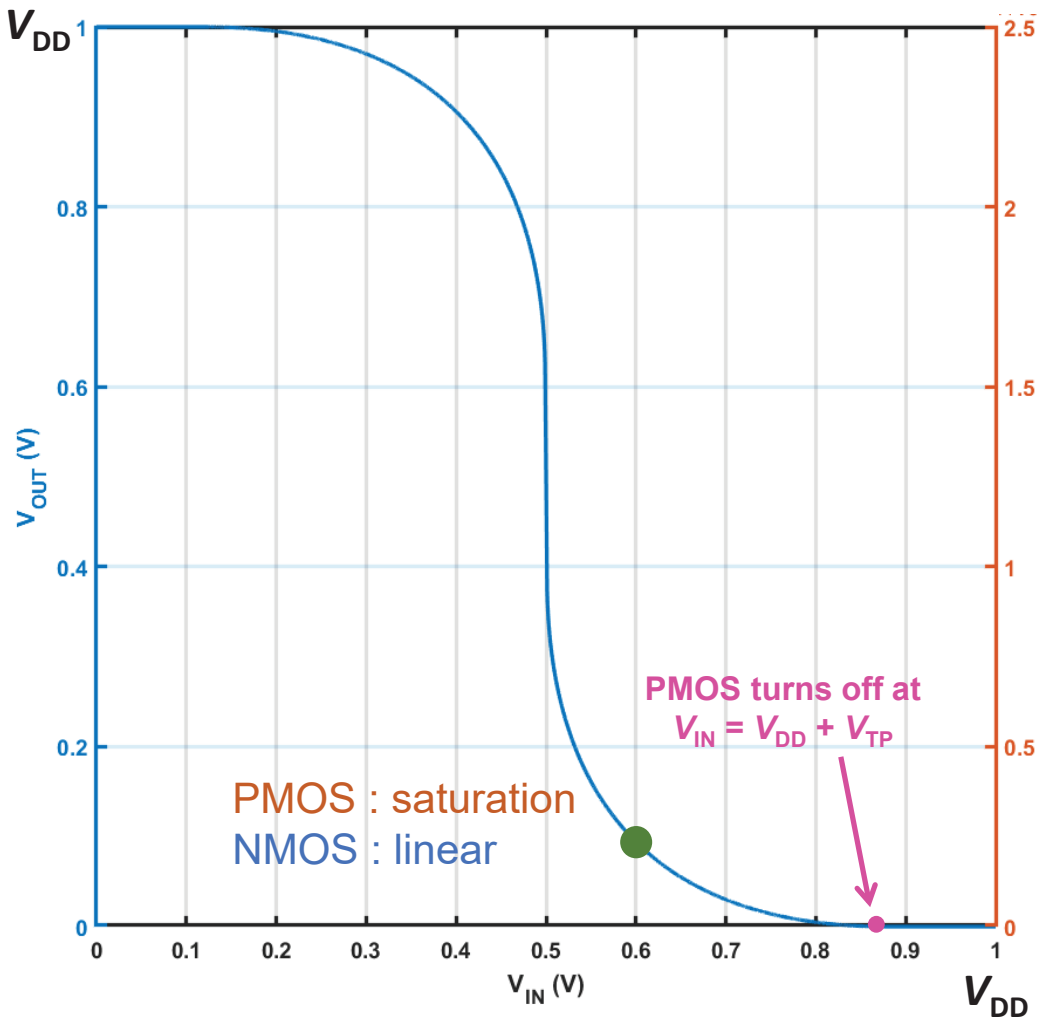


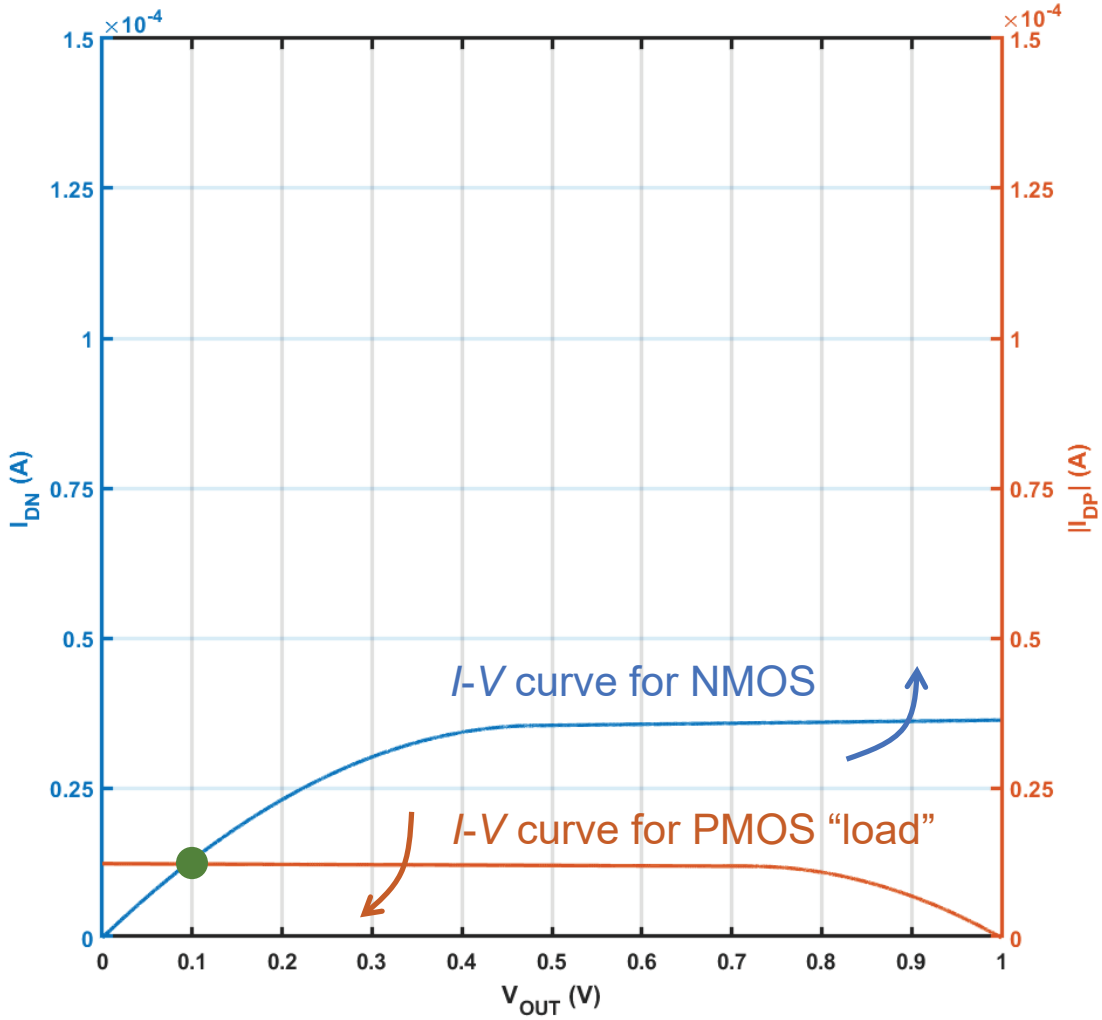
Load Line Analysis for Static CMOS Inverter



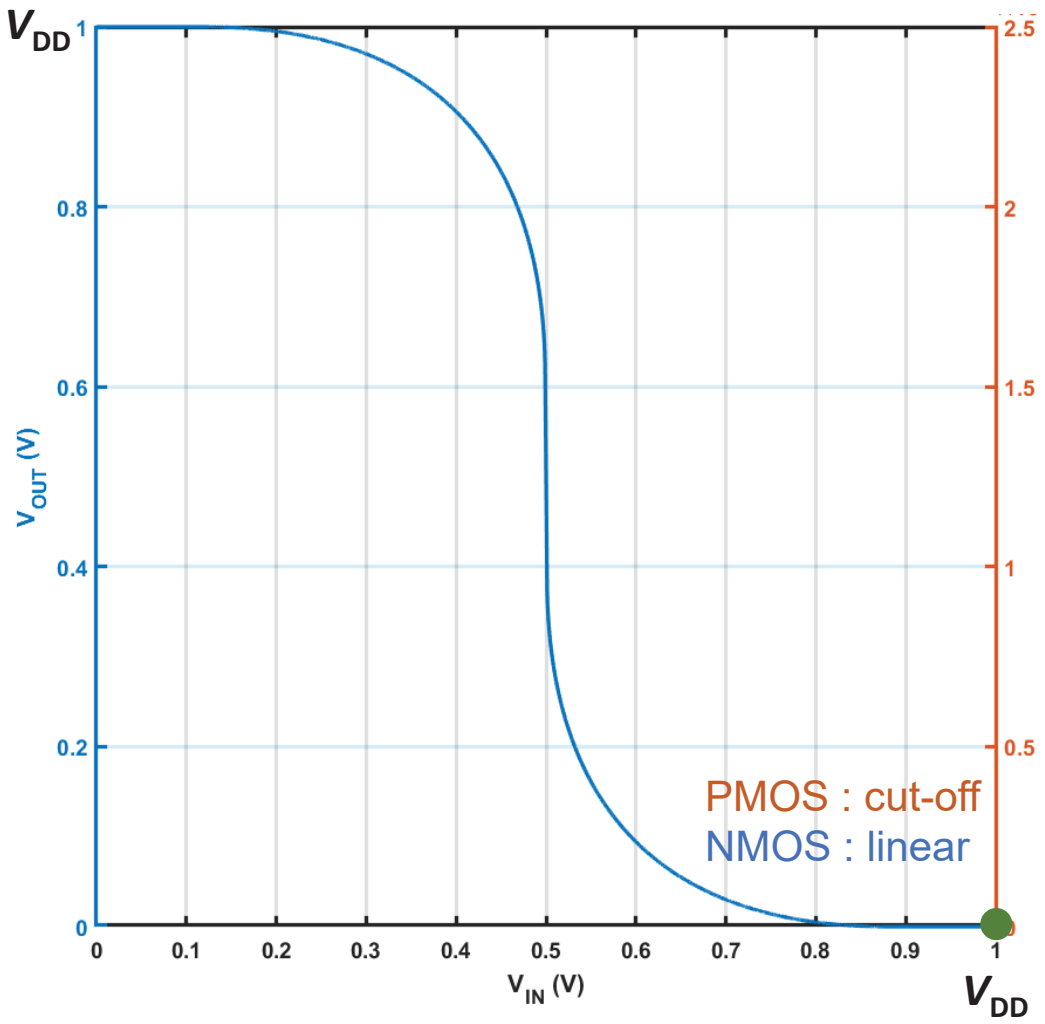


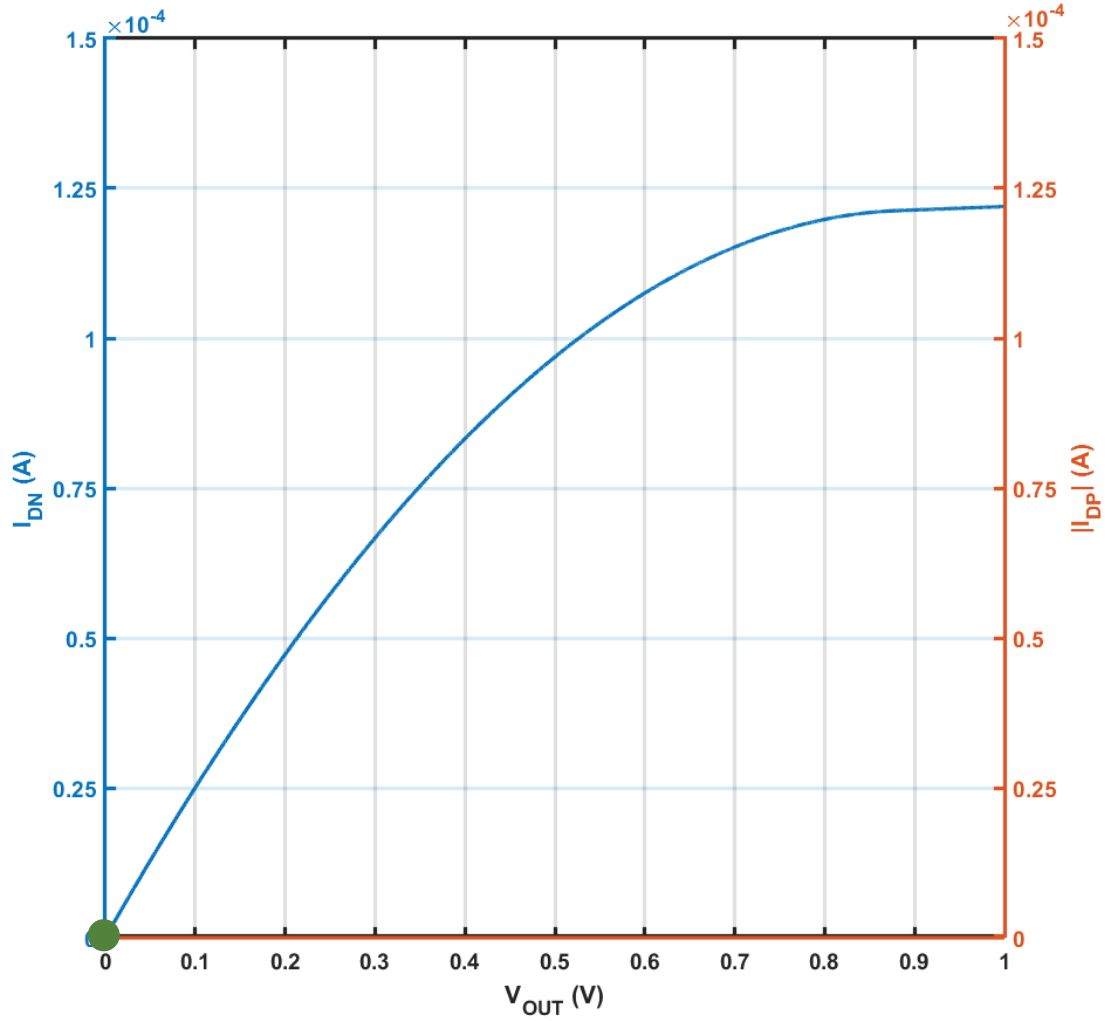
Load Line Analysis for Static CMOS Inverter



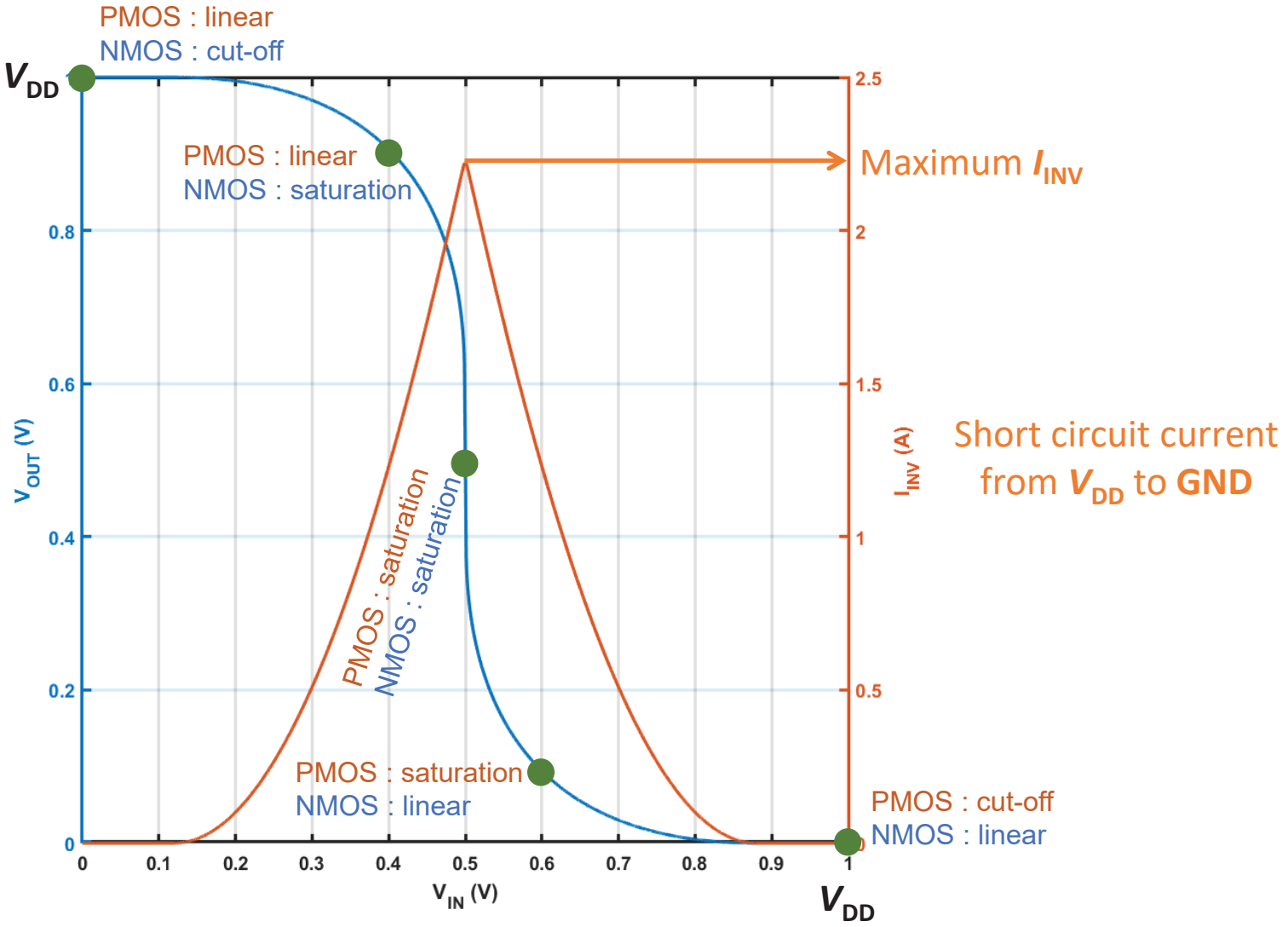


Load Line Analysis for Static CMOS Inverter





Static Behavior of CMOS Inverter



Short circuit current from V_{DD} to **GND**

Determination of V_M

In the inverter, if $\boldsymbol{V_{IN} = V_M}$, then $\boldsymbol{V_{OUT} = V_M}$ by definition.

For the n-MOSFET in the static CMOS inverter:

$$V_{GSn} = V_{DSn} = V_M$$

Also, $V_{DSn} > V_{GSn} - V_{TN}$ so NMOS is in saturation

For the p-MOSFET in the static CMOS inverter:

$$V_{GSp} = V_{DSp} = V_{DD} - V_M$$

Also, $V_{DSp} < V_{GSp} - V_{TP}$ so PMOS is in saturation

Note that both the n-MOSFET and p-MOSFET are in saturation. Moreover, $I_{DSn} = -I_{DSp}$.

Assuming short channel device and no channel length modulation,

$$\mu_n C_{OX} \frac{W_N}{L_N}\left(V_{GSn} - V_{TN} - \frac{V_{DS,SATn}}{2}\right)V_{DS,SATn} = \mu_p C_{OX} \frac{W_P}{L_P}\left(V_{GSp} - V_{TP} - \frac{V_{DS,SATp}}{2}\right)V_{DS,SATp}$$

$$\mu_n C_{OX} \frac{W_N}{L_N}\left(V_M - V_{TN} - \frac{V_{DS,SATn}}{2}\right)V_{DS,SATn} = \mu_p C_{OX} \frac{W_P}{L_P}\left(V_M - V_{DD} - V_{TP} - \frac{V_{DS,SATp}}{2}\right)V_{DS,SATp}$$

$$\beta_N \left(V_M - V_{TN} - \frac{V_{DS,SATn}}{2}\right)V_{DS,SATn} = \beta_P \left(V_M - V_{DD} - V_{TP} - \frac{V_{DS,SATp}}{2}\right)V_{DS,SATp}$$

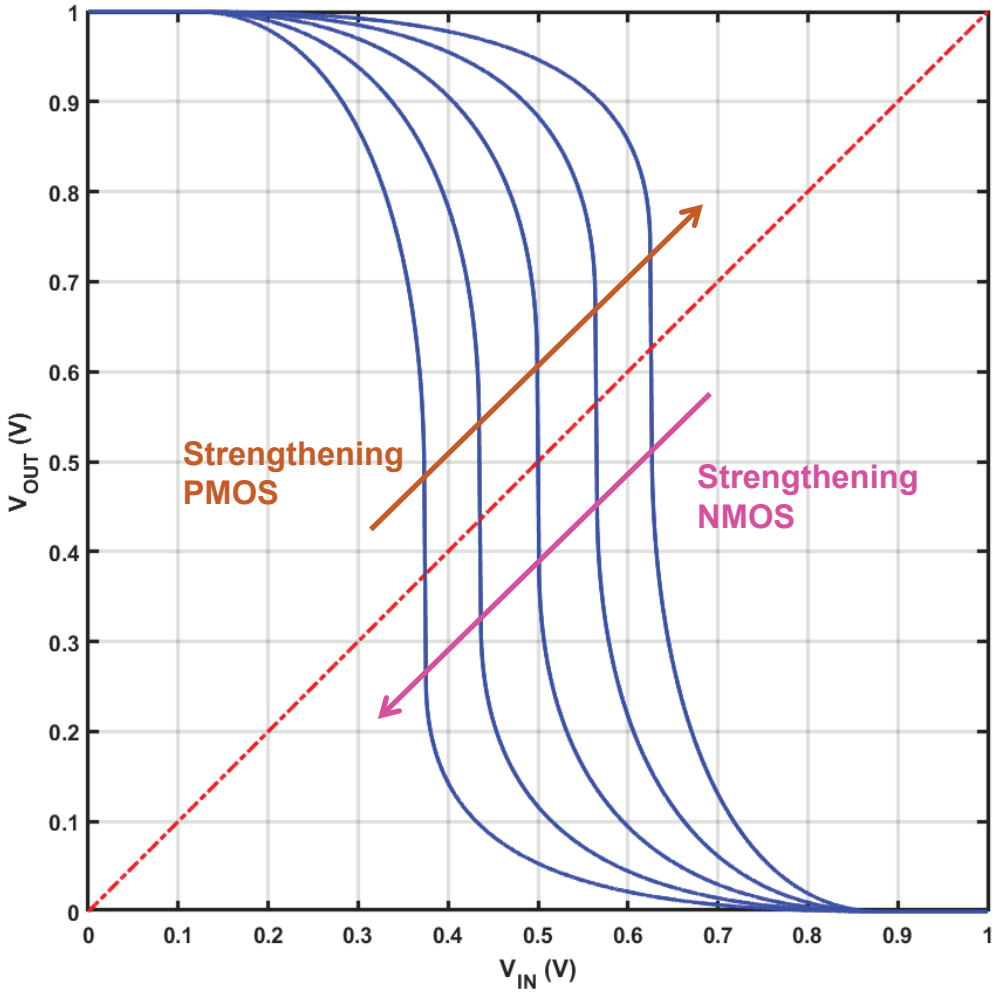
$$(\beta_N V_{DS,SATn} - \beta_P V_{DS,SATp})V_M = \beta_N V_{DS,SATn}\left(V_{TN} + \frac{V_{DS,SATn}}{2}\right) - \beta_P V_{DS,SATp}\left(V_{DD} + V_{TP} + \frac{V_{DS,SATp}}{2}\right)$$

$$\left(1 - \frac{\beta_P V_{DS,SATp}}{\beta_N V_{DS,SATn}}\right)V_M = \left(V_{TN} + \frac{V_{DS,SATn}}{2}\right) - \frac{\beta_P V_{DS,SATp}}{\beta_N V_{DS,SATn}}\left(V_{DD} + V_{TP} + \frac{V_{DS,SATp}}{2}\right)$$

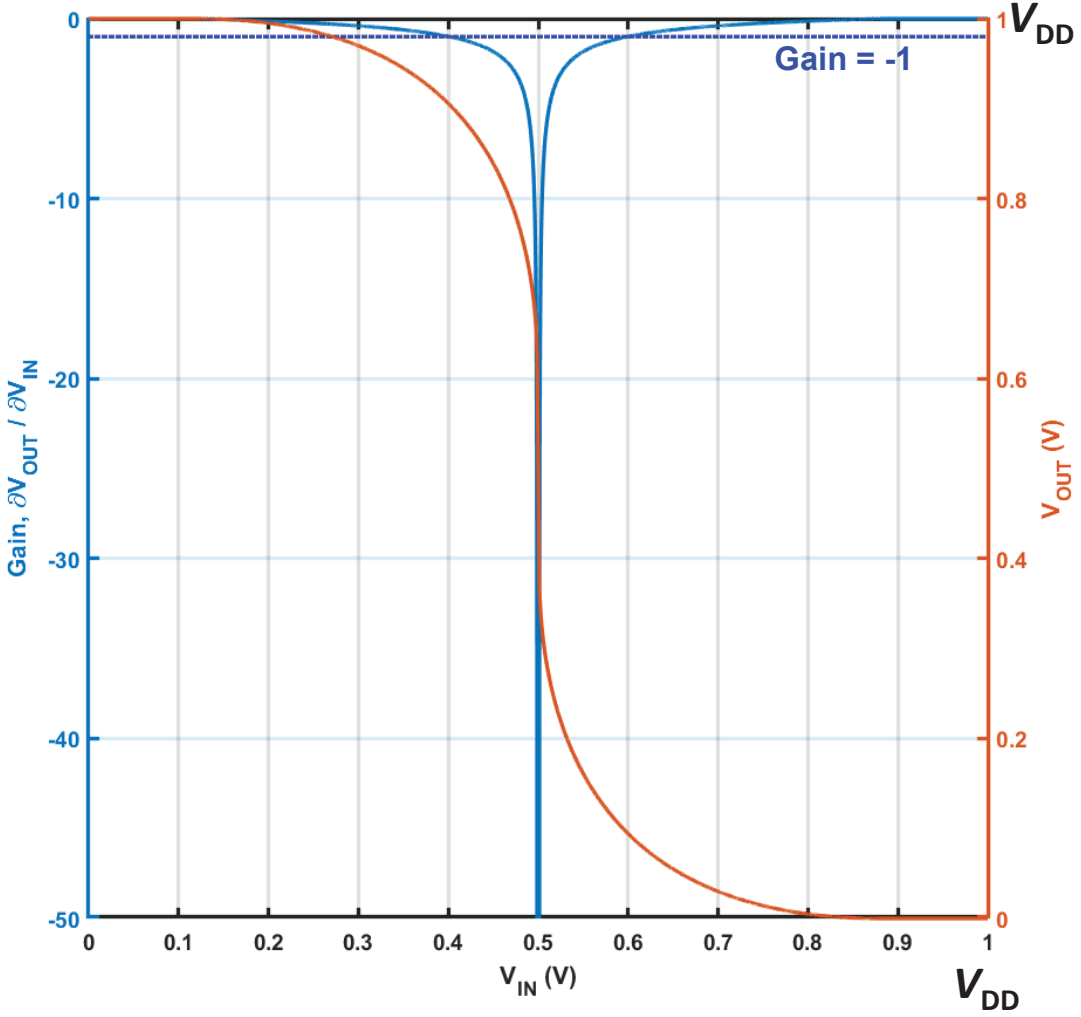
$$V_M = \frac{\left(V_{TN} + \frac{V_{DS,SATn}}{2}\right) + r\left(V_{DD} + V_{TP} + \frac{V_{DS,SATp}}{2}\right)}{1 + r}; r = \frac{-\beta_P V_{DS,SATp}}{\beta_N V_{DS,SATn}} = \frac{-\mu_p (W_P/L_P) V_{DS,SATp}}{\mu_n (W_N/L_N) V_{DS,SATn}}$$

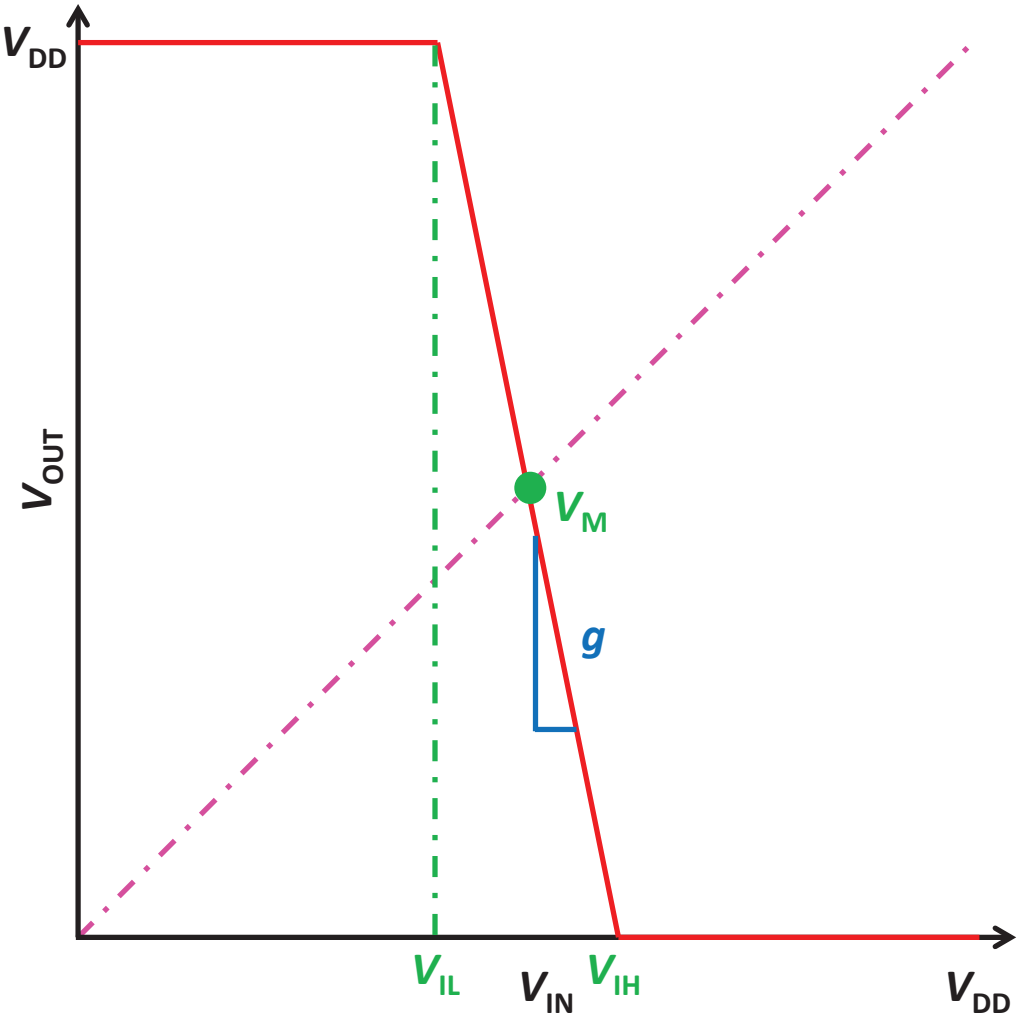
Relationship Between V_M and β-ratio

$$\beta\text{−ratio} = \frac{\beta_P}{\beta_N} = r \text{ for when } \left|\frac{V_{DS,SATp}}{V_{DS,SATn}}\right| = 1$$



Approximating the VTC





Approximating the VTC - II

Piecewise linear approximation to VTC

$$g = \frac{V_{DD}}{V_{IL} - V_{IH}} = \frac{V_M}{V_M - V_{IH}} = \frac{V_{DD} - V_M}{V_{IL} - V_M} < 0$$

$$\Longrightarrow V_{IH} = V_M - \frac{V_M}{g}$$

$$\Longrightarrow V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

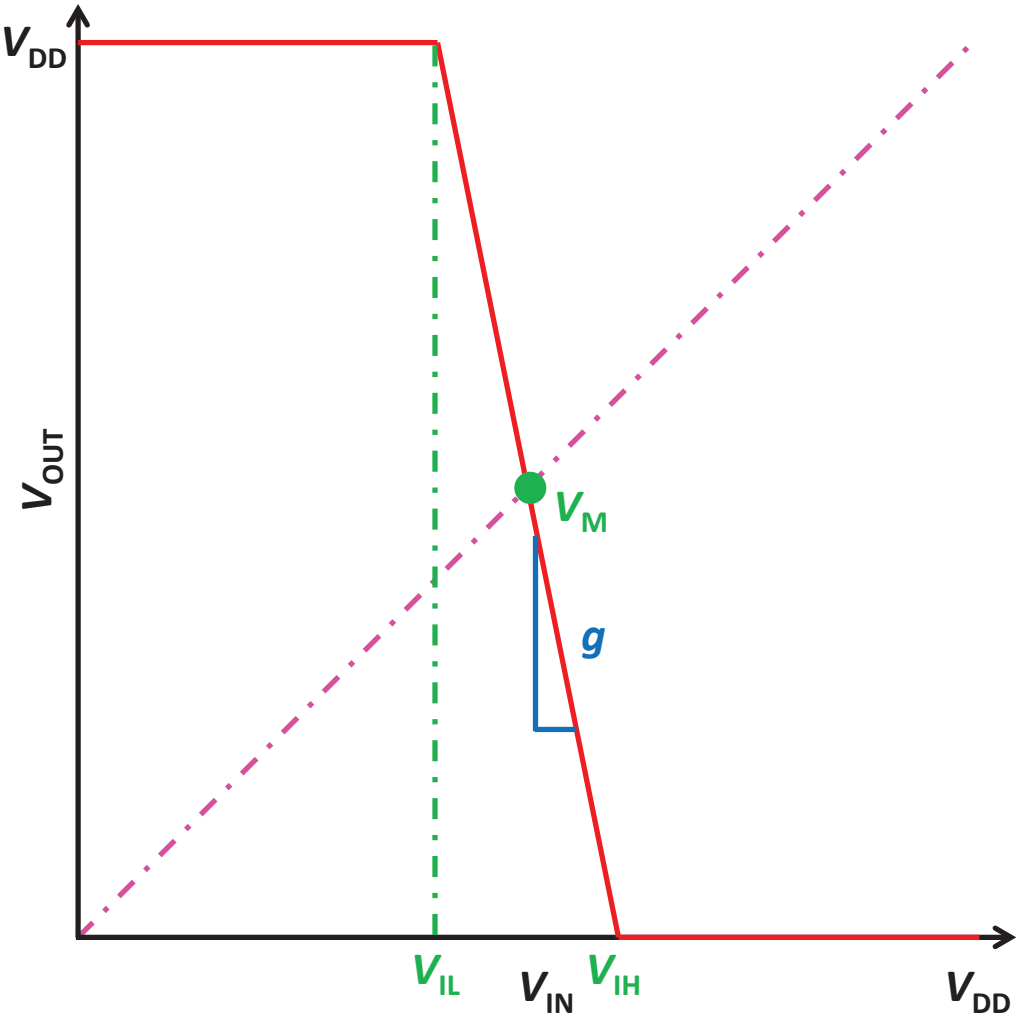
Peak gain occurs at $\boldsymbol{V_M}$,

$$g(V_M) = \left.\frac{\partial V_{OUT}}{\partial V_{IN}}\right|_{V_{IN}=V_M}$$

$$= \frac{-1}{I_D(V_M)} \cdot \frac{\beta_N V_{DS.SATn} - \beta_P V_{DS,SATp}}{\lambda_N - \lambda_P}$$

$$\approx -\frac{1 - r}{\left(V_M - V_{TN} - \frac{V_{DS,SATn}}{2}\right)(\lambda_N - \lambda_P)}$$

Peak gain is mostly determined by channel length modulation



Gain and Noise Margins

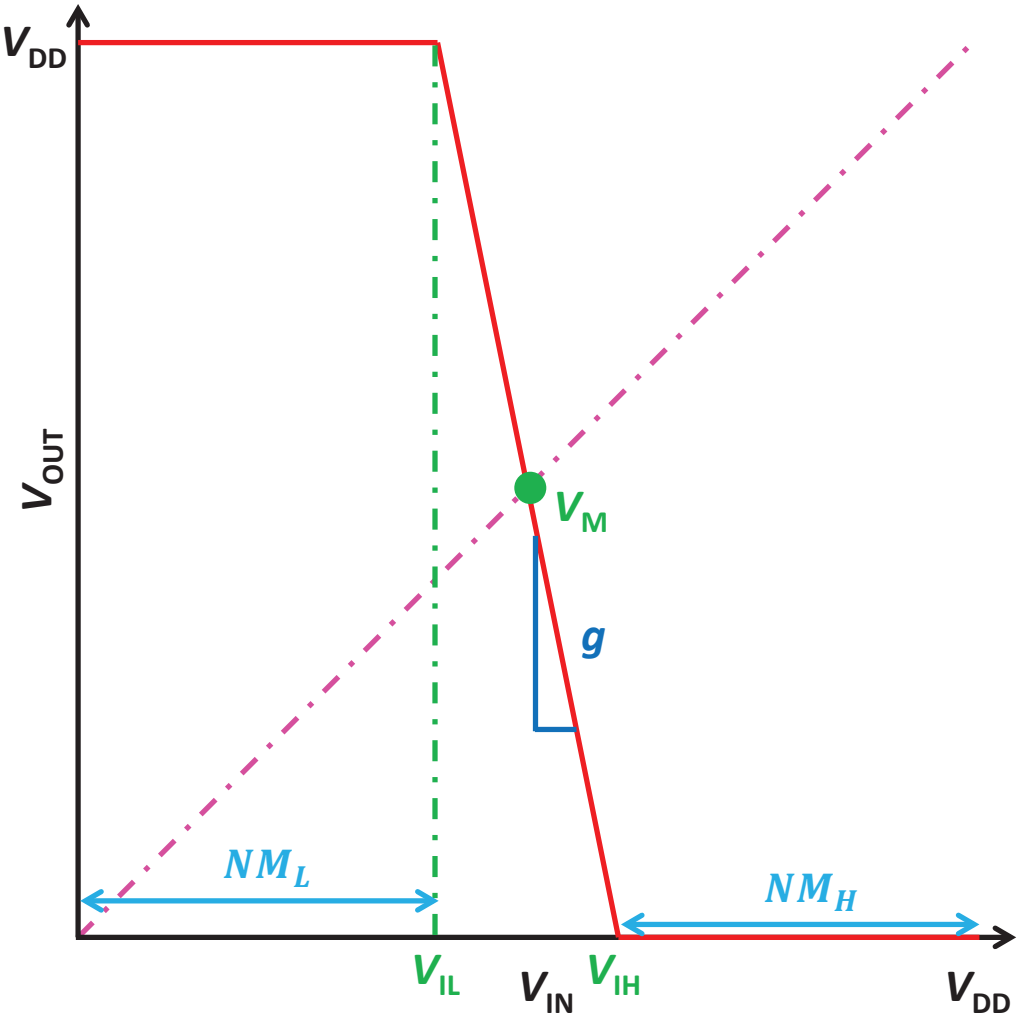
Noise margins are defined as

$$NM_L = V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

$$NM_H = V_{DD} - V_{IH} = V_{DD} - V_M + \frac{V_M}{g}$$

$$NM_L + NM_H = V_{DD} + \frac{V_{DD}}{g}$$

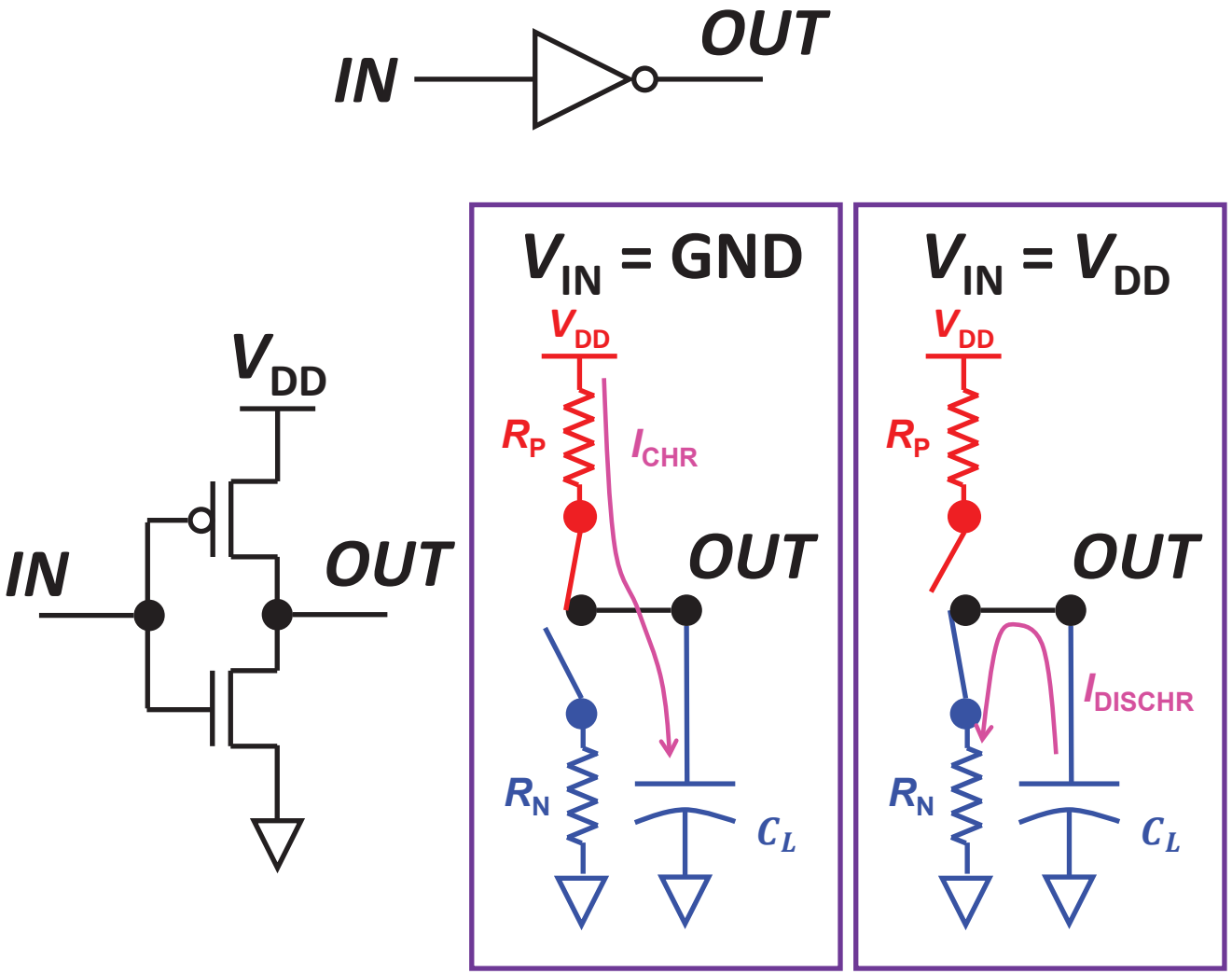
Since $g < 0$, want g to be as negative as possible (maximize magnitude) to maximize noise margin!



Week 2-7

Dynamic Response of the Static CMOS Inverter – Timing

Dynamic Response of the Static CMOS Inverter



- Dynamic response: the transient (time-dependent) change of V_{OUT} when V_{IN} is changed
- Analyze using switch model of MOSFET
  - C_L models the capacitances due to the MOSFET junction, inputs of other logic gates, interconnect wiring, etc.
  - When V_{IN} = **GND**, C_L is charged through PMOS channel (R_P)
    - Propagation delay, t_{pLH}

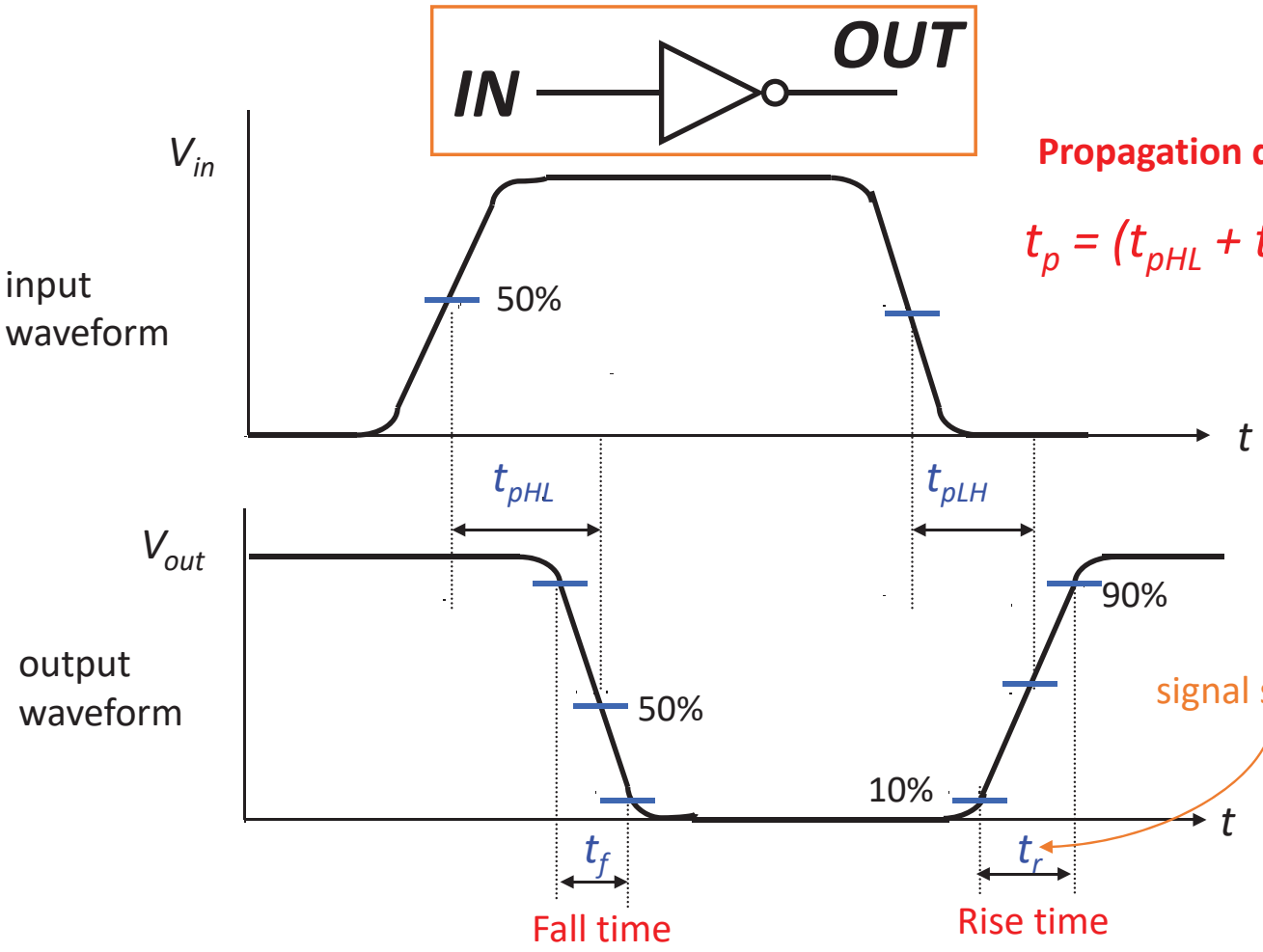
$$t_{pLH} = \gamma R_P C_L$$

  - When $V_{IN} = V_{DD}$, C_L is discharged through NMOS channel (R_N)
    - Propagation delay, t_{pHL}

$$t_{pHL} = \gamma R_N C_L$$

γ depends on our definition of propagation delay (when to stop)

Delay Definitions



Propagation delay:

$$t_p = (t_{pHL} + t_{pLH})/2$$

$\gamma = \ln(2)$ if propagation delay is measured with respect to 50% point

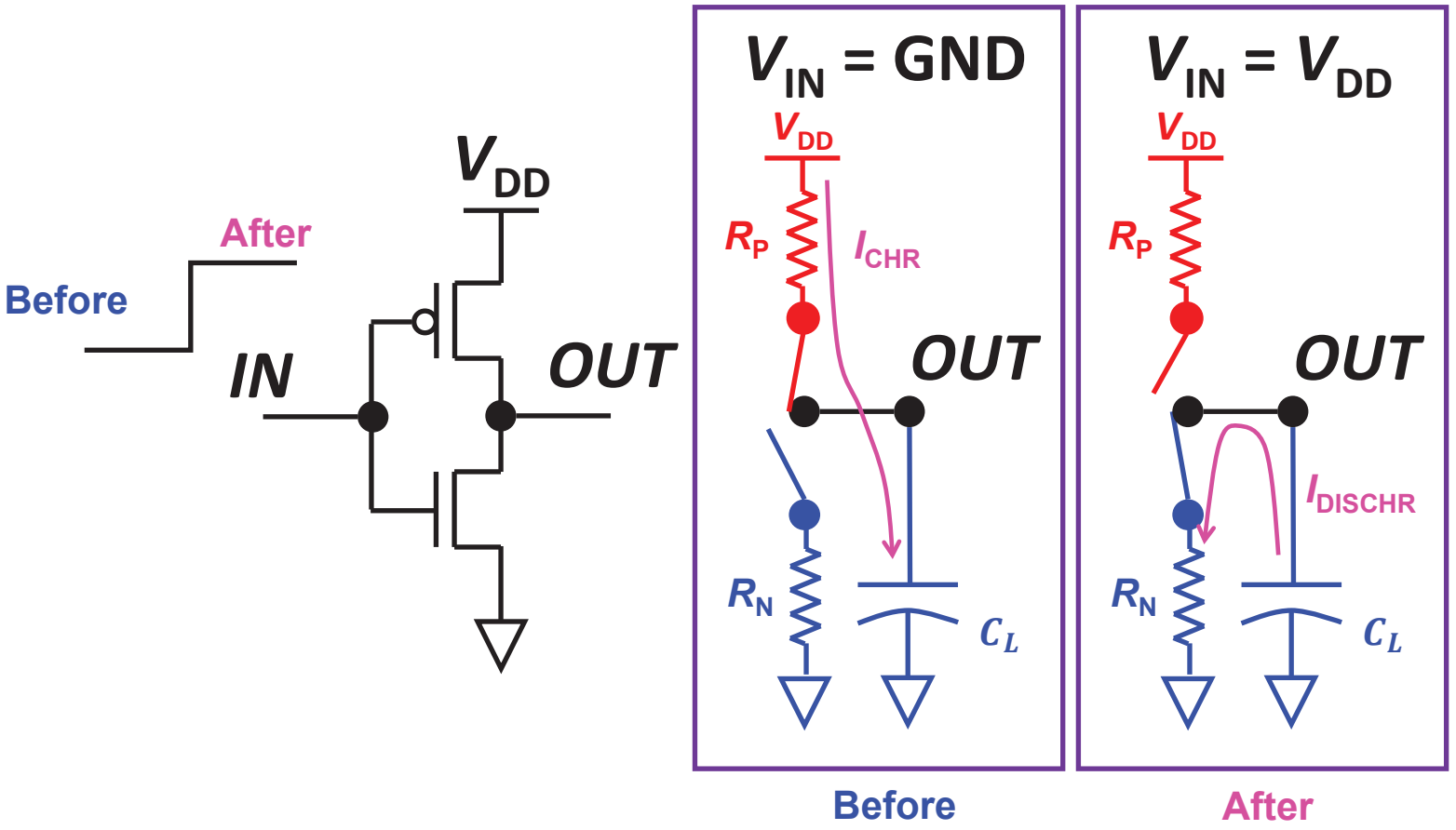
$$\gamma = \ln(2) = 0.69$$

$$t_{pLH} = 0.69 R_P C_L$$

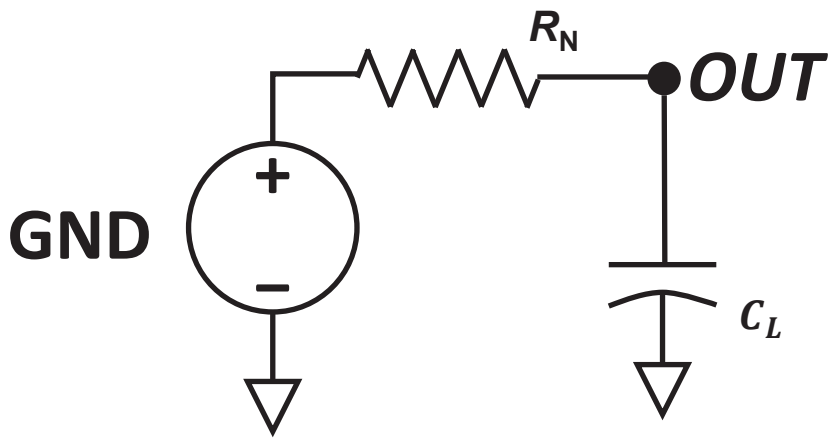
$$t_{pHL} = 0.69 R_N C_L$$

$$t_p = 0.69 \left(\frac{R_N + R_P}{2} \right) C_L$$

t_{pHL} of the Static CMOS Inverter



t_{pHL} of the Static CMOS Inverter



$$V_{OUT}(t) \approx V_{DD} \exp(-t/R_N C_L)$$

To get t_{pHL}, need time when

$$\frac{V_{OUT}(t_{PHL})}{V_{DD}} = \exp(-t_{pHL}/R_N C_L) = 0.5$$

$$t_{pHL} = 0.69 R_N C_L$$

- At $t = 0$
  - $V_{OUT}\ (t = 0) = V_{DD}$
  - $V_{GND} = 0$ V
  - $I_{C,L} = (V_{GND} - V_{OUT})/R_N = -V_{OUT}/R_N$
- For any capacitor
  - $i_c = C\frac{dv_c}{d\tau}$
- After equating the two we get:

$$C_L\frac{dv}{d\tau} = -\frac{v}{R_N}$$

- Rearranging,

$$\frac{1}{v}dv = \frac{-1}{R_N C_L}d\tau$$

- Integrating both sides,

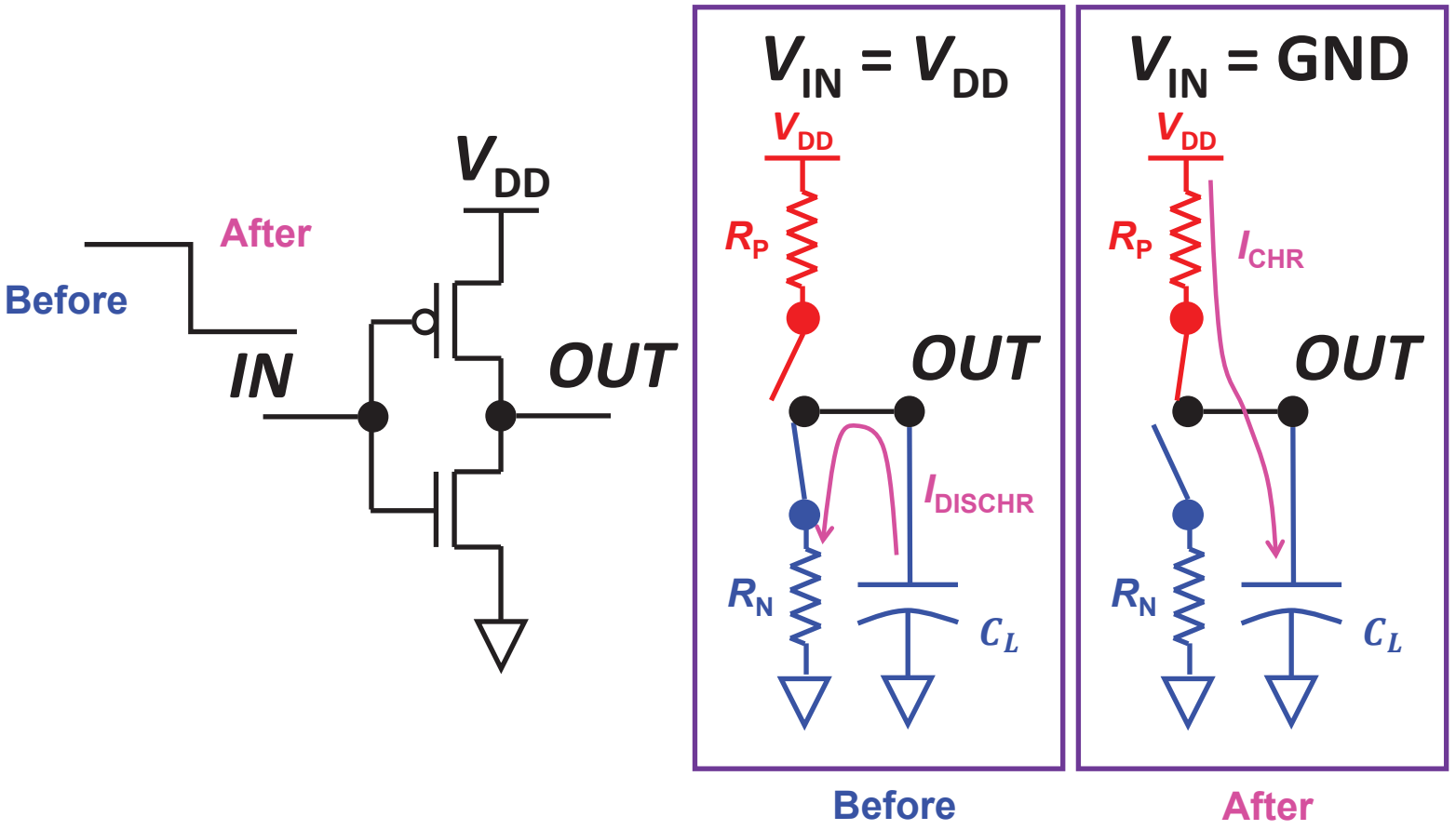
$$\int_{V_{DD}}^{V_{OUT}} \frac{1}{v}dv = \int_0^t \frac{-1}{R_N C_L}d\tau$$

- After integration,

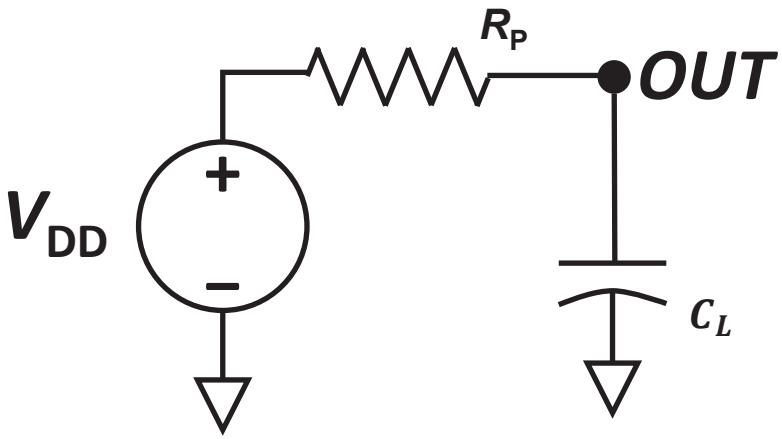
$$\ln(V_{OUT}) - \ln(V_{DD}) = \frac{-t}{R_N C_L}$$

$$\ln\left(\frac{V_{OUT}}{V_{DD}}\right) = \frac{-t}{R_N C_L}$$

t_{pLH} of the Static CMOS Inverter



t_{pLH} of the Static CMOS Inverter



$$V_{OUT}(t) \approx V_{DD}\left(1 - \exp\left(-\frac{t}{R_P C_L}\right)\right)$$

To get t_{pLH}, need time when

$$\frac{V_{OUT}(t_{pLH})}{V_{DD}} = \left(1 - \exp\left(-\frac{t_{pLH}}{R_P C_L}\right)\right) = 0.5$$

$$\boxed{t_{pLH} = 0.69 R_P C_L}$$

- Voltage of Node ***OUT*** at ***t*** = 0
  - $V_{OUT}\,(t = 0) = V_{GND}$
  - $I_{C,L} = (V_{DD} - V_{OUT})/R_P$
- For any capacitor
  - $i_c = C\frac{dv_c}{d\tau}$
- After equating the two we get:

$$C_L\frac{dv}{d\tau} = \frac{V_{DD} - v}{R_P}$$

- Rearranging,

$$\frac{1}{v - V_{DD}}dv = \frac{-1}{R_P C_L}d\tau$$

- Integrating both sides,

$$\int_0^{V_{OUT}} \frac{1}{v - V_{DD}}dv = \int_0^{t} \frac{-1}{R_P C_L}d\tau$$

- After integration,

$$\ln(V_{OUT} - V_{DD}) - \ln(-V_{DD}) = \frac{-t}{R_P C_L}$$

$$\ln\left(\frac{V_{DD} - V_{OUT}}{V_{DD}}\right) = \frac{-t}{R_P C_L}$$

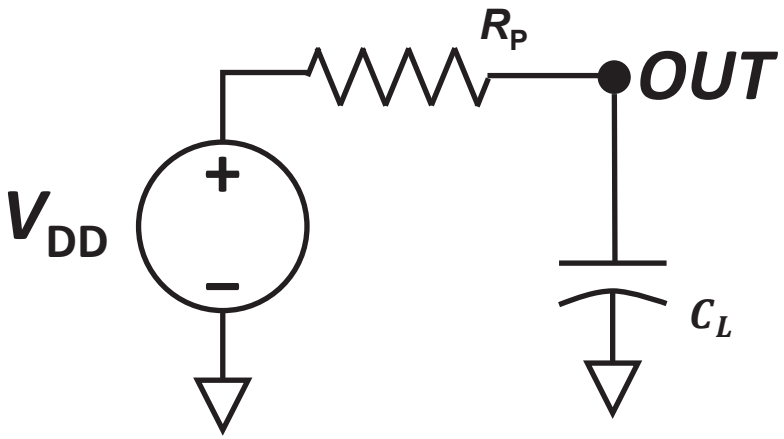
Common Design Requirements

- Balanced propagation delay
  - Design for $\boldsymbol{t_{pLH}} = \boldsymbol{t_{pHL}}$ (*i.e.*, $0.69\boldsymbol{R_N C_L} = 0.69\boldsymbol{R_P C_L}$); achieved by setting ($\boldsymbol{R_N} = \boldsymbol{R_P}$)
  - Since $\frac{R_P}{R_N} \propto \frac{(W_N/L_N)}{(W_P/L_P)}$, we achieve this by adjusting the aspect ratio (W/L ratio) of the MOSFETs
- Fastest speed (*i.e.*, smallest delay)
  - Reduce C_L
    - internal diffusion capacitance of the gate itself
      - keep the drain diffusion as small as possible
    - interconnect capacitance
    - fanout
  - Increase W/L ratio of the transistors
    - the most powerful and effective performance optimization tool in the hands of the designer
    - watch out for self-loading! – when the intrinsic capacitance dominates the extrinsic load
    - may come increase input capacitance which loads the gate that generates the input signal
  - Increase V_{DD}
    - trade-off energy for performance
    - increasing V_{DD} above a certain level yields only very minimal improvements
    - reliability concerns enforce a firm upper bound on V_{DD}

Week 2-8

Power Consumption of the Static CMOS Inverter

t_{pLH} of the Static CMOS Inverter



$$V_{OUT}(t) \approx V_{DD}\left(1 - \exp\left(-\frac{t}{R_P C_L}\right)\right)$$

To get t_{pLH}, need time when

$$\frac{V_{OUT}(t_{pLH})}{V_{DD}} = \left(1 - \exp\left(-\frac{t_{pLH}}{R_P C_L}\right)\right) = 0.5$$

$$\boxed{t_{pLH} = 0.69 R_P C_L}$$

- Voltage of Node ***OUT*** at ***t*** = 0
  - $V_{OUT}\,(t = 0) = V_{GND}$
  - $I_{C,L} = (V_{DD} - V_{OUT})/R_P$
  - $V_{GND} = 0$ V
  - $I_{C,L} = -V_{OUT}/R_P$
- For any capacitor
  - $i_c = C\frac{dv_c}{d\tau}$
- After equating the two we get:

$$C_L\frac{dv}{d\tau} = \frac{V_{DD} - v}{R_P}$$

- Rearranging,

$$\frac{1}{V_{DD} - v}dv = \frac{-1}{R_P C_L}d\tau$$

- Integrating both sides,

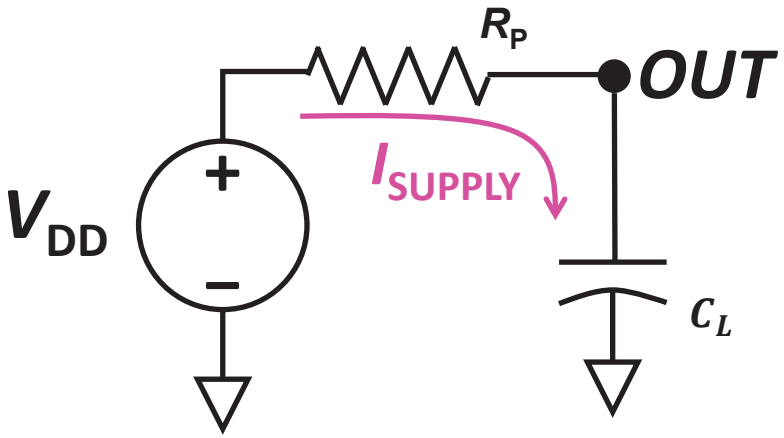
$$\int_0^{V_{OUT}} \frac{1}{V_{DD} - v}dv = \int_0^{t} \frac{-1}{R_P C_L}d\tau$$

- After integration,

$$\ln(V_{DD} - V_{OUT}) - \ln(V_{DD}) = \frac{-t}{R_P C_L}$$

$$\ln\left(\frac{V_{DD} - V_{OUT}}{V_{DD}}\right) = \frac{-t}{R_P C_L}$$

Power Consumption of Static CMOS Inverter (0→1)



$$I_{SUPPLY}(t) = I_C(t) \approx \frac{V_{DD}}{R_P} \exp\left(-\frac{t}{R_P C_L}\right)$$

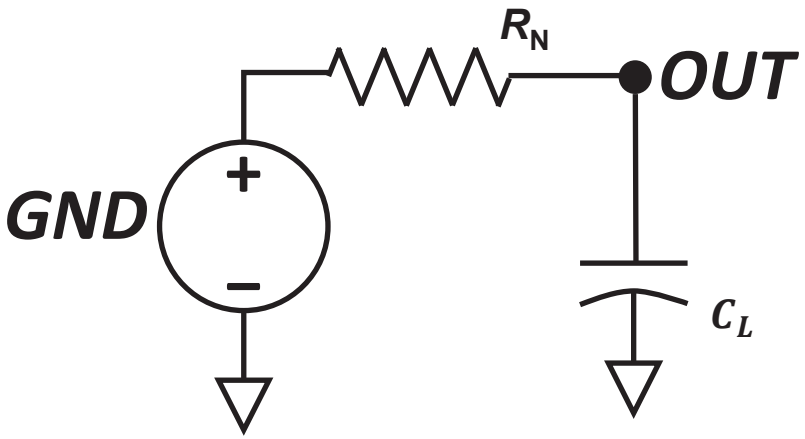
- Power supplied:
  - $V_{DD} \times I_{SUPPLY} = V_{DD} \times I_C$
- Energy supplied:
  - $\int_0^{+\infty} V_{DD} I_C \; d\tau$
- Substituting I_C,

$$\int_0^{+\infty} \frac{V_{DD}^2}{R_P} exp\left(-\frac{\tau}{R_P C_L}\right) d\tau$$

$$-\frac{V_{DD}^2 R_P C_L}{R_P} exp\left(-\frac{\tau}{R_P C_L}\right)\Bigg|_0^{+\infty}$$

$$E_{SUPPLY} = C_L V_{DD}^2$$

Power Consumption of Static CMOS Inverter (1→0)



- Power supplied:
  - $V_{DD} \times I_{SUPPLY}$
- No current is flowing from V_{DD} supply source and so no energy is drawn from power supply

$$E_{SUPPLY} = 0$$

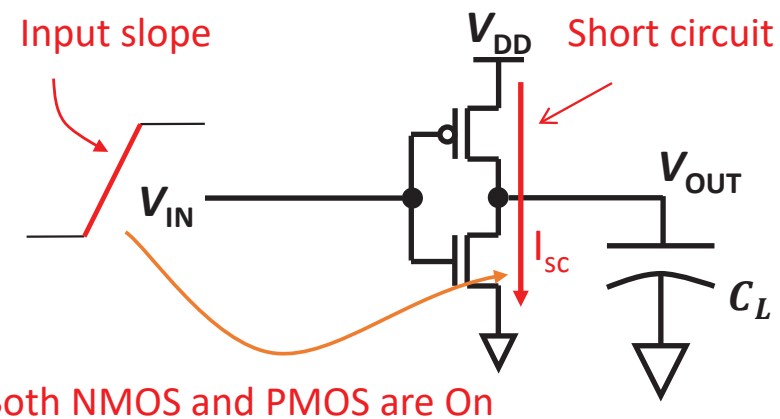
Dynamic Power Dissipation

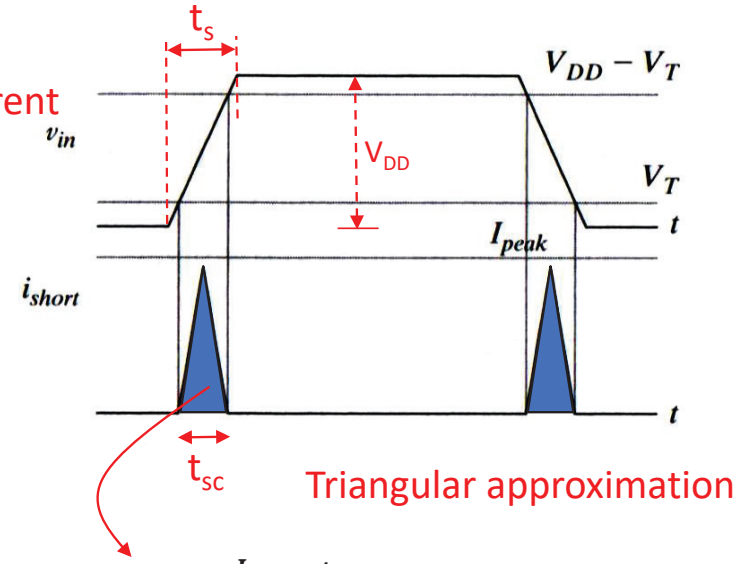
- During 0→1 transition (output node charged to $\boldsymbol{V_{DD}}$)
  - Total supplied = $\boldsymbol{C_L V_{DD}^2}$
  - Stored in load capacitor = $0.5\boldsymbol{C_L V_{DD}^2}$
  - Energy loss = $0.5\boldsymbol{C_L V_{DD}^2}$
- During 1→0 transition (output node discharged to **GND**)
  - Total supplied = 0
  - Stored in load capacitor = 0
  - Energy loss = $0.5\boldsymbol{C_L V_{DD}^2}$
- Energy is consumed by circuit (*i.e.* taken from power supply) only when there is 0→1 transition
- Dynamic/active Power = rate of energy consumption = $\boldsymbol{C_L V_{DD}^2 f_{0\to1}}$

$$= \boldsymbol{\alpha_{0\to1} C_L V_{DD}^2 f_{clk}}$$

$\boldsymbol{f_{clk}}$: operating frequency $\boldsymbol{\alpha_{0\to1}}$: activity factor (probability of 0→1 transition)

Short Circuit Power Dissipation





$$E_{sc} = V_{DD} \cdot \int_0^{t_{sc}} I_{sc}(t)dt \quad \Rightarrow P_{sc} = V_{DD} \cdot f \cdot \int_0^{t_{sc}} I_{sc}(t)dt$$

$$E_{sc} \approx 2V_{DD}\frac{I_{peak}t_{sc}}{2} = V_{DD}I_{peak}t_{sc}$$

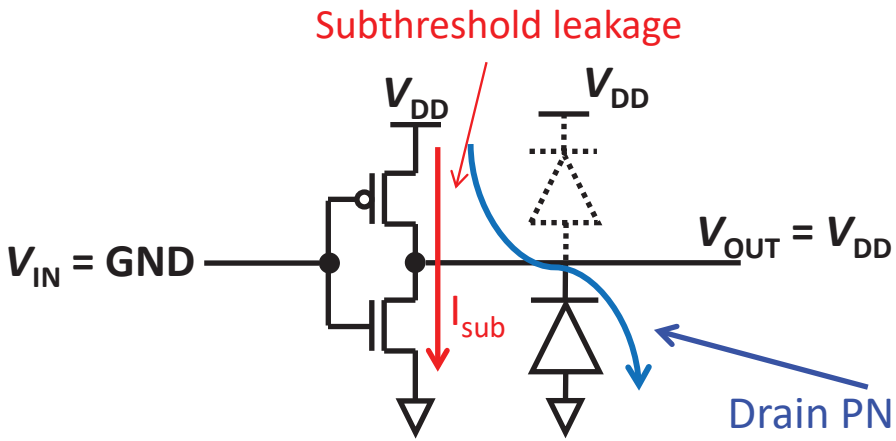
$$\boxed{P_{sc} = V_{DD}I_{peak}t_{sc}f}$$

$$Q_{sc} = \frac{I_{peak}t_{sc}}{2}$$

$$E_{sc} = 2V_{DD}Q = 2V_{DD}\frac{I_{peak}t_{sc}}{2} = V_{DD}I_{peak}t_{sc}$$

→ **P_{SC} is reduced when (1) V_{DD}, (2) t_{sc} and (3) *f* are lowered**

Static (Leakage) Power Dissipation

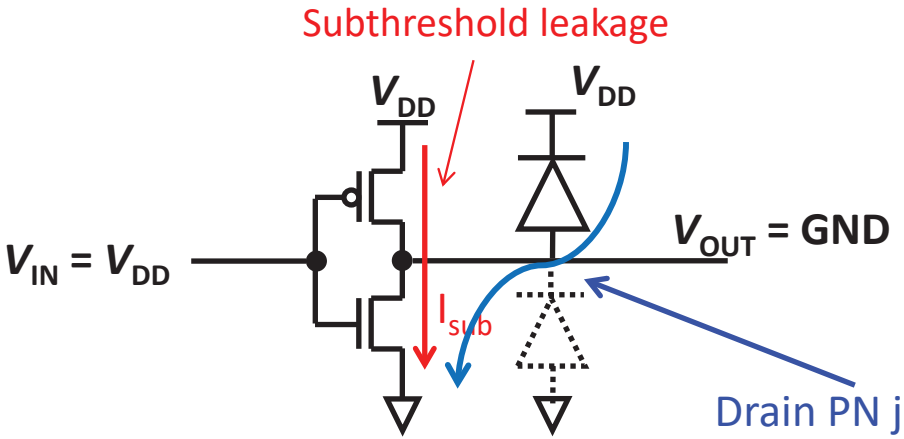


→ Static power consumption is caused by the leakages from V_{DD} to GND

- Leakage in CMOS includes drain/source to substrate/well junction leakage current and sub-threshold current;
- The P_{static} is

$$P_{static} = I_{stat} V_{DD} = (I_{junc} + I_{sub}) V_{DD}$$

Static (Leakage) Power Dissipation



→ Static power consumption is caused by the leakages from V_{DD} to GND

- Leakage in CMOS includes drain/source to substrate/well junction leakage current and sub-threshold current;
- The P_{static} is

$$P_{static} = I_{stat} V_{DD} = (I_{junc} + I_{sub}) V_{DD}$$

Threshold Voltage and Sub-threshold Leakage Current

- The sub-threshold slope, *S*:

$$I_D \propto e^{q(V_{GS}-V_{TH})/nk_BT}$$

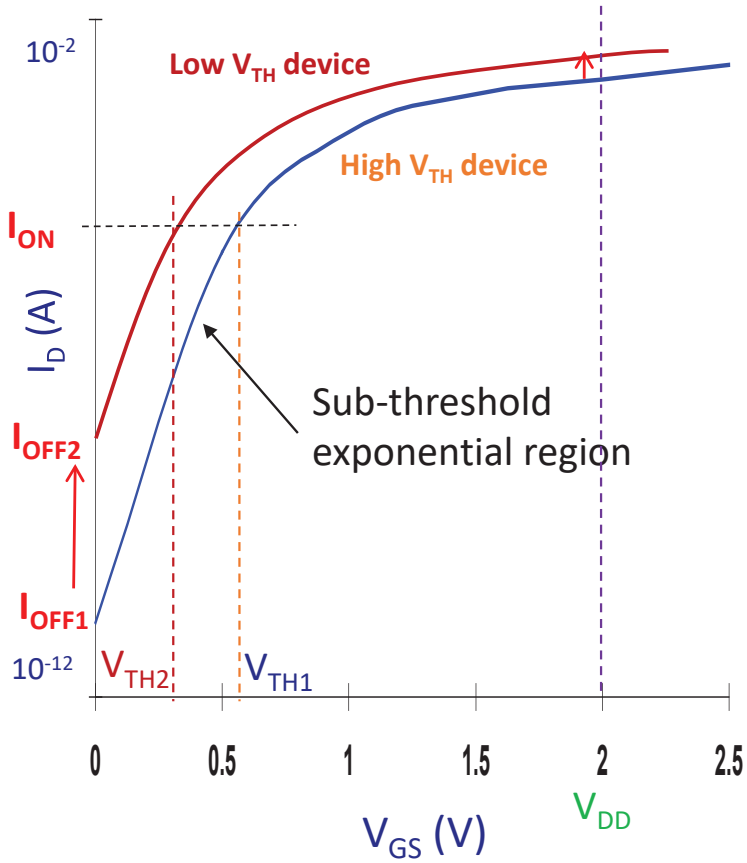
$$\boldsymbol{ln\, I_D = \text{constant} + \frac{V_{GS}}{n(k_BT/q)}}$$

$$\boldsymbol{log_{10}\, I_D = \text{constant} + \frac{V_{GS}}{2.3n(k_BT/q)}}$$

$$\boldsymbol{\frac{\partial(log_{10} I_D)}{\partial V_{GS}} = \frac{1}{2.3n(k_BT/q)} \ \frac{\text{decades of } I_D}{\text{Volts of } V_{GS}}}$$

$$\boldsymbol{S = \left(\frac{\partial(log_{10} I_D)}{\partial V_{GS}}\right)^{-1} = 2.3n\left(\frac{k_BT}{q}\right) \frac{\text{mV}}{\text{dec}}}$$

$$\boldsymbol{S \approx \begin{cases} 60 \text{ mV/dec when } n = 1 \\ 90 - 120 \text{ mV/dec, typically} \end{cases}}$$



e.g. Assuming ***S*** = 75mV / decade (fixed), reducing $\boldsymbol{V_{TN}}$ from 0.4 V to 0.1 V ($\boldsymbol{\Delta V_{TN}}$ = -0.3 V) can lead to **~10^4 times higher** sub-threshold leakage current