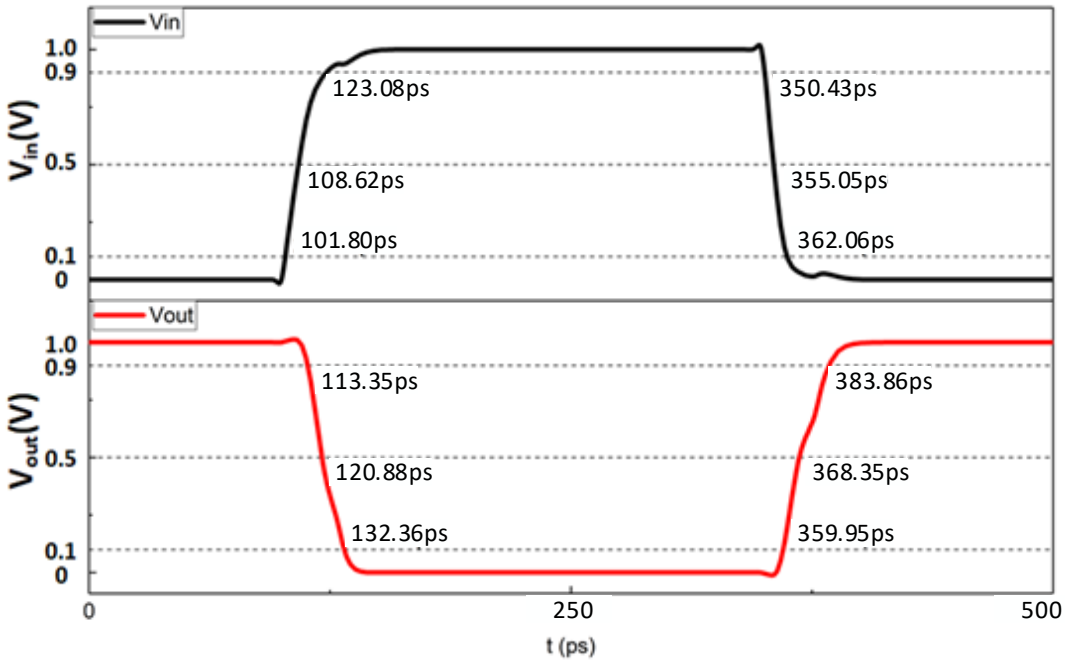
National University of Singapore
Electrical and Computer Engineering

CG2027 (Transistor-Level Digital Circuits)
Assignment #1 Solution

AY21/22 Semester 1
Issued: Aug. 10, 2021 Due: Aug. 15, 2021 (18:00)

Problem 1: Delay Calculation

The objective of this problem is to figure out correct delay / risetime / falltime of a CMOS inverter, based on the information given from the waveform.



a) What is the rise time (t_r), fall time (t_f) of the output waveform V_{out}?

➔ t_r =383.86-359.95 = 23.92 (ps), t_f =132.36 –113.35 = 19.01 (ps)

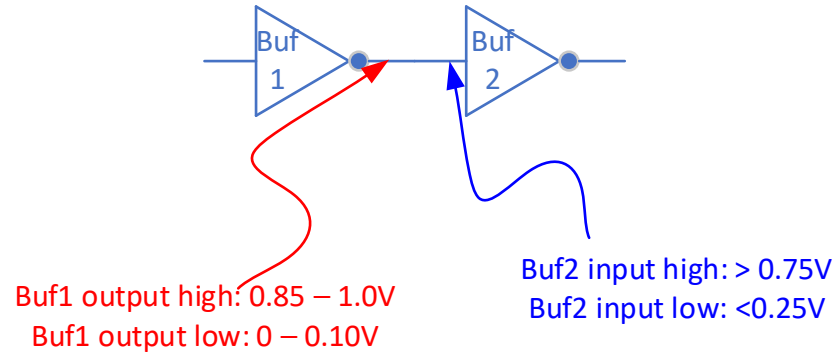
b) What is the high-to-low propagation delay (t_{pHL}) of the logic? ➔ t_{pHL} =120.88 – 108.62= 12.26 (ps)

c) What is the low-to-high propagation delay (t_{pLH}) of the logic? ➔ t_{pLH} = 368.35 – 355.05= 13.30 (ps)

d) If the given waveform is the half of the clock cycle with 50% duty, what is the clock frequency?

➔ You can choose any half-clock cycle points. E.g., 350.43-101.80 = 248.63ps (half cycle), 2 ×248.63ps ≈ 0.5ns (1 cycle). Therefore, the clock freq is approx. **2GHz** (note: ±5% difference is allowed)

Problem 2: Noise Margin



a) For the inverter chain given above, calculate the noise margin high (NM_H) and noise margin low (NM_L).

➔ $NM_H = |V_{OH1} - V_{IH2}| = |0.85 - 0.75| = 0.10$ (V)

➔ $NM_L = |V_{OL1} - V_{IL2}| = |0.10 - 0.25| = 0.15$ (V)

b) What happens if input high and input low of the Buf2 become the same? Explain.

➔ Noise margin high and noise margin low will be maximized.