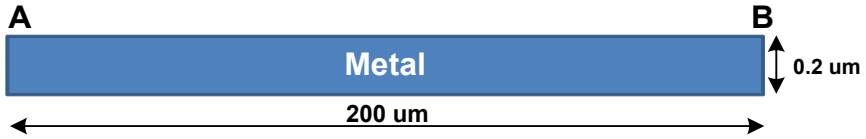
National University of Singapore
Electrical and Computer Engineering

CG2027 (Transistor-Level Digital Circuits)
Assignment #2

AY21/22 Semester 1
Issued: Aug. 17, 2021 Due: Aug. 22, 2021 (18:00)

Problem 1: Load Estimate (Capacitance and Resistance)

We assume a wire length of 200um, and width of 0.2um.



a) Calculate the value of C_{wire} for the wire segment A to B of the metal. Assume area capacitance is 19 AF/um2, and fringe capacitance is 61 AF/um.

b) Calculate the value of R_{wire} for the segment A to B. Assume the sheet resistance of the metal is given as 0.04/□.

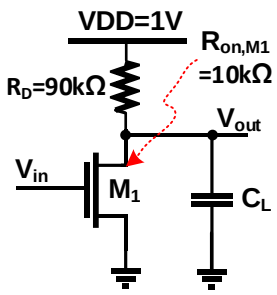
Problem 2: Propagation Delay and IR Drop

a) For the wire given in Problem 1, assuming 4mA of current is flowing through the segment, what is the IR drop?

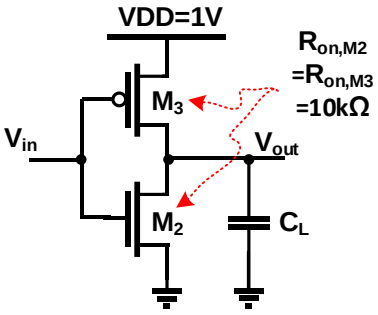
b) If a voltage source with 50Ω output impedance is driving this wire segment, what is the propagation delay t_p?

Problem 3: Inverter Output Voltage

We assume two inverters: (a) an NMOS inverter with pull-up resistor, and (b) a CMOS inverter, as shown below. Assume the on resistance of all the transistors (M1-M3) is 10kΩ.



(a) NMOS inverter with pull-up resistor



(b) CMOS inverter

a) For the NMOS inverter shown in the figure 3 (a), what is the steady-state V_{out} value when V_{in}=0V and 1V, respectively?

b) For the CMOS inverter shown in Fig. 3(b), what is the steady-state V_{out} value when V_{in}=0V and 1V, respectively?