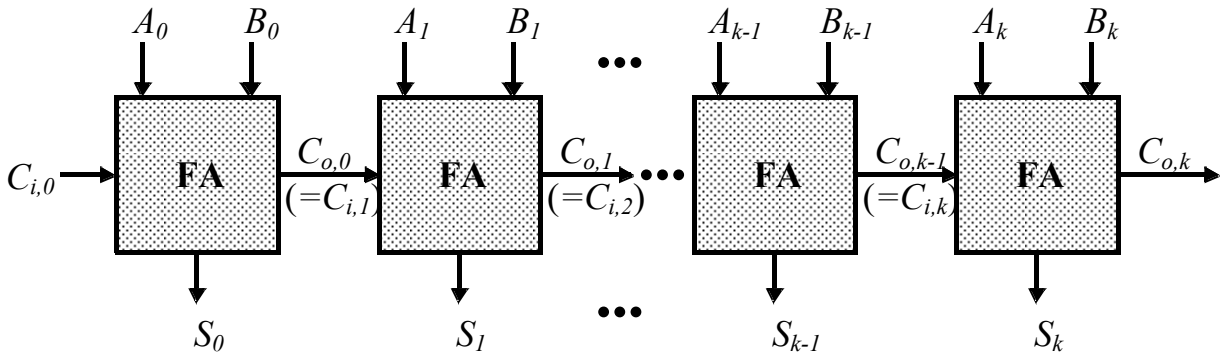
National University of Singapore
Electrical and Computer Engineering

CG2027 (Transistor-Level Digital Circuits)
Assignment #4

AY21/22 Semester 1
Issued: Aug. 31, 2021 Due: Sep. 05, 2021 (18:00)

Problem 1: Propagation delay of ripple-carry adder



Derive the values of A_k and B_k (k=0… N-1) so that the worst case delay is obtained for the ripple-carry adder shown above.

Problem 2: Ripple carry vs. Carry select adder

(a) Determine the worst-case delay of a 16-bit carry select adder. Assume $\boldsymbol{t_{setup}} = \boldsymbol{t_{sum}} = 2$, and $\boldsymbol{t_{carry}} = \boldsymbol{t_{mux}} = 1$. Compare this with the worst-case delay of a 16-bit ripple carry adder.

(b) If each stage has 4 bits, what is minimum number of bits (N) needed in order for the carry-select adder to start showing less delay than a ripple-carry adder? Assume $\boldsymbol{t_{setup}} = \boldsymbol{t_{sum}} = 2$, and $\boldsymbol{t_{carry}} = \boldsymbol{t_{mux}} = 1$.