National University of Singapore
Electrical and Computer Engineering

CG2027 (Transistor-Level Digital Circuits)
Assignment #5

AY21/22 Semester 1
Issued: Sep. 7, 2021 Due: Sep. 12, 2021 (18:00)

Problem 1: SRAM memory cell

In a SRAM cell shown in Fig. 1, assume all the transistors (M1 – M6) have the same unknown length (L), and M5, M6 have the width $W_{M5} = W_{M6} = 1\mu m$. Both BL and /BL are precharged to V_{DD}. Assume the on resistance (R_{on}) of a PMOS and a NMOS of the same width and length, are identical, $V_{th,NMOS} = |V_{th,PMOS}| = 0.4(V)$ and $V_{DD}=1(V)$.

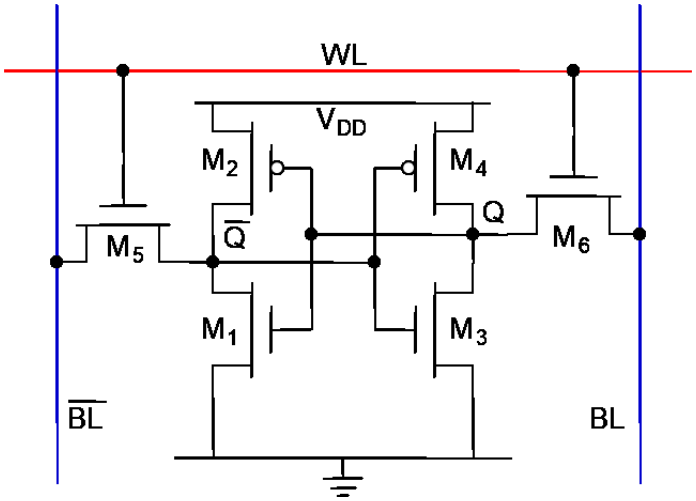

Figure 1. A SRAM cell

a) If Q = 1 and /Q =0 is currently stored in the SRAM cell, and we would like to read the data so that BL=1 and /BL=0 when WL is applied with "H", what should be the requirement (width) of M1 and M3? Why?

b) Now that W1 and W3 are determined from a). If Q = 1 and /Q =0 is currently stored in the SRAM cell, and we would like to write "Q=0, /Q=1" into the cell, then what is the requirement (width) of M2 and M4?

Problem 2: DRAM operation

In a 1T DRAM cell shown in Fig. 2, BL is precharged to $V_{BL} = V_{ccA}/2 = 1$ V, and C_S is initially discharged to GND. Assume $C_S = 20$fF, and C_{BL}=80fF and $V_{th,M1} = 0.4$V. There is NO sense amplifier attached to the BL.

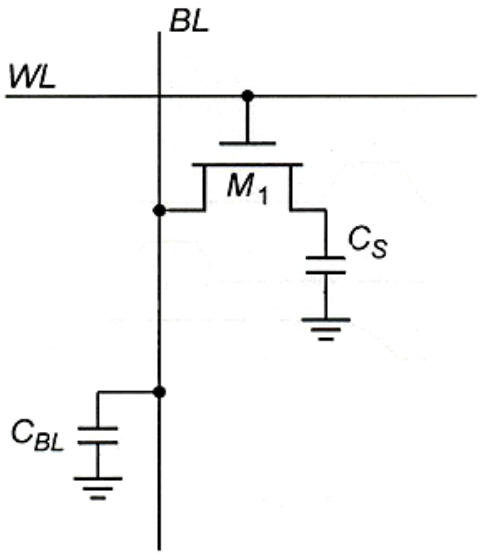

Figure 2. A 1T DRAM cell

(a) When WL is applied with V_{ccA}=2V, the access transistor M1 will turn on. At this point, will the final BL voltage (V_{Final}) increase or drop, compared with the precharge voltage? By how much (in mV)?

(b) We now want to write data "1" into C_S, by applying BL with V_{ccA}=2(V). If we apply WL with V_{ccA} (2V) to initiate the writing operation, is there any potential issue? If so, what is it? How can we avoid such issue?