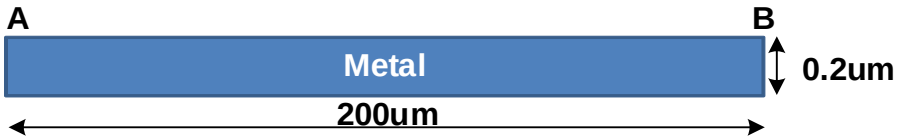
National University of Singapore
Electrical and Computer Engineering

CG2027 (Transistor-Level Digital Circuits)
Assignment #2 Solution

AY21/22 Semester 1
Issued: Aug. 17, 2021 Due: Aug. 22, 2021 (18:00)

Problem 1: Load Estimate (Capacitance and Resistance)

We assume a wire length of 200um, and width of 0.2um.



a) Calculate the value of C_{wire} for the wire segment A to B of the metal. Assume area capacitance is 19 aF/um^2, and fringe capacitance is 61 aF/um.

➔ Area Capacitance = (19 aF/um^2) * 200 um * 0.2 um = 0.76 fF

Fringe Capacitance= (61 aF/um) * 200 um * 2 = 24.4 fF

$C_{Total} = C_{Area} + C_{Fringe}$ = 0.76 fF + 24.4 fF = **25.16 fF**.

b) Calculate the value of R_{wire} for the segment A to B. Assume the sheet resistance of the metal is given as 0.04/□.

➔ Wire Resistance = (0.04 ohm/□) *200 um / 0.2um = **40 ohm**

Problem 2: Propagation Delay and IR Drop

a) For the wire given in Problem 1, assuming 4mA of current is flowing through the segment, what is the IR drop?

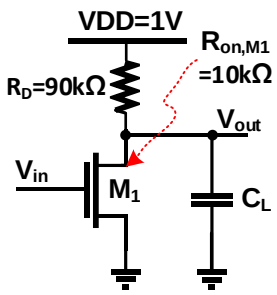
➔ IR drop = 4mA * 40 ohm = **160 (mV)**

b) If a voltage source with 50Ω output impedance is driving this wire segment, what is the propagation delay t_p?

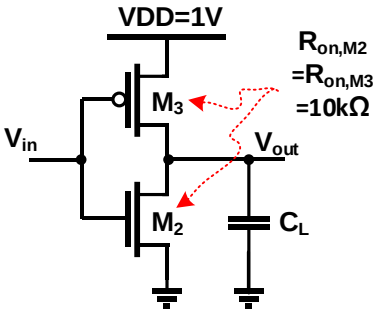
➔ t_p = 0.69RC = 0.69 * (50+40) ohm * 25.16*10^{-15} = **1.562 (ps)** (5% difference allowed)

Problem 3: Inverter Output Voltage

We assume two inverters: (a) an NMOS inverter with pull-up resistor, and (b) a CMOS inverter, as shown below. Assume the on resistance of all the transistors (M1-M3) is 10kΩ.



(a) NMOS inverter with pull-up resistor



(b) CMOS inverter

a) For the NMOS inverter shown in the figure 3 (a), what is the steady-state V_{out} value when V_{in}=0V and 1V, respectively?

➔ When V_{in} =0V, M1 is turned off, and V_{out} is charged to VDD=1(V) through R_D. Therefore, V_{out}=1(V).

➔ When V_{in} =1V, M1 is turned on, and a voltage divider is formed between R_D (90kΩ) and $R_{on,M1}$ (10kΩ). Therefore, V_{out}=1*(10k)/(10k+90k) = 0.1(V).

b) For the CMOS inverter shown in Fig. 3(b), what is the steady-state V_{out} value when V_{in}=0V and 1V, respectively?

➔ V_{in} =0V, M2 is turned off, and V_{out} is charged to VDD=1(V) through M3. Therefore, V_{out}=1(V).

➔ V_{in} =1V, M3 is turned off, and V_{out} is discharged to GND through M2. Therefore, V_{out}=0 (V).

Note the output voltage of the CMOS inverter is independent of the on resistance of M2 and M3.