National University of Singapore
Electrical and Computer Engineering

CG2027 (Transistor-Level Digital Circuits)
Tutorial #3 Solution

AY21/22 Semester 1
Assigned: Aug. 24, 2021 Due: Aug. 29, 2021 (18:00)

Problem 1: CMOS Logic

Consider the following CMOS logic circuits:

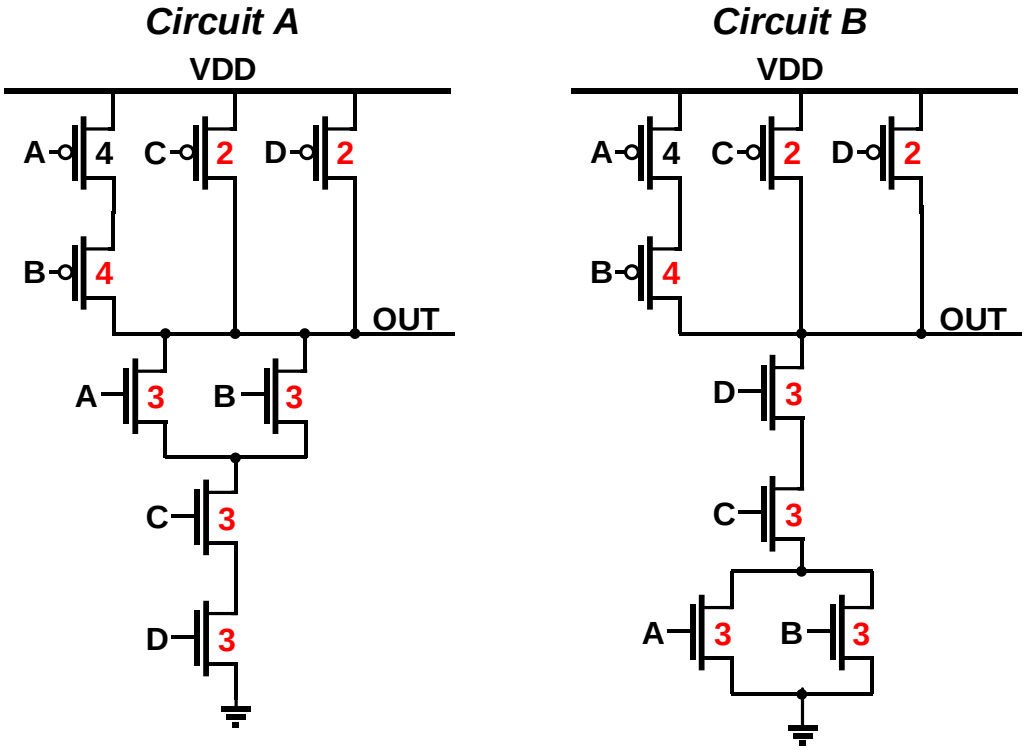


Figure 1: Two static CMOS gates.

a) Provide the Boolean expression for the circuits in **Figure 1** and show whether they implement the same logic function ➔ Yes, same function. $\overline{OUT} = (A + B) \cdot C \cdot D$

b) What is the appropriate transistor sizing for the logic circuit to have similar to 1X inverter delay? Fill in the empty boxes. Assume PMOS A has width of 4 (as shown above), and INV1X has W_{PMOS}:W_{NMOS} of 2:1.
➔ See the boxes above.

c) Assume the transistors have been sized to give a worst case output resistance of 12kohm in both pull-up and pull-down networks for the worst-case input patterns. What input patterns (A-D) give the lowest output resistance when the output is low? What is the value of that resistance?

➔ When output is low, the output resistance R_{OUT} is the lowest when ALL inputs are high, {A,B,C,D}={1,1,1,1}.

➔ $R_{OUT}= R_N+R_N+(R_N//R_N) = 12/3k + 12/3k + (12/3)/2k = 4k + 4k + 2k = 10k\Omega$.

d) What input patterns (A-D) give the lowest output resistance when the output is high? What is the value of that resistance?

➔ When output is high, the output resistance R_{OUT} is the lowest when ALL inputs are low, {A,B,C,D}={0,0,0,0}.

➔ $R_{OUT}= R_P// R_P // (1/2R_P+1/2R_P)= 12k // 12k // 12k = 4k\Omega$.

e) Neglecting parasitics and assuming a load capacitance of 100fF, calculate the best case t_{pLH} and t_{pHL}.

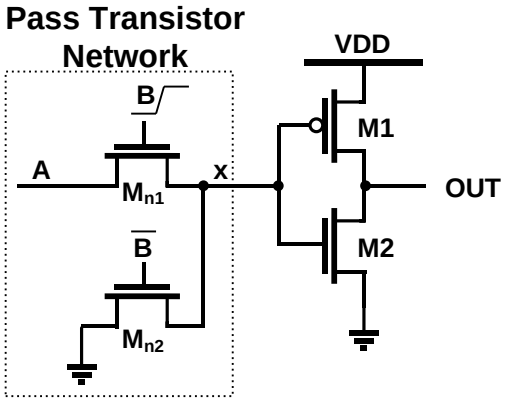
➔ Refer to the Lecture 2 slide 34.

➔ $t_{pLH,best} = 0.69 \cdot R_{PUN} \cdot C_L = 0.69 * 4k * 100f = 276$ (ps)

➔ $t_{pHL,best} = 0.69 \cdot R_{PDN} \cdot C_L = 0.69 * 10k * 100f = 690$ (ps)

Problem 2: Pass Transistor Logic and Level Restoration

Consider the circuits of **Figure 2**. Assume the inverter of M1 and M2 switches ideally at VDD/2, neglect body effect, channel length modulation and all parasitic capacitances throughout this problem. Use the parameters in the Table for NMOS and PMOS.



VDD =1.1V
$(W/L_{drawn})_2$ = 0.6um/45nm
$(W/L_{drawn})_1$ = 0.2um/45nm
$(W/L_{drawn})_{ni}$ = 0.2um/45nm

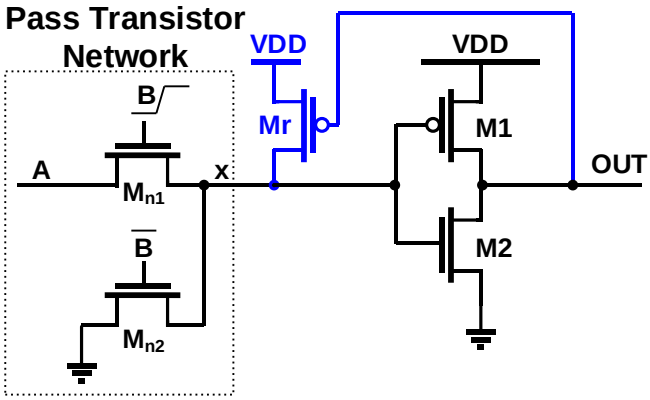
Figure 2: Level restoring circuit.

a) What is the logic function performed by this circuit?
➔ NAND: Pass Transistor Network performs AND, then followed by an inverter (by M1 and M2).

b) Explain why this circuit has non-zero static power dissipation?
➔ When A=B=1, the pass transistor Mn1 will pass only up to VDD-$V_{th,nmos}$ to the node X. This causes M1 to not completely turn off, and hence both M1 and M2 will be marginally on; static power will be dissipated.

c) Using only just 1 transistor, design a fix so that there will not be any static power dissipation. Explain how you chose the size of the transistor (use the parameters given above and show calculations).

➔ We can add M_r as shown below.



➔ Mr should be sized small enough so that Mn2 can pull the node x down to GND when B is 0. Mr conducts while switching which causes this problem to occur. As Mn2 is 0.6um/45nm, Mr could be 0.1um//45nm or even lower up to 45nm/45nm if allowed under design rules.

d) Replace the pass-transistor network in **Figure 2** with a pass transistor network that computes the following function: x=ABC at the node x. Assume you have the true and complementary versions of the three inputs A, B and C.

➔ Note below answer is an example. B, C high gives output A and is 1 if A=1. If B or C is low, one of M_{n2} or M_{n3} or both will pull output low. Other pass transistor logic that makes x=ABC out of A, B, C, /A, /B, /C will be also correct.