BASIC FABRICATION PROCESS

Basic Fabrication

- MOS device structure shown earlier is implemented in silicon with help of layout masks. The layout has mask names that usually indicate either a function or a material layer e.g. source/drain mask.
- Each of the process steps is depicted by its effect on Si wafer. The layout masks are 2D and hence a full view requires this mask and effect in 3D. However this is vary tedious and normally we only show 2D cross section along a line passing through 2D layout.
- These geometrical patterns on layout for each layer have to be transferred to Silicon. This is achieved by the lithography step in processing.
- The lithography is similar to photography process except it has an advance optical exposure system able to define nanometer size features needed for CMOS technology.

Basic Fabrication

- Actual mask sizes on layout are not transferred to silicon exactly and there is always variability which designers should consider in the design process.
- Similar variability also occurs for other processes such as amount of doping, junction depth of p or n region, etc.
- The normal step, which follows lithography, is selective removal of a material from the wafer from areas under mask regions called etching or selective doping to make Si n- or p-type.
- **Oxidation** is one of the most important steps in Silicon Processing as oxide can be used as
  - For isolating devices from each other,
  - as a dielectric for capacitance (gate oxide in MOSFET) or interlayer insulation, or
  - as a protective layer on Silicon against contamination.
- It is a high temperature process carried out in a furnace.

Basic Fabrication

- Ion implantation is a process of introducing impurity or other ions into Si for p- or n-type doping by giving them enough energy to penetrate into Si.

- Si wafer is heated to high temperature to overcome some side effects of ion implantation. This leads to dopant diffusion which increases the junction depth. This occurs from region of high concentration to low concentration.

- Both these processes introduce dopants vertically as well as laterally as shown in the figure below.

Basic Fabrication

- It is clear that, if source-drain separation is small, the junction depths must also be small as the lateral encroachment below can actually short source drain by making whole channel one doping type.
- For example, if the s-d separation is 100nm, we must choose junction depth such that they do not short i.e. highest allowed depth will be 50nm so that laterally dopants from both sides only enter 35nm from each side.

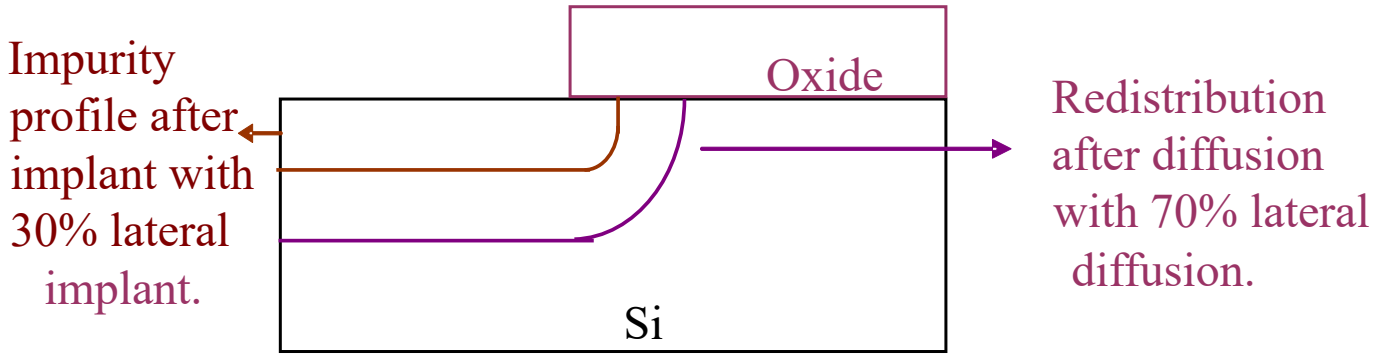


Figure : Redistribution of Implanted Impurities after diffusion

Process Sequence with Mask

- A common process sequence is normally done for each mask transfer to Si.
- It may involve

  Deposition

  Lithography (Exposure and Development)

  Selective Etching

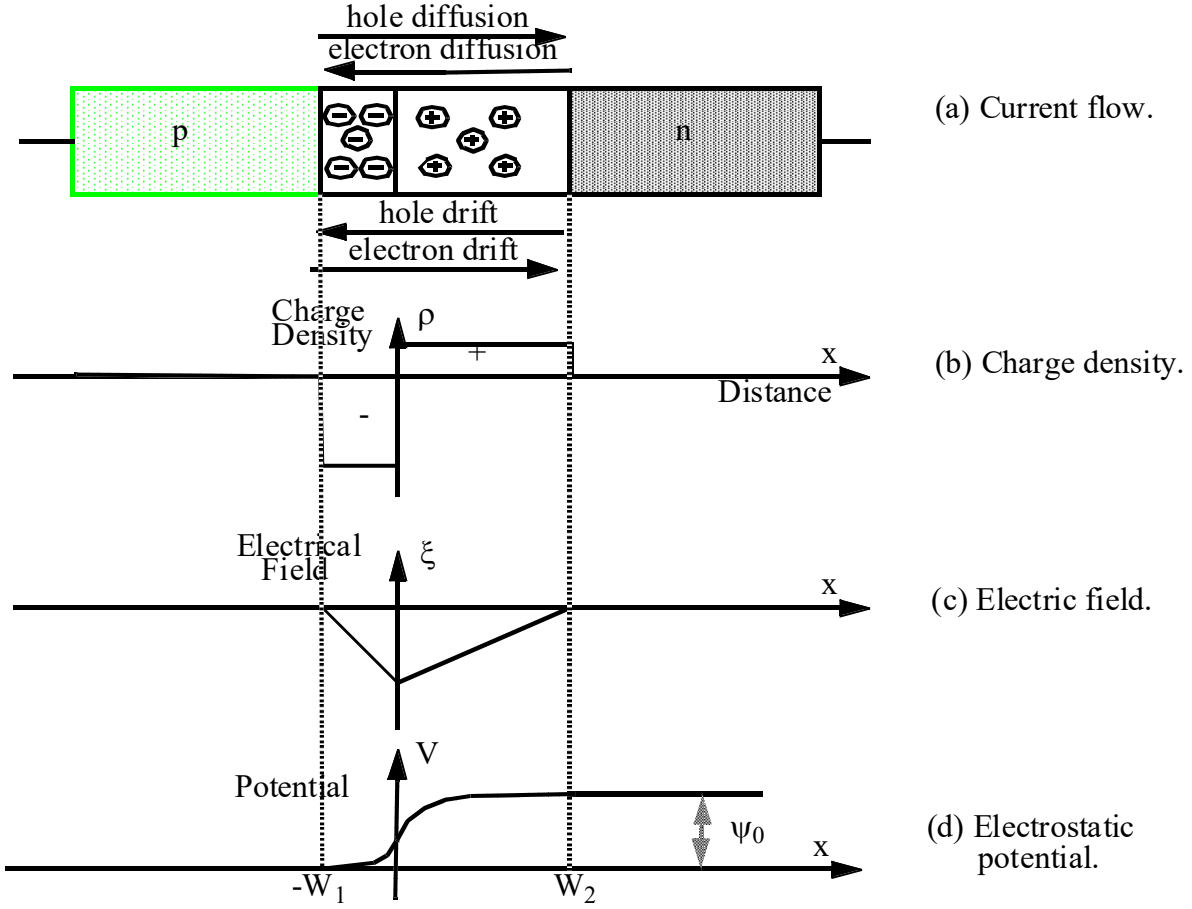
  Doping or other processing

  Removal of unwanted materials

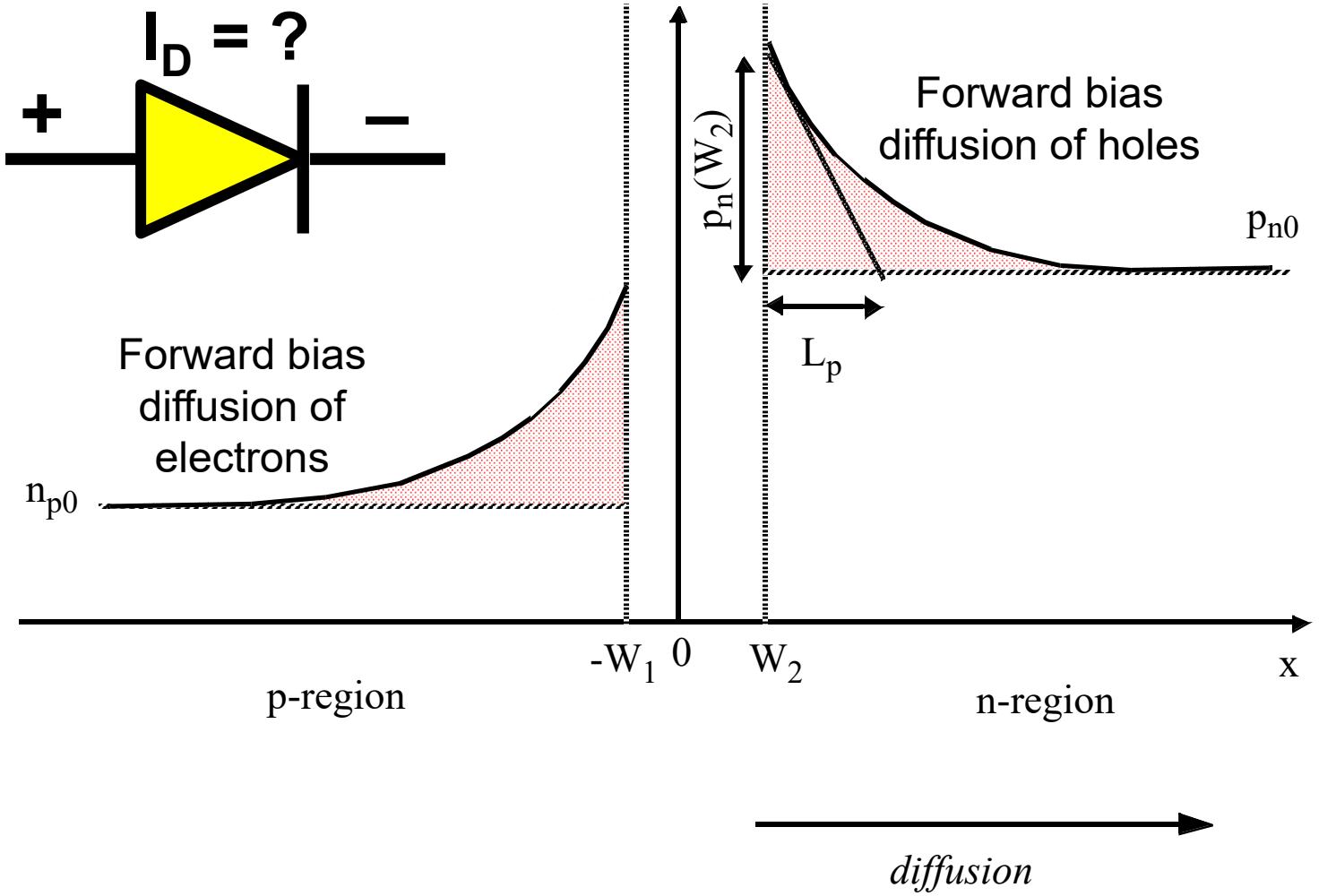
- As process development is not the main focus of this module, we will not go through all the process steps. We will only look at final cross section of the device and inverter.

SUPPLEMENTARY

Depletion Region

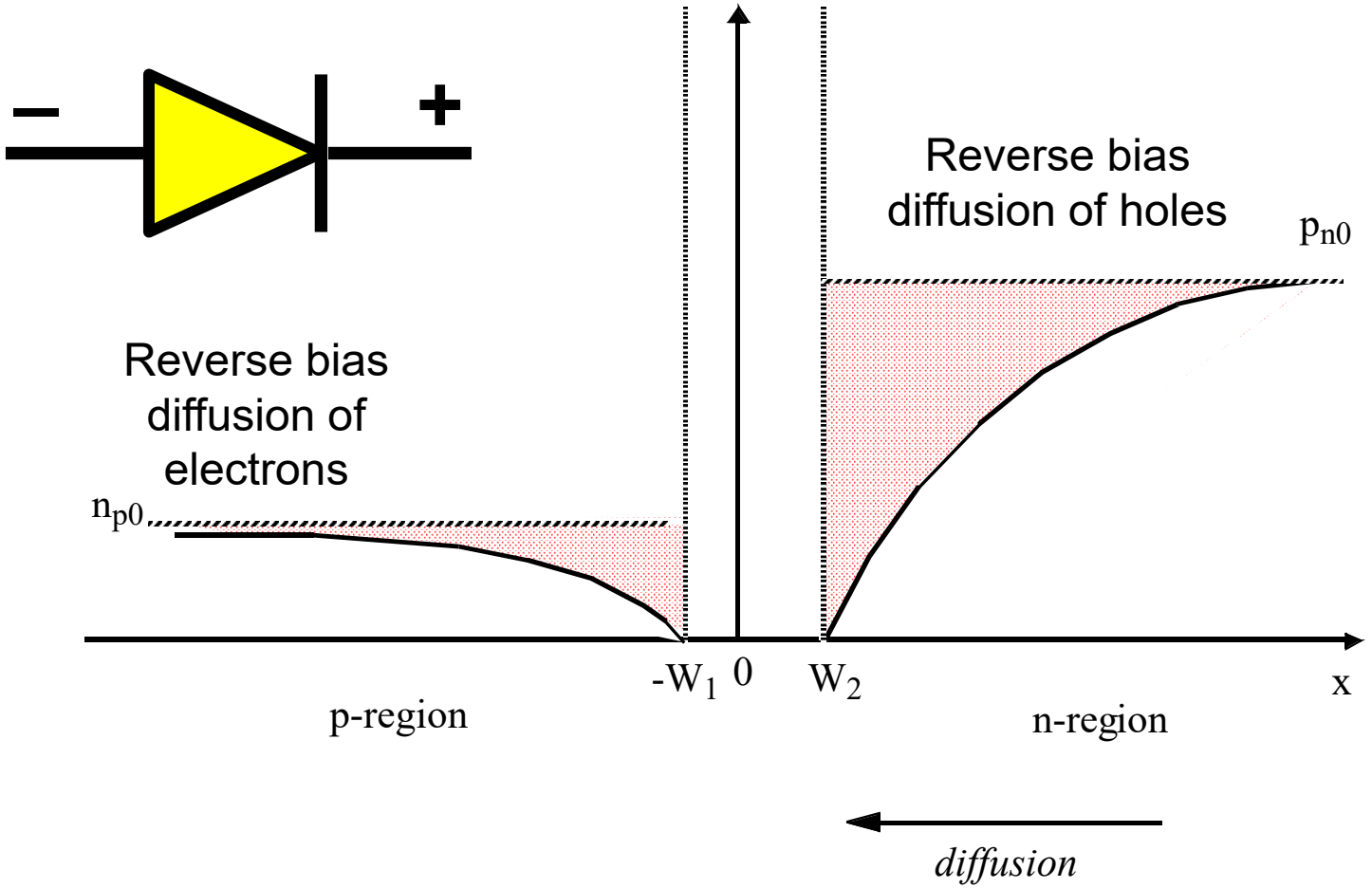


Forward Bias



Typically avoided in Digital IC
Diffusion current becomes dominant

Reverse Bias



The Dominant Operation Mode in Digital IC
Drift current becomes dominant