CG2027 Assignment 3

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1. a) The PUN for both circuits are the same

$\bar{A}$ is connected in series with $\bar{B}$ $\Rightarrow$ $\bar{A} \cdot \bar{B}$ (subnet 1)

Subnet1 is connected in parallel with $\bar{C}$ and $\bar{D}$ $\Rightarrow$ $(\bar{A} \cdot \bar{B}) + \bar{C} + \bar{D}$

$$\boxed{OUT = (\bar{A} \cdot \bar{B}) + \bar{C} + \bar{D}}$$

PDN for circuit A

A is connected in parallel with B $\Rightarrow$ A + B (subnet 1)

subnet 1 is connected in series with C and D $\Rightarrow$ $(A+B) \cdot C \cdot D$

$$\overline{OUT} = (A+B) \cdot C \cdot D$$

$$OUT = \overline{(A+B) \cdot C \cdot D}$$

$$= \overline{A+B} + \bar{C} + \bar{D}$$

$$= (\bar{A} \cdot \bar{B}) + \bar{C} + \bar{D}$$

PDN for circuit A is a dual network of PUN

PDN for circuit B

D is connected in series with C $\Rightarrow$ $D \cdot C$ (subnet 1)

Subnet1 is connected in series with A parallel with B $\Rightarrow$ $D \cdot C \cdot (A+B)$

$$\overline{OUT} = D \cdot C \cdot (A+B)$$

$$= (A+B) \cdot C \cdot D \quad \text{(commutativity of AND operator)}$$

$$OUT = \overline{(A+B) \cdot C \cdot D}$$

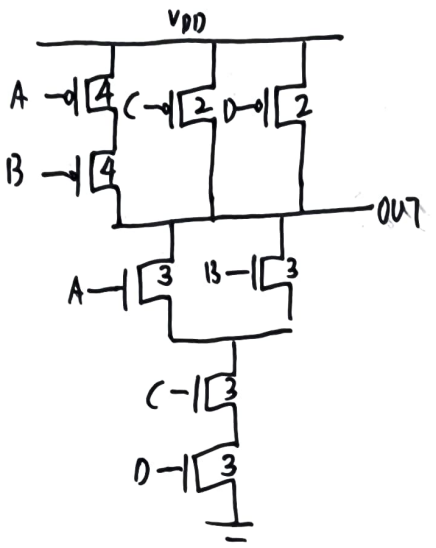
$$= (\bar{A} \cdot \bar{B}) + \bar{C} + \bar{D}$$

PDN for circuit B is a dual network of PUN

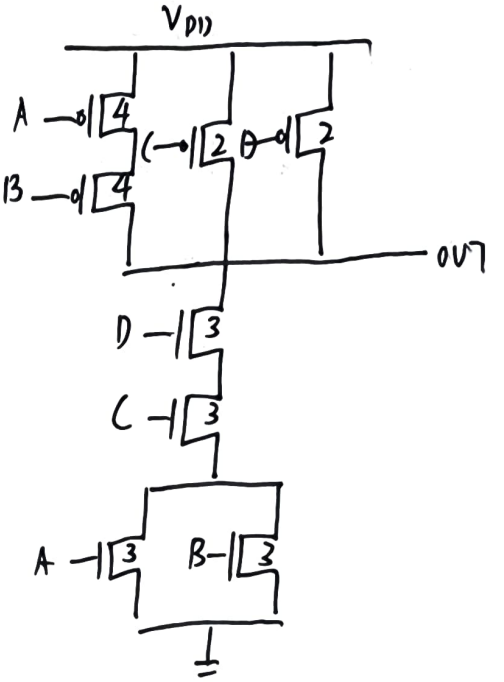
Both circuits implement the same logic function

b)

circuit A



circuit B



$R \propto \frac{1}{W}$

Let W_{PMOS} of INV1X be 2λ and the resistance of this PMOS be R_P

Let W_{NMOS} of INV1X be λ and the resistance of this NMOS be R_N

PUN

short circuit paths through PUN

A - B

C

D

For A-B, each PMOS has resistance $\frac{1}{2}R_P$ so $\frac{1}{2}R_P + \frac{1}{2}R_P = R_P$

A and B should be assigned width 4λ

since width of PMOS A = 4 $\Rightarrow$ $\lambda = 1$

A = 4, B = 4

For C and D, paths with a single transistor should have same size as reference

$C = 2\lambda = 2$

$D = 2\lambda = 2$

A = 4

B = 4

C = 2

D = 2

PDN

short circuit paths through PDN
A - C - D
B - C - D

For A - C - D, each NMOS has resistance $\frac{1}{3}R_N$ so $\frac{1}{3}R_N + \frac{1}{3}R_N + \frac{1}{3}R_N = R_N$

A, C, D should be assigned with 3λ

since $\lambda = 1$, $A = 3$, $C = 3$, $D = 3$

For B - C - D, since C and D have width 3 and resistance $\frac{1}{3}R_N$ each

resistance of B needs to be $R_N - \frac{1}{3}R_N - \frac{1}{3}R_N = \frac{1}{3}R_N$

B also has width 3λ

$A = 3$
$B = 3$
$C = 3$
$D = 3$

c)

when output is low, PDN is connected to GND

worst case output resistance of $12k\Omega$ when each independent series path is turned ON only (A - C - D or B - C - D)

$\Rightarrow$ each NMOS has resistance $12k\Omega \times 3 = 4k\Omega$

output resistance lowest when all paths are connected to GND

$\Rightarrow$ all input are high to turn ON each NMOS

$A = 1$
$B = 1$
$C = 1$
$D = 1$

$R_{NMOS} = R_A // R_B + R_C + R_D$

$= 2k\Omega + 4k\Omega + 4k\Omega$

$= \underline{10k\Omega}$

d) when output is high, PUN is connected to VDD

worst case output resistance of 12kΩ when each independent series connected path is turned ON only (A-B or C or D)

Resistance of A and B = 12kΩ ÷ 2 = 6kΩ

Resistance of C = 12kΩ

Resistance of D = 12kΩ

output resistance is lowest when all 3 paths are connected to GND

⇒ all input are low

A = 0
B = 0
C = 0
D = 0

$R_{MIN} = (R_A + R_B) // R_C // R_D$

$= 12k\Omega // 12k\Omega // 12k\Omega$

$= \underline{4k\Omega}$

e) best case t_{pLH} and t_{pHL} when output resistance is lowest

t_{pLH} is the propogation delay when capacitor is charged through PUN

best case $t_{pLH} = 0.69 \times R_{PUN} \times C$

$= 0.69 \times 4k\Omega \times 100fF$

$= \underline{276\,ps}$

t_{pHL} is the propogation delay when capacitor is discharged through PDN

best case $t_{pHL} = 0.69 \times R_{PDN} \times C$

$= 0.69 \times 10k\Omega \times 100fF$

$= \underline{690\,ps}$

2. a)

$x = A \cdot B + 0 \cdot \bar{B}$

$= A \cdot B$ (AND)

x is input to CMOS inverter

$OUT = \overline{A \cdot B}$ circuit performs NAND logic function

$= \bar{A} + \bar{B}$

b)

consider when $A = V_{DD}$ and B is initially OFF

when B is switched ON, current flows from $A = V_{DD}$ to charge X

The source of the NMOS pass gate is at x and drain at V_{DD}

so $V_{GS} = V_{DS} = V_{DD}$ immediately after $B \rightarrow 1$

$x = V_S$ keeps increasing until $I_D = 0$ when $V_{GS} = V_{TN}$ or $V_{DS} = 0V$

since V_{GS} will hit threshold first, $V_S = x$ can only increase until $V_{DD} - V_{TN}$

There is a V_{TN} voltage drop when trying to pass a 1

when x is not at V_{DD}, the PMOS transistor in CMOS inverter

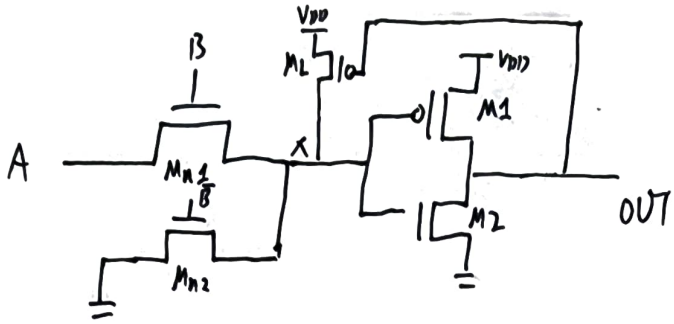
after the pass transistor network might not be completely off as its V_{GS} is not 0

Hence M1 and M2 might both be on simultaneously which causes

a short circuit current to flow through which results in non-zero

static power dissipation

c)



we could add a PMOS transistor which acts as a level restoring transistor M_L

To turn a weak 1 to a strong 1 at X, the inverter detects the weak 1 and passes a 0 to the level restoring PMOS which turns on and passes a strong 1 V_{DD} to X.

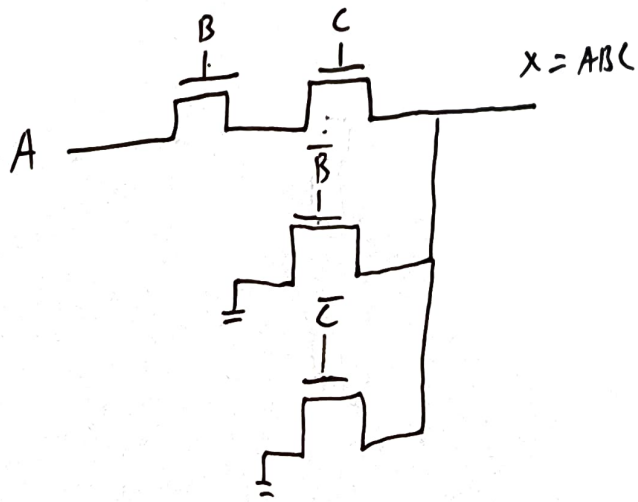
when A or B is switched to 0, the NMOS would want to pull a strong 0 while the level restoring PMOS wants to pass a strong 1

voltage at x is determined by relative values of resistance of NMOS and PMOS

To allow NMOS to pull x down to a voltage low enough such that the inverter sees a 0, resistance of PMOS has to be higher than NMOS

M_L should have a small enough size so that M_{n1} or M_{n2} can pull node x to a low enough voltage so inverter output will switch and turn off PMOS

d)



$X = ABL + 0\bar{B} + 0\bar{C}$

$= ABL$