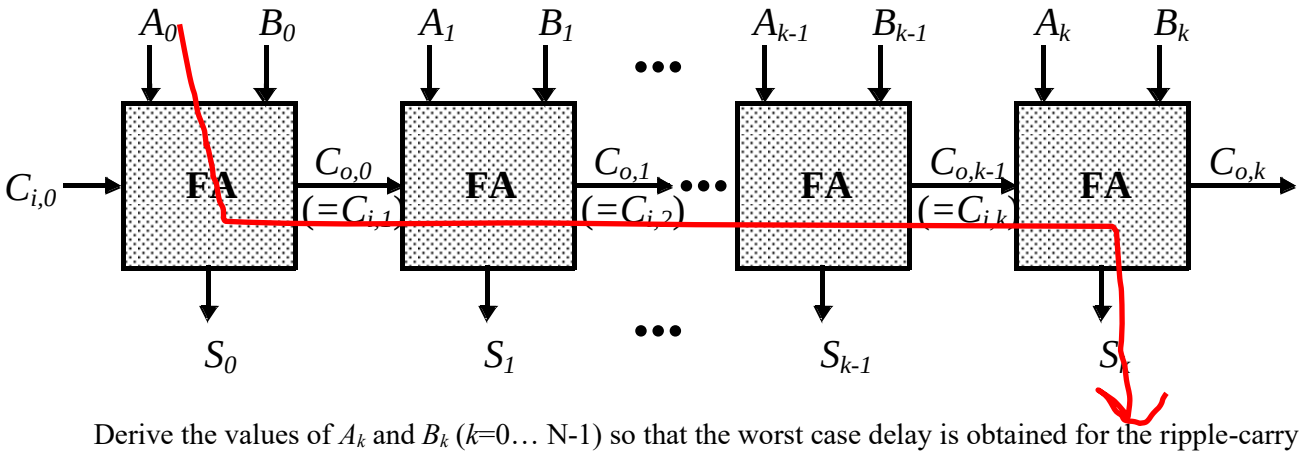
National University of Singapore
Electrical and Computer Engineering

CG2027 (Transistor-Level Digital Circuits)
Assignment #4 Solution

AY21/22 Semester 1
Issued: Aug. 31, 2021 Due: Sep. 05, 2021 (18:00)

Problem 1: Propagation delay of ripple-carry adder



Derive the values of A_k and B_k (k=0… N-1) so that the worst case delay is obtained for the ripple-carry adder shown above.

➔ Observing the figure, the worst case delay occurs when the carry is generated from the Least Significant Bit (LSB) $C_{o,0}$, then it ripples through all bit stages, from which finally $C_{o,k}$ is generated.

➔ If we assume $C_{i,0}$ is 0, and initial value of S_{N-1} is 0, A_0 and B_0 must be 1. All the other stages must be in **propagate** mode. Hence, either A_i or B_i must be 1. Since the initial value of S_{N-1} is 0, we should also arrange a 0→1 transition in SUM as well. This is achieved by setting both A_{N-1} and B_{N-1} to 0 (or 1), which yields a high sum bit given the incoming carry $C_{o,k-1}$ of 1.

➔ If we assume $C_{i,0}$ is 1, then one of (but not both) A_0 and B_0 must be 1.

➔ For example, {A, B}={ 00000001, 01111111 } is *one* of such combination. Note any {A, B} combination that satisfies aforementioned criteria yields the worst case delay.

Problem 2: Ripple carry vs. Carry select adder

(a) Determine the worst-case delay of a 16-bit carry select adder. Assume $\boldsymbol{t_{setup}} = \boldsymbol{t_{sum}} = 2$, and $\boldsymbol{t_{carry}} = \boldsymbol{t_{mux}} = 1$. Compare this with the worst-case delay of a 16-bit ripple carry adder.

➔ From the lecture, we note the delay of an N-bit linear carry-select adder with M-bits per stage is:

$$\boldsymbol{t_{add} = t_{setup} + Mt_{carry} + \left(\frac{N}{M}\right)t_{mux} + t_{sum}}$$

, so $t_{add} = 2+M+(16/M)+2 = 4+M+16/M$

We also note that the N-bit ripple carry adder is:

$t_{add,ripple-carry} = (N-1)t_{carry} + t_{sum}$, so $t_{add,ripple-carry} = 17$.

Comparing both, we can find that under given circumstances, if **M ≥ 2**, the carry select adder has less propagation delay than that of the ripple-carry adder.

(b) If each stage has 4 bits, what is minimum number of bits (N) do we need to have, in order for the carry-select adder to start showing less delay (when compared to a ripple-carry adder)? Assume $t_{setup} = t_{sum} = 2$, and $t_{carry} = t_{mux} = 1$.

➔ From the equations in (a), we let M=4.
$T_{add,carry-select} = 2+4*1+(N/4)*1+2 = (N/4) + 8$
$T_{add,ripple-carry} = (N-1)*1 + 2 = N + 1$
We let $T_{add,carry-select} \leq T_{add,ripple-carry}$. $(N/4) + 8 \leq N+1$. Therefore, $N \geq 9.3333\ldots$. ➔ If **N ≥ 10**, then the carry-select adder has less delay. Therefore, N=10.

Note, in an actual adder implementation, in case N is not multiples of M (such as N=10, M=4 shown above), then the number of muxes in a carry-select adder should be rounded up from (N/M). When we input N=10 and M=4, we will need 3 muxes; in such case the delay of ripple carry and carry select adder delay to be 11. Therefore, more accurate answer will be **N ≥ 11.**

We will consider both N=10 and N=11 as correct answers.