National University of Singapore
Electrical and Computer Engineering

CG2027 (Transistor-Level Digital Circuits)
Assignment #5

AY21/22 Semester 1
Issued: Sep. 7, 2021 Due: Sep. 12, 2021 (18:00)

Problem 1: SRAM memory cell

In a SRAM cell shown in Fig. 1, assume all the transistors (M1 – M6) have the same unknown length (L), and M5, M6 have the width $W_{M5} = W_{M6} = 1\mu m$. Both BL and /BL are precharged to V_{DD}. Assume the on resistance (R_{on}) of a PMOS and a NMOS of the same width and length, are identical, $V_{th,NMOS} = |V_{th,PMOS}| = 0.4(V)$ and $V_{DD}=1(V)$.

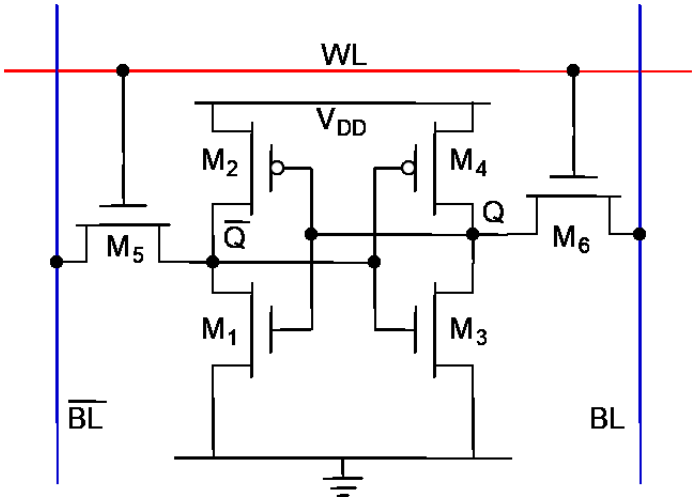

Figure 1. A SRAM cell

a) If Q = 1 and /Q =0 is currently stored in the SRAM cell, and we would like to read the data so that BL=1 and /BL=0 when WL is applied with "H", what should be the requirement (width) of M1 and M3? Why?

⇨ When Q=1 and /Q=0, M2 and M3 are off. When WL= "H" to read the data from the cell, then M5 and M1 form a voltage ladder, where /BL = VDD (precharged). Hence, /Q voltage at this point will be given as $V_{DD} * \frac{R_{M1}}{(R_{M5}+R_{M1})}$, and we need to ensure this does NOT exceed the V_{th} of M3 (otherwise, M3 will accidently turn on).

⇨ Hence $1 * \frac{R_{M1}}{(R_{M5}+R_{M1})} < 0.4$, $6R_{M1} < 4R_{M5}$, therefore, $R_{M1} < \frac{2}{3}R_{M5}$. Since $W_{M5}=1\mu m$, W_{M1} must be larger than 3/2 = 1.5μm. Also, W_{M1} and W_{M3} should have identical size (both widths should be larger 1.5 μm).

b) Now that W1 and W3 are determined from a). If Q = 1 and /Q =0 is currently stored in the SRAM cell, and we would like to write "Q=0, /Q=1" into the cell, then what is the requirement (width) of M2 and M4?

⇨ When Q=1 and /Q=0, M2 and M3 are off. From part a), we sized M1 and M5 so that the /Q will not exceed 0.4V, so writing /Q= "1" cannot be done by M1 and M5, but rather should be done by M4-M6 pairs.

⇨ When WL= "H" to write data into the cell, then M4 and M6 form a voltage ladder, where BL = GND (because we are to write "0" into the cell). Hence, Q voltage at this point will be given as $V_{DD} * \frac{R_{M6}}{(R_{M4}+R_{M6})}$, and we need to ensure this does NOT exceed the V_{th} of M1 (otherwise, M1 will accidently turn on, causing /Q to be pulled down).

⇨ Hence, $1 * \frac{R_{M6}}{(R_{M4}+R_{M6})} < 0.4$, $6R_{M6} < 4R_{M4}$, therefore, $R_{M6} < \frac{2}{3}R_{M4}$. Since W_{M6}=1μm, W_{M4} must be smaller than 2/3 μm. Also, W_{M2} and W_{M4} should have identical size (both widths should be smaller than 2/3 μm).

Problem 2: DRAM operation

In a 1T DRAM cell shown in Fig. 2, BL is precharged to $V_{BL} = V_{ccA}/2 = 1$ V, and C_S is initially discharged to GND. Assume $C_S = 20$fF, and C_{BL}=80fF and $V_{th,M1} = 0.4$V. There is NO sense amplifier attached to the BL.

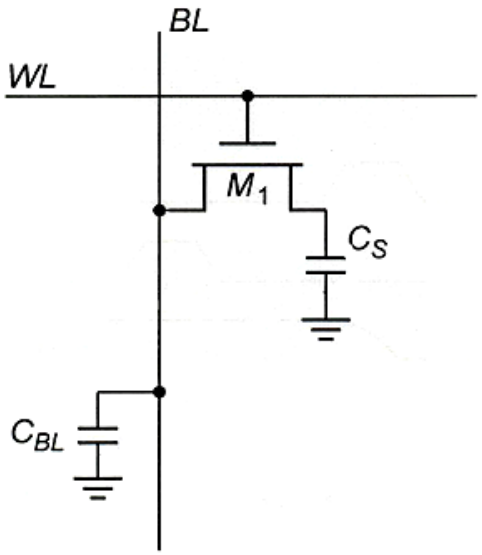

Figure 2. A 1T DRAM cell

(a) When WL is applied with V_{ccA}=2V, the access transistor M1 will turn on. At this point, will the final BL voltage (V_{Final}) increase or drop, compared with the precharge voltage? By how much (in mV)?

⇨ As an analogy, we can think of C_{BL} and C_S as large and small water buckets, respectively. Voltage represents the water level at each bucket. When the M1 is on, the charge from bitline will be shared with the storage capacitor C_S (Which is initially empty), **so the voltage level will drop**.

⇨ Q (charge)= CV, and overall charge of the DRAM cell remains constant (charge conservation). Therefore, $Q_{Overall(Final)} = Q_{BL(initial)} + Q_{S(initial)}$, where $Q_{BL(initial)} = C_{BL} * V_{BL\ (precharge)}$ and $Q_{S\ (initial)} = C_S * V_S = 0$. Note $Q_{Overall(Final)} = (C_{BL}+C_S)*V_{Final}$.

⇨ Hence, (80fF + 20fF) $*V_{Final}$ = 80fF*1(V) ➔ V_{Final}=0.8(V), therefore the dropping amount is 1V - 0.8V = **0.2(V)**.

(b) We now want to write data "1" into C_S, by applying BL with V_{ccA}=2(V). If we apply WL with V_{ccA} (2V) to initiate the writing operation, is there any potential issue? If so, what is it? How can we avoid such issue?

⇨ Yes, there will be a threshold drop issue from M1. When both BL and WL is applied with 2V, then the top plate of C_S, which is connected to the source of M1, can only reach up to M1's V_{GS}-V_{th}= 2 -0.4 = 1.6 (V).

⇨ To prevent such voltage drop (and to fully charge the C_S to the full V_{ccA}), **M1's gate (WL voltage) needs to have at least $V_{th,M1}$ higher than the BL voltage**, i.e., 2.0 + 0.4 = 2.4(V) or higher. This is called bootstrapping of the WL voltage.