# CG2027 Take Home Assessment (Quiz 2)
# AY20/21 Semester I
# Due on 03 October 2020 at 14:59 (GMT +8)

1. Read all instructions and questions carefully before attempting to answer them.
2. Submit a copy of the exam declaration form signed by you together with each of the PDF file you submit.
3. This assessment consists of TWO (2) questions in FIVE (5) pages. You are required to answer all questions.
4. The marks available for Questions 1 and 2 are 30 and 70, respectively.
5. You are allowed to discuss the questions with your peers or instructors to help you better understand the question. However, the **worked solutions you submit for grading should be yours and yours alone**. Your submissions will be passed through software to check for plagiarism, which will constitute as academic dishonesty.
6. If not clearly stated in the question, please clearly highlight your numerical answers to specific calculations, and state them to FOUR (4) significant figures.
7. Codes and analysis reports are to be saved as separate files and uploaded into separate folders on LumiNUS before the submission deadline. *Reports are to be saved as PDF file and MATLAB codes are to be saved with .m file extension*. Please save your files using the following file naming scheme:
   <MATRIC_NUMBER>-CG2027-Quiz2-Q<QUESTION_NUMBER>
   *e.g.* A01234567H-CG2027-Quiz2-Q2.PDF

Q1. (30 marks) In Week 4, you learned about the mirror-adder (see Figure Q1-2), which is composed of several static CMOS logic gates–an inverting majority gate, two inverters, and a logic gate that generates the sum bit, *S*, from the inputs $C_I$, *A*, *B* and $C_O$. For this question, assume that the channel length, *L*, of transistors cannot be changed.

Submit a report and a MATLAB function for this question. The MATLAB function (modify the template given) will perform some design calculations for the mirror adder and must meet the specifications stated below. The report should clearly explain the calculations your MATLAB function performs, including the derivation of any equation.

- Include the capacitances at all intermediate nodes of the adder in your calculations
- The capacitor model for a single MOSFET is shown in Figure Q1-1.

Inputs to function:

| | |
|---|---|
| R_N | ON channel resistance between source and drain of the NMOS transistor when its width is 1 µm |
| R_P | ON channel resistance between source and drain of the PMOS transistor when its width is 1 µm |
| C_GN | The effective gate capacitance of the NMOS transistor when its width is 1 µm |
| C_GP | The effective gate capacitance of the PMOS transistor when its width is 1 µm |
| C_NI | The effective capacitance at the source/drain terminal of the NMOS transistor when its width is 1 µm |
| C_PI | The effective capacitance at the source/drain terminal of the PMOS transistor when its width is 1 µm |
| R_PDN | the desired worst-case resistance along the corresponding pull-down network when $\overline{C_O} = 0$, and when $\bar{S} = 0$ |
| R_PUN | the desired worst-case resistance along the corresponding pull-up network when $\overline{C_O} = 1$, and when $\bar{S} = 1$ |

Outputs to function:

| | |
|---|---|
| NRatio_Arr | Array of W/L ratios for all NMOS transistors in the schematic under the assumption that the width of the reference NMOS transistor is 1 µm. Array index corresponds to numbers in Figure Q1-2. |
| PRatio_Arr | Array of W/L ratios for all PMOS transistors in the schematic under the assumption that the width of the reference PMOS transistor is 1 µm. Array index corresponds to numbers in Figure Q1-2. |
| tp_Arr | Array of longest propagation delays (estimated using the Elmore delay model) to the outputs, $\overline{C_O}$ and $\bar{S}$, for all possible combinations of $A$, $B$ and $C_I$ in the sequence $\{A, B, C_I\} = \{0,0,0\}$, $\{0,0,1\}$, $\{0,1,0\}$, $\{0,1,1\}$, $\{1,0,0\}$, $\{1,0,1\}$, $\{1,1,0\}$ and $\{1,1,1\}$. |


Figure Q1-1. The capacitance models for the MOSFETs may be simplified so that only three capacitors instead of five capacitors need to be included.

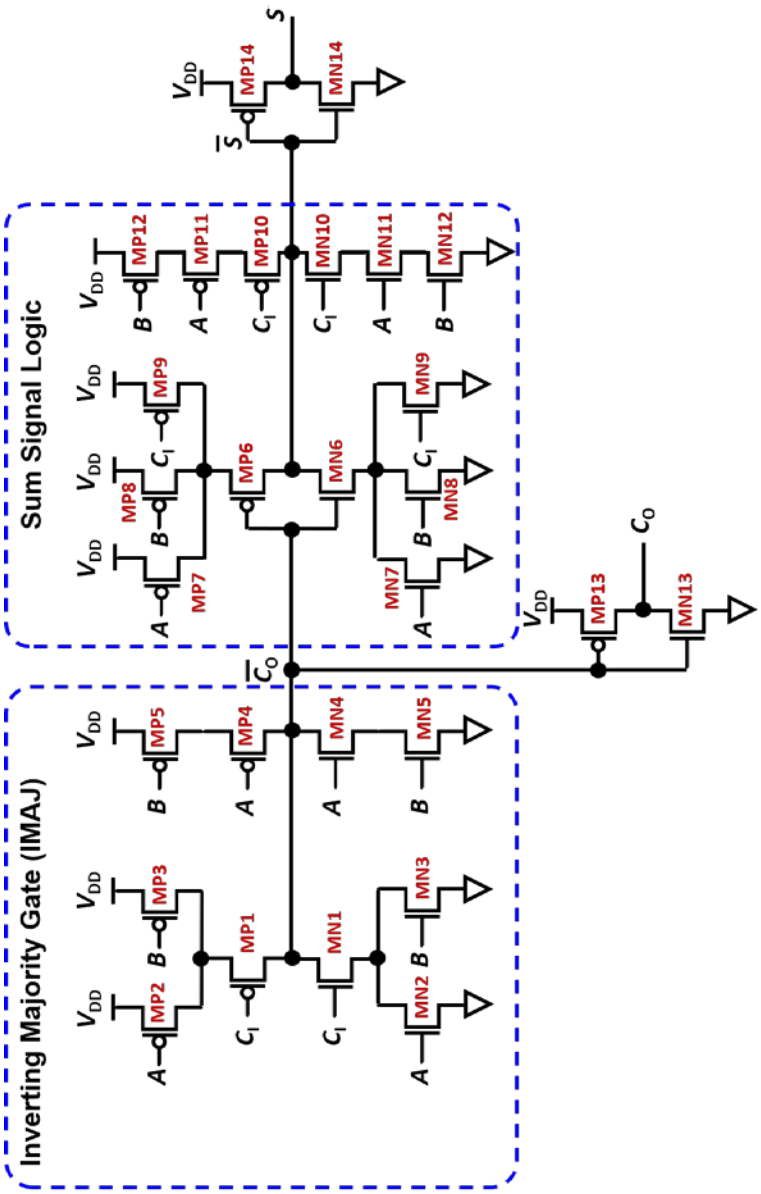


Figure Q1-2. The schematic of a mirror adder showing all transistors in the circuit, which have been grouped to show the various static CMOS logic gates that constitute the adder.

Q2. (70 marks) In Week 5, you learned about adders and the Manchester carry chain (MC2), which is used to speed up the propagation of the carry signal in the carry-bypass and carry-select adders. For this question, you will analyze the design of an adder/subtractor that takes as inputs two 128-bit signed integers (*A* and *B*) and generates an output that is 129-bit wide (128 sum bits plus the final carry-out). For this question, assume that:

i) complementary signals are available for all input bits to the 128-bit adder/subtractor (the carry-in at the LSB and all the bits of the inputs *A* and *B*), and

ii) the channel length, *L*, of the MOSFETs cannot be changed.

Submit a report for the analysis you will be doing for this question. Clearly state all assumptions.

Since all carry-bits are determined by the MC2, the 128-bit adder/subtractor can be built by adding to the MC2 the sum signal logic circuit in the mirror adder (see Figure Q1-2) that can generate all the individual sum bits.

(a) Assuming the MC2 that is available is as shown in Figure Q2-1. Draw the schematic of the sum signal logic gate, modified from that in Figure Q1-2, that will give the correct sum bits from the MC2 in Figure Q2-1. To save on area and power consumption, ensure your circuit has the fewest additional inverters.

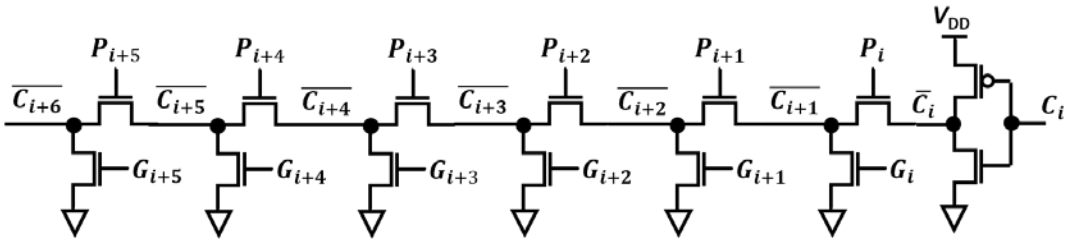


Figure Q2-1. Schematic for a Manchester carry chain.

(b) Write down the (W/L) ratios of all NMOS and PMOS transistors in the sum signal logic gate from Q2(a) so that the worst-case resistance of the PDN is the same as the ON resistance between the source and drain of an NMOS transistor that has $(W/L)_N = 4$, and the worst-case resistance of the PUN is the same as the ON resistance between the source and drain of a PMOS transistor that has $(W/L)_P = 8$.

(c) The capacitor model for the MOSFET is shown in Figure Q2-2 for this question. You are given that C_NI and C_PI are directly proportional to (W/L) of the corresponding transistor, and when $(W/L)_N = 1 = (W/L)_P$, C_NI = C_PI and C_GN = C_GP = 10 C_NI. If $(W/L)_N = 1$ and $(W/L)_P = 2$ for the transistors in the MC2, what are the effective capacitances at the carry nodes for all bit positions of the 128-bit adder/subtractor (from the carry-in to the LSB all the way to the carry-out of the MSB) that is built by connecting the MC2 in Q2-1 with the sum signal logic gates in Q2(b)?

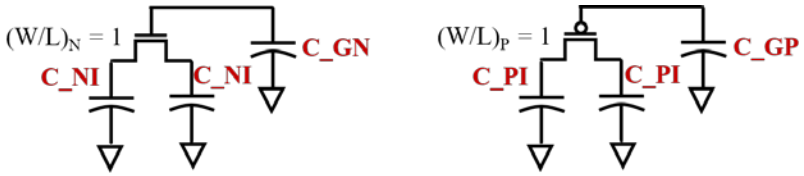


Figure Q2-2. The capacitance models for the MOSFETs may be simplified so that only three capacitors instead of five capacitors need to be included.

(d) In class, we learned that the delay of the pass transistor logic gate scales as $N^2$, where $N$ is the number of series connected transistors. One technique that can help to alleviate this design issue is to insert buffers as shown in Figure Q2-3. The sum signal logic gate in Figure Q1-2 can be used for the part of the MC2 where the carries are active high, and the sum signal logic gate for Q2(a) can be used for the part of the MC2 where the carries are active low. Draw the schematic of the sum signal logic gate to be used with the part of the MC2 where the carriers are active high, and give the sizes of the transistors in the logic gate according to the same sizing rules as in Q2(b).

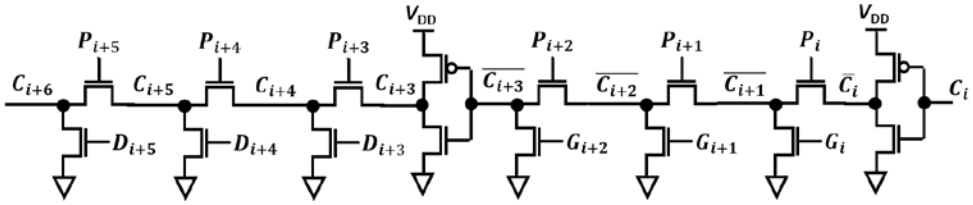


Figure Q2-3. The MC2 in Figure Q2-1 is partitioned into to stages covering 3-bits in each stage. A static CMOS inverter is inserted to interface the two stages of the MC2.

(e) Based on the results from Q2(c) and (d), what are the effective capacitances at all the carry nodes for all bit positions if the MC2 used in the 128-bit adder/subtractor has two stages (64-bits per stage)? In your answer, include an additional load capacitance for the carry-out of the MSB of the adder/subtractor.

(f) We will now analyze the critical path delay of the staged design of the Manchester carry chain based on the model you develop in Q2(d). As clearly seen in Figure Q2-3, consecutive stages of the buffered MC2 will alternate between active high and active low carry signals. Calculate the critical path delays of the staged MC2 design with different number of bits per stage and clearly show whether the number of bits per stage of the MC2 can be adjusted to minimize the critical path delay. In this analysis, consider only cases where the number of bits per stage is a power of two (*i.e.*, 2, 4, 8, 16, 32, 64, 128).