CG2027 Assignment 4

Zhuang Jianming
A0214561N

1. since calculating the carry out and sum bit in each subsequent Full Adder depends on the carry in (carry out generated in the previous Full Adder), the worst case delay for the ripple-carry adder happens when the carry bit generated from the LSB (1st FA) is propagated throughout all the Full Adders and computes the final sum bit.

$$t_{add,ripple-carry} = (N-1)\,t_{carry} + t_{sum}$$

$P = A \oplus B$ $\qquad$ $C_o = G + PC_i$

$G = AB$ $\qquad$ $S = P \oplus C_i$

To generate a carry out from the LSB, $G_0 + P_0 C_{i,0} = 1$

If $C_{i,0} = 0$, A_0 and B_0 must be both 1 ($G_0 = 1 = A_0 \cdot B_0$)

If $C_{i,0} = 1$, A_0 or B_0 can be 1 ($G_0 = 1$ or $P_0 = 1$)

To propagate this carry throughout all the Full Adders, they must all be in propagate mode

$P_i = A_i \oplus B_i = 1 \Rightarrow A_i \neq B_i$ ($i = 1 \ldots N-2$)

A_i	B_i
0	1
1	0

For the final sum bit S_{N-1}, if there is a $0 \to 1$ transition

$S_{N-1} = P_{N-1} \oplus C_{i,N-1} = 1$

since $C_{i,N-1} = 1$ (propagated through whole ripple-carry adder)

then P_{N-1} must be 0 $\Rightarrow A_{N-1} \oplus B_{N-1} = 0$

$\Rightarrow$ either A_{N-1} and $B_{N-1} = 0$ or A_{N-1} and $B_{N-1} = 1$

Hence, a possible set of value for A_K and B_K ($K = 0 \ldots N-1$) is

$A_0 = 1$	$A_i = 1$	for ($i = 1 \ldots N-2$)	$A_{N-1} = 0$
$B_0 = 1$	$B_i = 0$		$B_{N-1} = 0$

2. a)

For a linear carry-select adder with N bits and M bits / stage

$$t_{add,\,carry\text{-}select} = t_{setup} + M\,t_{carry} + \frac{N}{M}\,t_{mux} + t_{sum}$$

$$N=16 \Rightarrow t_{add,\,carry\text{-}select} = 2 + M + \frac{16}{M} + 2$$

$$= 4 + M + \frac{16}{M}$$

square root?

$\frac{16}{M}$ vs $\sqrt{32}$

For an N bit ripple carry adder

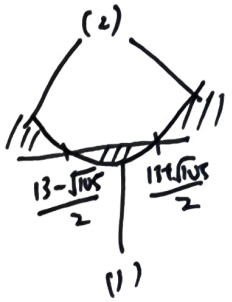
$$t_{add,\,ripple\text{-}carry} = (N-1)\,t_{carry} + t_{sum}$$

$$N=16 \Rightarrow t_{add,\,ripple\text{-}carry} = 15 + 2$$

$$= 17$$

comparing both $\quad 4 + M + \frac{16}{M} = 17$

$$M^2 - 13M + 16 = 0$$



(1) For carry select adder to have better worst case delay than ripple carry adder, $\frac{13-\sqrt{105}}{2} < M < \frac{13+\sqrt{105}}{2}$

$$\approx 2 \le M \le 11 \quad (\text{integer } M)$$

(2) For ripple carry adder to have better worst case delay than carry select adder $\quad M < \frac{13-\sqrt{105}}{2}$ or $\frac{13+\sqrt{105}}{2} < M \le 16$

$$\approx M \le 1 \text{ or } 12 \le M \le 16 \quad (\text{integer } M)$$

b)

$M=4 \Rightarrow t_{add,carry\text{-}select} = 2+4+\frac{N}{4}+2$

$= 8+\frac{N}{4}$

$t_{add,ripple\ carry} = N-1+2$

$= N+1$

For carry select adder to show less delay than ripple carry adder

$8+\frac{N}{4} \leq N+1$

$\frac{3}{4}N \geq 7$

$N \geq \frac{28}{3}$

$\Rightarrow N \geq 10$ (integer N)

Minimum number of bits is <u>10</u>