CG2027 Assignment 5

Zhuang Jianming
A0219561M

1. a) When $Q = 1$ and $\bar{Q} = 0$, transistors M2 and M3 are turned off while transistors M1 and M4 are turned on. During the read operation when $WL = 1$, current will need to flow through M5 and M1 to discharge the voltage of $\overline{BL}$ to 0V. For the current to flow, V_{DS} of M1 cannot be 0, hence voltage of $\bar{Q}$ must be greater than 0. However, voltage of $\bar{Q}$ cannot increase beyond the trip point of the inverter formed by M3 and M4, else data stored in cell becomes corrupted. Thus, voltage of $\bar{Q}$ cannot exceed $V_{th,NMOS}$ of M3 which will turn it on.

We can adjust the cell ratio $\frac{W_1/L_1}{W_5/L_5}$ such that M_1 is stronger than M5 so $\bar{Q}$ stays close to 0.

The transistors M1 and M5 act like a voltage divider

$$\bar{Q} = \frac{R_1}{R_1 + R_5} \times V_{DD} \quad (\text{precharged } \overline{BL})$$

$$\bar{Q} < 0.4 \Rightarrow \frac{R_1}{R_1+R_5} \times 1 < 0.4 \Rightarrow 0.6R_1 < 0.4R_5$$

since $R \propto \frac{1}{W}$, $\frac{0.6}{W_1} < \frac{0.4}{W_5} \Rightarrow W_1 > \frac{0.6}{0.4} W_5$

If $W_5 = 1\mu m$, $W_1 > \frac{3}{2}\mu m$

Due to symmetry in the structure, the $\frac{W}{L}$ ratios of pull down transistors are the same, hence W_2 also $> \frac{3}{2}\mu m$

b)

when $Q = 1$ and $\bar{Q} = 0$, transistors M2 and M3 are turned off while transistor M1 and M4 are turned on. To write $Q = 0$, $\bar{Q} = 1$, BL should be grounded while $\overline{BL}$ is charged to 1. When $WL = 1$, M5 is fighting with M1 to pass a 1 while M6 is fighting M4 to pass a 0. However, since we already sized M1 and M5 such that $\bar{Q} < 0.4V$, writing $\bar{Q} = 1$ should be done by passing 0 to Q and inverting.

we can adjust the pull-up ratio $\frac{W_4/L_4}{W_6/L_6}$ such that M6 can overcome M4 and pull the voltage of Q down to 0

The transistors M4 and M6 act like a voltage divider

$$Q = \frac{R_6}{R_6 + R_4} \times V_{DD} \quad (\text{source of M4})$$

Q must be pulled below the trip point of the inverter formed by M1 and M2 so that M1 is kept off and 0 can be written to Q. ($V_{th,NMOS}$ of M1)

$$Q < 0.4 \Rightarrow \frac{R_6}{R_6 + R_4} \times 1 < 0.4 \Rightarrow 0.6R_6 < 0.4R_4$$

$$\text{since } R \propto \frac{1}{W} \Rightarrow \frac{0.6}{W_6} < \frac{0.4}{W_4} \Rightarrow W_4 < \frac{2}{3} W_6$$

If $W_6 = 1\mu m$, $W_4 < \frac{2}{3}\mu m$

Due to symmetry in the structure, $\frac{W}{L}$ of all pull up transistors are the same, hence W_2 also $< \frac{2}{3}\mu m$

2.a) when $WL = V_{CCA}$, access transistor M1 is turned on.

storage node Q becomes electrically shorted to BL, thus charges stored on bit line capacitance and storage capacitance will distribute themselves according to the charge sharing principle

$$Q_{BL} = C_{BL} \cdot V_{BL} = 80fF \cdot 1V$$

$$Q_{CS} = C_S \cdot V_{Partial} = 20fF \cdot 0V$$

$$Q_{total} = Q_{BL} + Q_{CS} = 80fF \cdot 1V$$

$$\Delta V_{BL} = \left(\frac{Q_{total}}{C_{BL} + C_S}\right)_{\rightarrow V_{Final}} - V_{precharge}$$

$$= \frac{80fF \cdot 1V}{80fF + 20fF} - 1V$$

$$= -0.2V$$

final BL voltage $V_{Final} = 0.8V$ will drop by 0.2 V compared to precharge voltage of 1V

b)

If both WL and BL are applied with $V_{CCA} = 2V$, the voltage at storage node Q can only be charged up to $V_{CCA} - V_{TN} = 2V - 0.4V = 1.6V$ due to a V_{TN} voltage drop when trying to write a 1.

This is because voltage at Q can only increase until $I_D = 0$ when $V_{GS} = V_{TN}$ or $V_{DS} = 0V$. Hence, to avoid the issue of voltage drop, M1's gate voltage V_{WL} should be higher than M1's drain V_{BL} by at least the threshold $V_{th,M1}$ => $2.0V + 0.4V = 2.4V$

charge loss can be circumvented by bootstrapping word line, to a higher value than bitline