

# Week 1-1

Semiconductor Materials and Doping

# Electrical Properties of Materials

	Material	Typical Resistivity* ( $\Omega\text{-cm}$ )	Typical Carrier Concentration ( $\text{cm}^{-3}$ )
Metal	Copper	$1.69 \times 10^{-6}$	$\sim 10^{23}$
	Gold	$2.20 \times 10^{-6}$	
	Aluminum	$2.67 \times 10^{-6}$	
	Stainless Steel	$70-78 \times 10^{-6}$	
Semiconductor	Germanium	46	Wide range up to $\sim 10^{18-19}$ (with doping)
	Silicon	$2.3 \times 10^5$	
	Gallium Arsenide	$10^8$	
Insulator	Silicon Nitride	$10^{14}$	Negligible
	Silicon Dioxide	$10^{14}-10^{16}$	
	Polyimide	$10^{18}$	

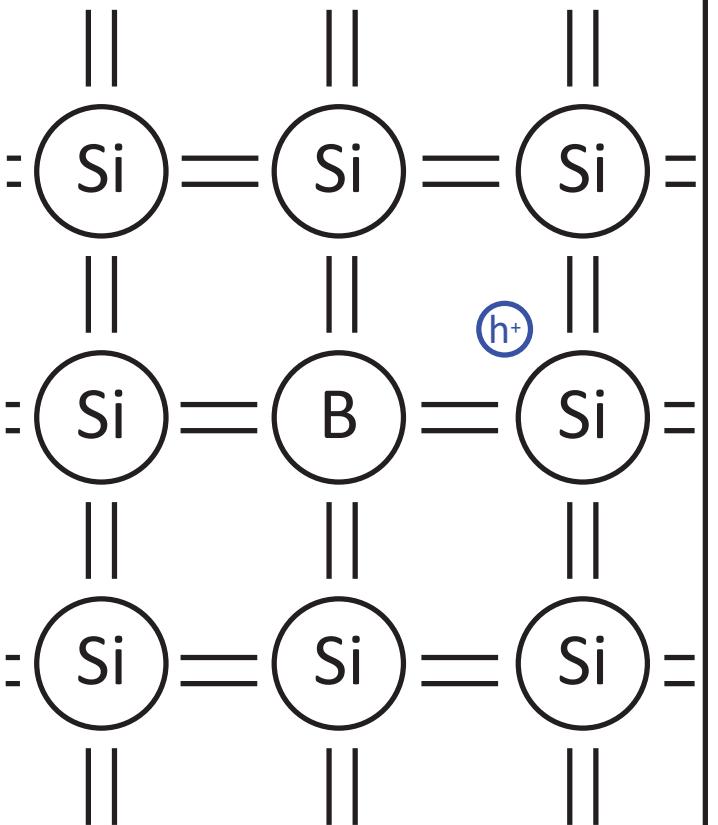
# The Periodic Table of Elements

	Group																									
	I	II																								
	1 H	4 Be																								
Metals	3 Li	11 Na	19 K	37 Rb	55 Cs	87 Fr	20 Ca	38 Sr	56 Ba	88 Ra	89 Ac	21 Sc	22 Ti	23 V	24 Cr	25 Mn	26 Fe	27 Co	28 Ni	29 Cu						
	Alkali Metals	Alkaline Earth Metals	Lanthanoids	Poor Metals	Reactive Non-Metals	Actinoids	Transition Metals	Metalloids	Noble Gases	Unknown Properties		12 Mg	20 Ca	38 Sr	39 Y	40 Zr	41 Nb	42 Mo	43 Tc	44 Ru	45 Rh					
																46 Pd	47 Ag	48 Cd	49 In	50 Sn	51 Sb					
Nonmetals												*	72 Hf	73 Ta	74 W	75 Re	76 Os	77 Ir	78 Pt	79 Au	80 Hg	81 Tl				
												*	72 Hf	73 Ta	74 W	75 Re	76 Os	77 Ir	78 Pt	79 Au	80 Hg	81 Tl	82 Pb			
												*	104 Rf	105 Db	106 Sg	107 Bh	108 Hs	109 Mt	110 Ds	111 Rg	112 Cn	113 Nh	114 Fl			
												*														
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												*														
												*														
												*														
												*														
												*														
												*	58 Ce	59 Pr	60 Nd	61 Pm	62 Sm	63 Eu	64 Gd	65 Tb	66 Dy	67 Ho	68 Er	69 Tm	70 Yb	71 Lu
												*	90 Th	91 Pa	92 U	93 Np	94 Pu	95 Am	96 Cm	97 Bk	98 Cf	99 Es	100 Fm	101 Md	102 No	103 Lr

# Covalent Bonding

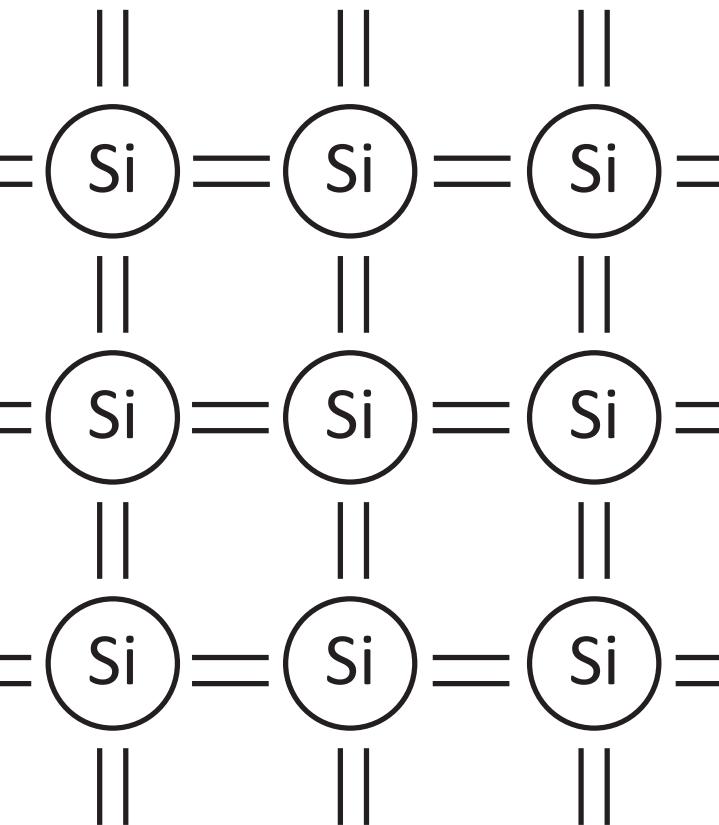
Acceptor-Doped Silicon

p-type or p-doped



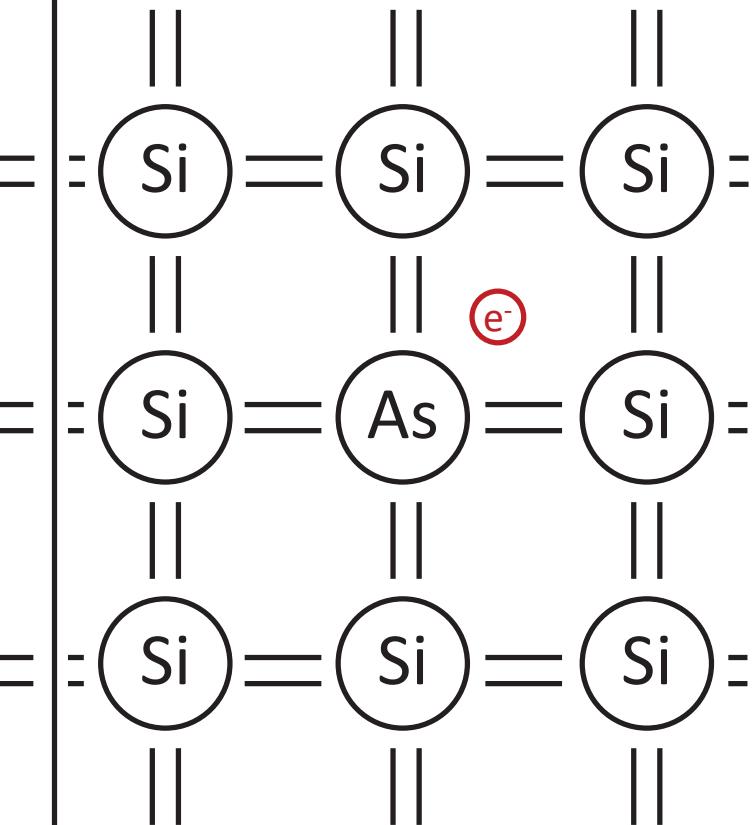
“Perfect” Silicon Crystal

intrinsic



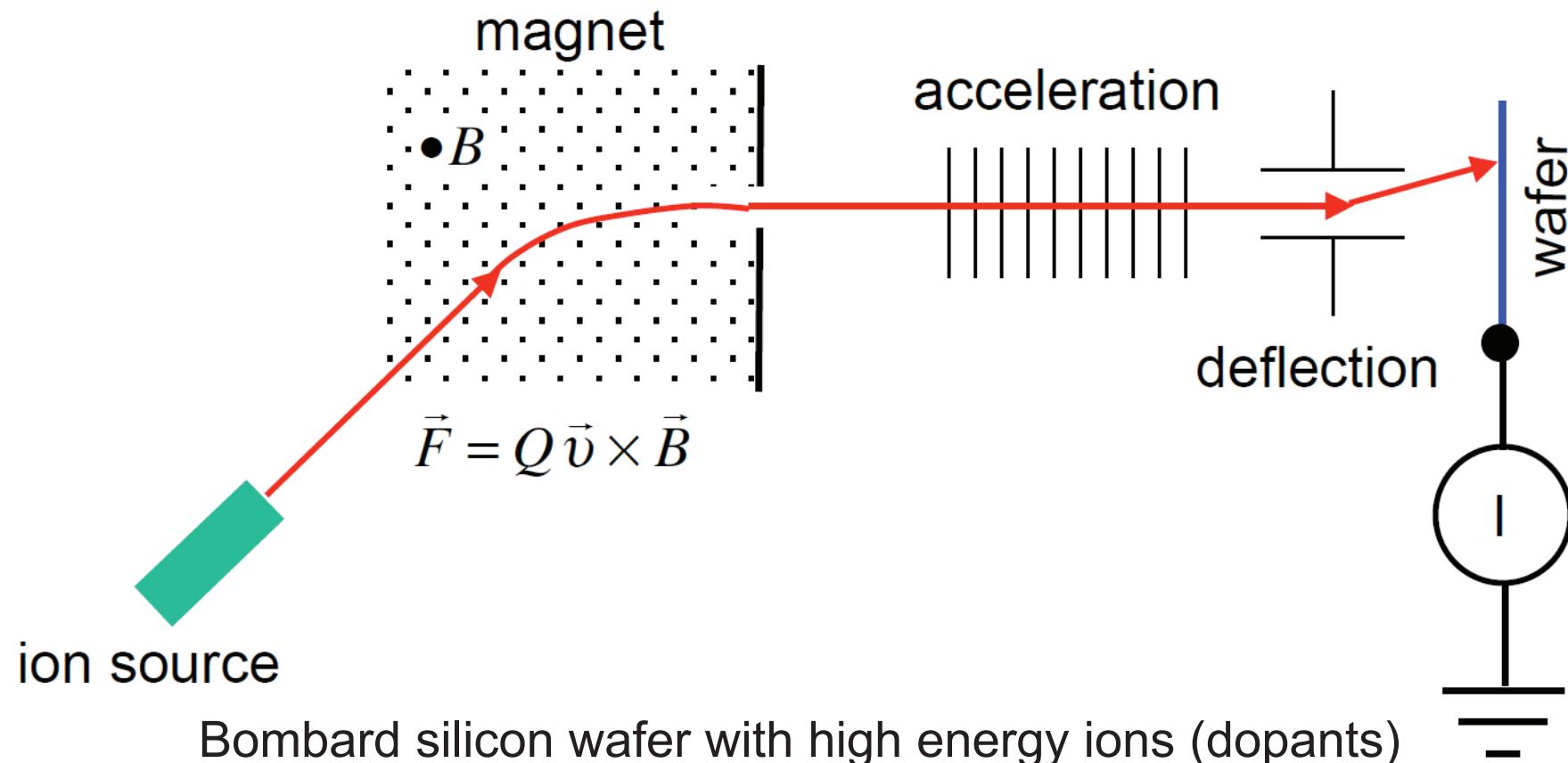
Donor-Doped Silicon

n-type or n-doped



Free electrons and holes support conduction of electricity (current flow)

# Ion Implantation and Doping



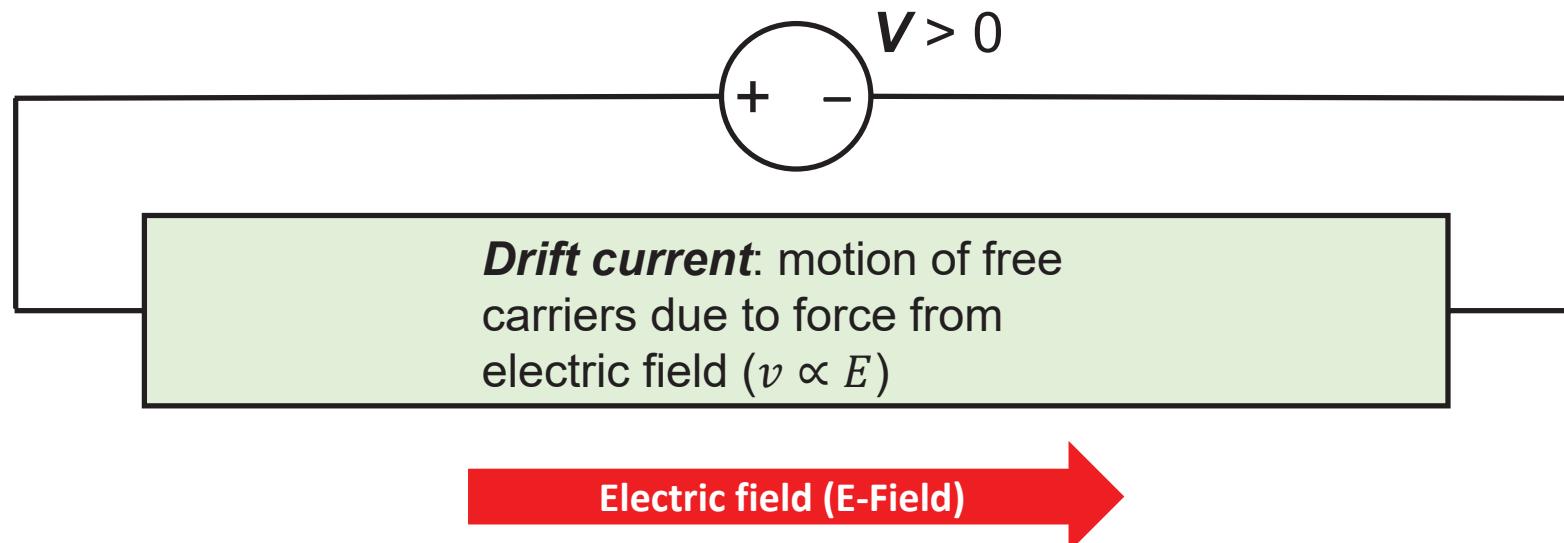
Bombard silicon wafer with high energy ions (dopants)

- Energy of ions: depth of implantation from surface
- Time of exposure: concentration of impurities added

# Week 1-2

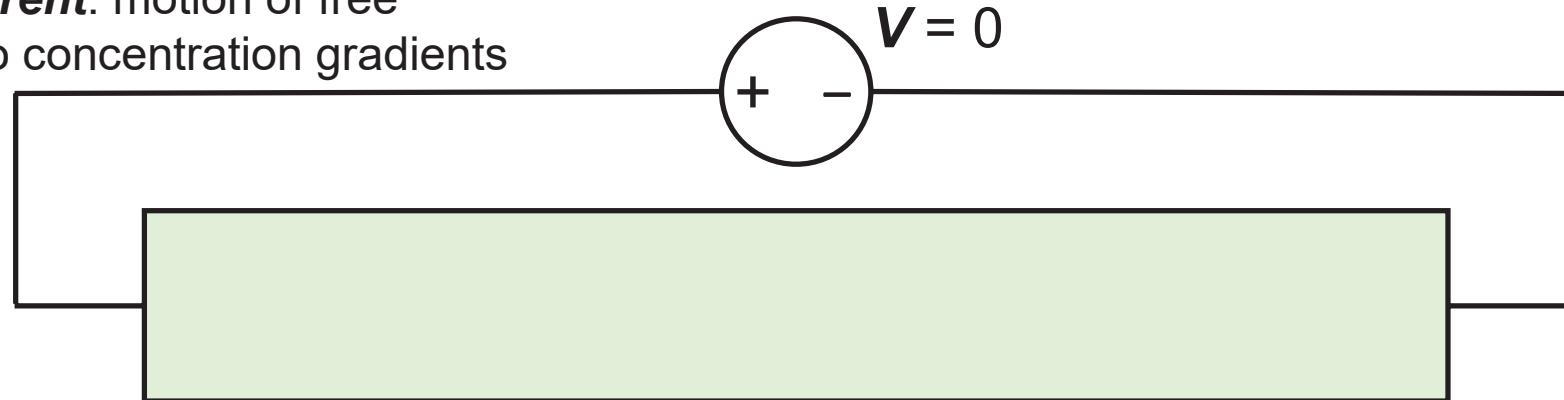
Current Flow in a Semiconductor

# Types of Current Flow in a Semiconductor



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**Diffusion current:** motion of free carriers due to concentration gradients



# Calculating Current Flow in Semiconductors

Carrier Concentration	Drift Current Density	Diffusion Current Density
$n$	$qn\mu_n E$	$-qD_n \Delta n$
Total Current Density	Sum of <u>drift and diffusion</u> current densities for <u>electrons and holes</u>	

$$J_{TOTAL} = q_e n \mu_n E + q_h p \mu_p E - q_e D_n \Delta n - q_h D_p \Delta p$$

Drift      Diffusion

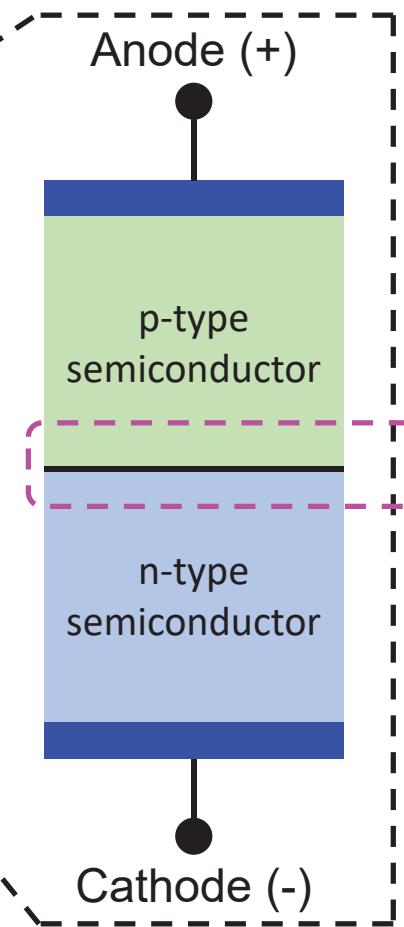
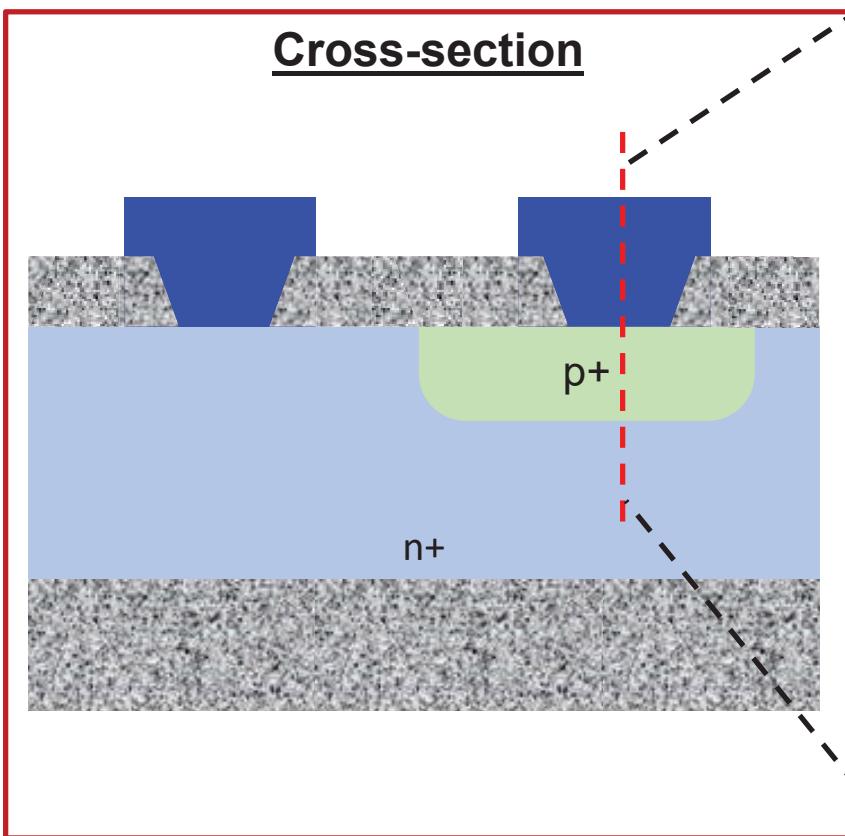
# Current Flow in Circuit Elements

Devices	Movement Mechanism in on-state	Type of Carriers
Resistor	Drift	<ul style="list-style-type: none"><li>▪ Electrons (Metal)</li><li>▪ Electrons and holes (Semiconductor)</li></ul>
Diode	Diffusion	<ul style="list-style-type: none"><li>▪ Electrons and holes</li></ul>
Bipolar Junction Transistor	Diffusion	<ul style="list-style-type: none"><li>▪ Electrons and holes</li></ul>
MOSFET	Drift	<ul style="list-style-type: none"><li>▪ Electrons (NMOS)</li><li>▪ Holes (PMOS)</li></ul>

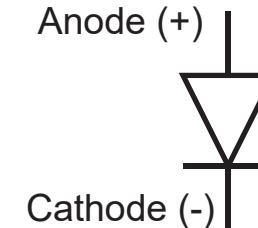
# Week 1-3

Introduction to the pn-Junction Diode

# The pn-junction Diode

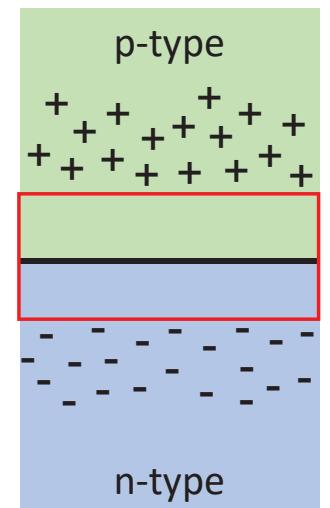


## Circuit Symbol

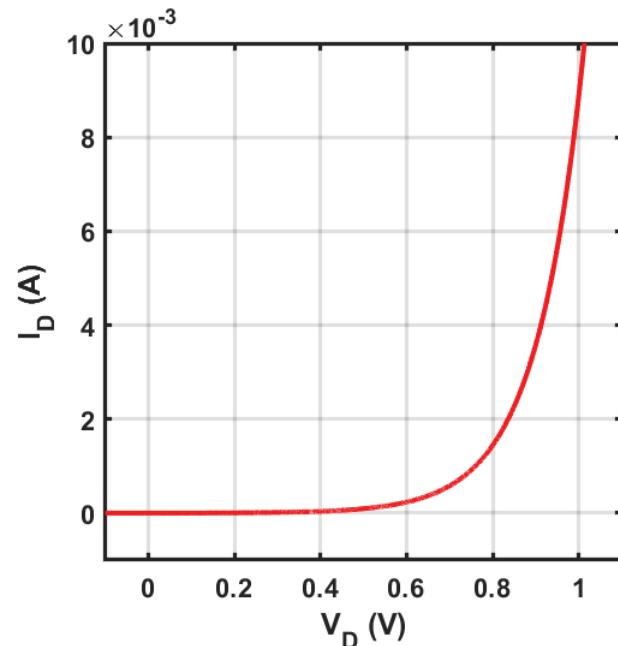


## Metallurgical Junction

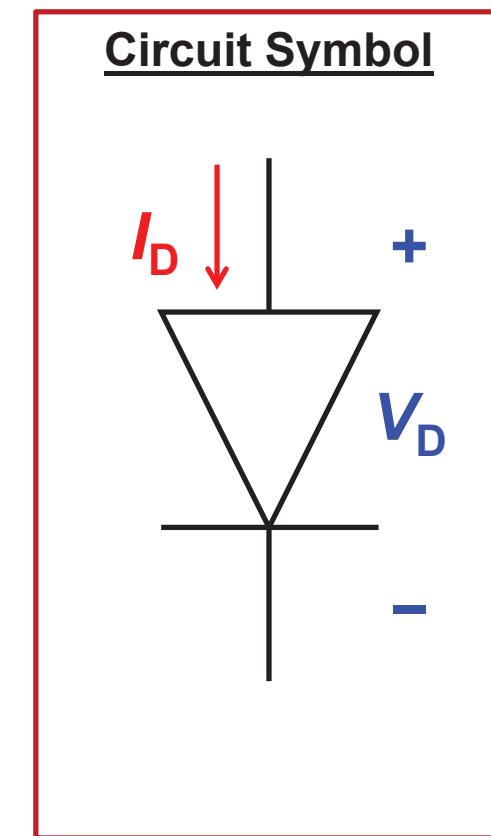
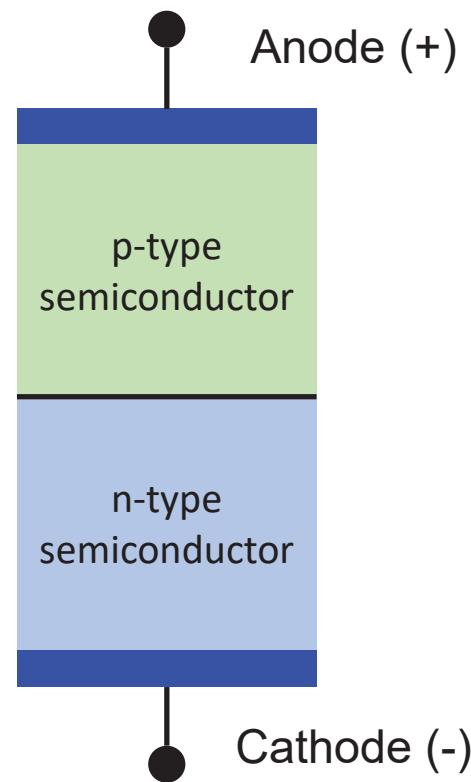
- Depletion region: No free charges due to proximity to region of different doping
- “High” electric field
- Free carriers can diffuse into depletion region and drift across it



# The pn-junction Diode



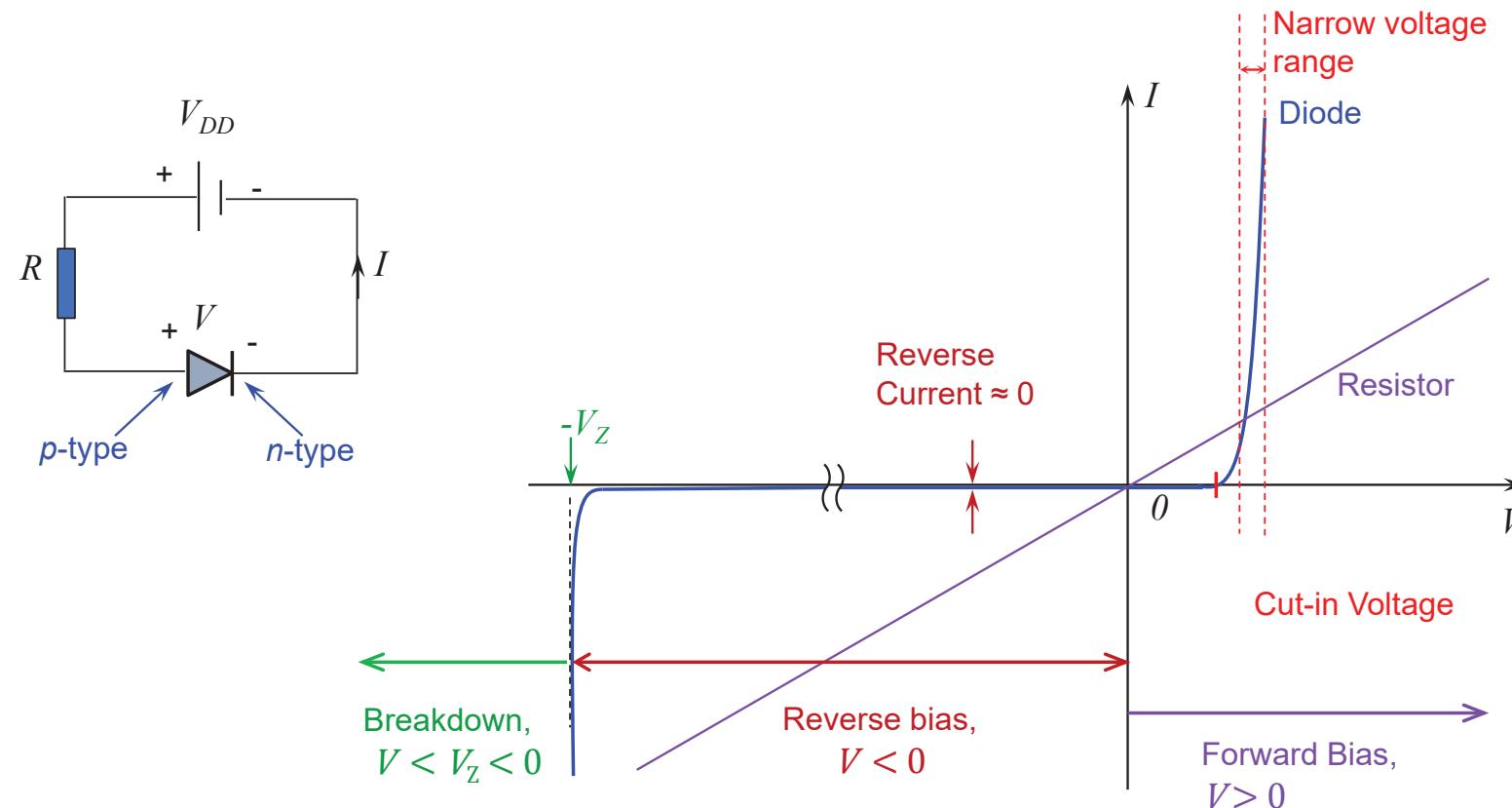
$$I_D = I_{D0} \left( e^{\frac{V_D}{\eta V_T}} - 1 \right)$$



$V_T$  : threshold voltage

$\eta$  : non-ideality factor

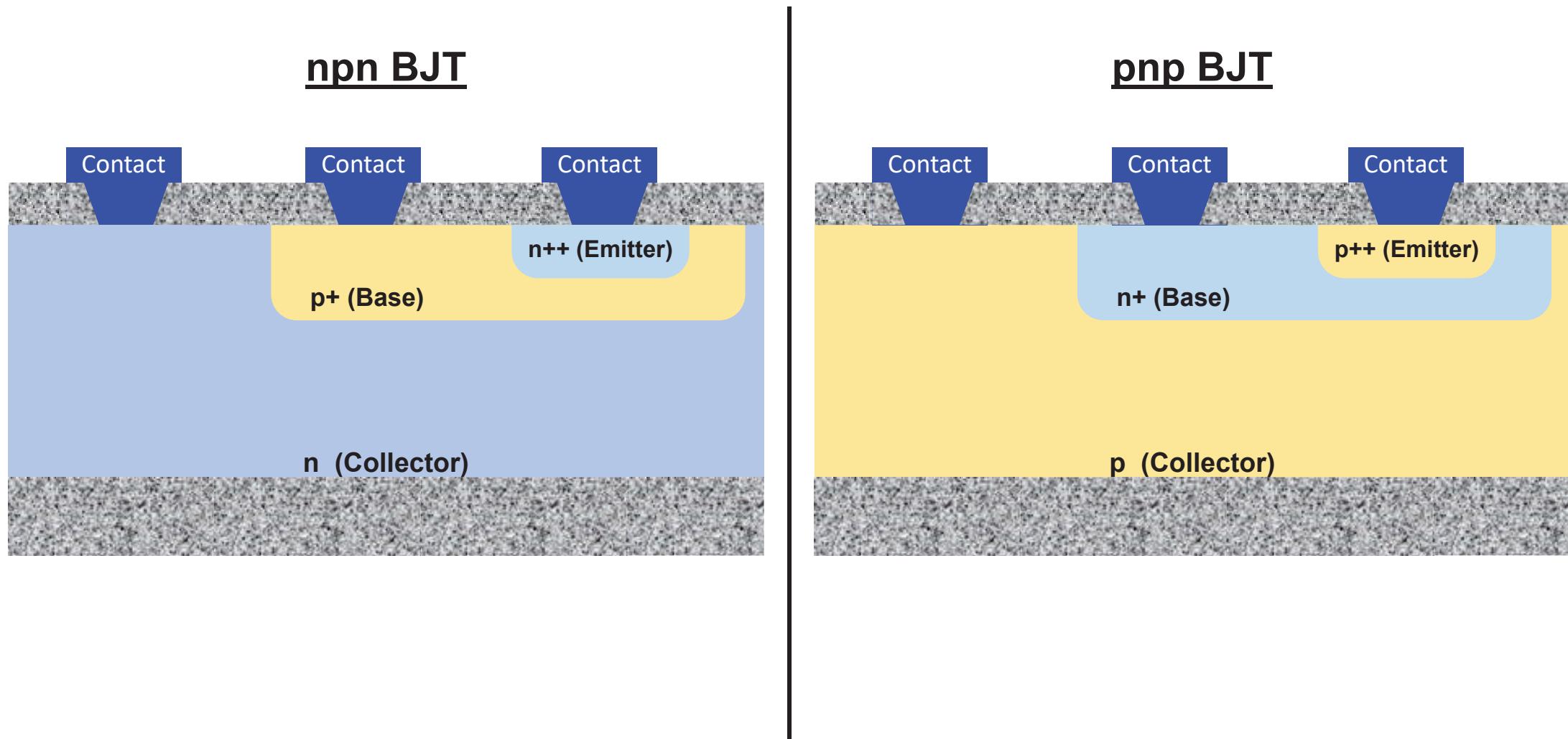
# Operating Characteristic of a Diode



# Week 1-4

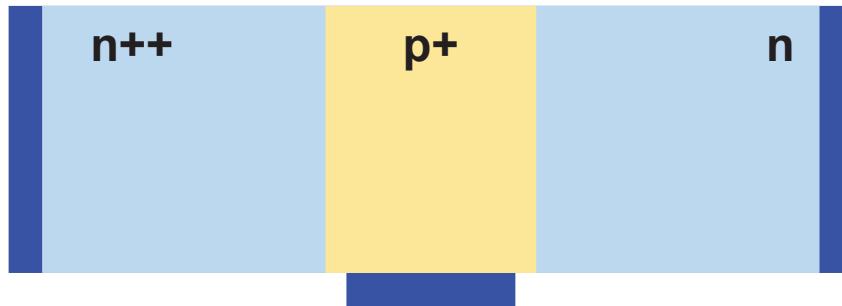
Introduction to the Bipolar Junction Transistor (BJT)

# The Bipolar Junction Transistor (BJT)

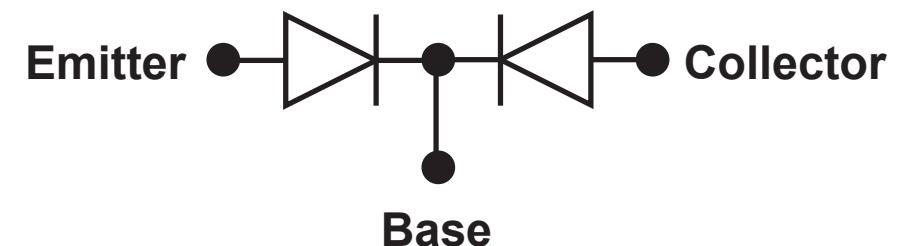
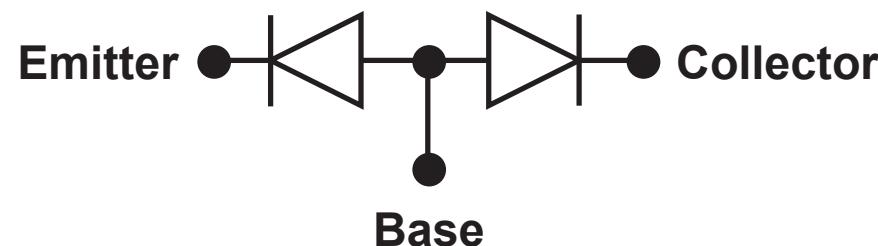
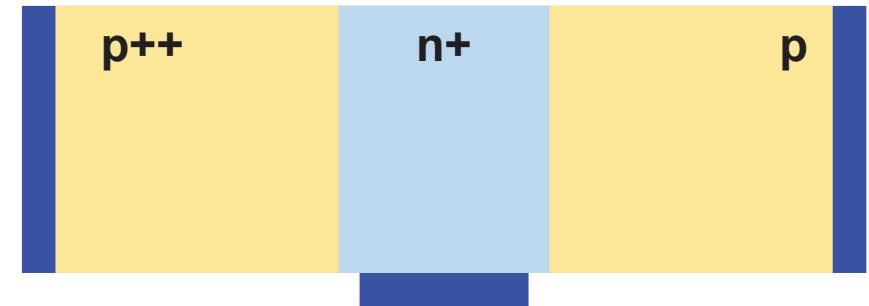


# The Bipolar Junction Transistor (BJT)

npn BJT

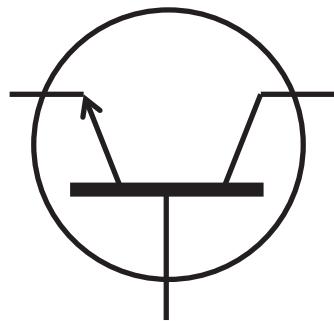


pnp BJT

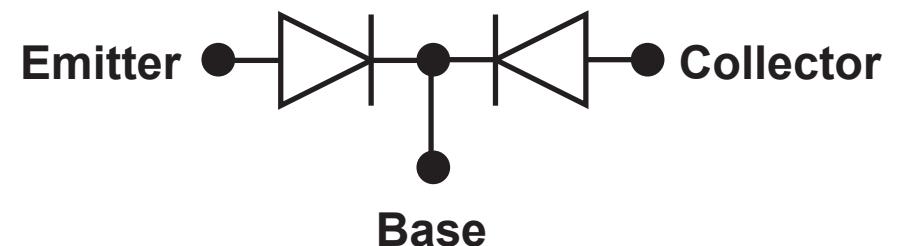
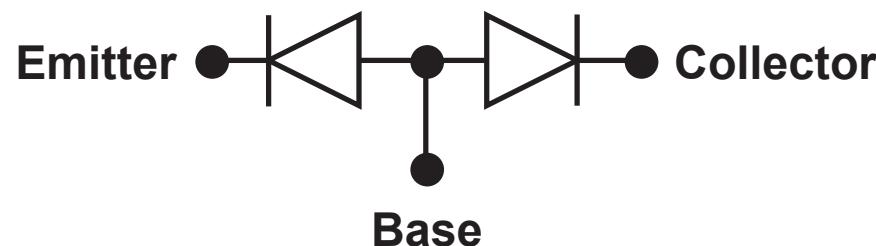
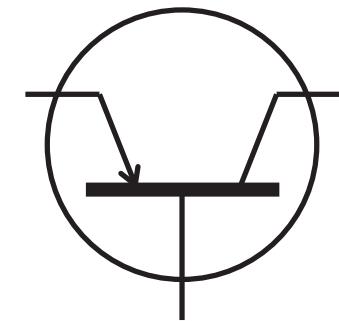


# The Bipolar Junction Transistor (BJT)

npn BJT

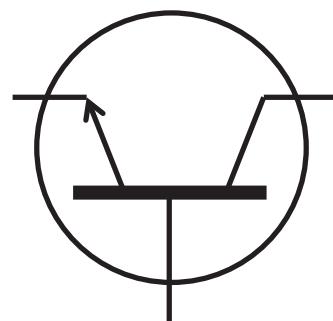


pnp BJT

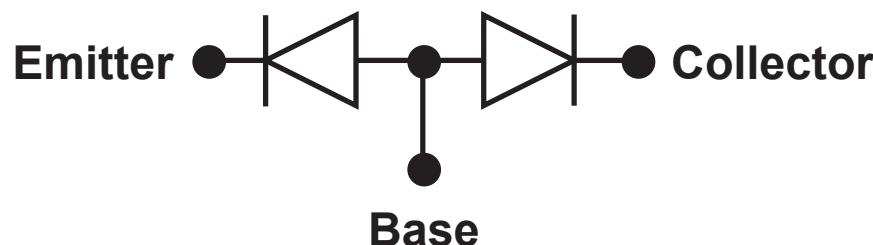


# The Bipolar Junction Transistor (BJT)

npn BJT



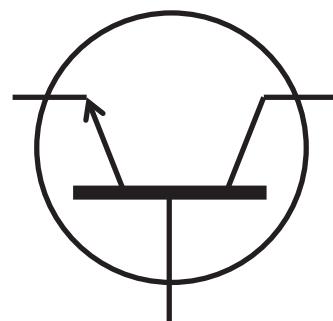
Region of Operation	Biassing of BE junction	Biassing of BC junction
Cut-off	Reverse	Reverse
Saturation	Forward	Forward
(Forward) Active	Forward	Reverse
(Reverse) Active	Reverse	Forward



**Reverse active region is usually avoided**

# The Bipolar Junction Transistor (BJT)

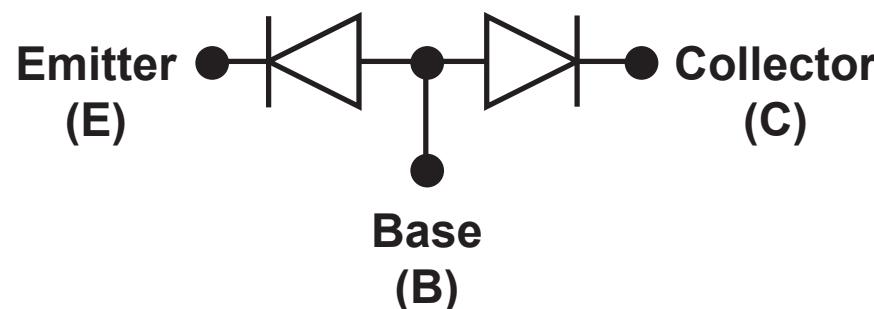
npn BJT



Region of Operation	Biasing of BE junction	Biasing of BC junction
Cut-off	Reverse	Reverse
Saturation	Forward	Forward
(Forward) Active	Forward	Reverse

$$V_{BE} = V_B - V_E \quad V_{BC} = V_B - V_C$$

$$V_{CE} = V_C - V_E = V_{BE} - V_{BC}$$

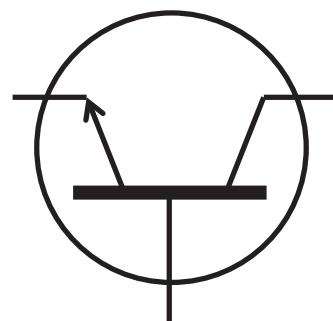


**Cut-off:**  $V_{BE} < 0.7 \text{ V}$  for Si pn-junctions

**Logic – OFF state**

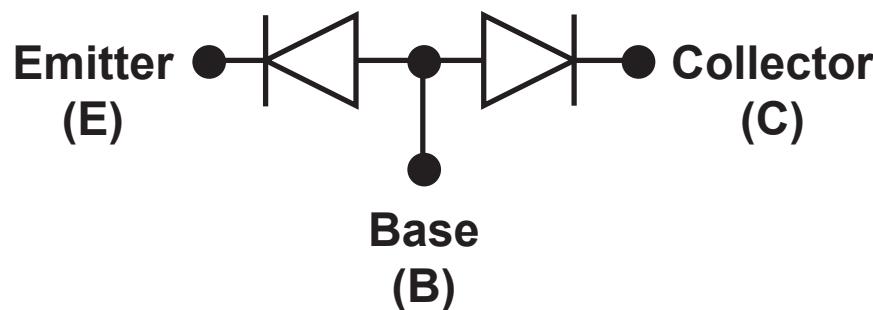
# The Bipolar Junction Transistor (BJT)

npn BJT



Region of Operation	Biasing of BE junction	Biasing of BC junction
Cut-off	Reverse	Reverse
<b>Saturation</b>	<b>Forward</b>	<b>Forward</b>
(Forward) Active	Forward	Reverse

$$V_{BE} = V_B - V_E \quad V_{BC} = V_B - V_C \\ V_{CE} = V_C - V_E = V_{BE} - V_{BC}$$



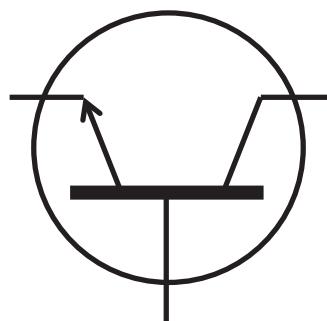
**Saturation:**

$V_{BE} \geq 0.7 \text{ V}$       for Si pn-junctions  
 $V_{BC} \geq 0.7 \text{ V}$

**Used for amplifier operation**

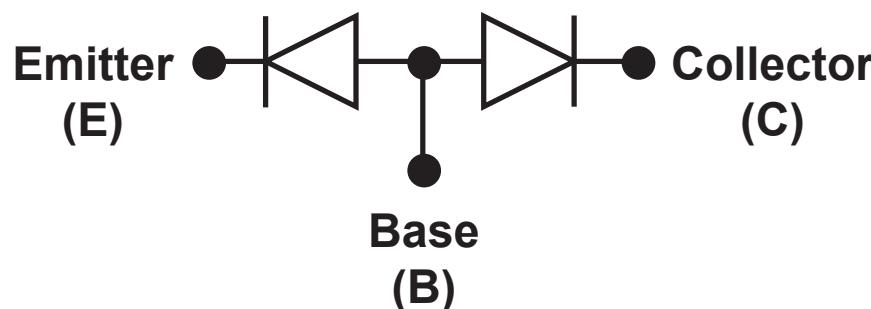
# The Bipolar Junction Transistor (BJT)

npn BJT



Region of Operation	Biasing of BE junction	Biasing of BC junction
Cut-off	Reverse	Reverse
Saturation	Forward	Forward
(Forward) Active	Forward	Reverse

$$V_{BE} = V_B - V_E \quad V_{BC} = V_B - V_C \\ V_{CE} = V_C - V_E = V_{BE} - V_{BC}$$

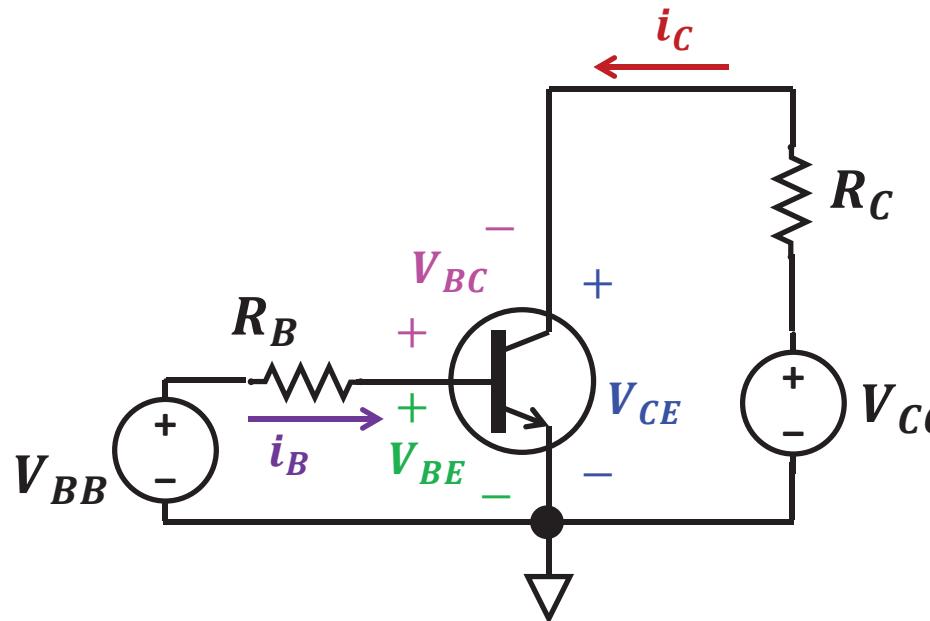


**Forward active:**

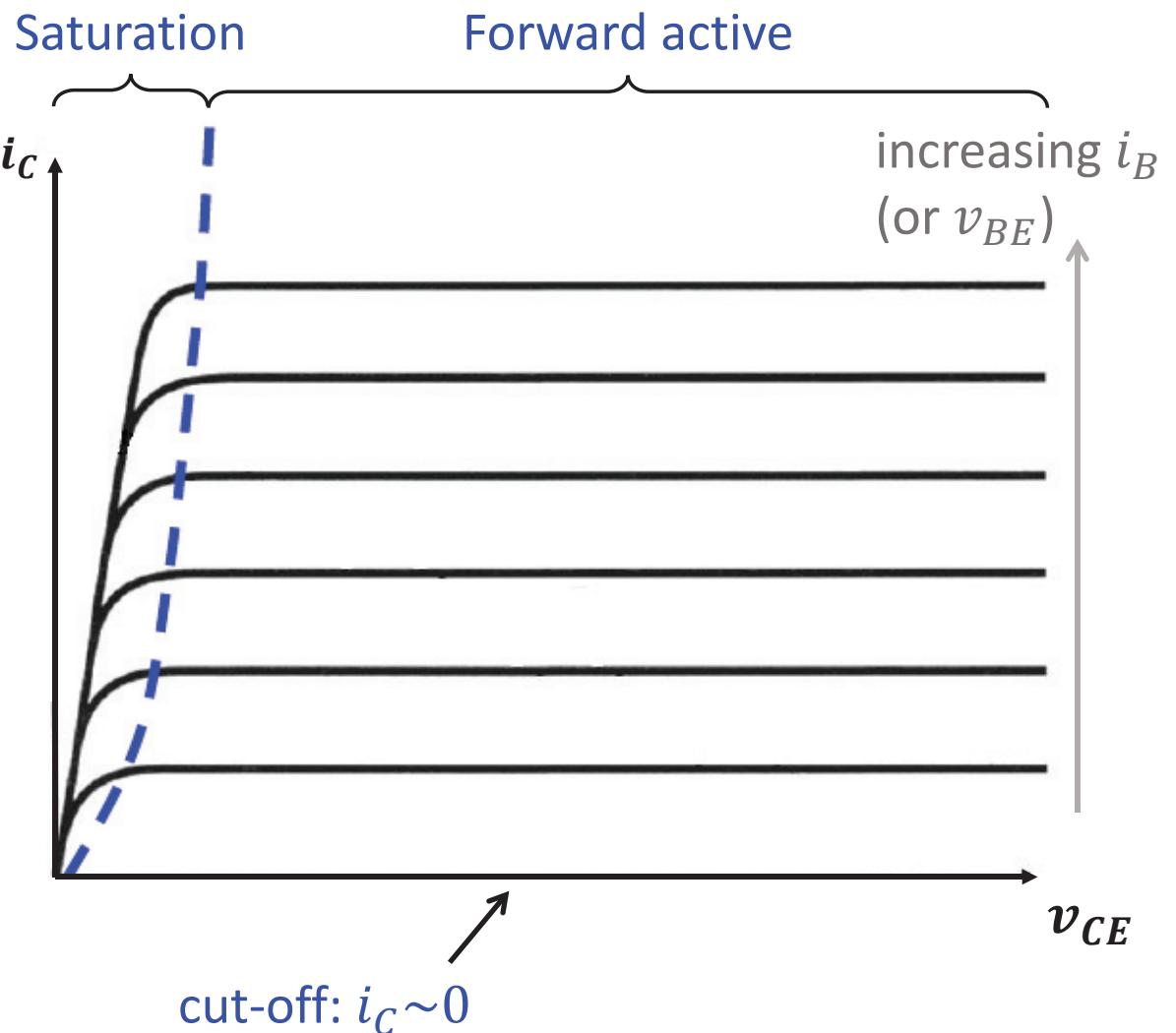
$V_{BE} \geq 0.7 \text{ V}$       for Si pn-junctions  
 $V_{BC} < 0.7 \text{ V}$

**Logic – ON state**

# $I-V$ Characteristics of the BJT



$i_C / i_B \geq 100$  in forward active  
good for amplifier operation



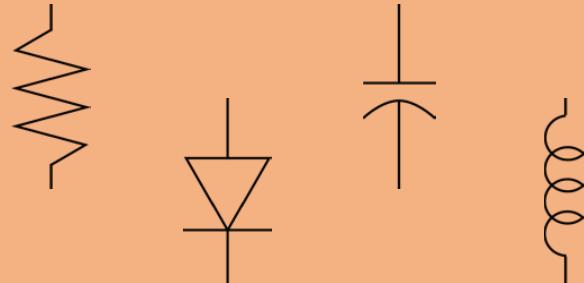
# Week 1-5

Introduction to the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET)

# Types of Devices

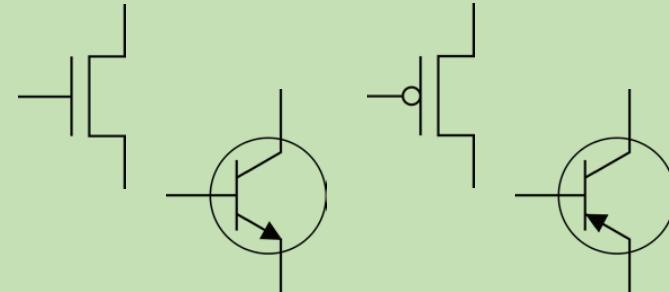
## Circuit Elements

### Passive Elements



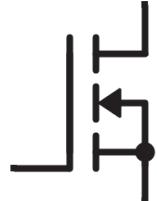
- Energy consumers or storage

### Active Elements



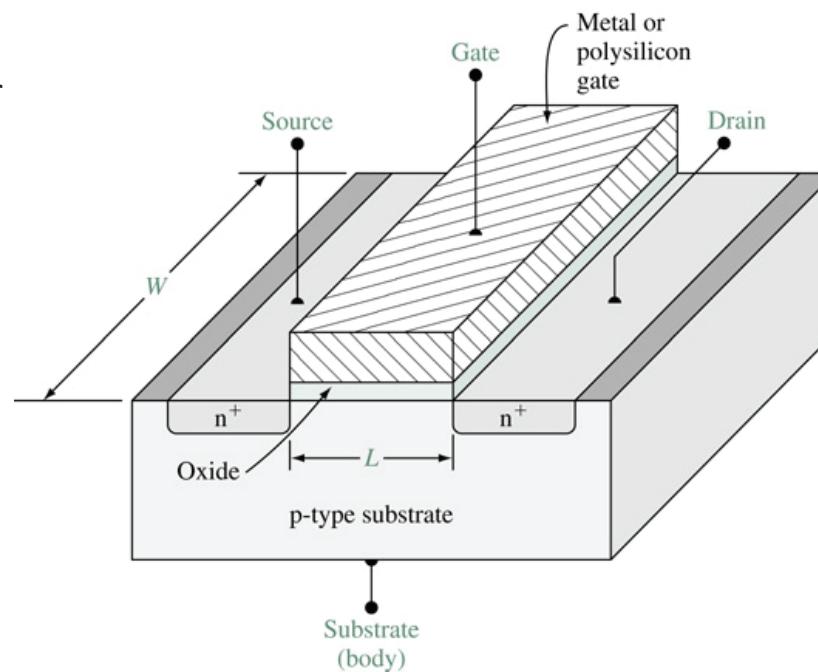
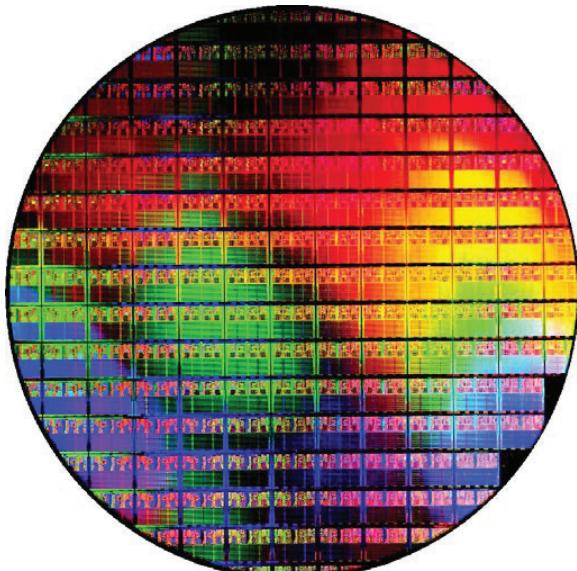
- Help provide energy/power gain
- Controls current direction
- Current and voltage control

# The Metal-Oxide-Semicon. Field-effect Transistor (FET)

	Enhancement Mode	Depletion Mode
n-channel	 A circuit diagram showing a vertical line representing the drain, a horizontal line representing the source, and a curved arrow pointing from the drain towards the source, indicating electron flow.	 A circuit diagram showing a vertical line representing the drain, a horizontal line representing the source, and a curved arrow pointing away from the drain towards the source, indicating electron flow.
p-channel	 A circuit diagram showing a vertical line representing the drain, a horizontal line representing the source, and a curved arrow pointing from the source towards the drain, indicating hole flow.	 A circuit diagram showing a vertical line representing the drain, a horizontal line representing the source, and a curved arrow pointing away from the source towards the drain, indicating hole flow.

# The Structure of Field-effect Transistor

- Substrate is crystalline silicon
  - Usually a big wafer that is 8" or 12" in diameter
  - Sometimes has flat sides or notches to indicate crystal orientation or doping

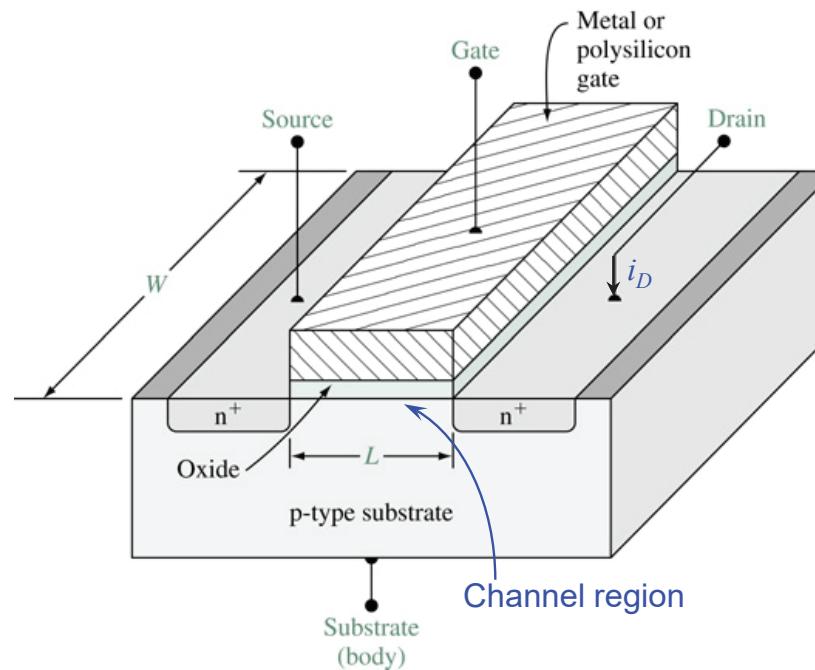


**Basic structure of an n-channel Enhancement mode MOSFET**

- A sequence of process steps is performed to physically make transistors
- Patterns of “windows” are created using combination of photoresist and photolithography steps (with the aid of a mask)
- Exposes areas on the silicon wafer where material needs to be deposited or removed
- Deposition:
  - Sputtering, ALD, electroplating, ion implantation for doping, oxidation
- Removal:
  - Wet/dry etching, ion milling, CMP

# The Structure of Field-effect Transistor

- Channel Width,  $W$
- Gate Length,  $L$ 
  - Usually the smallest dimension
  - Also called “Feature Size”
- Gate vs Channel Length
  - $L_{\text{gate}}$  versus  $L_{\text{channel}}$

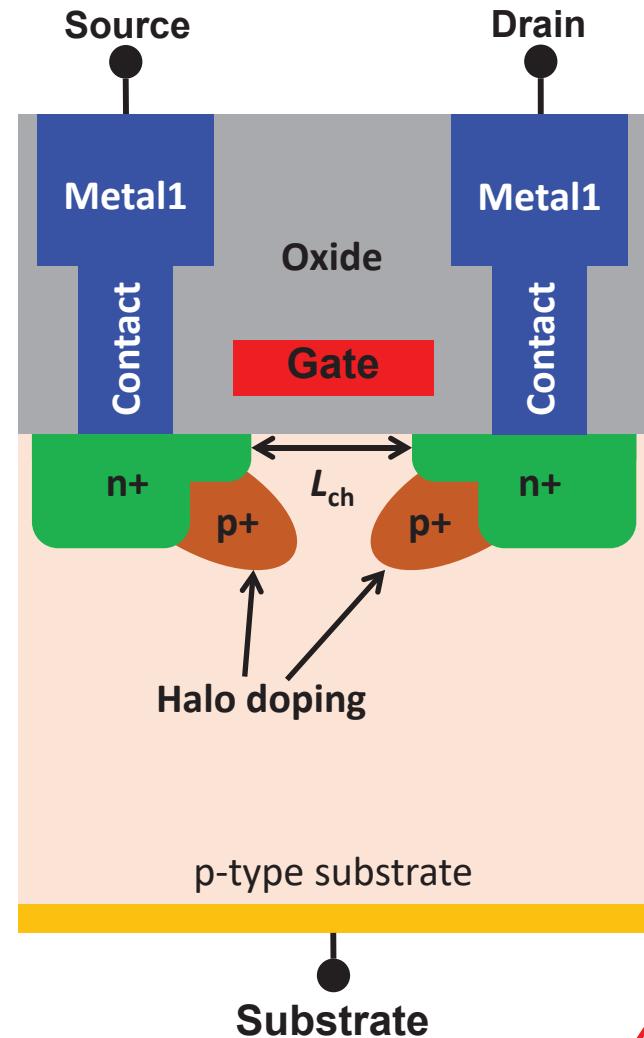


- Drain has higher voltage than source
- Current flows:
  - Into drain from external circuit
  - from drain to source inside the channel region
  - Out of source to external circuit

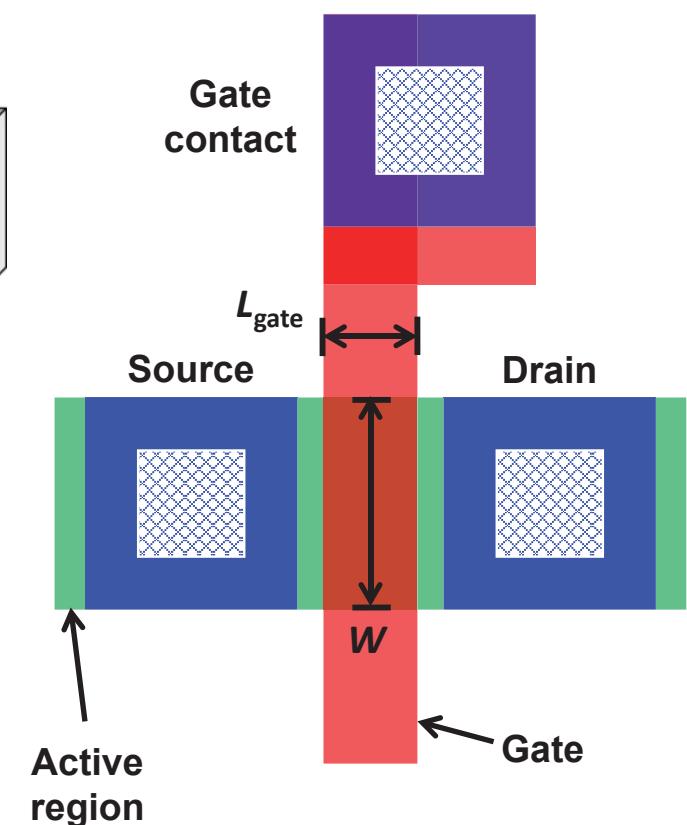
**Basic structure of an n-channel Enhancement mode MOSFET**

# The Structure of Field-effect Transistor

Side cross-section view

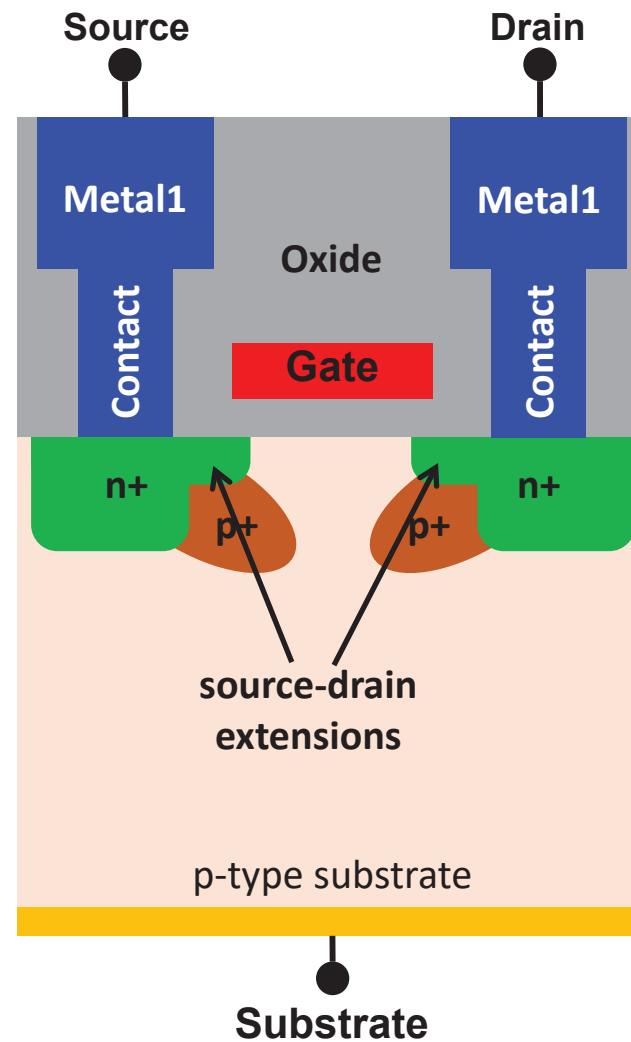


Top-down Layout view

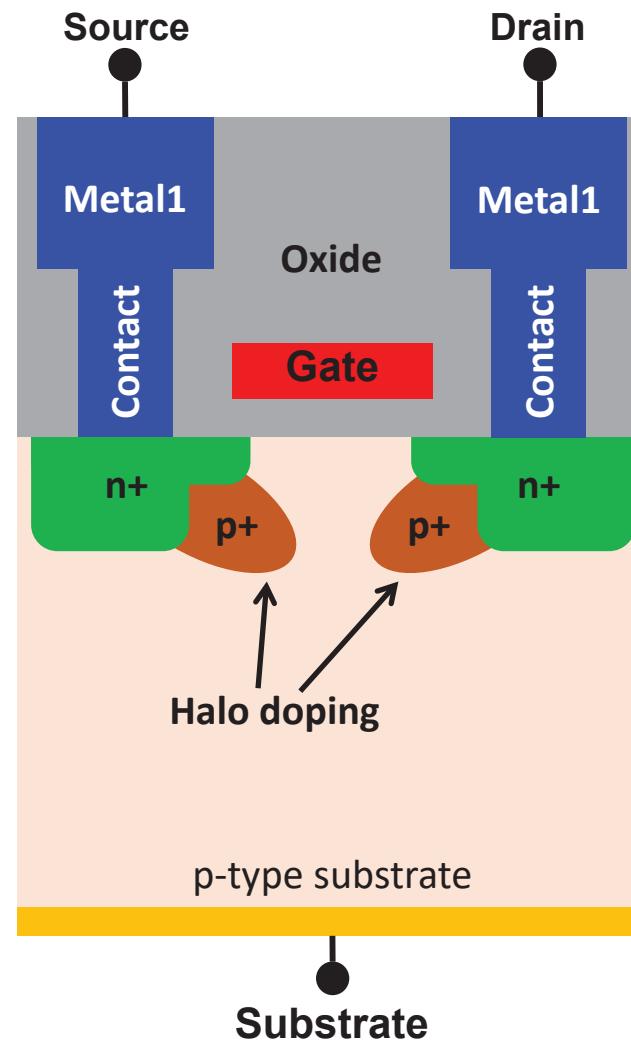


Basic structure of an n-channel  
Enhancement mode MOSFET

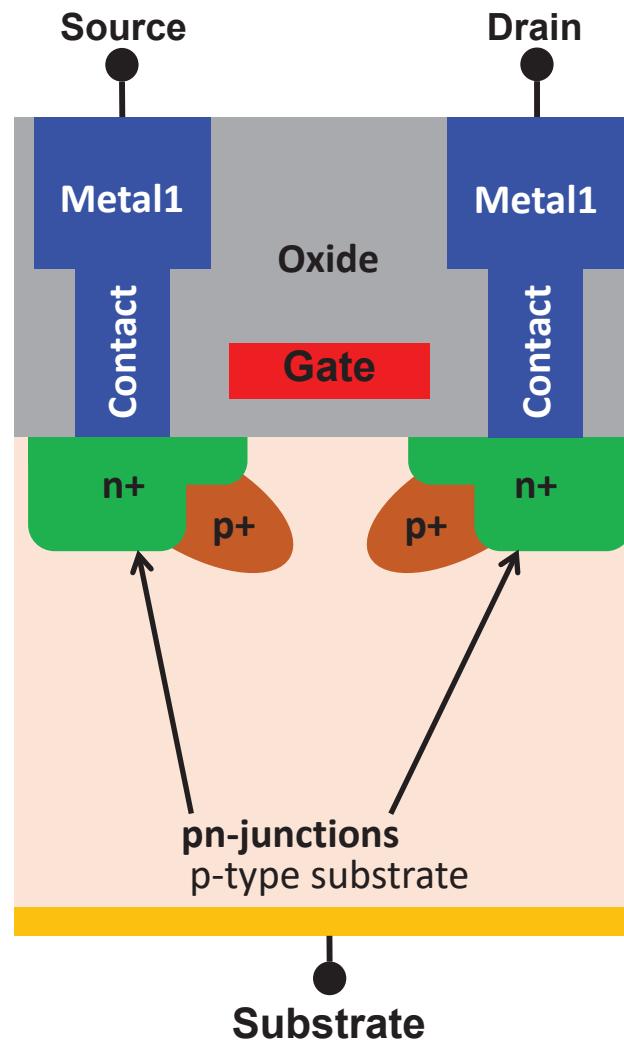
# Parts of the Field-effect Transistor



# Parts of the Field-effect Transistor

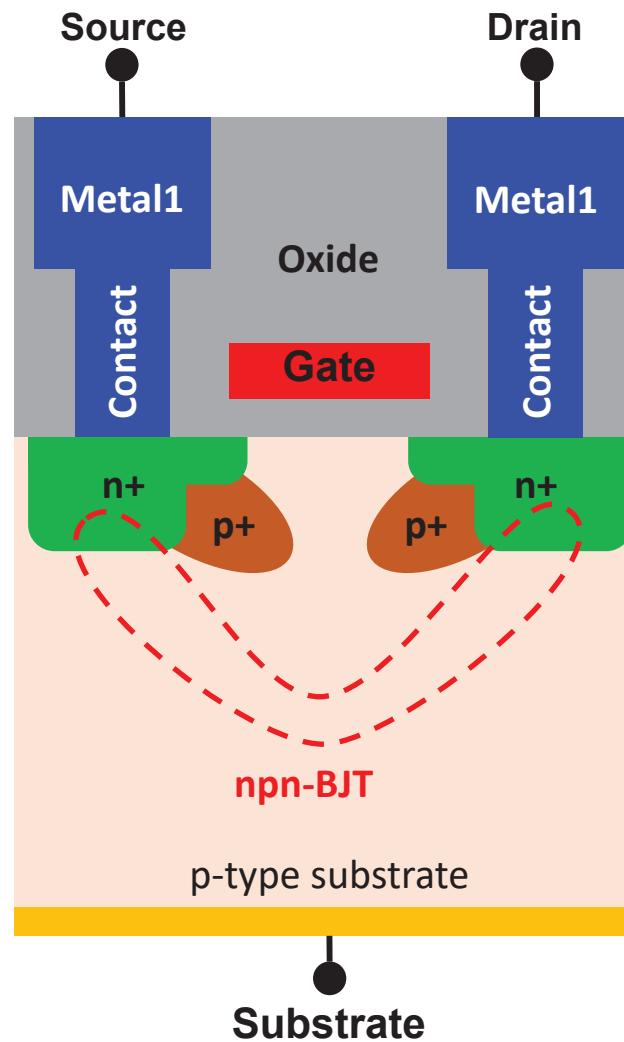


# Parts of the Field-effect Transistor



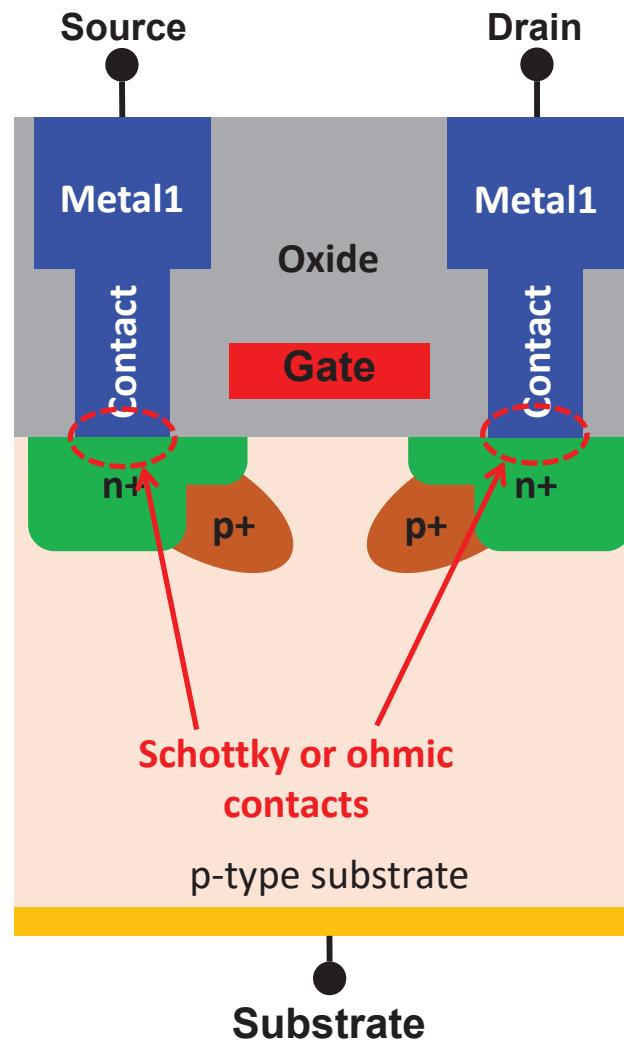
- pn-junctions form a parasitic diodes
- Diodes are rectifying elements
  - Good at passing current from p-type to n-type semiconductor

# Parts of the Field-effect Transistor



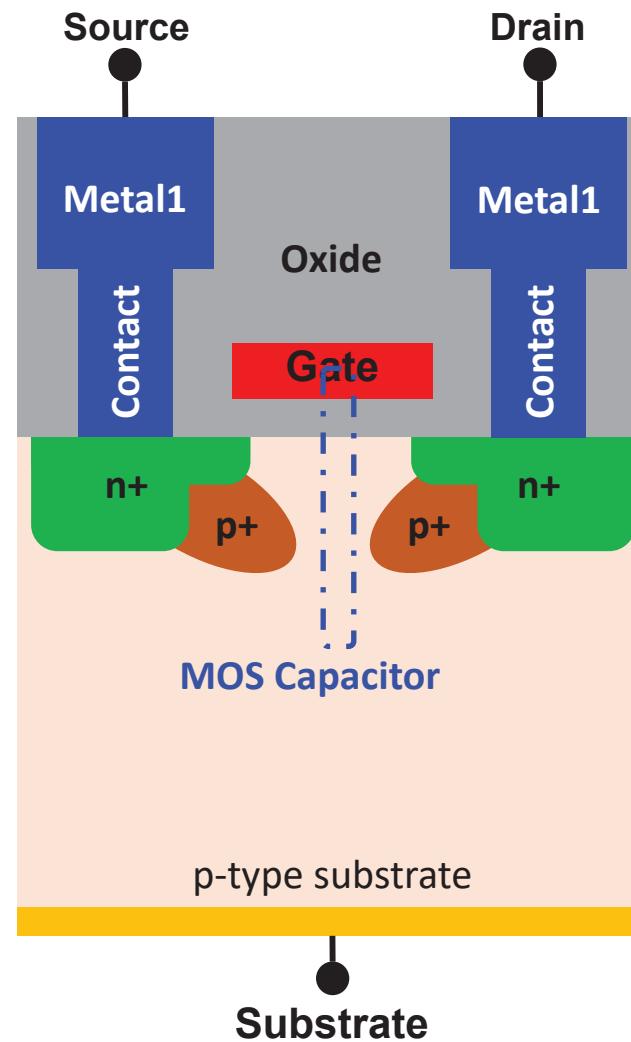
- Parasitic bipolar junction transistor (BJT) formed by back-to-back pn-junctions

# Parts of the Field-effect Transistor



- Schottky contact has rectifying characteristic like pn-junction
- Ohmic contact like a resistor

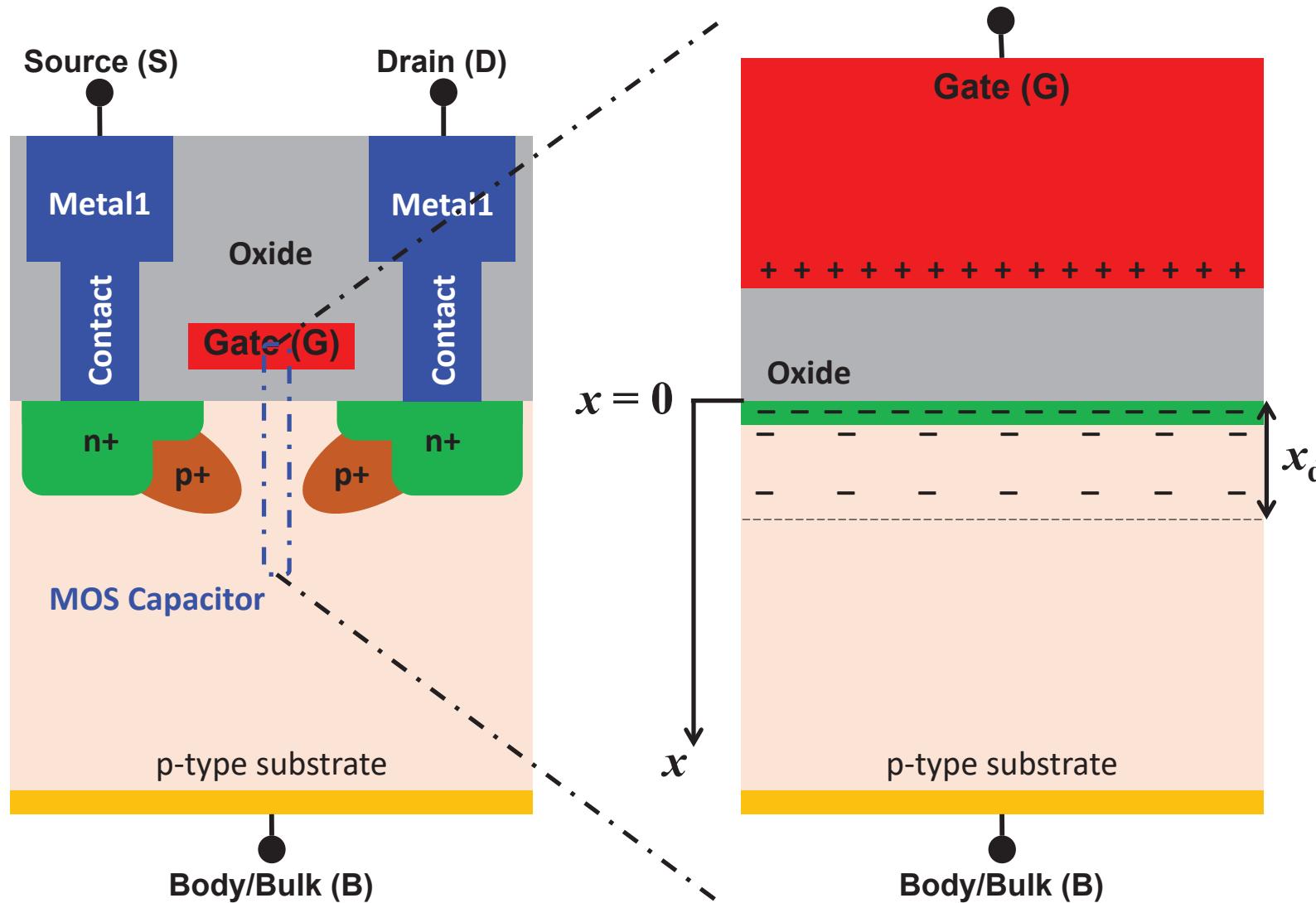
# Parts of the Field-effect Transistor



# Week 1-6

IV Characteristic of the n-Channel Enhancement Mode MOSFET

# Electrical Characteristic of the Field-effect Transistor



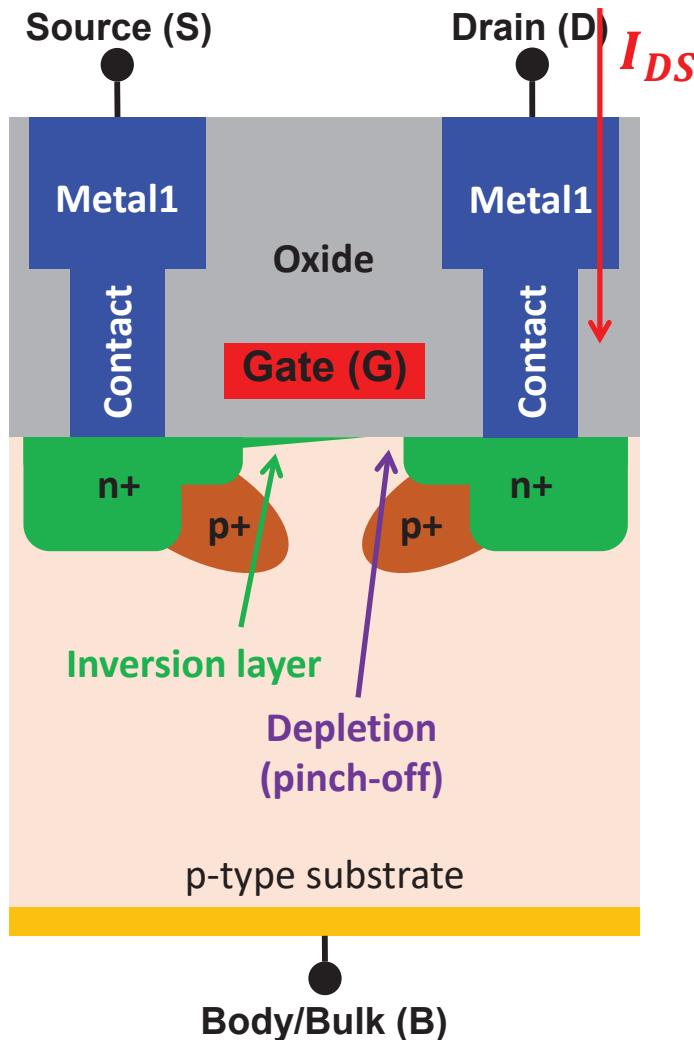
- Charges added to gate must be balanced by charges in substrate so that overall charge is zero (charge neutrality)
- Formation of inversion layer shorts the source and drain terminals
- Low resistance that allows current to flow easily

# Terminology

Variable	Meaning
$I_{DS}$ or $I_D$	The current flowing <u>into</u> the drain terminal of the MOSFET
$V_G$	Voltage of the gate terminal
$V_S$	Voltage of the source terminal
$V_D$	Voltage of the drain terminal
$V_B$	Voltage of the body terminal
$V_{GS}$	$V_G - V_S$
$V_{DS}$	$V_D - V_S$
$V_{SB}$	$V_S - V_B$

$$V_{AB} = V_A - V_B$$

# The Square Law Model



Generally,

$$I_{DS} = \beta_n \left( V_{GS} - V_{TN} - \frac{V_{DS,SAT}}{2} \right) V_{DS,SAT} (1 + \lambda_n V_{DS}) \quad (\text{saturation})$$

$$I_{DS} = \beta_n \left( V_{GS} - V_{TN} - \frac{V_{DS}}{2} \right) V_{DS} (1 + \lambda_n V_{DS}) \quad (\text{linear / triode})$$

$$I_{DS} \approx 0 \quad (\text{off / cut-off})$$

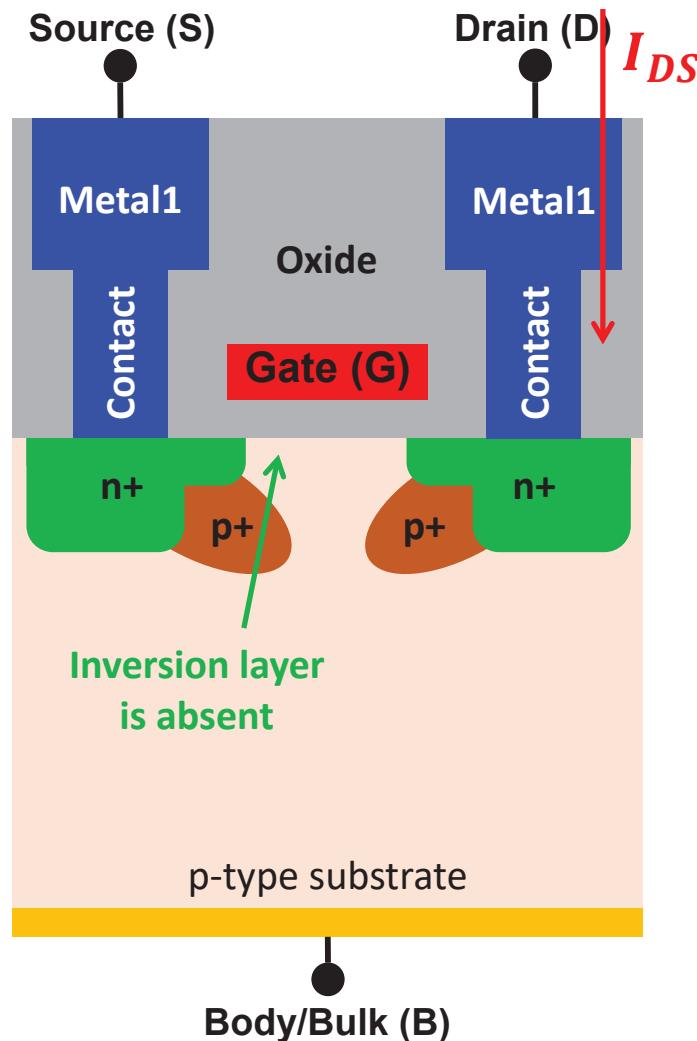
$$\lambda_n, \beta_n = k_n \frac{W}{L_{ch}} = \frac{\mu_n C_{OX} W}{L_{ch}} > 0$$

**Cut-off:**  $V_{GS} < V_{TN}$

**Linear:**  $V_{GS} \geq V_{TN}; V_{DS} < V_{DS,SAT}$

**Saturation:**  $V_{GS} \geq V_{TN}; V_{DS} \geq V_{DS,SAT}$

# n-channel Enhancement Mode MOSFET in Cut-off

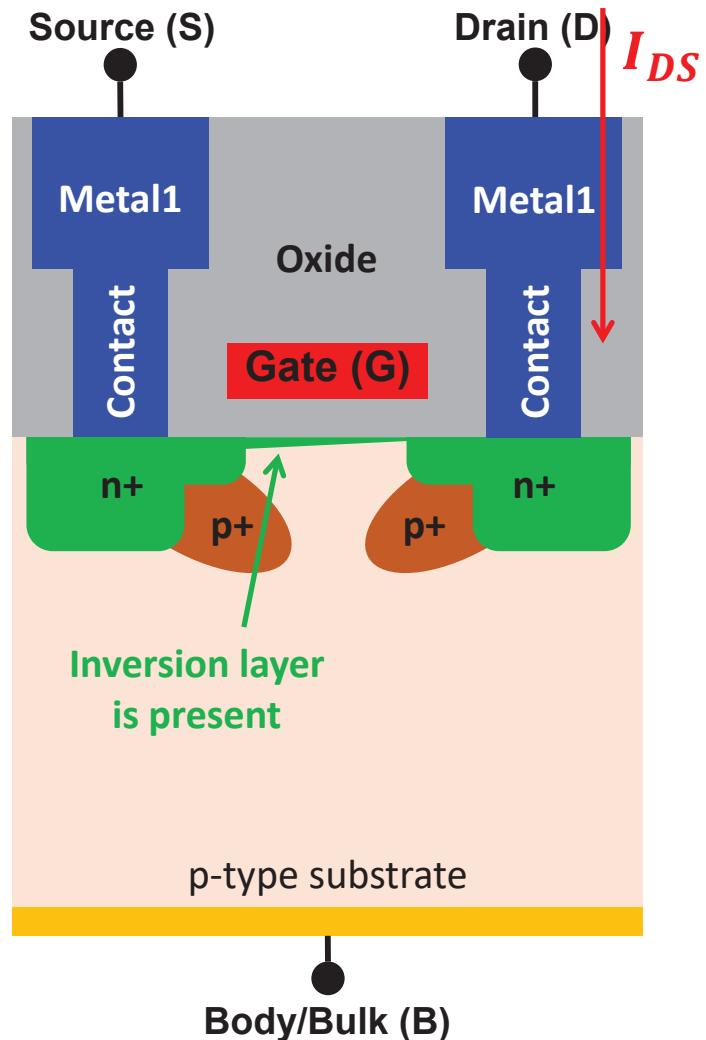


$$V_{GS} < V_{TN}$$

- Too few charges on gate to induce formation of inversion layer
- High resistance (low conductance) between source and drain terminals

$$I_D \approx 0 \text{ A (ideally)}$$

# n-channel Enhancement Mode MOSFET in Linear



$$V_{GS} \geq V_{TN}; V_{DS} < V_{DS,SAT}$$

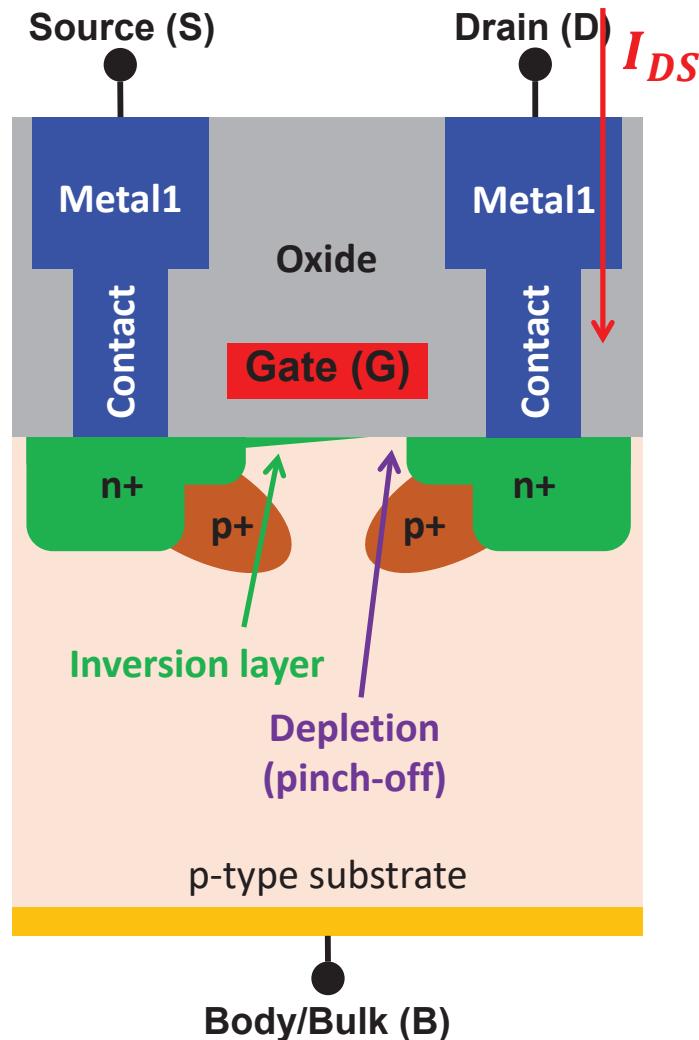
- Inversion layer is formed completely between source and drain terminals
- Low resistance (high conductance) between source and drain terminals

$$I_D = \mu_n C_{OX} \frac{W}{L_{ch}} \left( V_{GS} - V_{TN} - \frac{V_{DS}}{2} \right) V_{DS}$$

Channel length modulation neglected

$$I_D \approx \mu_n C_{OX} \frac{W}{L_{ch}} (V_{GS} - V_{TN}) V_{DS} \text{ at small } V_{DS}$$

# n-channel Enhancement Mode MOSFET in Saturation



$$V_{GS} \geq V_{TN}; V_{DS} \geq V_{DS,SAT}$$

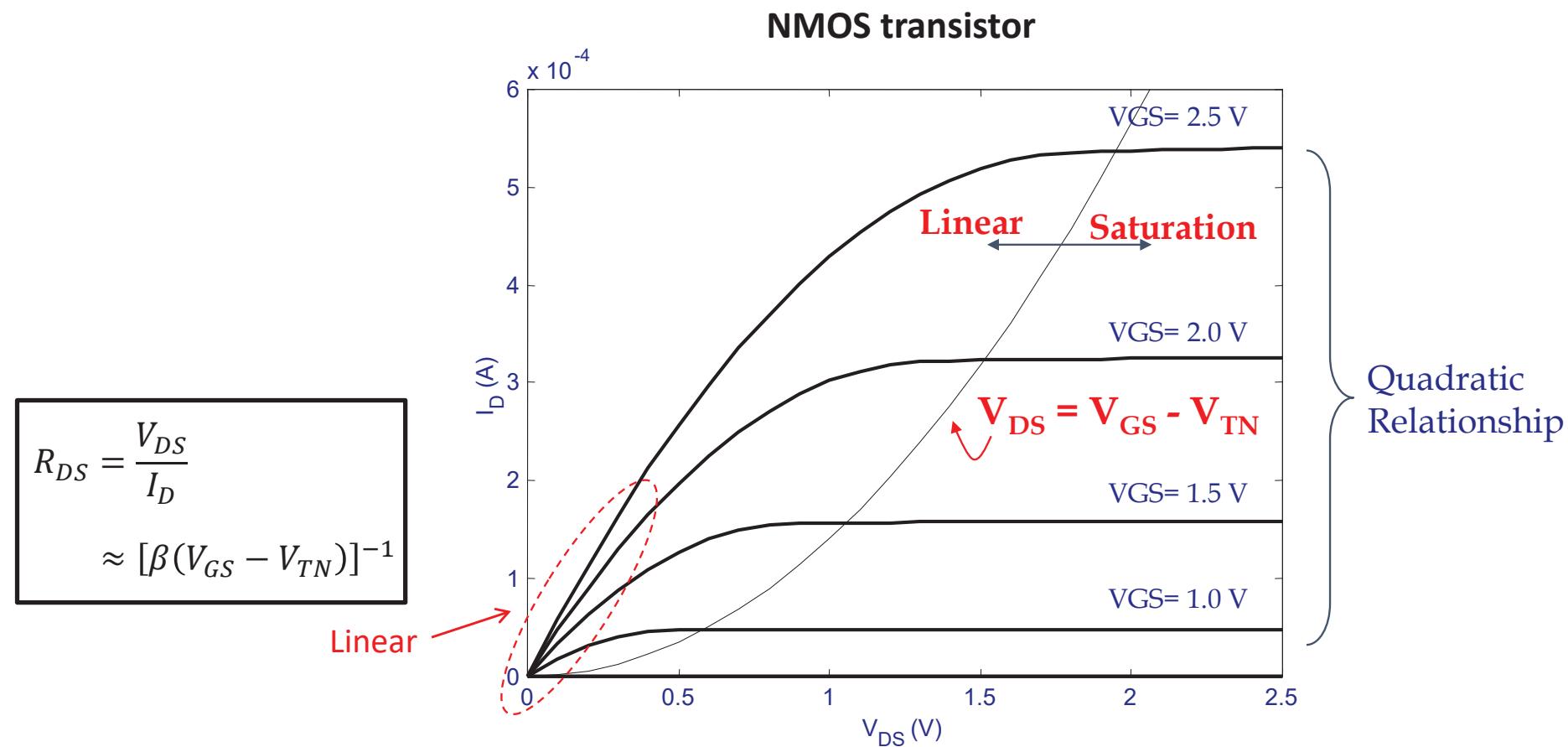
- Inversion layer is pinched-off near drain terminal
- Like a current source between source and drain terminals

$$I_D = \mu_n C_{ox} \frac{W}{L_{ch}} \left( V_{GS} - V_{TN} - \frac{V_{DS,SAT}}{2} \right) V_{DS,SAT}$$

Channel length modulation neglected

$$V_{DS,SAT} = V_{GS} - V_{TN} \text{ (long channel MOSFET)}$$

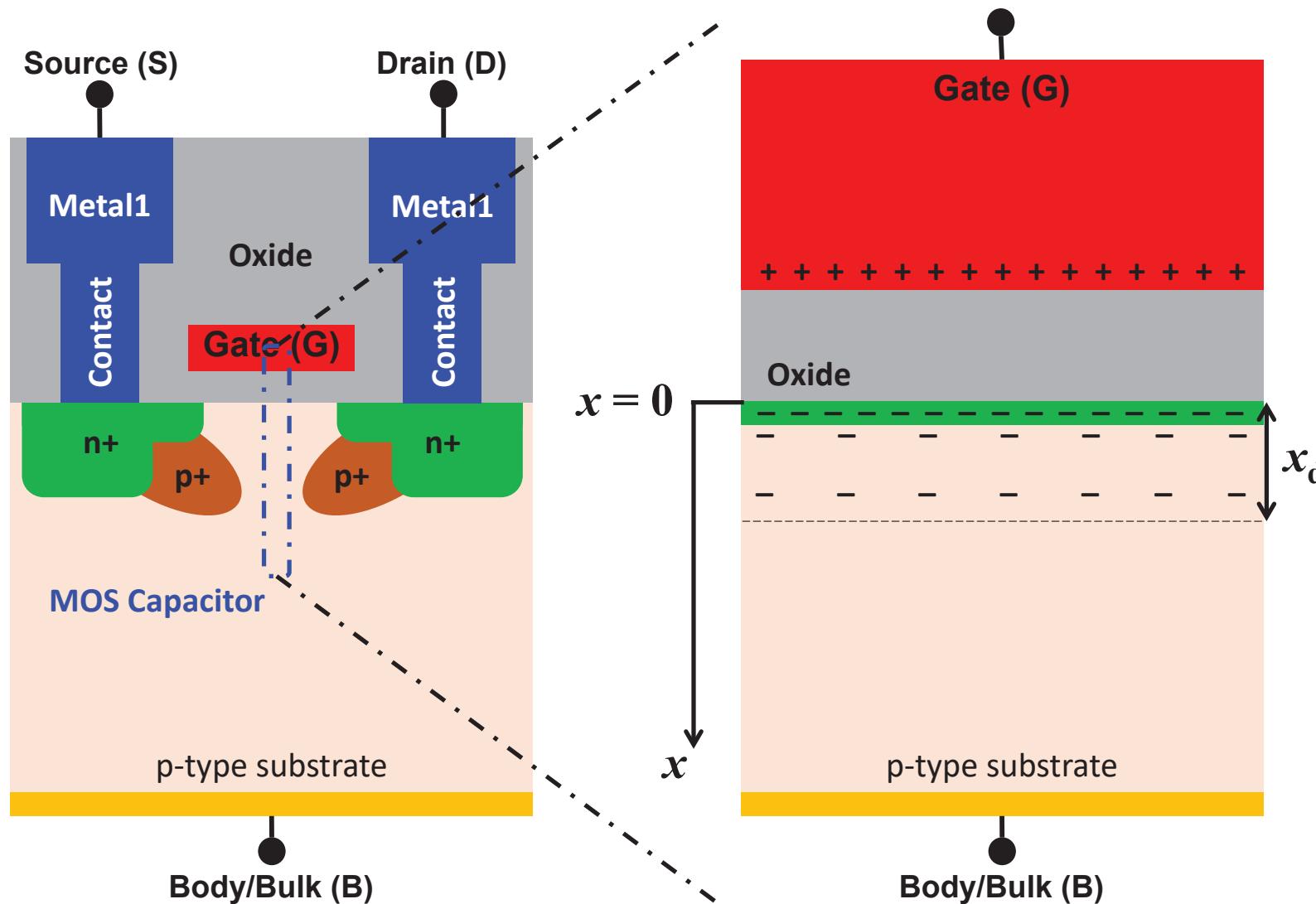
# The $I$ - $V$ Characteristic



# Week 1-7

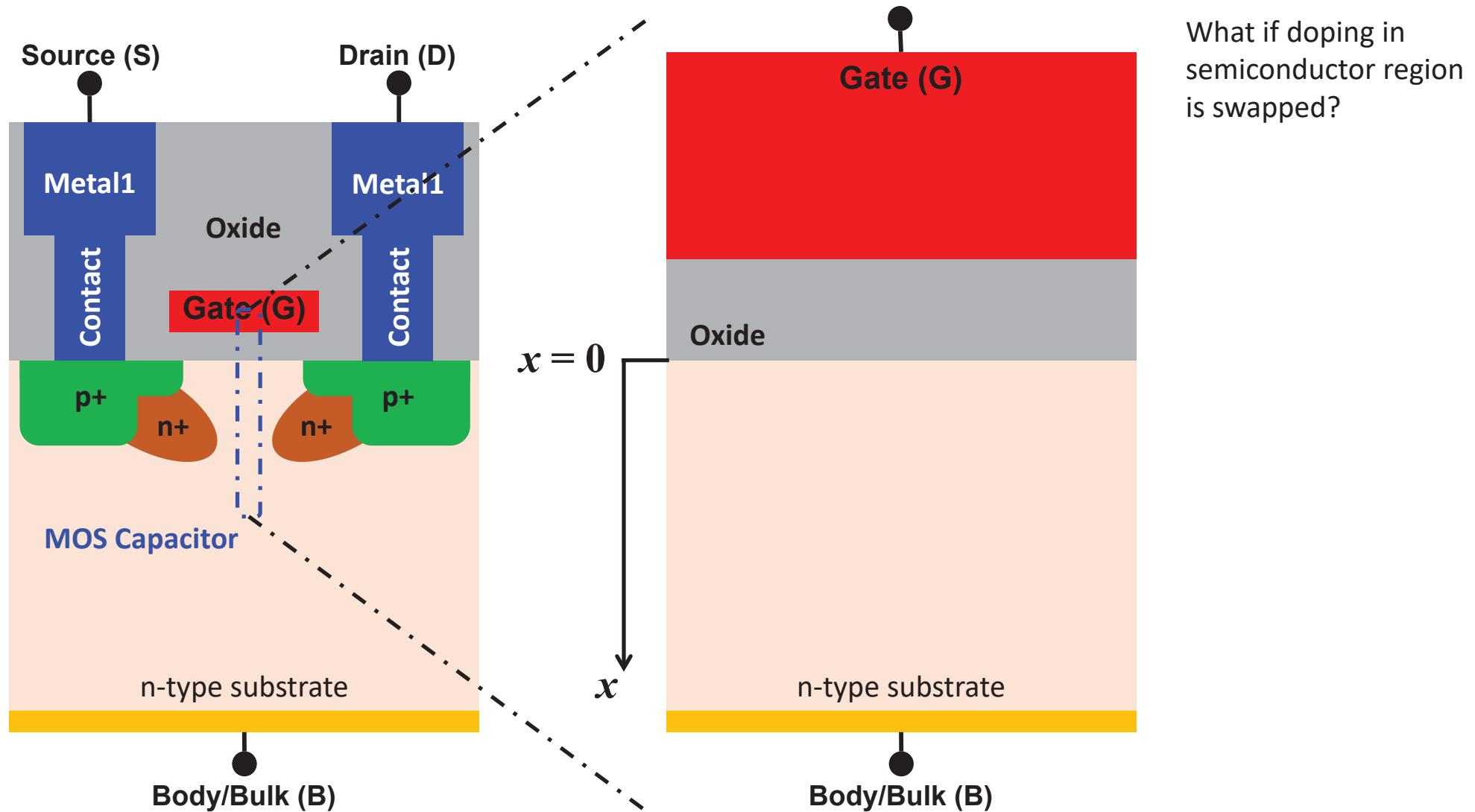
IV Characteristic of the p-Channel Enhancement Mode MOSFET

# n-Channel Enhancement Mode Field-effect Transistor

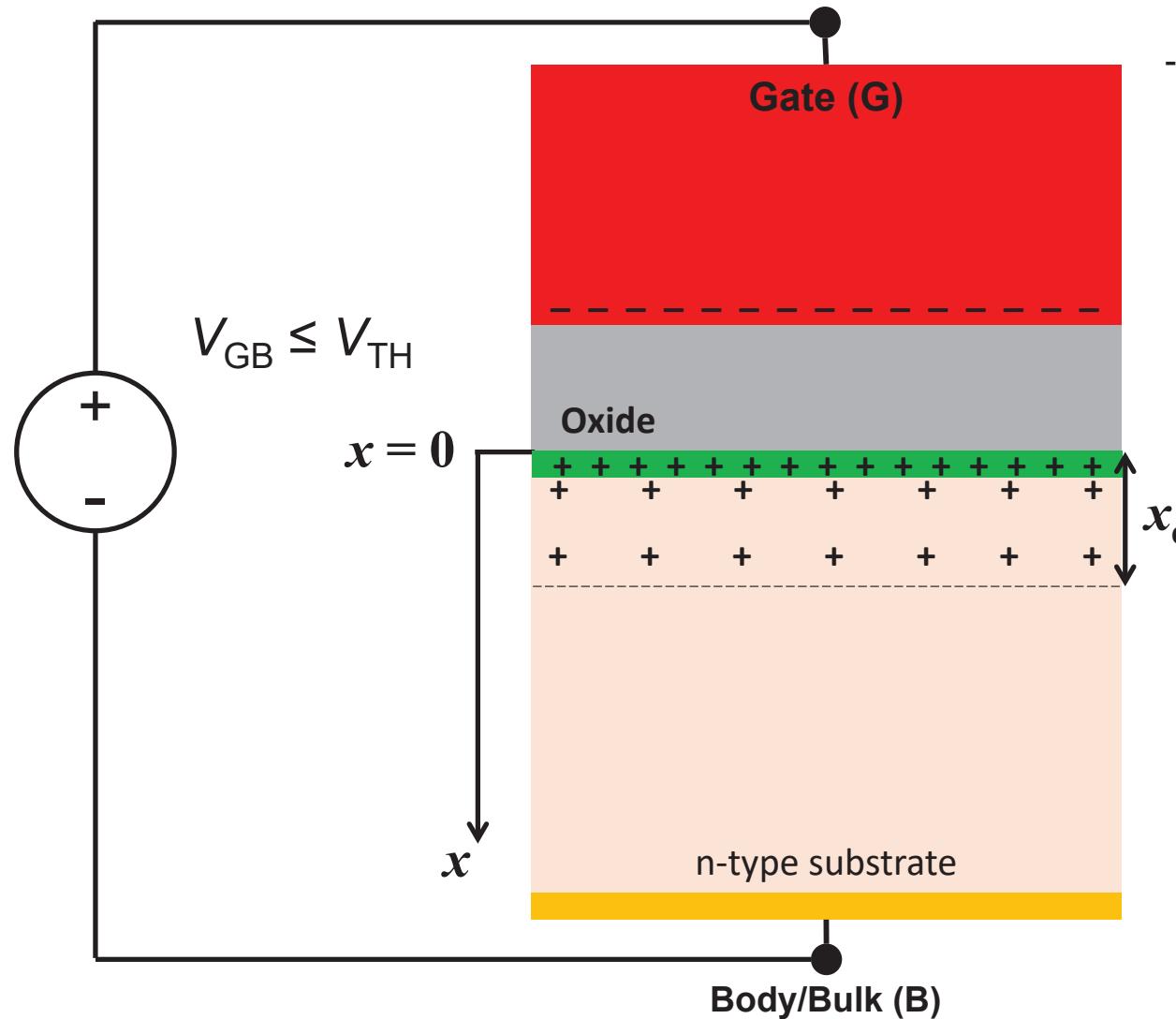


- Charges added to gate must be balanced by charges in substrate so that overall charge is zero (charge neutrality)
- Formation of inversion layer shorts the source and drain terminals
- Low resistance that allows current to flow easily

# p-Channel Enhancement Mode Field-effect Transistor

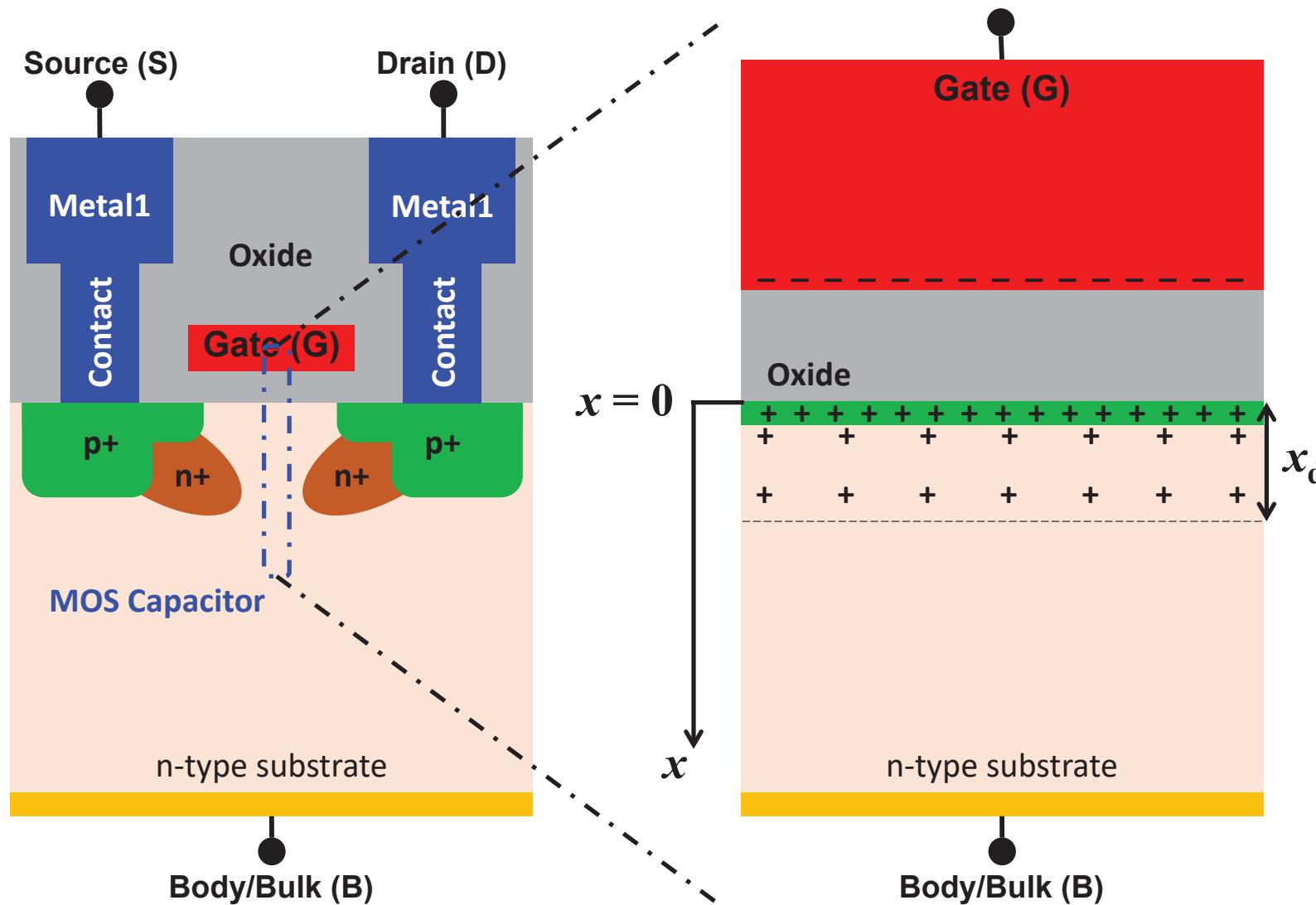


# MOS Capacitor – Inversion



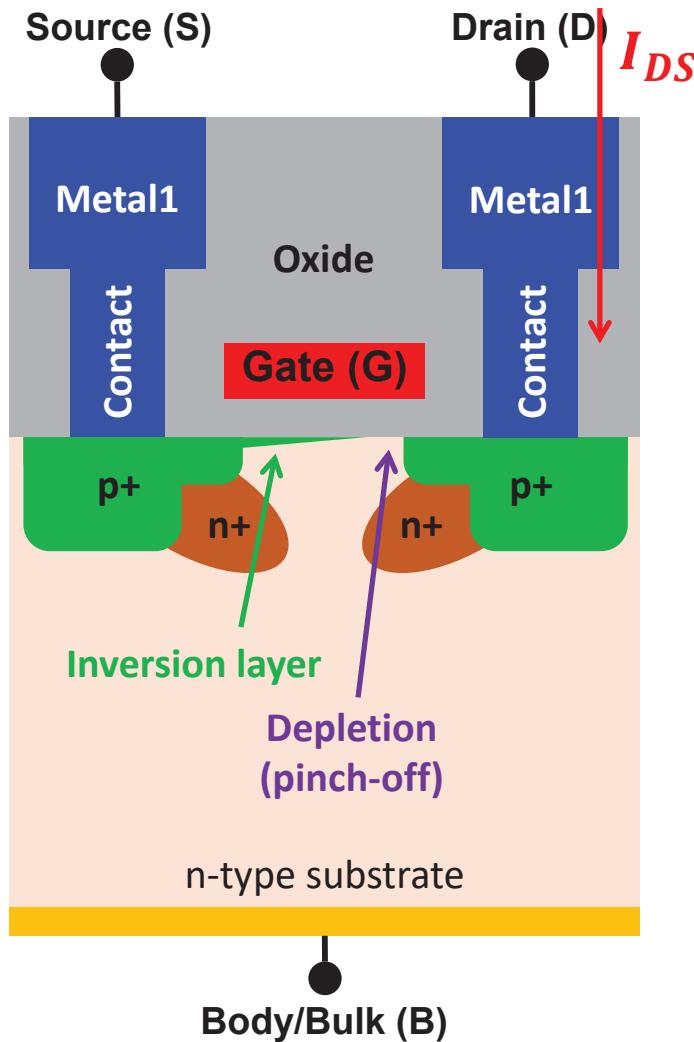
- MOS capacitor operation works conceptually the same
  - Voltage polarity is swapped since negative charges are added onto gate to create inversion layer

# p-Channel Enhancement Mode Field-effect Transistor



- Conceptually the same as n-channel
- Opposite charges
  - Polarity of voltage is opposite
- Formation of inversion layer shorts the source and drain terminals
- Low resistance that allows current to flow easily

# The Square Law Model



Generally,

$$I_{DS} = \beta_p \left( V_{GS} - V_{TP} - \frac{V_{DS,SAT}}{2} \right) V_{DS,SAT} (1 + \lambda_p V_{DS}) \quad (\text{saturation})$$

$$I_{DS} = \beta_p \left( V_{GS} - V_{TP} - \frac{V_{DS}}{2} \right) V_{DS} (1 + \lambda_p V_{DS}) \quad (\text{linear / triode})$$

$$I_{DS} \approx 0 \quad (\text{off / cut-off})$$

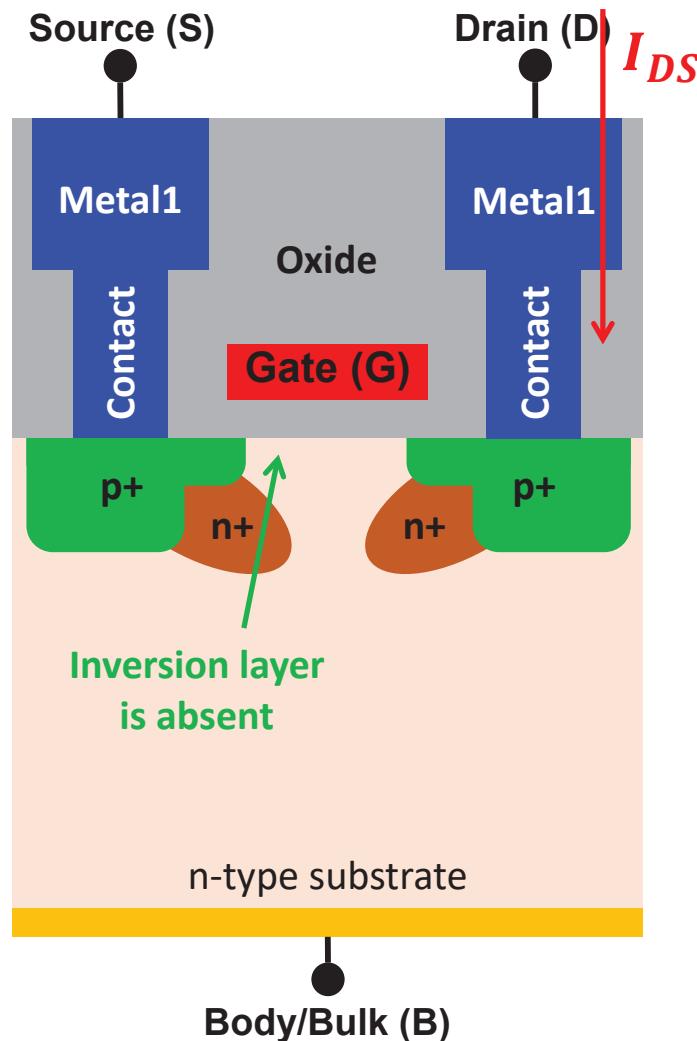
$$\lambda_p, \beta_p = k_p \frac{W}{L_{ch}} = \frac{\mu_p C_{OX} W}{L_{ch}} < 0$$

**Cut-off:**  $V_{GS} > V_{TP}$

**Linear:**  $V_{GS} \leq V_{TP}; V_{DS} > V_{DS,SAT}$

**Saturation:**  $V_{GS} \leq V_{TP}; V_{DS} \leq V_{DS,SAT}$

# p-channel Enhancement Mode MOSFET in Cut-off

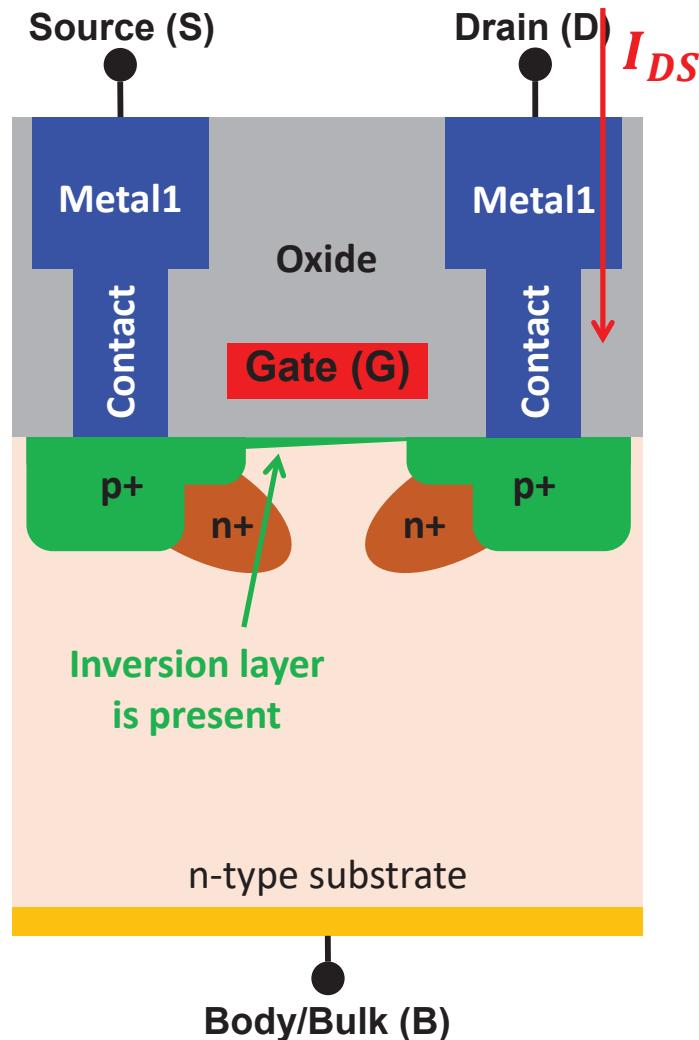


$$V_{GS} > V_{TP}$$

- Too few charges on gate to induce formation of inversion layer
- High resistance (low conductance) between source and drain terminals

$$I_D \approx 0 \text{ A (ideally)}$$

# p-channel Enhancement Mode MOSFET in Linear



$$V_{GS} \leq V_{TP}; V_{DS} > V_{DS,SAT}$$

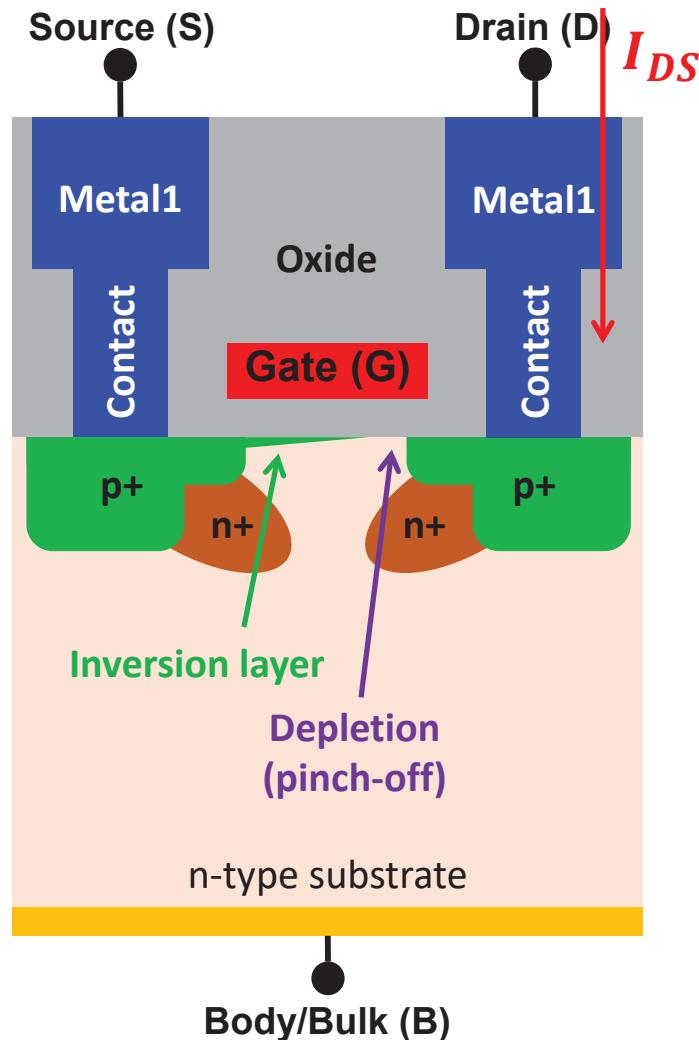
- Inversion layer is formed completely between source and drain terminals
- Low resistance (high conductance) between source and drain terminals

$$I_D = \mu_p C_{OX} \frac{W}{L_{ch}} \left( V_{GS} - V_{TP} - \frac{V_{DS}}{2} \right) V_{DS}$$

Channel length modulation neglected

$$I_D \approx \mu_p C_{OX} \frac{W}{L_{ch}} (V_{GS} - V_{TP}) V_{DS} \text{ at small } V_{DS}$$

# p-channel Enhancement Mode MOSFET in Saturation



$$V_{GS} \leq V_{TP}; V_{DS} \leq V_{DS,SAT}$$

- Inversion layer is pinched-off near drain terminal
- Like a current source between source and drain terminals

$$I_D = \mu_p C_{OX} \frac{W}{L_{ch}} \left( V_{GS} - V_{TP} - \frac{V_{DS,SAT}}{2} \right) V_{DS,SAT}$$

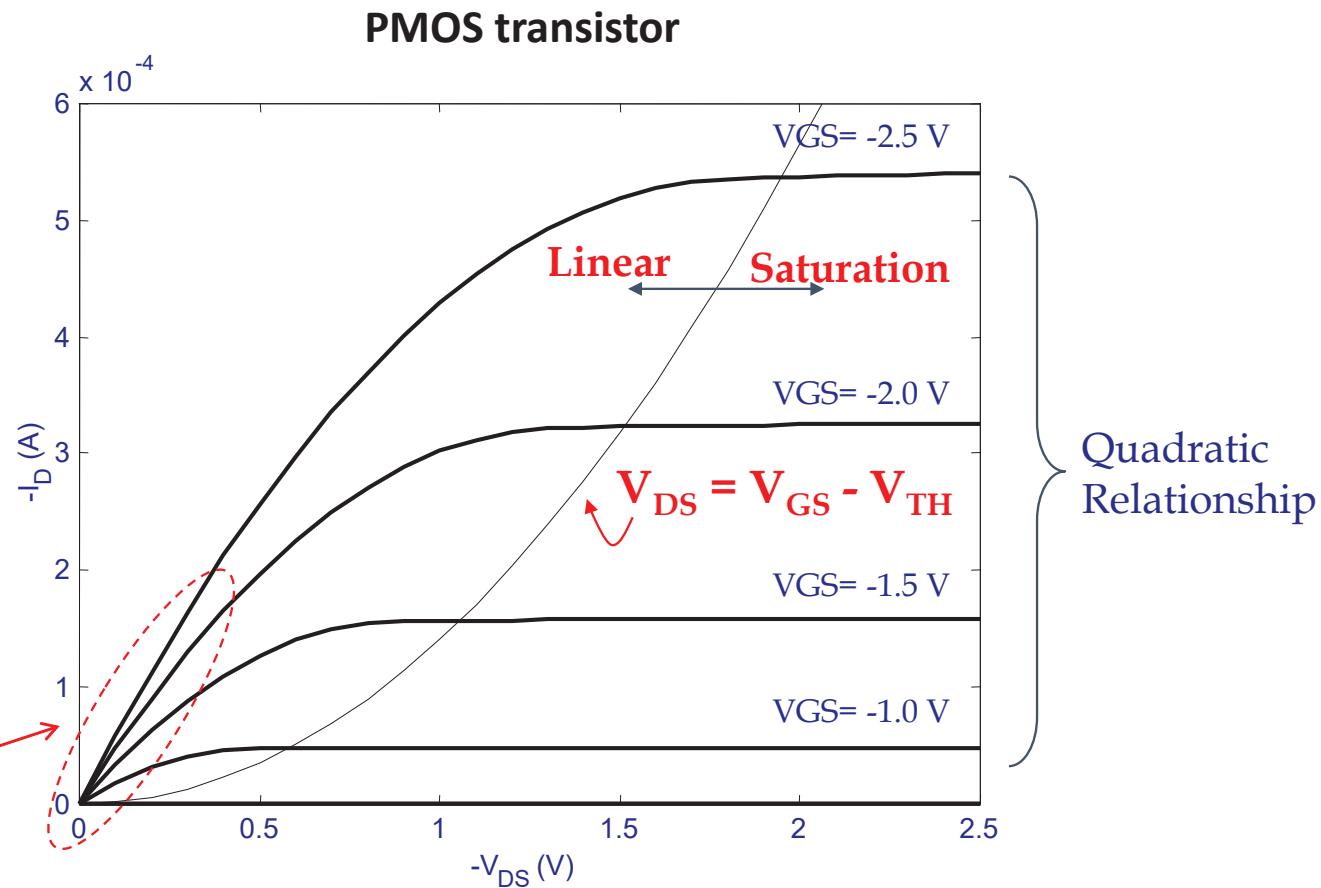
Channel length modulation neglected

$$V_{DS,SAT} = V_{GS} - V_{TP} \text{ (long channel MOSFET)}$$

# The $I-V$ Characteristic

$$R_{DS} = \frac{V_{DS}}{I_D}$$

$$\approx [\beta(V_{GS} - V_{TP})]^{-1}$$



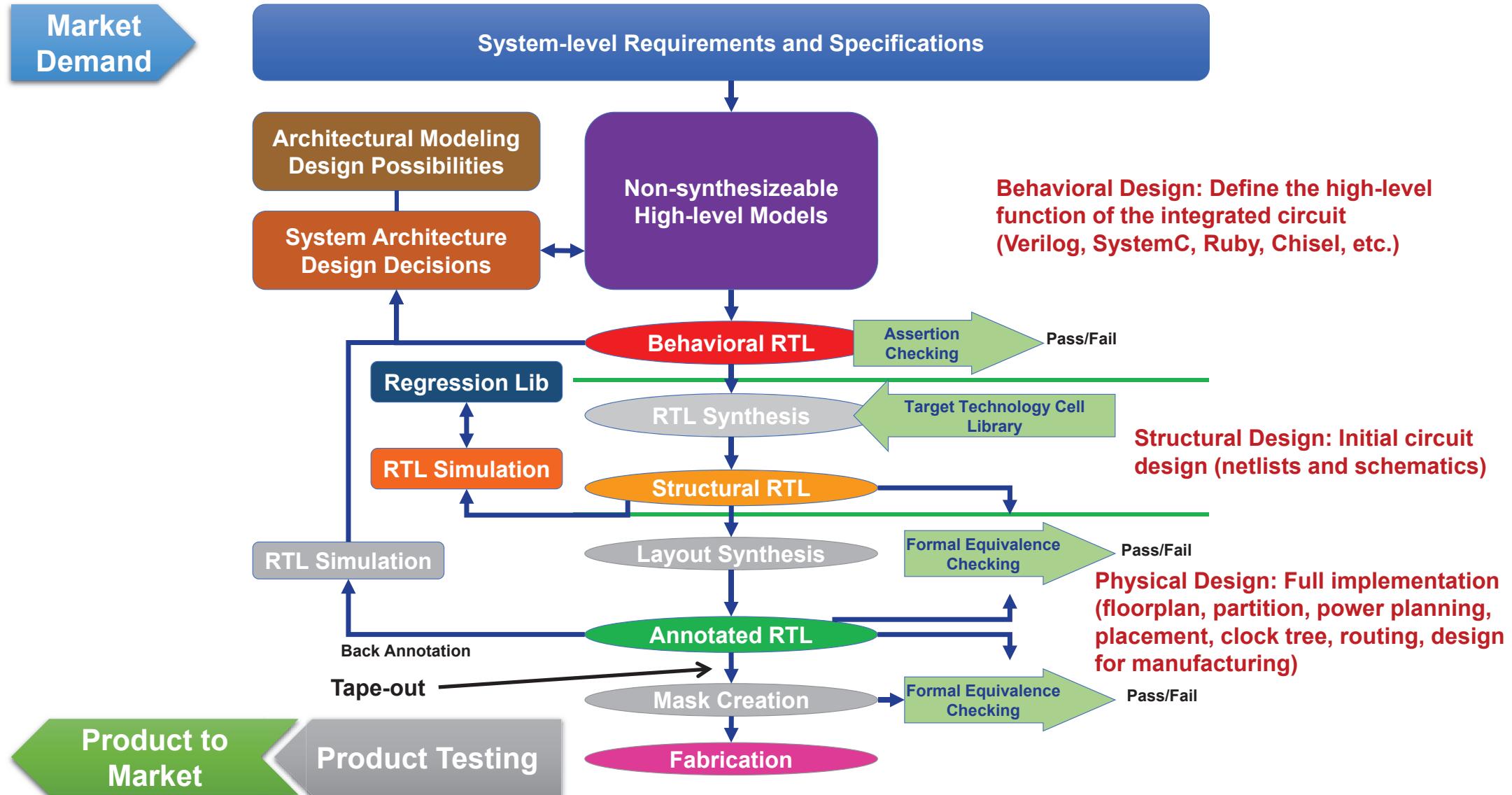
# Week 1-8

Introduction to the Design Flow

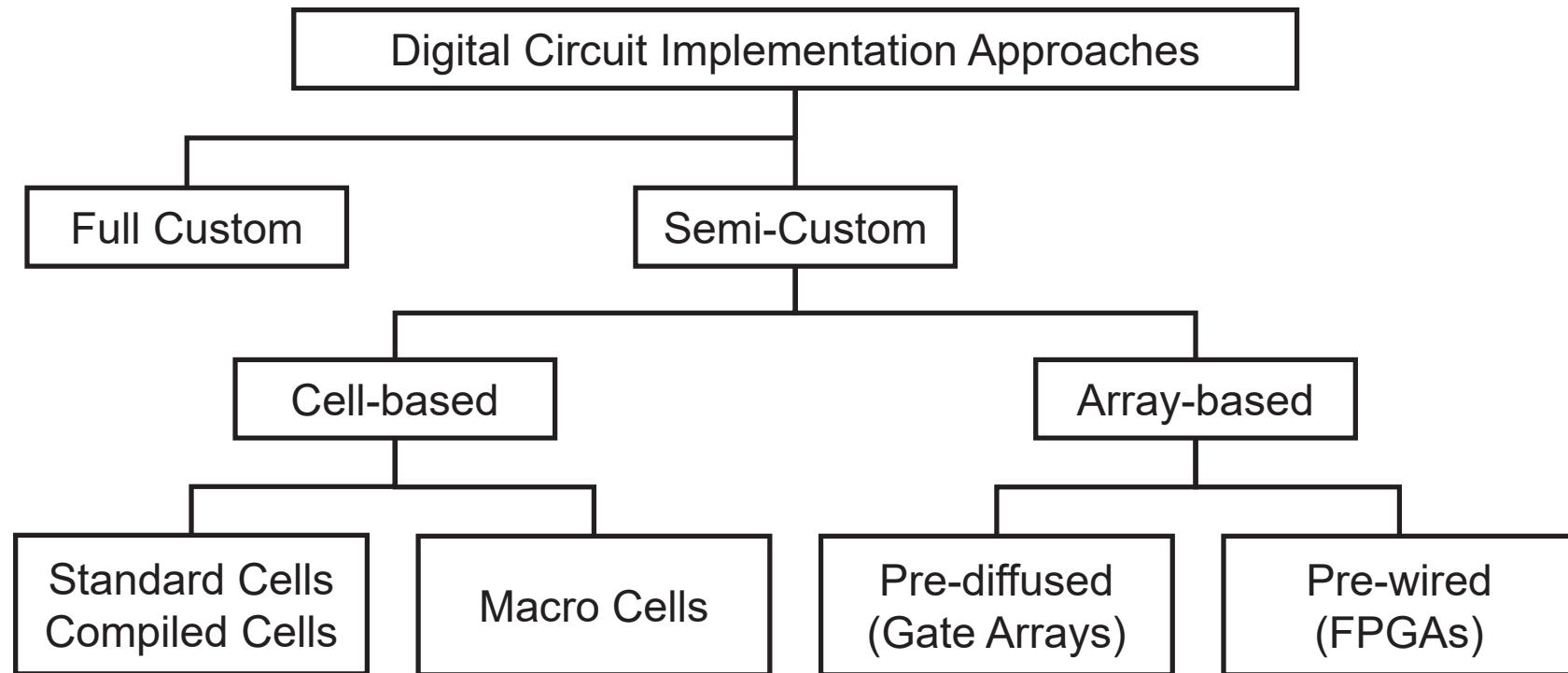
# The Design Flow for Integrated Circuits

- What is a design flow?
  - Shows the stages and phases in an IC design project from idea conception to delivery of final product to the customer
- Why is a design flow needed?
  - IC design is highly complex, time consuming and expensive
  - Provides an organized structure to solving various problems or issues that can arise in the project
    - Highlight where possible problems might arise
    - Predetermine the issues each phase should tackle and solve
  - Optimize design effort & resources, reduce cost, improve success rate!

# From Concept to Implementation



# Implementation Choices



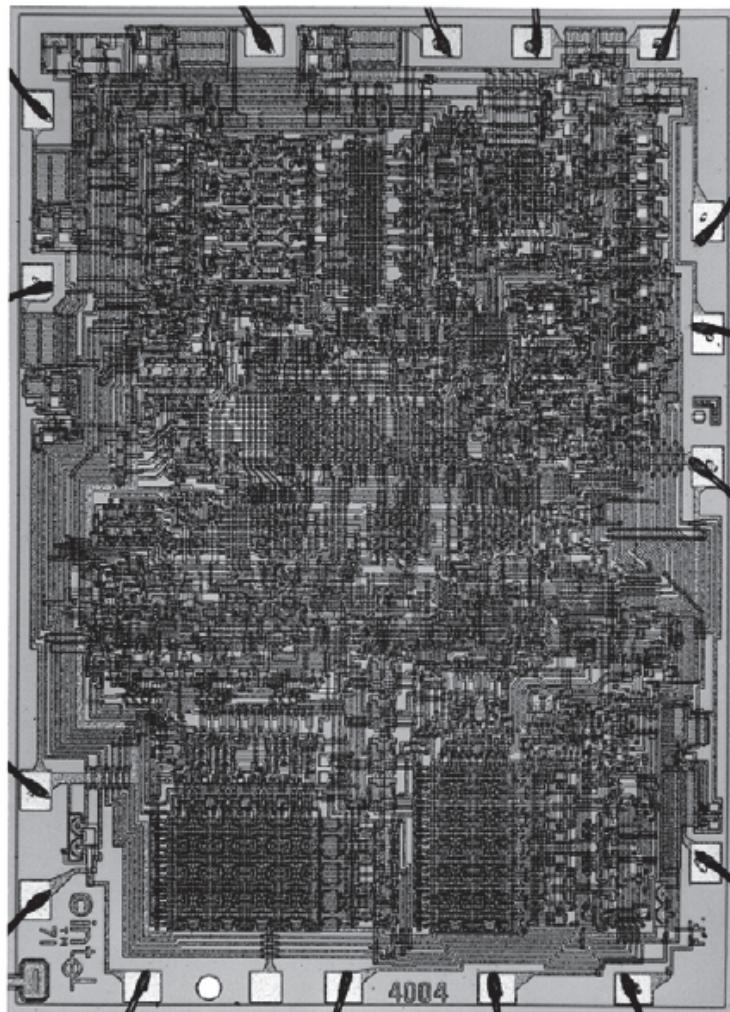
*Approach taken depends on desired tradeoffs between time-to-market, cost, design complexity, aggressiveness of design specifications*

*Design for fast time-to-market: design automation techniques*  
*Design for high performance/high density: handcrafted full custom design*

# Full Custom Design

- Complete control over transistor and interconnect dimensions (within design rule constraints)
- Design rules:
  - Minimum spacing between metal lines (varies by layer)
  - Line width
  - Transistor channel length
- Circuit designers create application-specific building blocks (e.g., IP)
  - Technology Provider (foundry) provides SPICE/HSPICE transistor models, parasitic extraction tools
  - Models are used to drive transistor sizing/layout constraints
- Continual verification of design as it becomes more defined
- Pros:
  - Produces optimized design (density, power, performance)
- Cons:
  - Time-consuming
  - Error-prone
  - Highest non-recurring engineering (NRE) cost

# The Full Custom Approach – Early Days



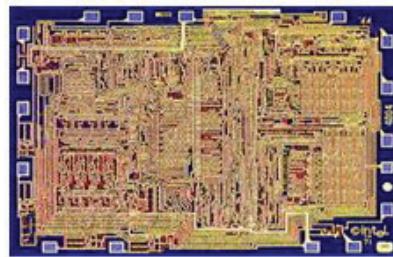
Courtesy Intel

Intel 4004 Microprocessor  
(108 kHz, 2300 transistors, 10 $\mu$ m)

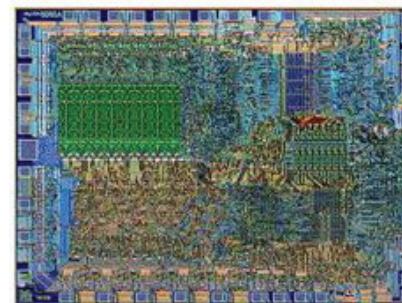
*When performance or  
design density are critical,  
handcrafting circuit topology  
and physical design seems  
to be the only option*

- High cost
  - Long time-to-market
- It is OK when
- Custom blocks can be reused
  - Cost can be amortized over a large volume (e.g.,  $\mu$ P, memories)
  - Cost is not primary design criterion (e.g., supercomputers)

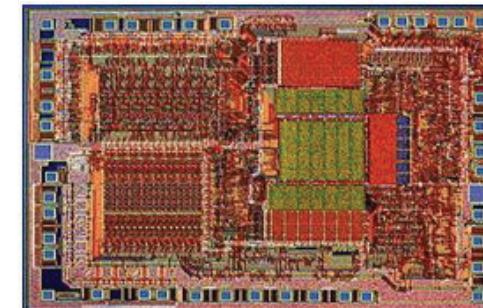
# Transition to Automation and Regular Structures



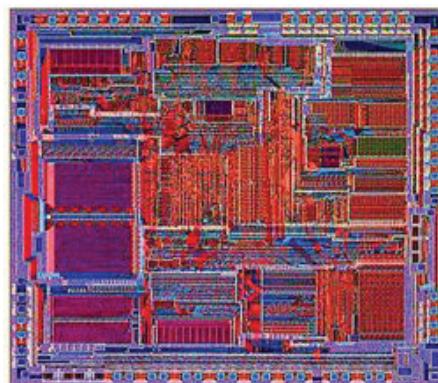
Intel 4004



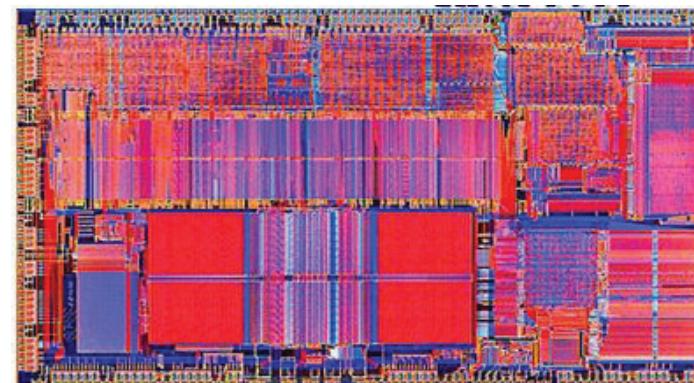
Intel 8080



Intel 8085



Intel 8286



Intel 8486

Evolution of full custom design

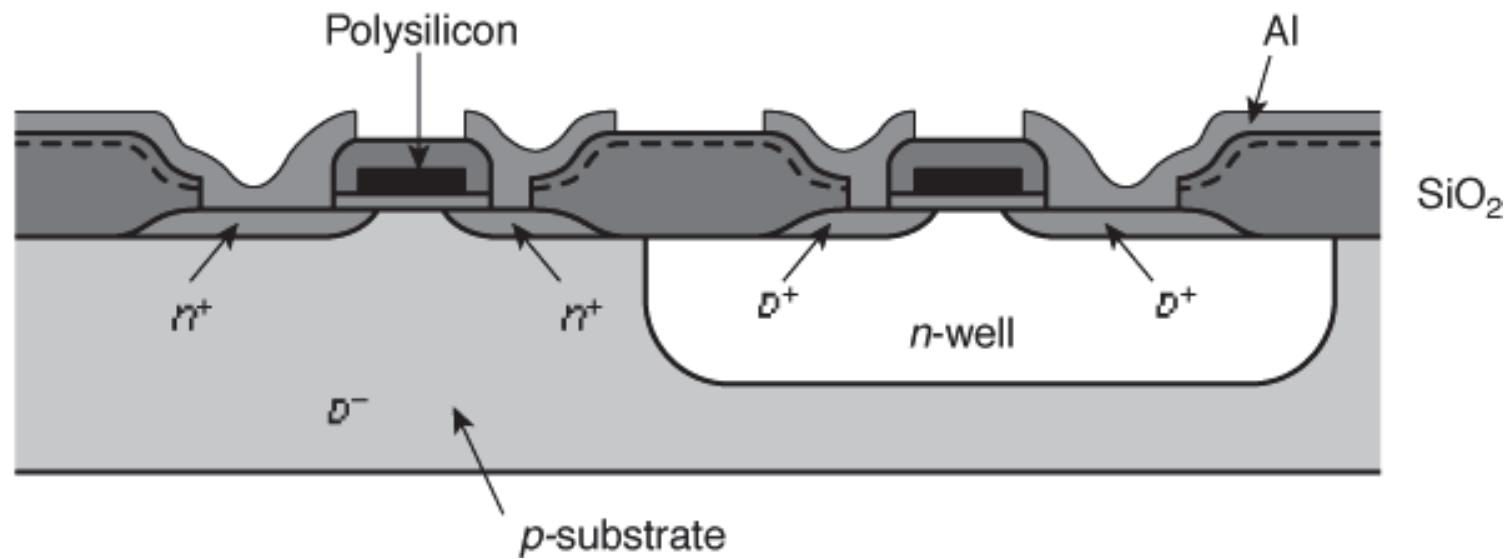
- Replication of the same custom-designed block multiple times (e.g., memories)
- Composition of different custom-designed blocks with a regular composition pattern  
In both cases, **regularity enables automation**

Courtesy Intel

# Week 1-9

Design (Layout) Rules

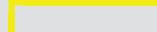
# Cross-section of CMOS Technology



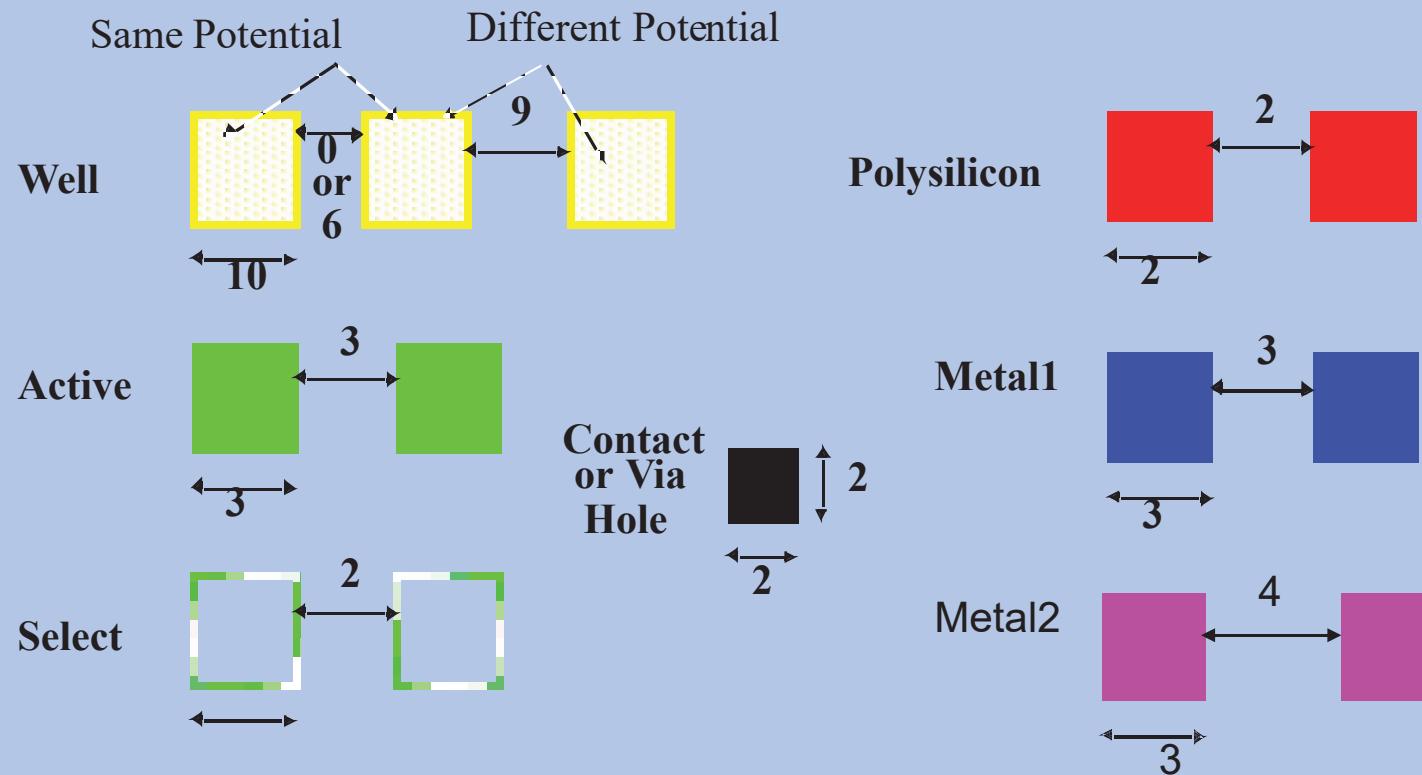
# Design (Layout) Rules

- Interface between designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: Minimum line width
  - scalable design rules: lambda parameter
  - absolute dimensions (micron rules)

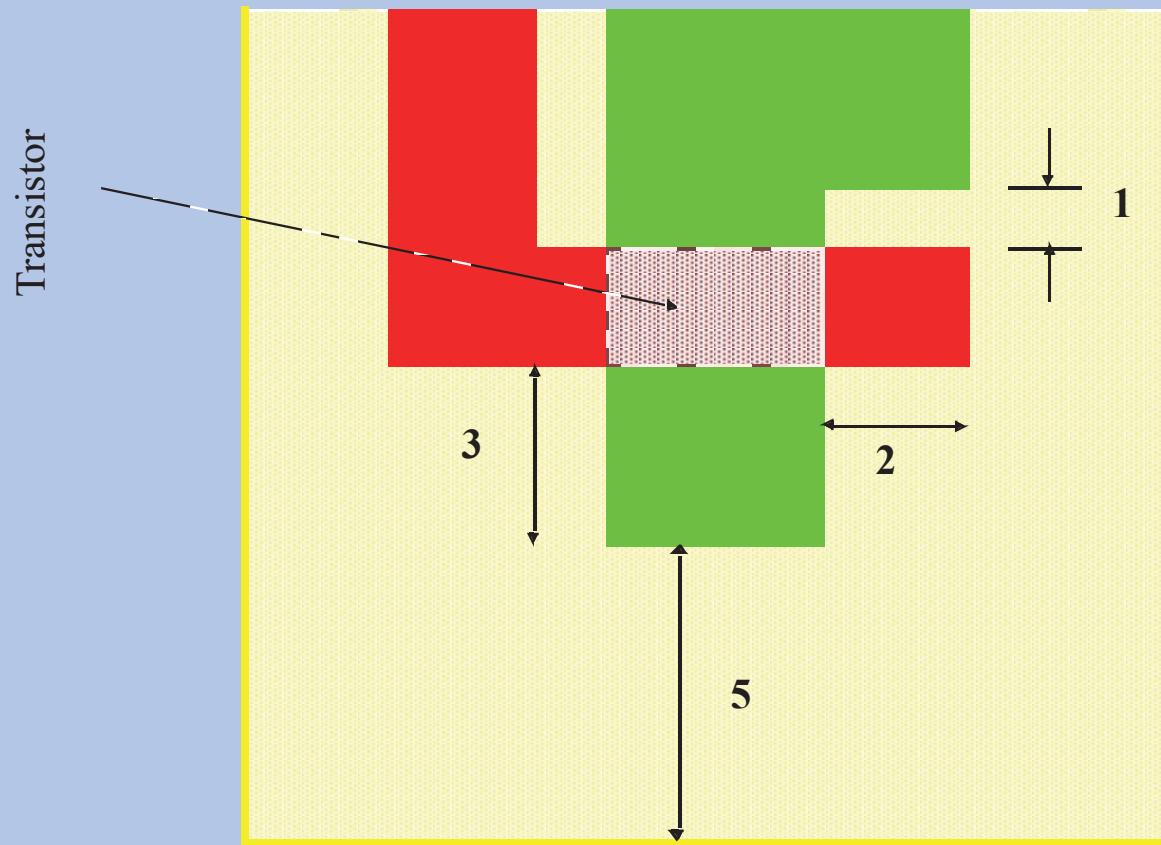
# CMOS Process Layers

Layer	Color	Representation
Well (p,n)	Yellow	
Active Area (n+,p+)	Green	
Select (p+,n+)	Green	
Polysilicon	Red	
Metal1	Blue	
Metal2	Magenta	
Contact To Poly	Black	
Contact To Diffusion	Black	
Via	Black	

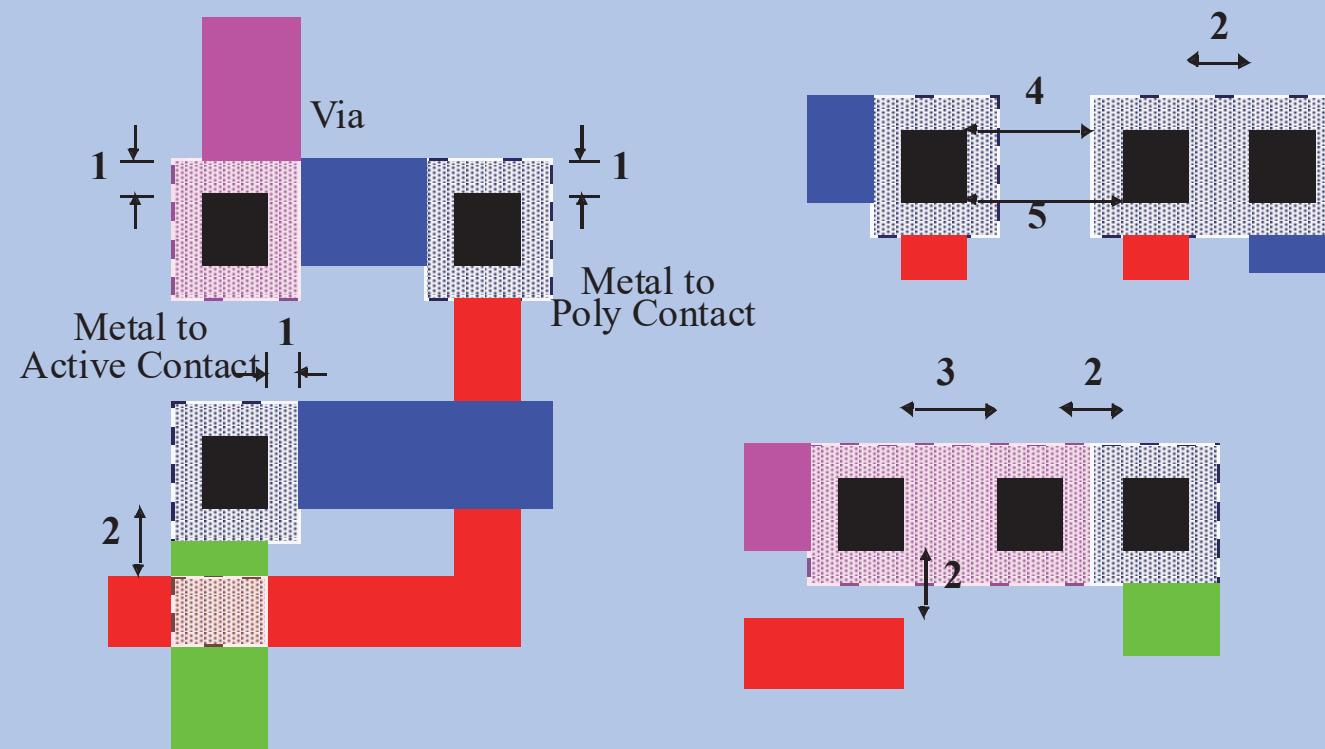
# Intra-layer Design Rules



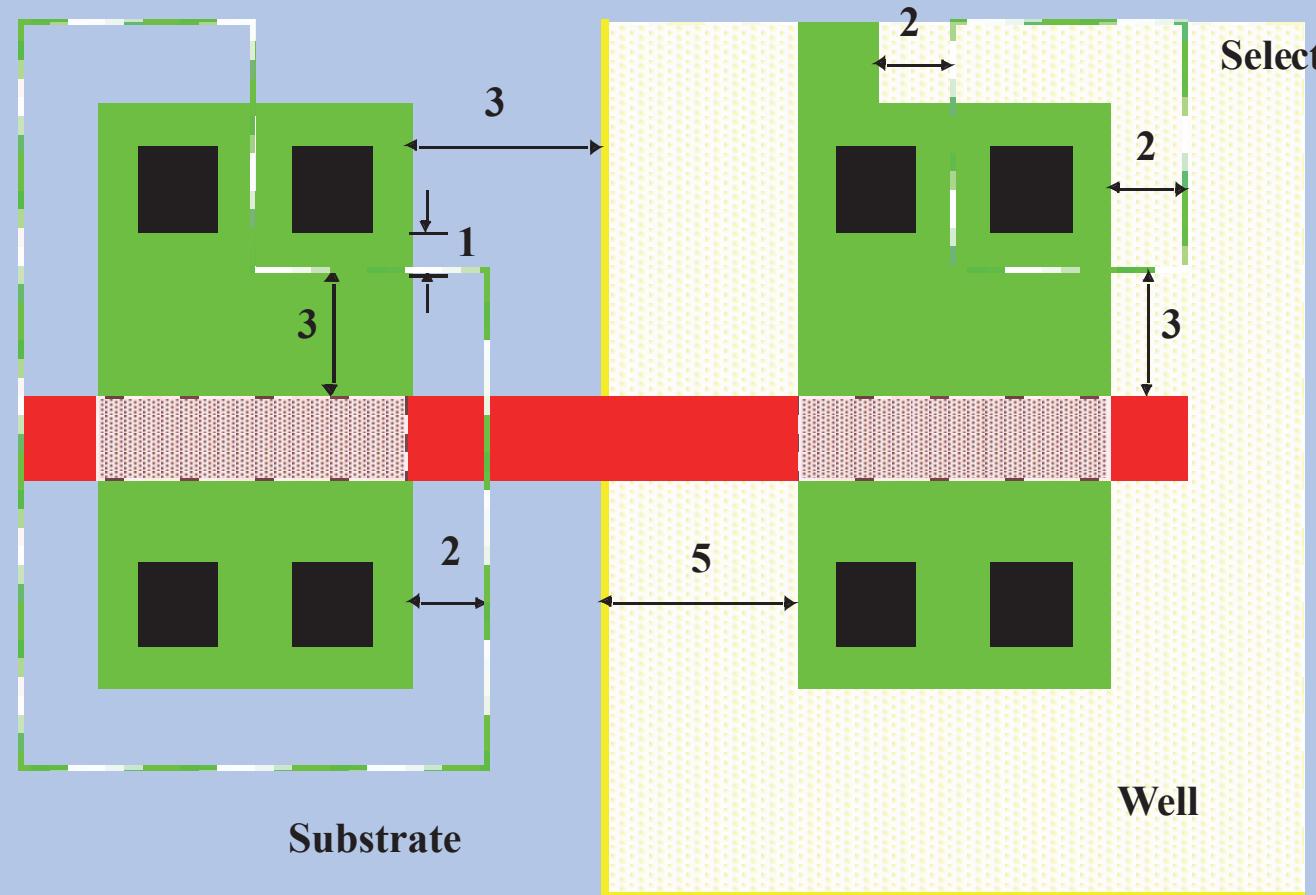
# Transistor Layout



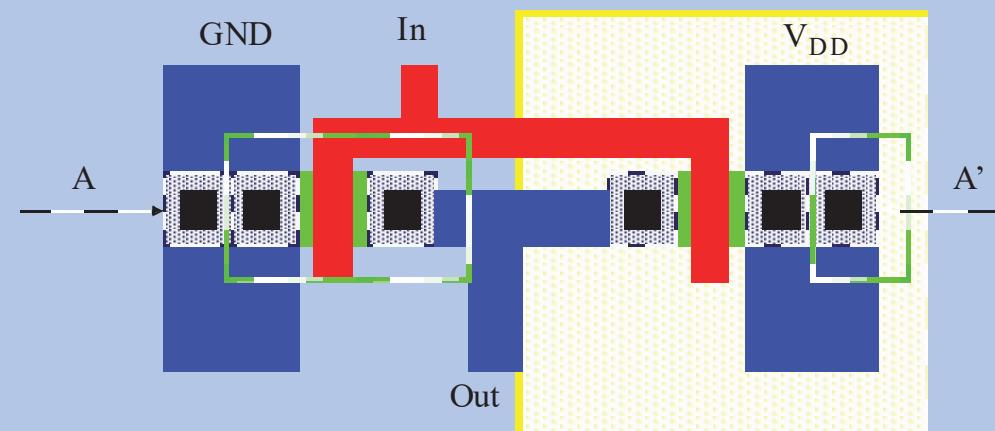
# Via's and Contacts



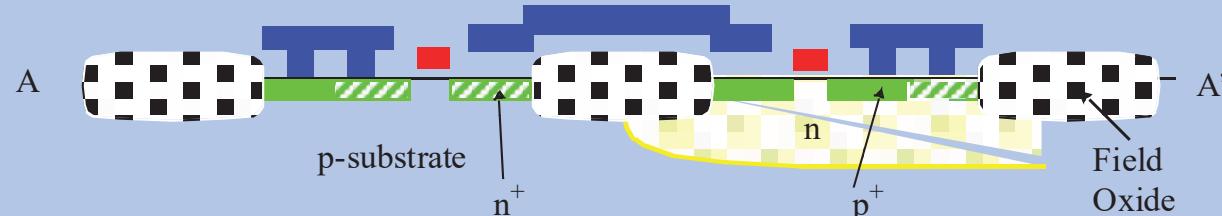
# Select Layer



# CMOS Inverter Layout



(a) Layout



(b) Cross-Section along A-A'

# Planar versus 3D FET (Fin- & GAA-FET)

