# National University of Singapore
# Electrical and Computer Engineering

## CG2027 (Transistor-Level Digital Circuits)
## Assignment #3

AY21/22 Semester 1
Issued: Aug. 24, 2021 Due: Aug. 29, 2021 (18:00)

### Problem 1: CMOS Logic

Consider the following CMOS logic circuits:

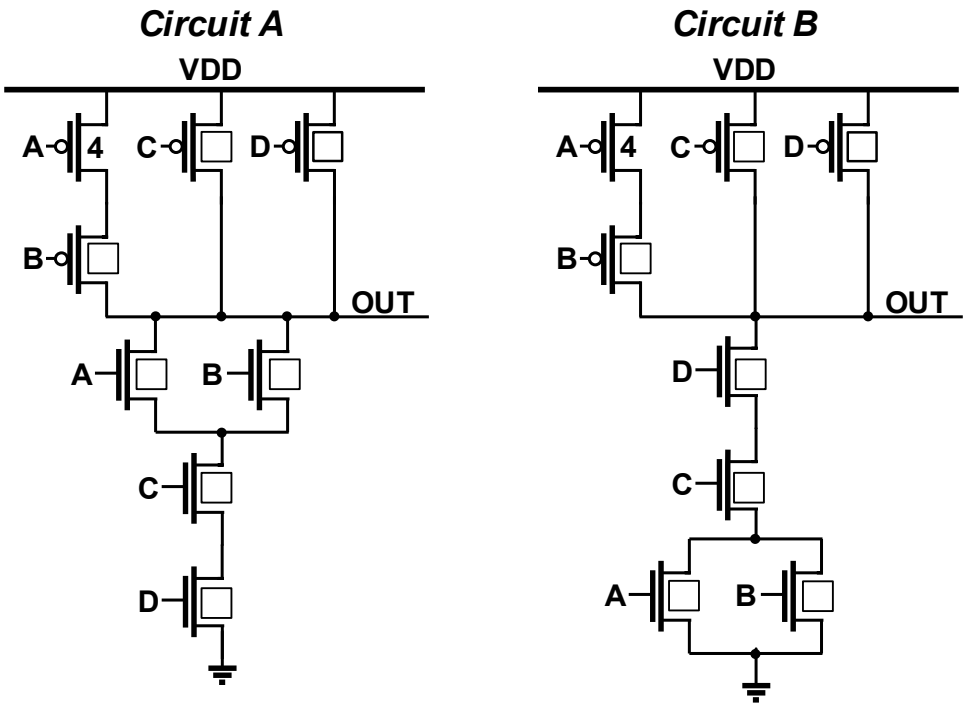


**Figure 1: Two static CMOS gates.**

a) Provide the Boolean expression for the circuits in **Figure 1** and show whether they implement the same logic function.

b) What is the appropriate transistor sizing for the logic circuit to have similar to 1X inverter delay? Fill in the empty boxes. Assume PMOS A has width of 4 (as shown above), and INV1X has $W_{PMOS}$:$W_{NMOS}$ of 2:1.

c) Assume the transistors have been sized to give a worst case output resistance of 12kohm in both pull-up and pull-down networks for the worst-case input patterns. What input patterns (A-D) give the lowest output resistance when the output is low? What is the value of that resistance?

d) What input patterns (A-D) give the lowest output resistance when the output is high? What is the value of that resistance?

e) Neglecting parasitics and assuming a load capacitance of 100fF, calculate the best case $t_{pLH}$ and $t_{pHL}$.

## Problem 2: Pass Transistor Logic and Level Restoration

Consider the circuits of **Figure 2**. Assume the inverter of M1 and M2 switches ideally at VDD/2, neglect body effect, channel length modulation and all parasitic capacitances throughout this problem. Use the parameters in the Table for NMOS and PMOS.

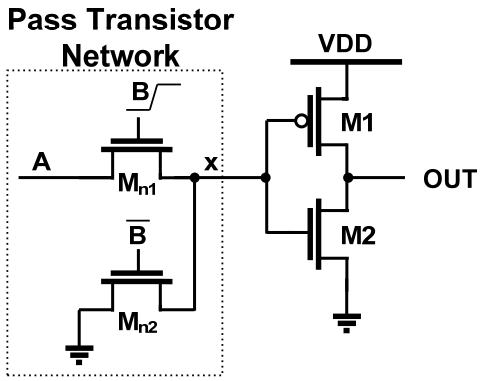


**Figure 2: Level restoring circuit.**

a) What is the logic function performed by this circuit?

b) Explain why this circuit has non-zero static power dissipation?

c) Using only just 1 transistor, design a fix so that there will not be any static power dissipation. Explain how you chose the size of the transistor.

d) Replace the pass-transistor network in **Figure 2** with a pass transistor network that computes the following function: x=ABC at the node x. Assume you have the true and complementary versions of the three inputs A, B and C.