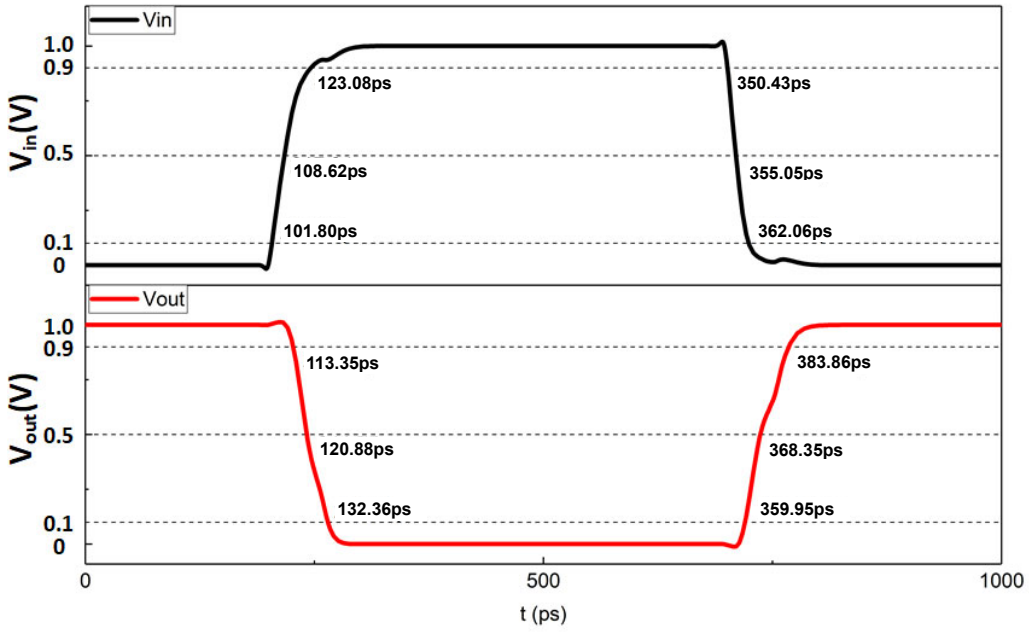
National University of Singapore
Electrical and Computer Engineering

CG2027 (Transistor-Level Digital Circuits)
Tutorial #1

AY21/22 Semester 1
Issued: Aug. 10, 2021 Due: Aug. 15, 2021 (18:00)

Problem 1: Delay Calculation

The objective of this problem is to figure out correct delay / risetime / falltime of a CMOS inverter, based on the information given from the waveform.



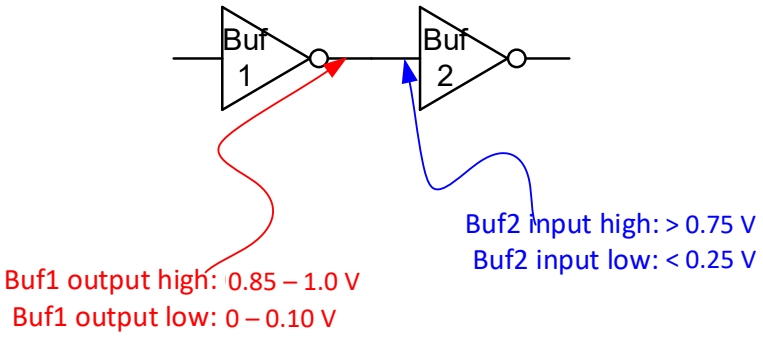
a) What is the rise time (t_r), fall time (t_f) of the output waveform V_{out}?

b) What is the high-to-low propagation delay (t_{pHL}) of the logic?

c) What is the low-to-high propagation delay (t_{pLH}) of the logic?

d) If the given waveform is a part of a clock signal with 50% duty, what is the clock frequency?

Problem 2: Noise Margin



a) For the inverter chain given above, calculate the noise margin high (NM_H) and noise margin low (NM_L).

b) What happens if input high and input low of the Buf2 become the same? Explain.