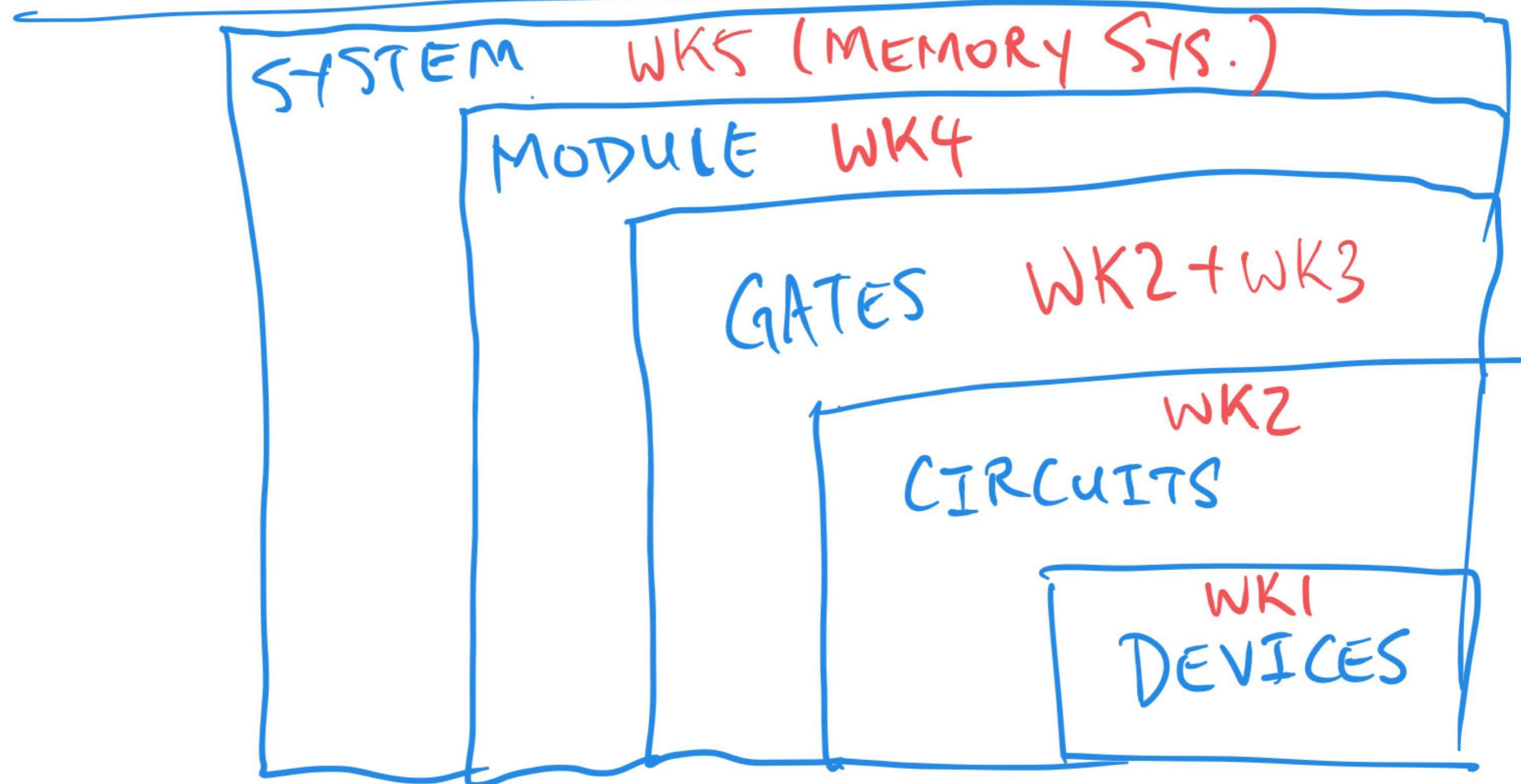


CG2027 Week 6 - Recap

ANNOUNCEMENTS

- CHECK EMAIL & LUMINUS REGARDING FINAL QUIZ
- PLEASE GIVE FEEDBACK ABOUT MODULE
 - BE CONSTRUCTIVE!
 - PLEASE GIVE POSITIVE & NEGATIVE FEEDBACK TO HELP IMPROVE THE MODULE
- PLEASE ATTEMPT ALL LESSON VIDEO QUIZZES ASAP

LEVELS OF DESIGN ABSTRACTION



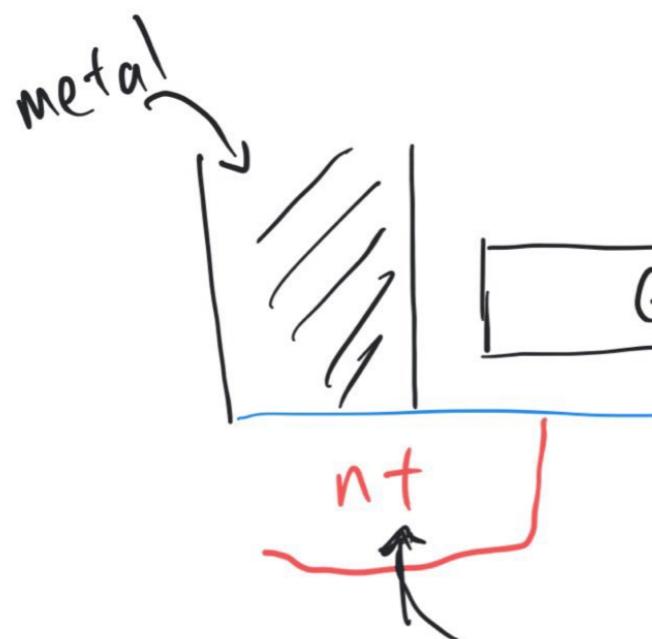
DEVICES

pn-junction diode

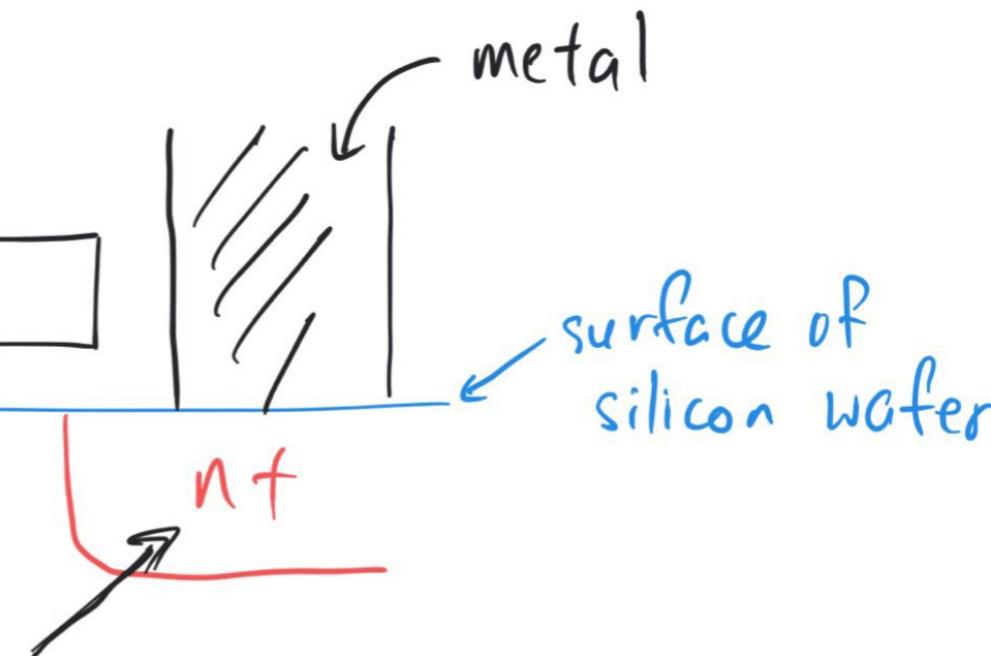
bipolar junction transistor

metal-oxide-semicond. transistor (MOSFET) enhancement mode

n-MOSFET



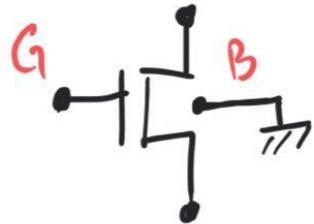
p-MOSFET



p-sub.

I-V characteristic of the MOSFET

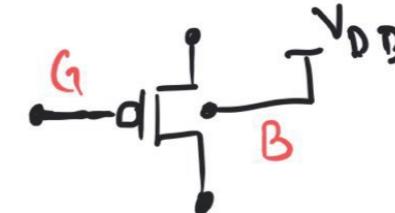
n-channel
MOSFET



→ source is always at lower voltage than drain

- Current must always flow from drain to source

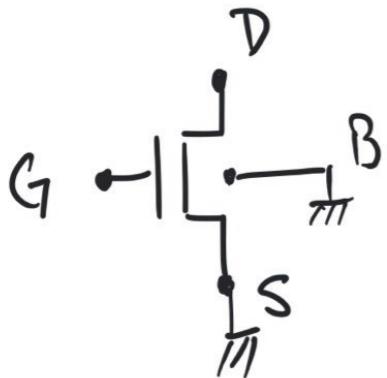
p-channel
MOSFET



→ source is always at higher voltage than drain

- current must always flow from source to drain

n-channel
MOSFET



Regions of op.

$$V_{GS} < V_{TH} \Leftarrow \text{cut-off: } I_D \text{ or } I_{DS} \approx 0$$

$$V_{GS} \geq V_{TH} \left\{ \begin{array}{l} \text{linear/triode: } I_D = \mu_n C_{ox} \frac{W}{L} \left(V_{DS}(V_{GS} - V_T) - \frac{V_{DS}^2}{2} \right) \\ V_{DS} < V_{DS,SAT} \\ V_{DS,SAT} = V_{GS} - V_{TH} \times (1 + \lambda_n V_{DS}) \\ \text{saturation: } V_{DS} = V_{DS,SAT} = V_{GS} - V_{TH} \\ I_D = \mu_n C_{ox} \frac{W}{2L} (V_{GS} - V_{TH})^2 (1 + \lambda_n V_{DS}) \end{array} \right.$$

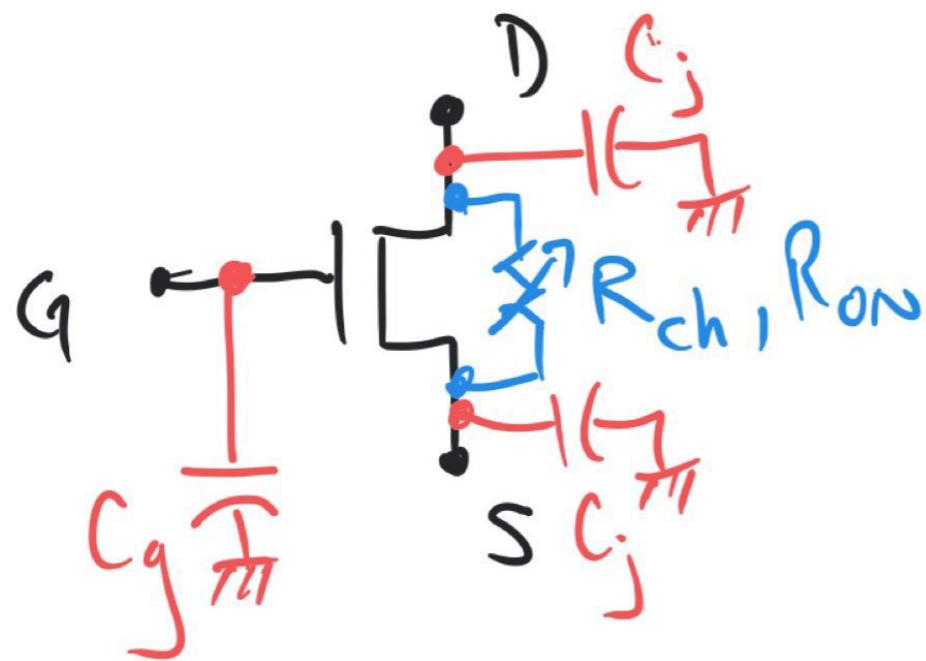
$$V_{DS} \geq V_{DS,SAT}$$

→ Form inversion layer in channel of n-MOSFET when it is turned on

→ MOSFETs can be treated as switches.

→ electrically-controlled switch between (gate voltage control)

- MOSFET is not an ideal switch



$C_g \propto W$ $W = \text{width of MOSFET}$

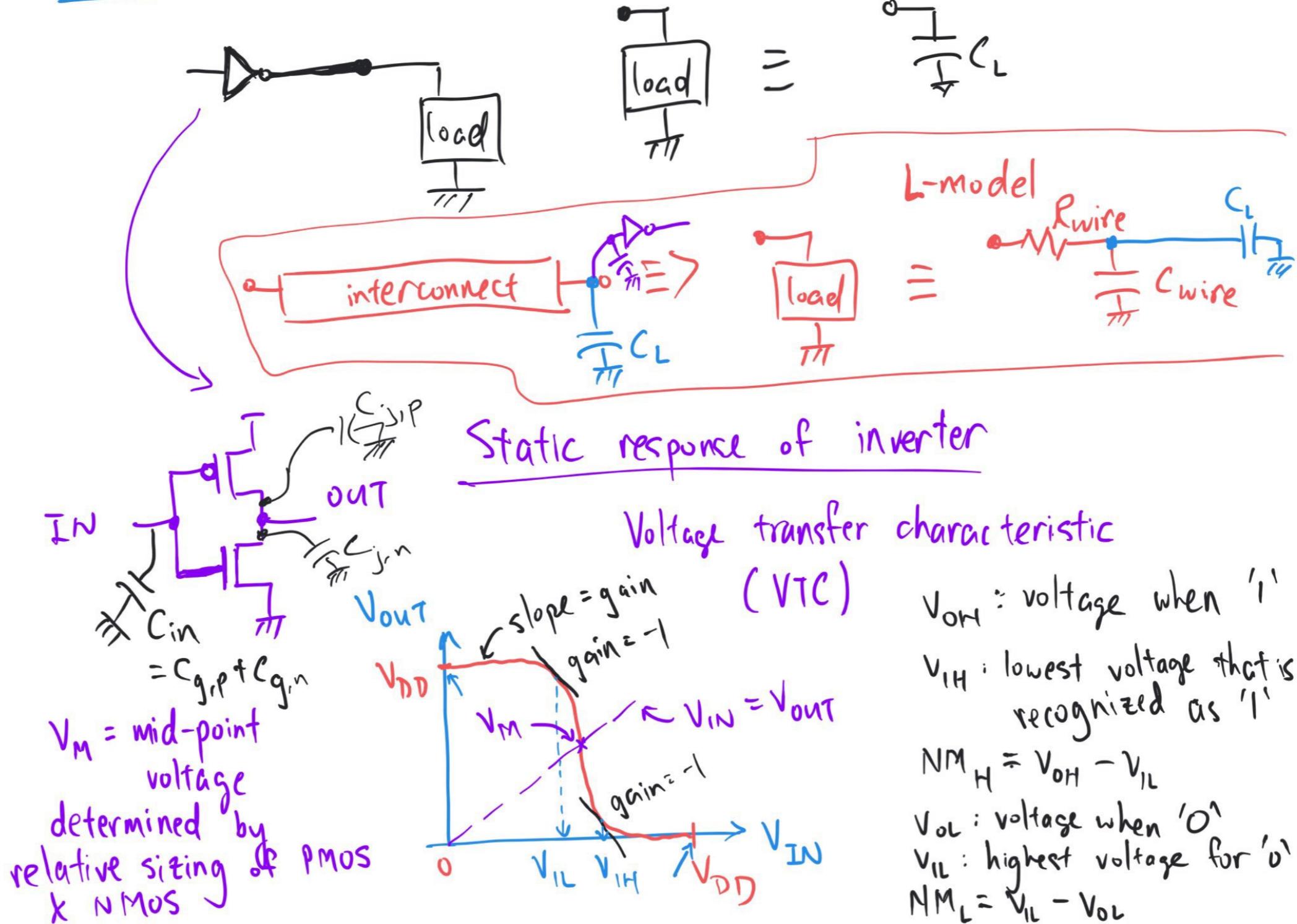
$$C_j \propto W$$

$$R_{ON} \propto \frac{L}{I_D}$$

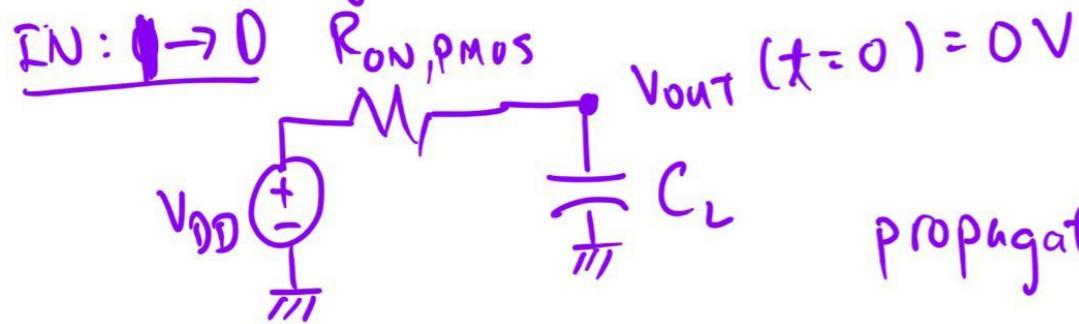
$$\Rightarrow R_{ON} \propto \frac{L}{W}$$

$$R_{ch} = \sum R_{ON}$$

Circuits



Dynamic response of inverter



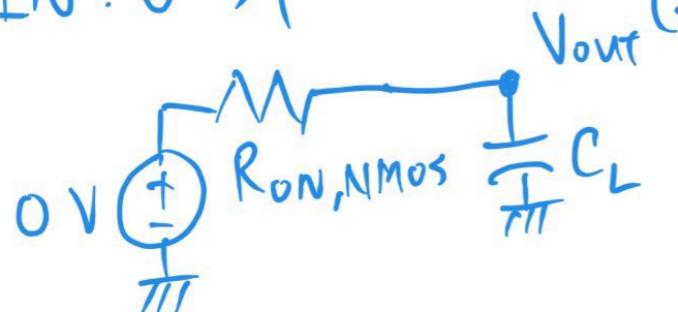
$$V_{out}(t) = V_{DD} \left(1 - e^{-\frac{t}{R_{ON,PMOS} C_L}}\right) \quad (1)$$

propagation delay:

delay between $V_{in} = \frac{V_{DD}}{2}$ & $\underline{\underline{V_{out}}} = \frac{V_{DD}}{2}$

$$\underline{t_{PLH} = 0.69 R_{ON,PMOS} C_L}$$

IN: $0 \rightarrow 1$



$$V_{out}(t) = V_{DD} \left(e^{-\frac{t}{R_{ON,NMOS} C_L}}\right) \quad (2)$$

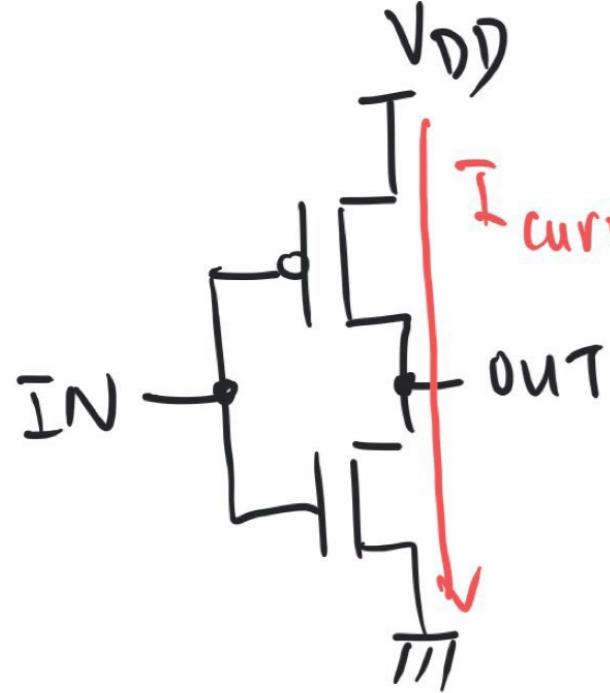
$$\underline{t_{PHL} = 0.69 R_{ON,NMOS} C_L}$$

rise time: delay between $V_{out} = 0.1 V_{DD}$ to $V_{out} = 0.9 V_{DD}$

fall time: " " " $V_{out} = 0.9 V_{DD}$ to $V_{out} = 0.1 V_{DD}$

$$t_r \approx \underline{\underline{R_{ON,PMOS} C_L}}$$

$$t_f \approx \underline{\underline{R_{ON,NMOS} C_L}}$$

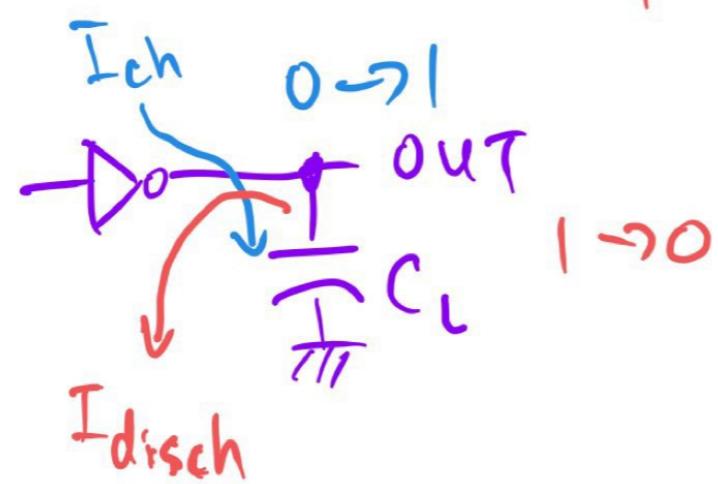


$I_{\text{current}} \neq 0$ during switching

1) short-circuit power dissipation = $V_{DD} \cdot I_{\text{short-circuit}}$
(static power diss.)

2) leakage power diss. = $V_{DD} \cdot I_{\text{leakage}}$

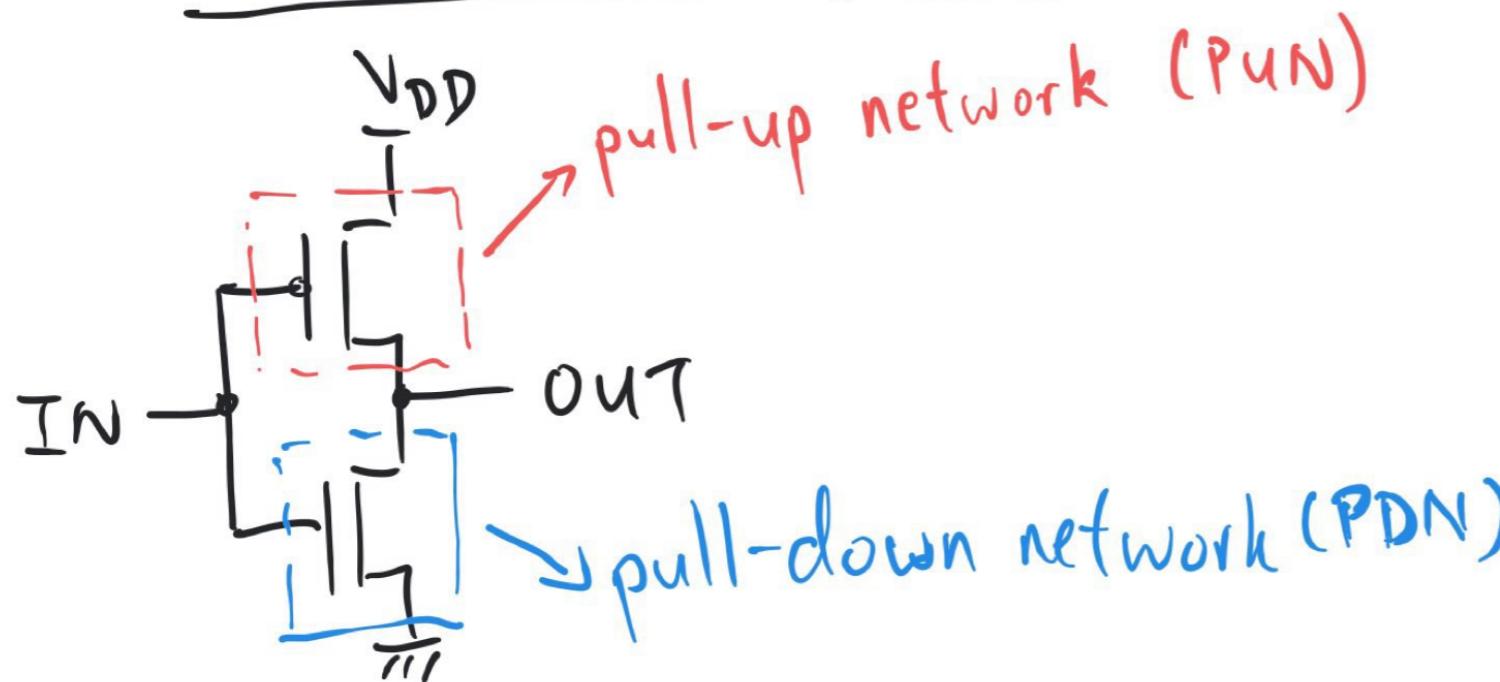
3) active power dissipation = $\overline{\alpha_{0 \rightarrow 1}} C_L V_{DD}^2 f_{\text{clk}}$



activity
factor

"prob. out changes
from 0 to 1"

Static CMOS logic gate

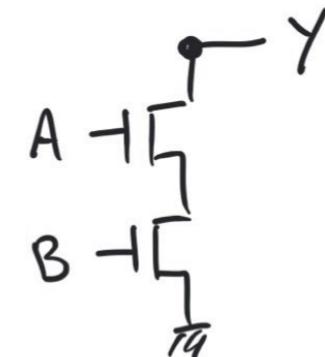


Series connection of switches \Rightarrow AND (since need both switches to close to get SC)

parallel connection of switches \Rightarrow OR (since need either one of switch to close to get SC)

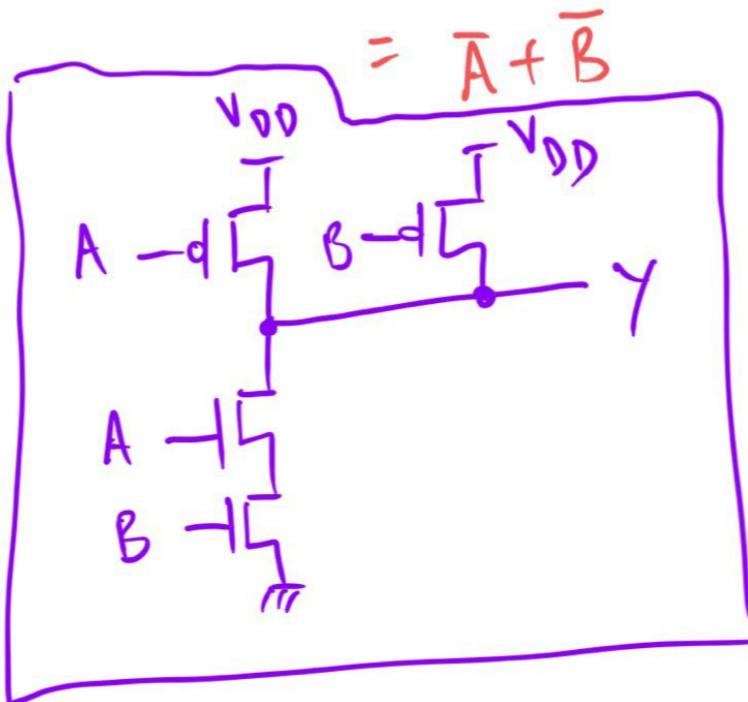
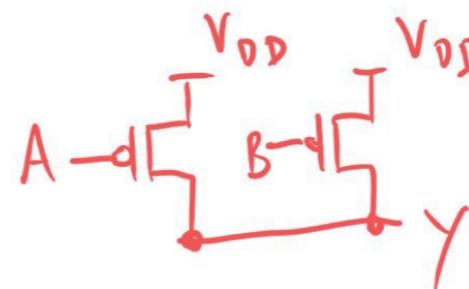
NAND gate : $Y = \overline{A \cdot B}$

(PDN) : $\bar{Y} = A \cdot B$



(PUN) : $Y = \overline{\overline{A \cdot B}}$

$$= \overline{\overline{\overline{A} + \overline{B}}}$$



$$Y = \overline{A_0 A_1 + B_0 B_1}$$

$$\Rightarrow Y = B_0 + A_0 A_1$$

Assume $\overline{B_0}, \overline{A_0}, \overline{A_1}$

When assigning the sizes to transistors
 → worst case t_{PLH} & t_{PHL} are matched to some reference.

$$t_p : 0.69 R_{ON} \cdot C_L \quad R_{ON} \propto \frac{L}{W}$$

$$Y = B_0 + A_0 A_1 \quad \text{Assume } \bar{B}_0, \bar{A}_0, \bar{A}_1 \text{ are available}$$

$$\bar{Y} = \bar{B}_0 \cdot (\bar{A}_0 \bar{A}_1)$$

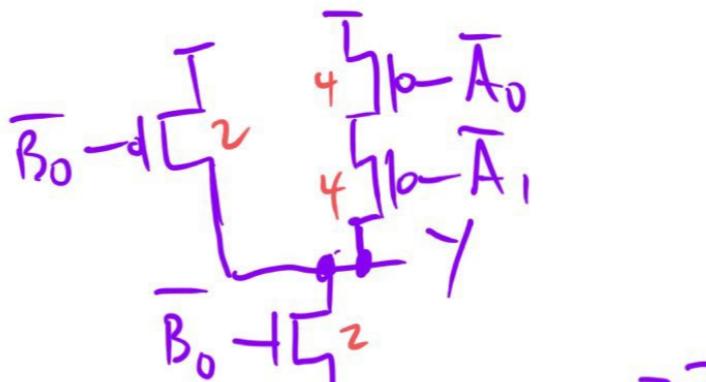
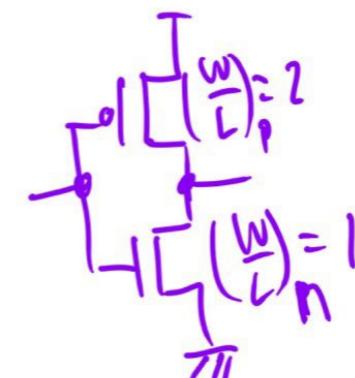
$$= \bar{B}_0 \cdot (\bar{A}_0 + \bar{A}_1)$$

$$\Rightarrow \bar{Y} = \overline{\bar{B}_0 + \bar{A}_0 \bar{A}_1} \quad \bar{A}_0 \rightarrow \boxed{2} \quad \bar{A}_1 \rightarrow \boxed{2}$$

$$= \bar{B}_0 \cdot (\overline{\bar{A}_0 \bar{A}_1})$$

$$= \bar{B}_0 \cdot (\bar{A}_0 + \bar{A}_1)$$

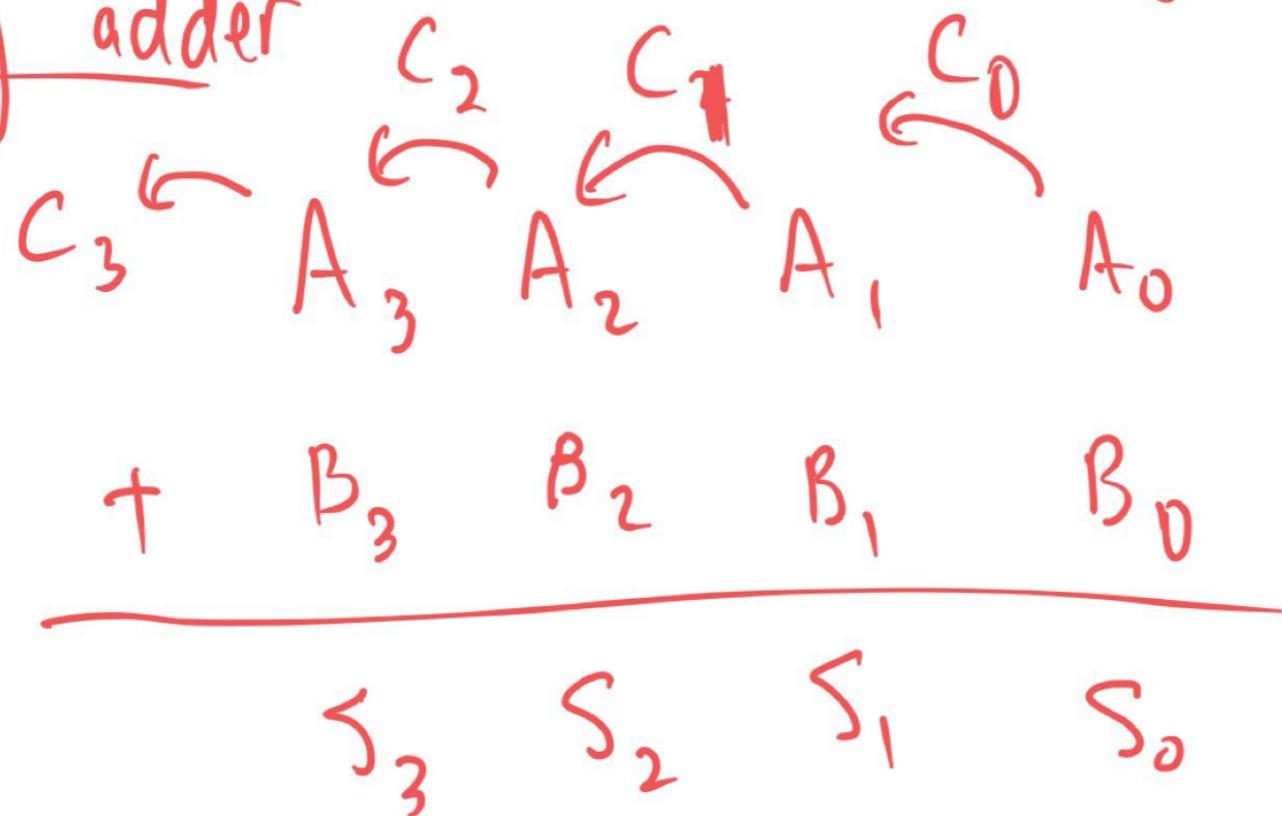
$$\bar{B}_0 \cdot (A_0 + A_1) \rightarrow$$


 \Rightarrow


Gates \rightarrow Adders & shifters.

\hookrightarrow multiplexers arranged & connected so we get bit shifting.
 \rightarrow binary
 \rightarrow barrel
 \rightarrow logarithmic

Ripple carry adder

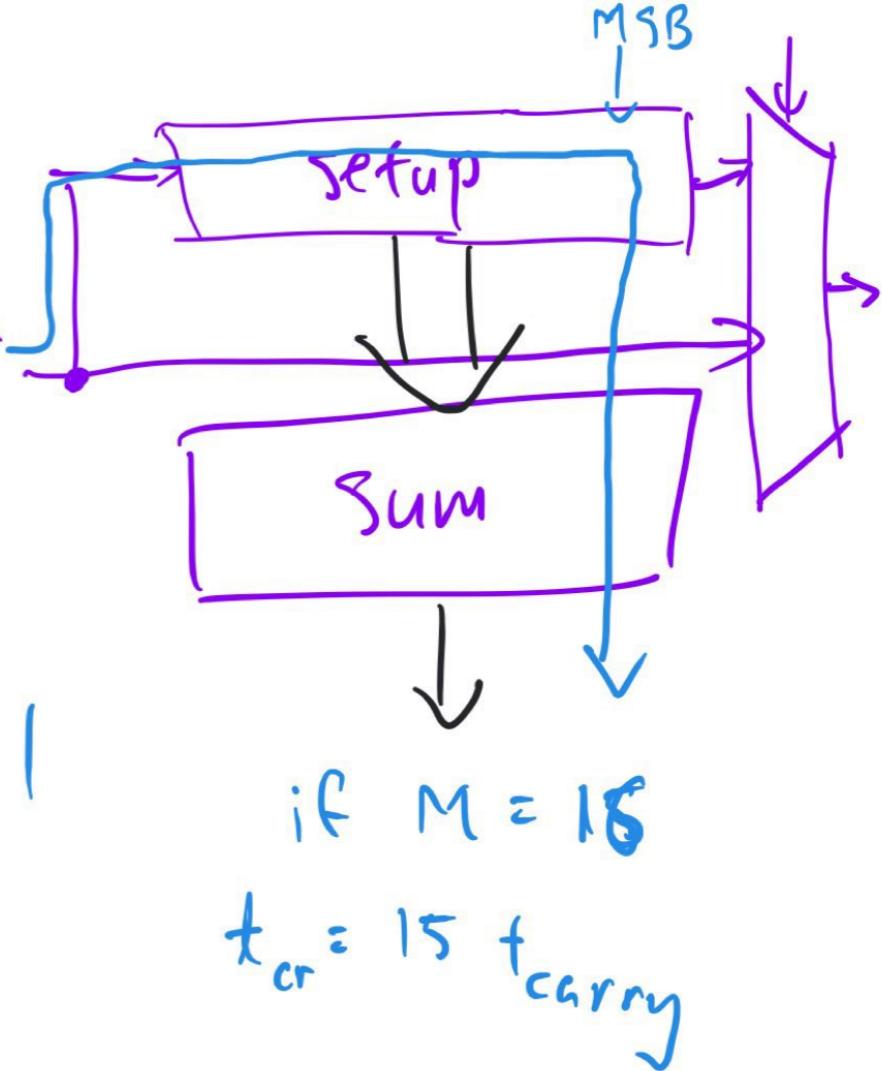


Full-adder

A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		1

$$S = A \oplus B \oplus C_{in} \Rightarrow \text{rewrite in terms of } G, P, D, P$$

"generate", $G=1$
 "propagate", $P=1$
 "delete", $D=1$



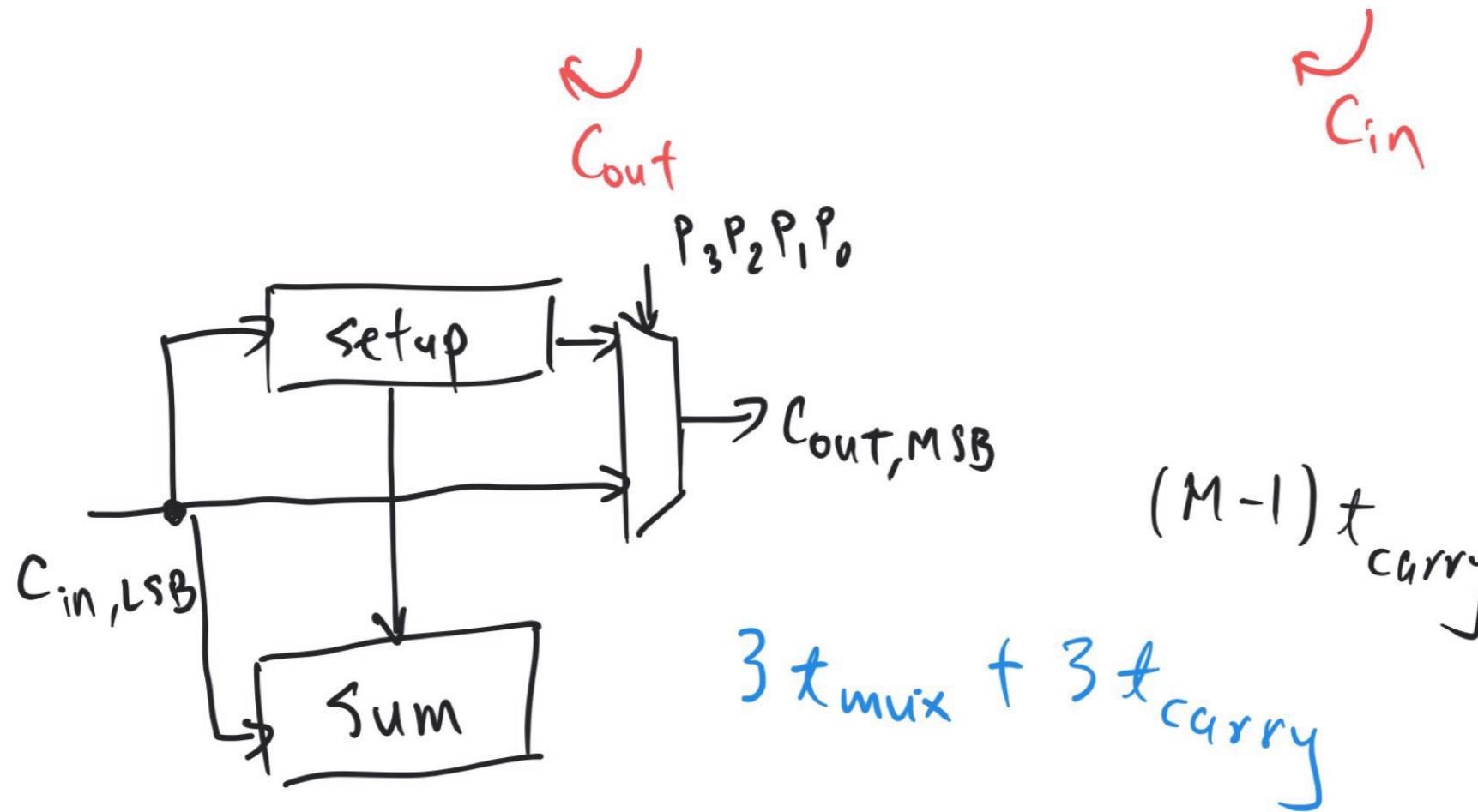
if $M = 15$

$$t_{cr} = 15 + t_{carry}$$

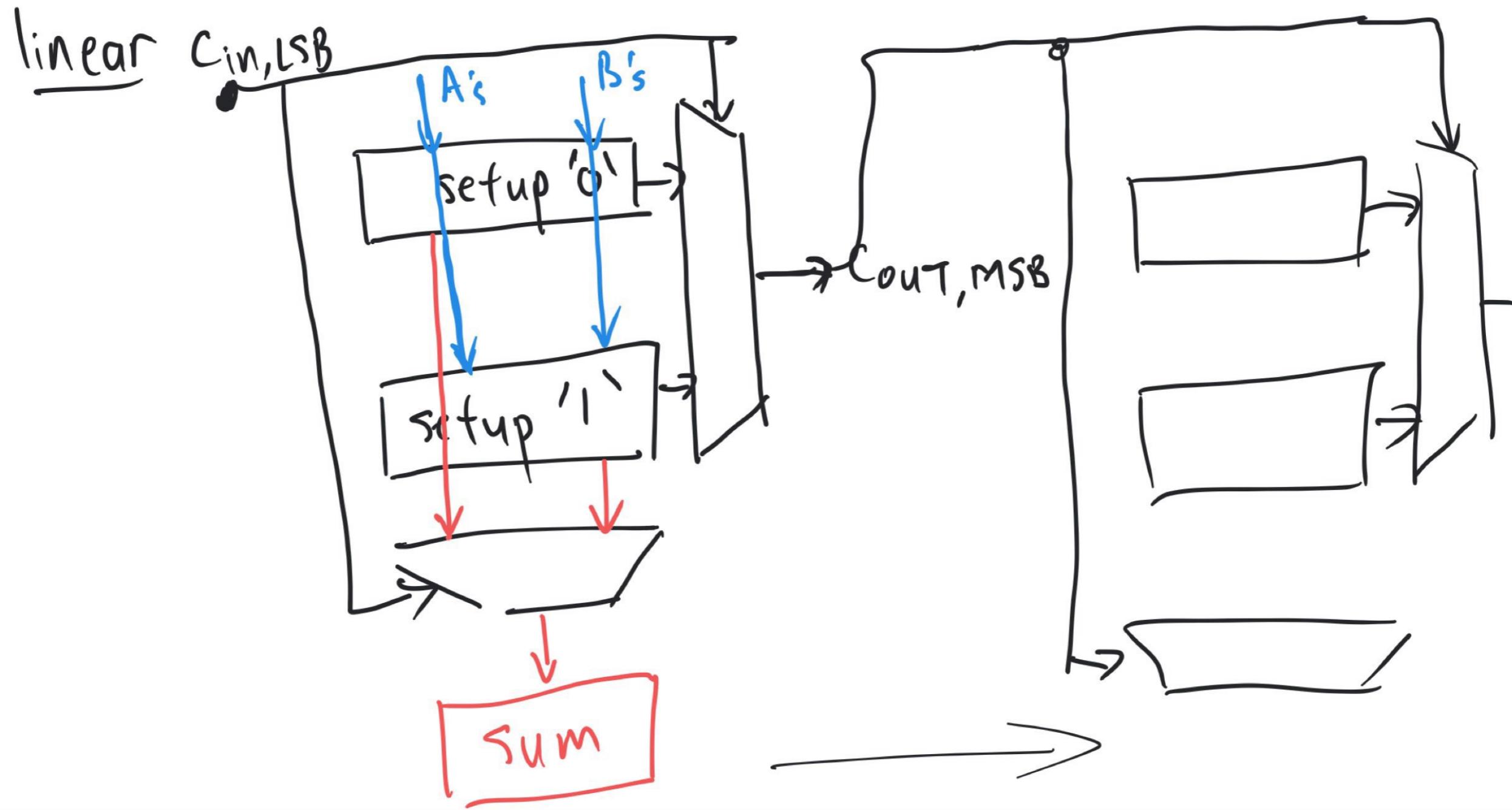
carry - bypass adder

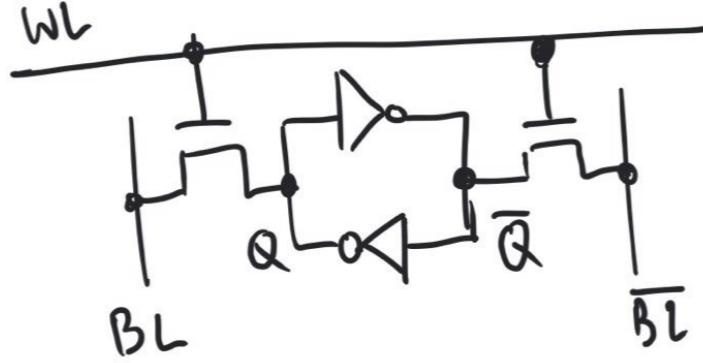
$P_3 \quad P_2 \quad P_1 \quad P_0$

if all are '1' $\rightarrow C_{out, MSB} = C_{in, LSB}$



carry-select adder





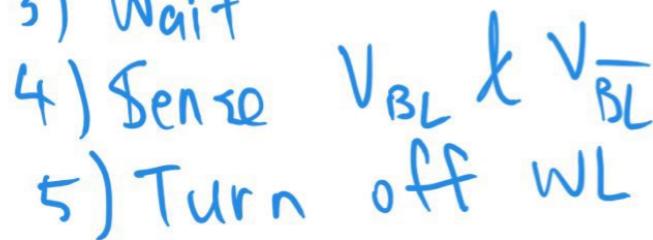
Write op.

Initially $V_{WL} = 0V = V_{BL} = V_{\bar{BL}}$

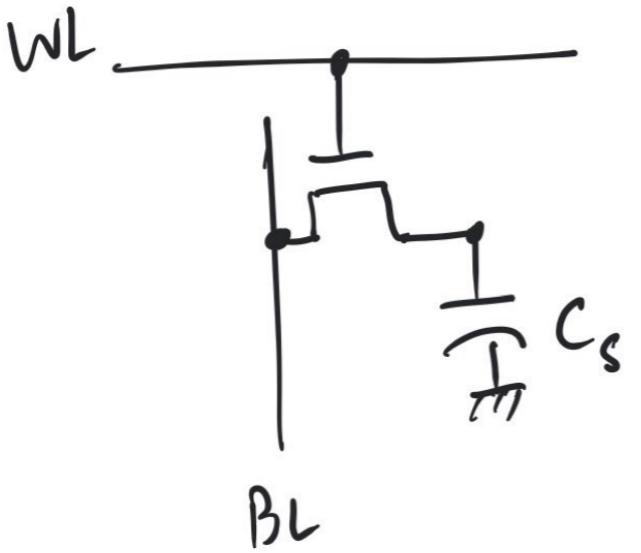
- 1) Set V_{BL} & $V_{\bar{BL}}$ according to
 { data to be stored
 (driven by voltage sources)
- 2) Turn on WL (i.e. $V_{WL} \rightarrow V_{DD}$)
- 3) Wait for a delay for
 data to be written
- 4) Turn off WL (i.e. $V_{WL} \rightarrow 0V$)
- 5) Disconnect BL & \bar{BL} from
 voltage sources

Read op.

- 1) Prech. V_{BL} & $V_{\bar{BL}}$ to V_{DD}
- 2) Turn on WL
- 3) Wait
- 4) Sense V_{BL} & $V_{\bar{BL}}$
- 5) Turn off WL



DRAM



Write ops.

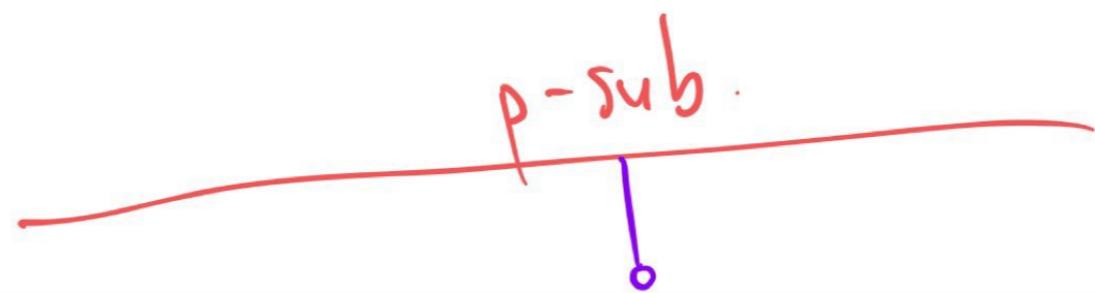
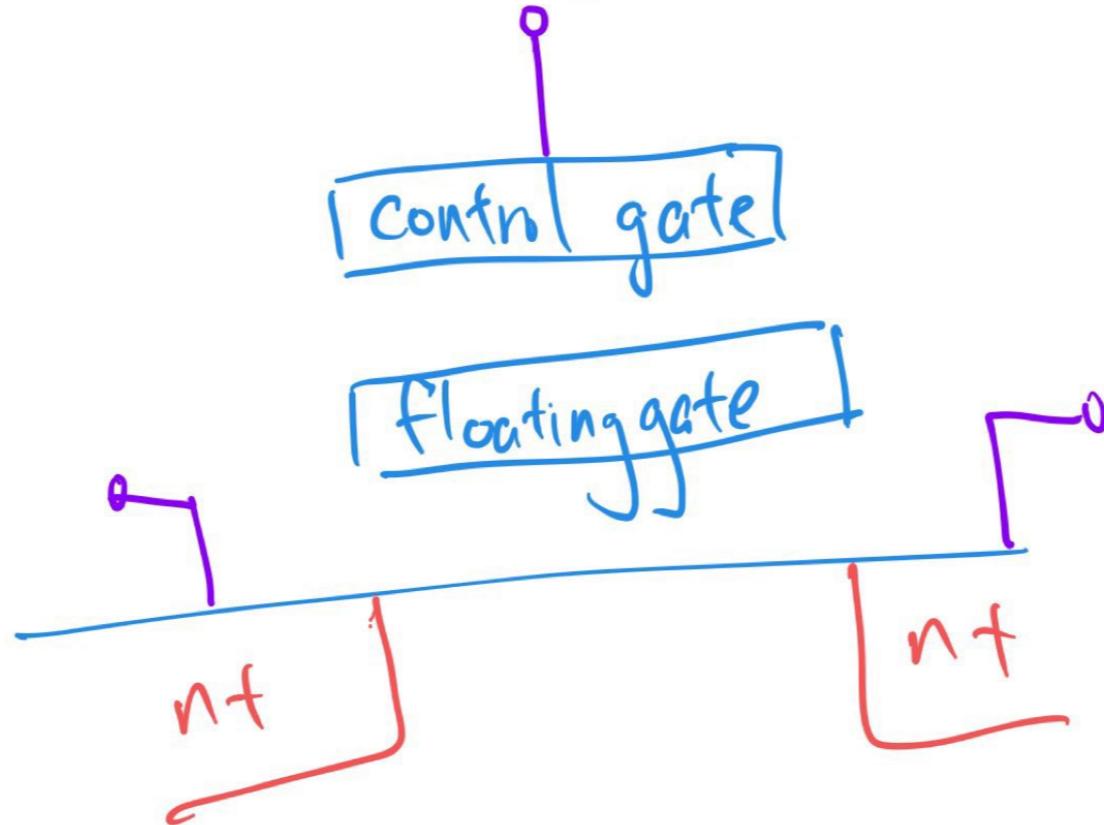
- 1) Put data on BL
(set V_{BL})
- 2) Turn on WL
- 3) Wait
- 4) Turn off WL
- 5) Disconnect BL

Read ops.

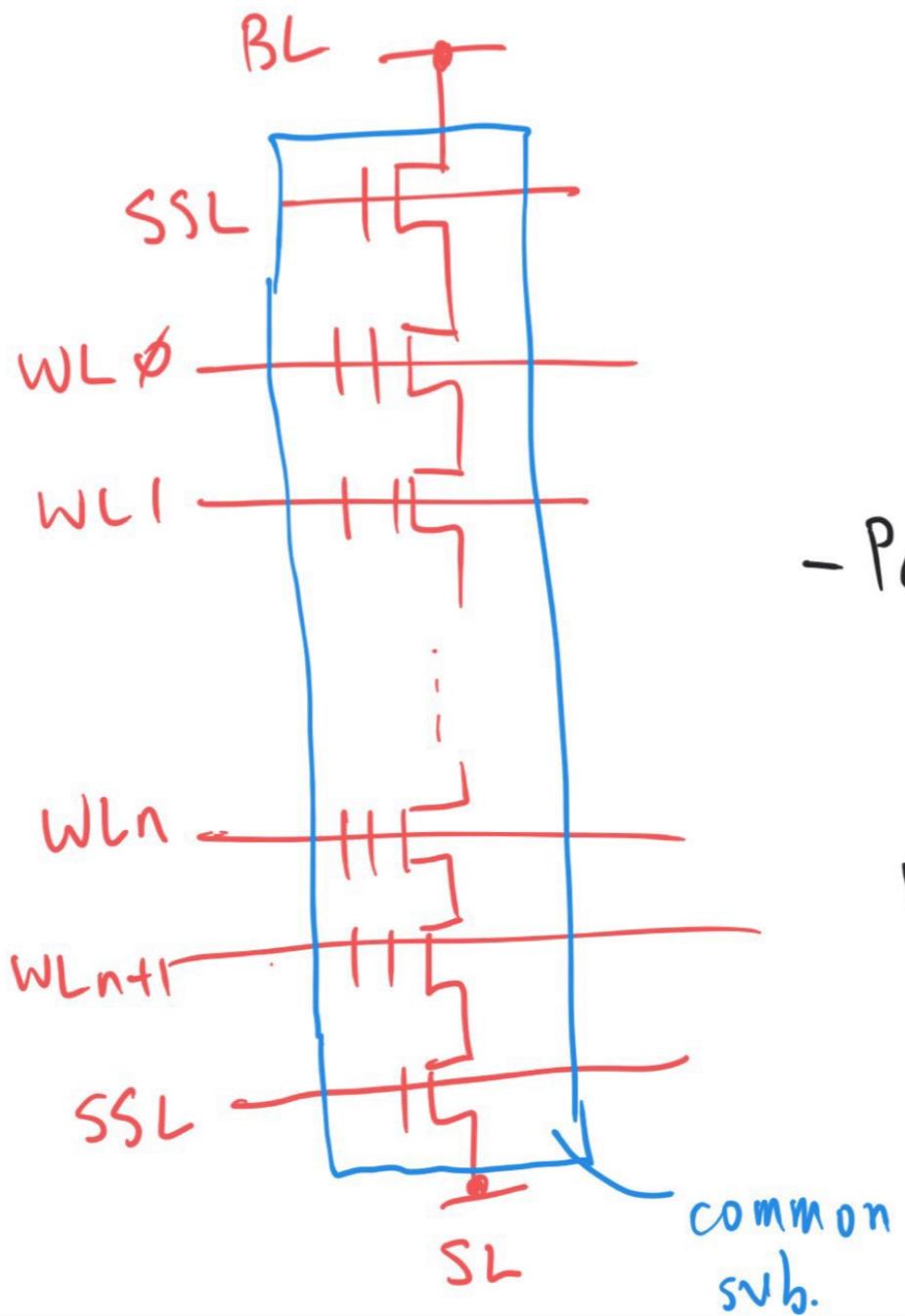
- 1) Prech. V_{BL}
- 2) Turn on WL
- 3) Wait
- 4) Sense V_{BL}
- 5) Turn off WL

Flash mem.

(FAMOS) floating gate transistor.



NAND String



Block : multiple NAND strings with common sub.

Page : multiple NAND strings with common SSL, BL/SL, WL_x.

Program

- Page - program

Erase

- Block - erase

Read

WL_x : V_{DD}

WL_n : V_{read}