NATIONAL UNIVERSITY OF SINGAPORE
Department of Electrical and Computer Engineering

CG2028 Computer Organization

Tutorial 5
Cache Memory Principles

1. A computer system has 3 devices in the memory hierarchy – cache, RAM and Solid State Drive (SSD), having access times of 10 ns, 1 μs and 100 μs respectively. The access frequencies of two of the devices (not in any particular order) are 0.9 and 0.001. Compute the average access time for the memory system.

2. A computer system has main memory capacity of 8192 blocks whereas the cache can hold 256 blocks, organized into 64 sets. What is the maximum number of comparisons required before the cache controller can determine whether the data addressed by the CPU is present in the cache? How many bits will need to be stored as overhead for the tag field in each cache block?

3. A cache can hold 3 blocks and is fully associative. Consider a request sequence as follows – 1, 2, 1, 2, 3, 3, 4, 1, 5, 2, 4, 2, 5. Draw a diagram that identifies the block to be replaced whenever a miss occurs, assuming an optimal replacement algorithm is used.

4. Which mapping strategy is used for level 1 cache by the latest processors from Intel? (not examinable)