Q.1 (a) The formula for the determining the volume of a sphere with radius *r* is

$$V = \frac{4}{3}\pi r^3$$

Write the main body of an ARMv7-M assembly language function that calculates the sum of the volumes of *N* spheres with radii r_i, where $i = 1, .., N$.

The assembly language function does not need to deal with floating point numbers and only needs to handle integer values. Assume that all floating-point values have been scaled by a scaling factor α to get scaled integer approximations before the assembly language program is executed.

The scaled integer approximations of the r_i values are stored in consecutive 4-byte words in main memory starting from location RADIUS. The value of *N* is stored at location N and the result should be stored in a 4-byte word at location RESULT.

(10 marks)

(b) Explain how a main program and the assembly language function in part Q.1 (a) can be used to calculate the sum of the volumes of spheres with the radii values shown in Table Q.1(b).

Table Q.1(b)

i	r_i
1	9.962
2	4.671
3	3.293
4	0.939
5	1.745

(4 marks)

(c) What is the largest unsigned integer value that a word of length 4 bytes can hold?

(3 marks)

(d) Assuming that $r_i \leq 10$ and $N \leq 5$, determine an appropriate scaling factor α such that overflow does not occur and the loss of precision in the numerical values is minimized. The same scaling factor α should be used for all floating-point quantities in the expression shown in part Q.1 (a) above.

For the radii values shown in Table Q.1(b), complete Table Q.1(d) using the scaling factor α that you have determined.

Table Q.1(d)

Word address	Content
RADIUS	
RADIUS+4	
RADIUS+8	
RADIUS+12	
RADIUS+16	

(8 marks)

Q.2 (a) Most real-world data memory modules require the processor to assert a MemRead signal when a read operation is to be performed. This MemRead signal is generated by the control unit of the processor, just like other control signals. Derive an expression for generating this MemRead signal. You may refer to the appendix for the instruction formats.

(6 marks)

(b) A cache has a total of 4 blocks and is 2-way set-associative. The main memory has 256 blocks. Each block is composed of 4 words, and the memory is word-addressable. Explain how the cache controller uses the address issued by the processor to check if the requested word is present in the cache. Include details of how each bit of the address is used.

(6 marks)

(c) For the scenario in Q.2 (b), assume that the processor requests for main memory blocks in the sequence 0, 1, 2, 3, 4, 6, 2, 0, 3, 1. Draw a diagram which clearly shows all requests which result in a cache hit, and which block is replaced for each miss, assuming that the FIFO replacement algorithm is used.

(7 marks)

(d) What is the minimum number of independent instructions / NOPs between the two instructions below in a 5-stage pipelined processor? Explain clearly what will happen if the two instructions are not sufficiently spaced apart. You may refer to the appendix for the diagram of a 5-stage pipelined processor.

```
ADD R1, R2, R3
STR R1, [R4]
```

(6 marks)

APPENDIX

Table A.1 : Definition of fields for the instruction formats in Figure A.1

Field	**Definition** (all values are in binary)
op	00 for Data Processing (DP), 01 for Memory, 10 for Branch
I	0 for DP register, 1 for DP immediate
cmd	Command executed by the ALU
S	0 for instructions which do not set flags, 1 for instructions which set flags
M	0 for usual DP, 1 for multiplication
L	0 for store, 1 for load
U	0 when immediate is subtracted, 1 when immediate is added
PW	00 for post-indexed, 10 for offset mode, 11 for pre-indexed
cond	condition code for branch