NATIONAL UNIVERSITY OF SINGAPORE

SCHOOL OF COMPUTING

ASSESSMENT FOR
Semester 2 AY2019/2020

CG2271 – Real-Time Operating Systems

Mar 2020 **Time Allowed: 1 hour**

INSTRUCTIONS TO STUDENTS:

1. This assessment paper contains **FIFTEEN (15)** questions and comprises **EIGHT (8)** printed pages, including this page, and **FIVE (5)** printed pages of Appendix.
2. Students are required to answer **ALL** the questions.
3. Shade your answers on the OCR Answer sheet using a 2B pencil. The OCR sheet is the only thing that will be collected back at the end of the test.
4. A Single A4 (Double-Sided) Reference Sheet is allowed.
5. You are allowed to use Stand-Alone Calculators. Handphone Calculators are NOT allowed.
6. When multiple options can be the answer, choose the most appropriate combination from the available options.

QUESTIONS

You are given the following code.

```
#define SW_POS                  6
#define MASK(x)                 (1 << (x))

#define PORT_ALPHA_MASK         0xF0000u
#define PORT_ALPHA_SHIFT        16
#define PORT_ALPHA_WIDTH        4
#define PORT_ALPHA(x)           (((x)<<PORT_ALPHA_SHIFT) & PORT_ALPHA_MASK)

#define PORT_BETA_MASK          0x700u
#define PORT_BETA_SHIFT         8
#define PORT_BETA_WIDTH         3
#define PORT_BETA(x)            (((x)<<PORT_BETA_SHIFT) & PORT_BETA_MASK)

init()
{
    SIM->SCGC5 |= SIM_SCGC5_PORTD_MASK;             // LINE 1
    PORTD->PCR[SW_POS] |= PORT_ALPHA(0x0a | 0x01);  // LINE 2
    PORTD->PCR[SW_POS] |= PORT_BETA(~0xFE);         // LINE 3
    PTD->PDDR &= ~MASK(SW_POS);                     // LINE 4

    NVIC_SetPriority(PORTD_IRQn,1);
    NVIC_ClearPendingIRQ(PORTD_IRQn);
    NVIC_EnableIRQ(PORTD_IRQn);
}
```

You can refer to the Appendix for the full description of the registers.
LINE 4 configures Port D Pin 6 as an input pin.

1. With reference to the code above, what is the objective of LINE 2?

    a) Enable the Internal Pull-Up Resistor for Port D Pin 6.
    b) Enable DMA Request Interrupt on Rising Edge of Port D Pin 6.
    c) Enable Interrupt on Falling Edge of Port D Pin 6.
    d) Enable Interrupt on Both Rising and Falling Edge of Port D Pin 6.
    e) Enable Interrupt when the Pin has a Logic 1.

2. With reference to the code above, what is the objective of LINE 3?

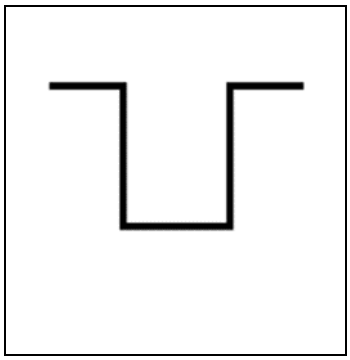
   S1. Enable Internal Pull-Up Resistor for Port D Pin 6.

   S2. Enable the Slew Rate for Port D Pin 6.

   S3. Enable GPIO Functionality for Port D Pin 6.

   a) Only S1 and S2 are correct.
   b) All three statements, S1, S2 and S3 are correct
   c) Only S1 and S3 are correct
   d) Only S3 is correct
   e) All three statements, S1, S2 and S3 are wrong

3. The following signal is generated by the Switch connected to Port D Pin 6 whenever it is pressed and released. When it is pressed, a negative transition is generated, and when it is released a positive transition is generated.



   How many Interrupt Requests will be registered by the Microcontroller based on the current configuration?

   a) 1
   b) 2
   c) 3
   d) 4
   e) 5

4. It is known that Port D is mapped to IRQ 31. The priority is configured in IPR7 which is shown below.

Bits	31:30	29:24	23:22	21:16	15:14	13:8	7:6	5:0
IPR7	IRQ31	reserved	IRQ30	reserved	IRQ29	reserved	IRQ28	reserved

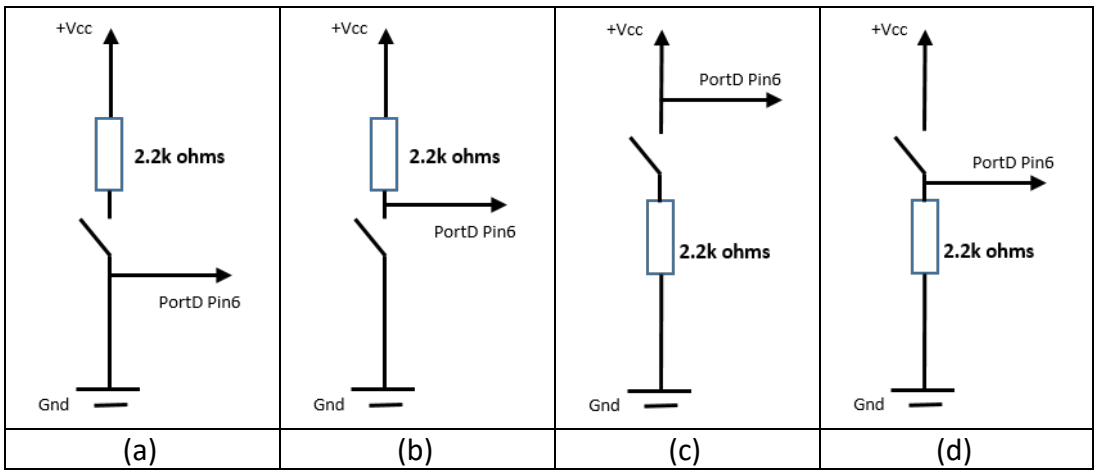
No other interrupts are configured in the system. What is the 32-bit value in the IPR register based on the given code?

a) 0x10000000
b) 0x00000010
c) 0x00000040
d) 0x40000000
e) 0x80000000

5. Which of the following lines correctly configures the IRQ Priority Level for Port D. Assume that IPR7 register can be directly accessed as shown below.

```
a) IPR7 |= (0x1 << 32);
b) IPR7 |= (0x1 << 31);
c) IPR7 |= (0x1 << 30);
d) IPR7 |= (0x1 << 6);
e) IPR7 |= (0x1 << 1);
```

6. The following figures are possible options for designing the Switch that is connected to Port D Pin 6. Which of the following designs will generate the signal based on the figure and the description in Question 3?



(a)	(b)	(c)	(d)

7. The Cortex M0+ has a Periodic Interrupt Timer (PIT) module. Which of the following statements is TRUE?

   S1. The Timer Start Value can be changed anytime.
   S2. We can configure Interrupts to be triggered whenever the Timer counts down to 0.
   S3. We can configure Interrupts to be triggered whenever the Timer counts up to a specific value.

   a) All three statements S1, S2 and S3 are TRUE.
   b) Only statements S1 and S2 are TRUE
   c) Only statements S1 and S3 are TRUE
   d) Only statements S2 and S3 are TRUE
   e) Only S2 is TRUE

8. The earlier program is updated with the code to allow the PIT module to generate Interrupts. The following sequence takes place.

   - The main() code is running and the Push Button is pressed.
   - Immediately after that, the PIT module generates an Interrupt.

   Here are possible scenarios on what will happen next.

   S1. The moment the PIT generates an Interrupt, the code will immediately jump to the IRQ Handler for the PIT module.

   S2. The Push Button IRQ Handler will complete first and then we will execute the PIT IRQ Handler.

   S3. The PIT module's Interrupt request can be programmed so that it is ignored and the interrupt is never serviced.

   Which of the above statements is TRUE?

   a) Only S1 is TRUE
   b) Only S2 is TRUE
   c) Only S1 and S2 can be TRUE
   d) Only S2 and S3 can be TRUE
   e) All statements S1, S2 and S3 can be TRUE

9. Which of the following statements is TRUE for a volatile global variable?

   S1. Whenever the data is accessed in the code, it will use the last fetched data that is stored in the internal registers of the processor.

   S2. Whenever the data is accessed in the code, a new copy of the data is always fetched from memory.

   S3. It can be accessed by a task and an interrupt.

   a) Only S1 is TRUE
   b) Only S1 and S3 are TRUE
   c) Only S2 and S3 are TRUE
   d) S1, S2 and S3 are all TRUE
   e) S1, S2 and S3 are all FALSE

10. The UART2 module in the Cortex M0+ is configured to operate in Interrupt mode for both Transmit and Receive Data. Which of the following statements is TRUE?

    S1. There are TWO separate IRQ Handlers for the Transmit and Receive Interrupts.

    S2. There is only ONE IRQ Handler for both the Transmit and Receive Interrupts.

    S3. There are TWO separate Interrupt Flags for Transmit and Receive Interrupts.

    a) Only S1 and S2 are correct.
    b) Only S2 and S3 are correct.
    c) Only S1 and S3 are correct.
    d) S1, S2 and S3 are all correct.
    e) S1, S2 and S3 are all wrong.

The following questions are to be answered in the context of a RTX-RTOS based system with default settings.

11. A task (T1) that is **RUNNING** gets switched to the **READY** state. Which of the following could be the cause?

    a) Another task acquired a resource that was being held by T1.
    b) T1 attempted to acquire a resource and was successful.
    c) T1 attempted to acquire a resource that is currently unavailable.
    d) T1 chose to call osDelay(1) in its code to voluntarily give up the CPU.
    e) None of the above statements are valid.

12. A task (T1) that is **RUNNING** gets switched to a **BLOCKED** state. Which of the following statements is TRUE?

    a) T1 has been preempted by a higher priority task.
    b) T1 attempted to acquire a resource but was unable to get it.
    c) T1 was allocated a resource that it was waiting for.
    d) T1 was preempted by another task with the same priority as T1.
    e) Option (b) and (d) are both TRUE.

13. A task is currently in the **RUNNING** state with all the required resources. The scheduler will still perform a context switch after some time to ensure that other equal-priority tasks have a chance to execute.

    a) True
    b) False

14. A system has FOUR tasks labelled T1, T2, T3 and T4, in order of priority (T1 being the highest). It is observed that only T1 is in the **RUNNING** state most of the time. Tasks T2 and T3 only got a chance to go to the **RUNNING** once. Task t4 gets to go to the **RUNNING** state occasionally.

    Examine the following statements:

    S1. This can only happen if Task t1 is always in the RUNNING state preventing the lower priority tasks from running.

    S2. Tasks t2 and t3 and always stuck in the READY state from the start of the program.

    S3. Task t1 is holding onto a resource that is required by Task t2 and t3.

    S4. Task t4 is holding onto a resource that is required by Task t2 and t3.

Which of the above statements can be TRUE?

a) Only S1 and S2
b) Only S2
c) Only S3
d) Only S3 and S4
e) None of the statements can be true

15. The following code snippet shows the creation of TWO threads in the main() function.

```
int main (void) {

  // System Initialization
  SystemCoreClockUpdate();
  InitGPIO();
  offRGB();
  // ...

  osKernelInitialize();                 // Initialize CMSIS-RTOS
  osThreadNew(led_red_thread, NULL, NULL);    // Create application led_red threa
  osThreadNew(led_green_thread, NULL, NULL);  // Create application led_green thr
  osKernelStart();                      // Start thread execution
  for (;;) {}
}
```

Examine the following statements.

S1. The InitGPIO() function is necessary to ensure that the GPIO pins used by the RTOS scheduler are correctly initialized.

S2. The scheduler will randomly decide which of the TWO threads will run first.

S3. The moment we complete the osKernelInitialize() function, we have switched over to the RTOS multi-threaded environment.

Which of the above statements is TRUE?

a) Only S2 is TRUE
b) Only S1 and S2 are TRUE
c) Only S1 and S3 are TRUE
d) Only S2 and S3 are TRUE
e) All of the statements, S1, S2 and S3 are FALSE.

THE END