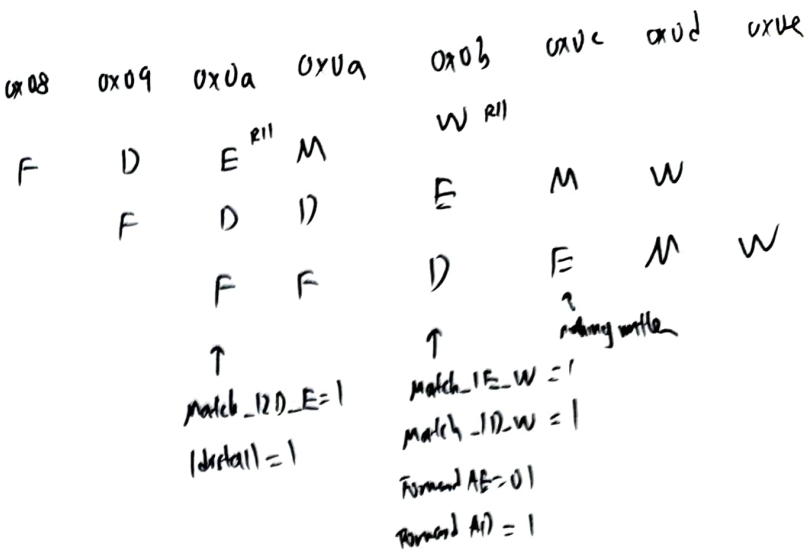
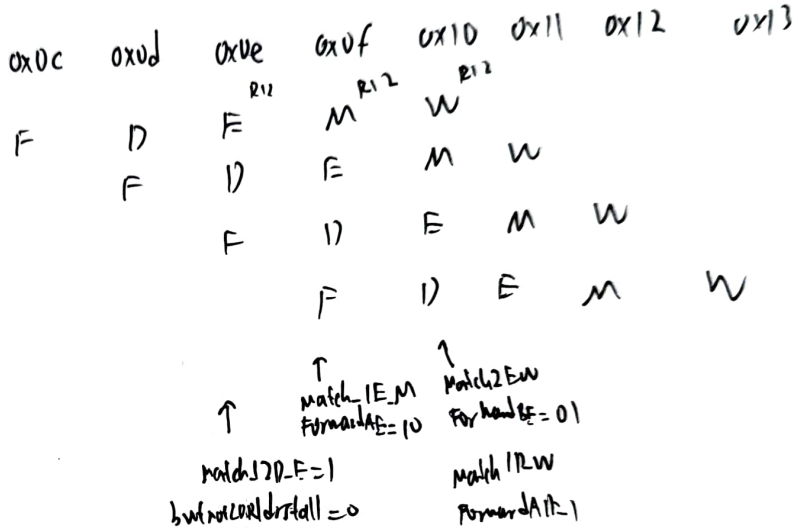
Load and Use Hazard

```
0x08  LDR  R11, HUNDRED
0x09  RSBS R12, R11, R6
0xUa  RSCS R12, R11, R6
```



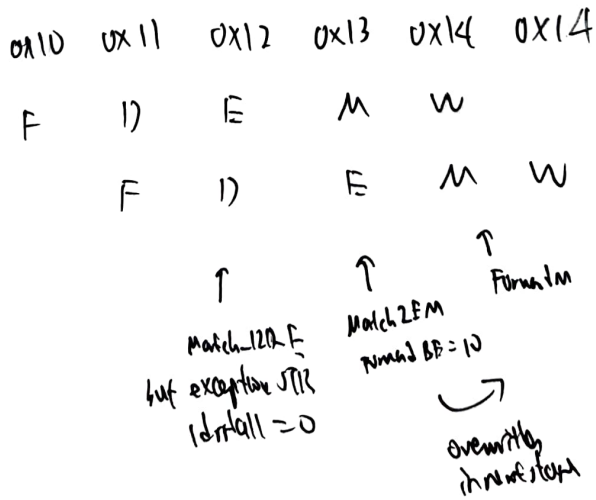
Data Forwarding

```
0x0c  RSCS R12, R11, R6
0x0d  ADC  R13, R12, #101
0x0e  TST  R11, R12
0x0f  TBB  R12, #2
```



LDR STR mem_mem Copy

```
0x10  LDR  R12, BOTH_WAIT
0x11  STR  R12, [R4]
```



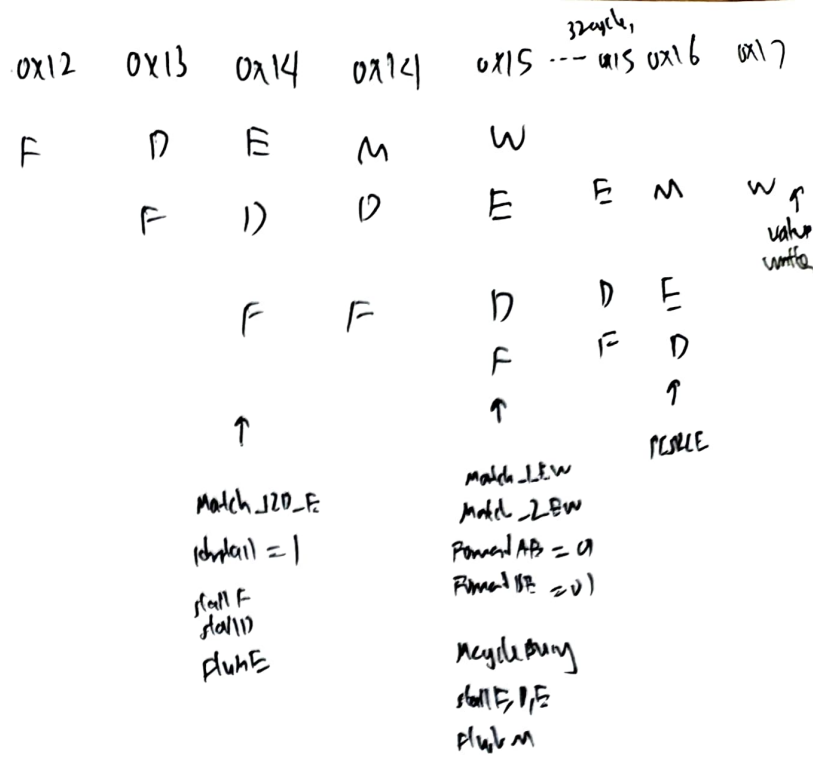
Load & Use + Mcycle stall

0x12 LDR R12, LARGEST_VAL

0x13 MUL R15, R12, R12

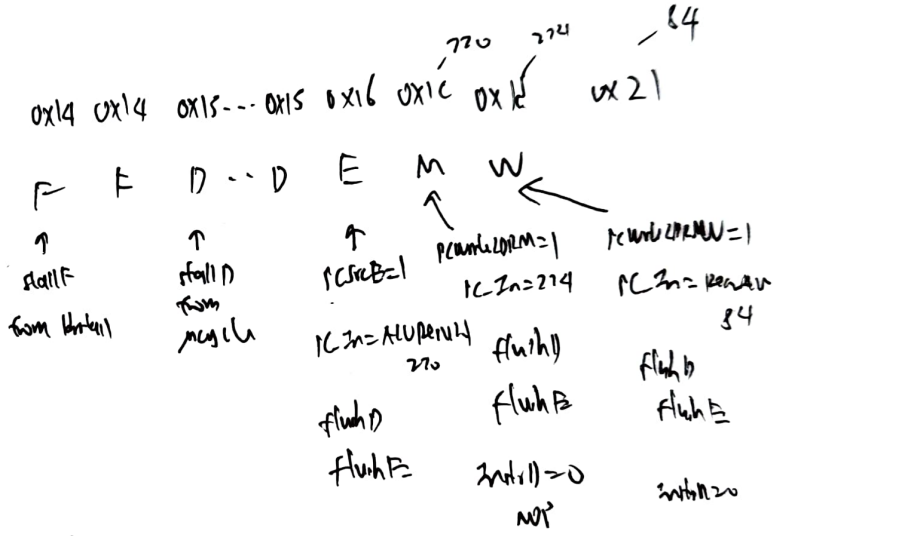
0x14 LDR R15, PC_LDR_ADDR

0x15 ORR R12, R6, #255



LDR PC

0x14 LDR R15, PC_LDR_ADDR (0x14)



exception to no stall for B, LDR, STR, PP from RA 2

should flush P!

BTA

0x21 B ; map_back (0x84)