

Load and Use Hazard

0x08 LDR R11, HUNDRED
0x09 RSB3 R12, R11, R6
0x0a RSC3 R12, R11, R6

| | | | | | | |
|--------|--------|------------------|--------|----------------|--------------------|--------|
| $0x08$ | $0x09$ | $0x0a$ | $0x0b$ | $0x0c$ | $0x0d$ | $0x0e$ |
| F | D | E ^{R11} | M | E | M | W |
| | F | D | D | E | | |
| | | F | F | D | E | M W |
| | | | | | ? reading write | |
| | | ↑ | | ↑ | | |
| | | match_ID_E = 1 | | match_IE_W = 1 | | |
| | | (distall) = 1 | | match_ID_W = 1 | | |
| | | | | Forward AB = 0 | | |
| | | | | Forward A? = 1 | | |

Data Forwarding

0x0C RSCS R12, R14, R6
 0x0D ADC R13, R12, #101
 0x0E TST R11, R12
 0x0F TBL R12, #2

| 0x0C | 0x0D | 0x0E | 0x0F | 0x10 | 0x11 | 0x12 | 0x13 |
|------|------|----------------|----------------|----------------|------|------|------|
| | | ^{R12} | ^{R12} | ^{R12} | | | |
| F | D | F | M | W | | | |
| | F | D | F | M | W | | |
| | | F | D | F | M | W | |
| | | | F | D | F | M | W |

↑ match IE_M
 format_{IE} = 10

↑ match 2EW
 format_{EW} = 01

match 1RW
 format_{1RW} = 1

match 12D-F = 1
 but not 12D-F stall = 0

L172
 5112 mem-mem copy

0x10 LDR R12, BOTH_wan
0x11 STR R12, [P4]

| 0x10 | 0x11 | 0x12 | 0x13 | 0x14 | 0x14 |
|------|------|------|------|------|------|
| F | 1) | E | M | W | |
| | | | | | |
| F | 1) | E | M | W | |

↑ Match 128 F
 but exception still
 idr=all = 0

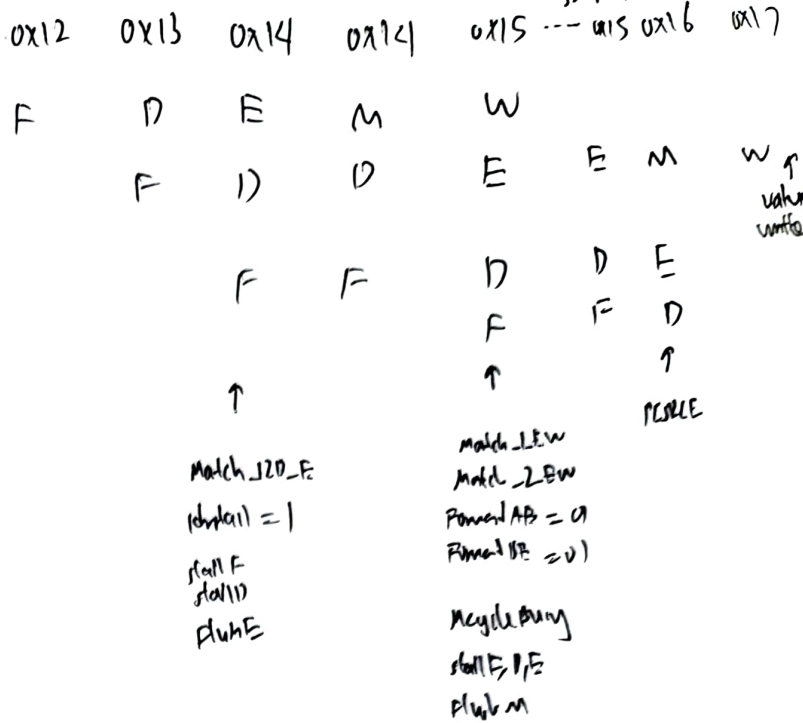
↑ Match 2EM
 NumB BB = 10

↑ Form 1m

↘
 overwrt
 in next steps

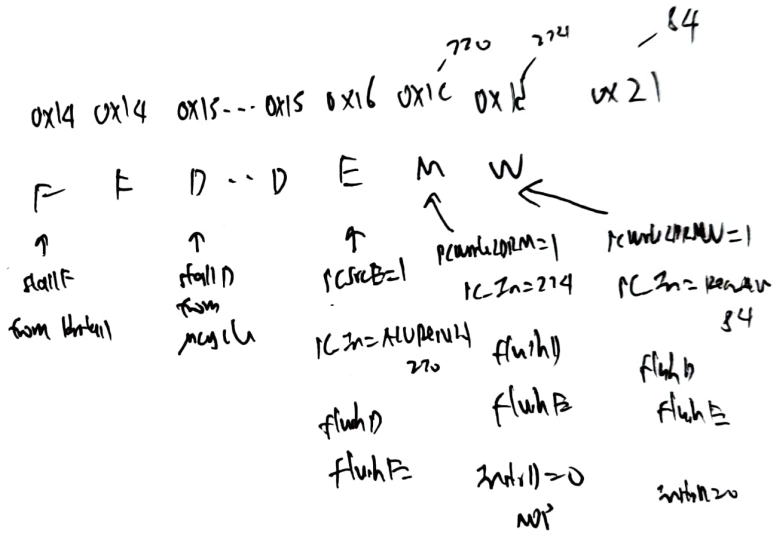
Load & Use + Micycle fail

0x12 LDR R12, LARGEST_VAL
 0x13 MUL R15, R12, R12
 0x14 LDR R15, PC-LDR-ADDR
 0x15 ORR R12, R6, #255



LDR PC

0x14 LDR R15, PC-LDR-ADDR



exception is not stall for B, LDR, STR, PP since RA 2

should flush P!

BTA

0x21 B, wrap-back 0x54

0x21 0x22 0x23
 F D E

PCStallB=1
 PCIn=ALUResult
 0x16
 /