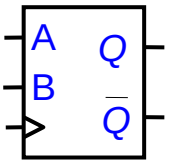
Tutorial 8 Questions (Part 2)

Design Method for Flip-Flops and Counters

1. Implement the A-B flip-flop shown below using a D flip-flop and minimum logic gates. The A-B flip-flop's condensed characteristic table is shown below (right).

   (i) Develop the characteristic table of the AB flip-flop.
   (ii) Draw a functional block diagram for the AB flip-flop.
   (iii) Design & implement the flip-flop using a D FF.
   (iv) Implement your design in Verilog. Test your solution using the Xilinx tools.



A	B	Q+
0	0	1
0	1	Q
1	0	$\overline{Q}$
1	1	0

Condensed Characteristic Table

2. Design a mod-4 counter with the count sequence 1, 2, 4, 8, 1… using D Flip-flops and a minimum number of logic gates.
   (i) Construct the functional block diagram of this counter.
   (ii) Determine the next state table of this counter.
   (iii) Design & implement the counter.

3. A positive-edge triggered 2-bit counter counts has four modes of operation depending on a two-bit control synchronous input **X**, as shown in the table below:

X	Modes
00	Hold
01	Count in forward sequence
10	Count in reverse sequence
11	Clear

   Carry out the following to implement the 2-bit counter using D FFs.
   (i) Construct the functional block diagram of this counter.
   (ii) Determine the next state table of this counter.
   (iii) Design & implement the counter using D FFs.