EE2026: DIGITAL DESIGN

Academic Year 2020-2021, Semester 2

LAB 2: Combinational Circuits in Verilog

OVERVIEW:

A combinational circuit is one where the outputs depend only on the current inputs. In this lab, we will be designing some combinational circuits that are able to perform addition.

The pre-requisite for this lab requires one to be able to:

- Create a Verilog project and design source in Vivado.
- Create a testbench to simulate the design source.
- Generate the RTL schematic and the synthesised circuit schematic of design source.
- Map and implement a design on the Basys 3 development board.
- Understand well the contents of Lectures 1, 2, and especially 3: Introduction to Verilog.

This lab will cover the following:

- Designing a one-bit full adder circuit using the dataflow modelling method.
- Designing a two-bit parallel adder circuit using the structural modelling method.

Tasks for this lab include:

- Designing the Verilog code of a one-bit full adder.
- Designing, simulating and implementing a four-bit parallel adder on the FPGA.
- Understanding a 1-bit two-to-one multiplexer that can be used in the graded post-lab assignment.

GRADED ASSIGNMENT [LUMINUS SUBMISSION: MONDAY 15th FEBRUARY 2021, NOON]:

- Designing, simulating and implementing an n-bit subtractor with overflow detection, on the Basys 3 development board

Further details are available at the end of this lab manual

ONE-BIT-FULL ADDER:

Consider the binary addition shown in ***Figure 2.1***. To design a circuit that would perform the addition of two one-bit values, the circuit would need to have three input bits and two output bits.

Figure 2.1: *Binary Addition and functional block diagram of the one-bit full adder*

Such a circuit is called a one-bit full adder. It adds two bits (**A**, **B**) and the carry ($\mathbf{C_{in}}$) from a previous stage of addition, and produces a sum (**S**) and a carry ($\mathbf{C_{out}}$), as illustrated through a truth table in ***Figure 2.2***. By simplifying the truth table, the Boolean expressions for **S** and $\mathbf{C_{out}}$ can be obtained.

A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$S = A \oplus B \oplus C_{in}$$

$$C_{out} = AB + C_{in}\,(A \oplus B)$$

Figure 2.2: *Truth table and boolean expressions of the one-bit full adder*

Note: A half adder, in contrast to a full adder, does not involve a carry input. Thus, for a half adder, $S = A \oplus B$, *and* $C_{out} = AB$

UNDERSTANDING | TASK 1

Using the dataflow method, complete the Verilog code for the one-bit full adder. Verify that the RTL schematic is as shown.

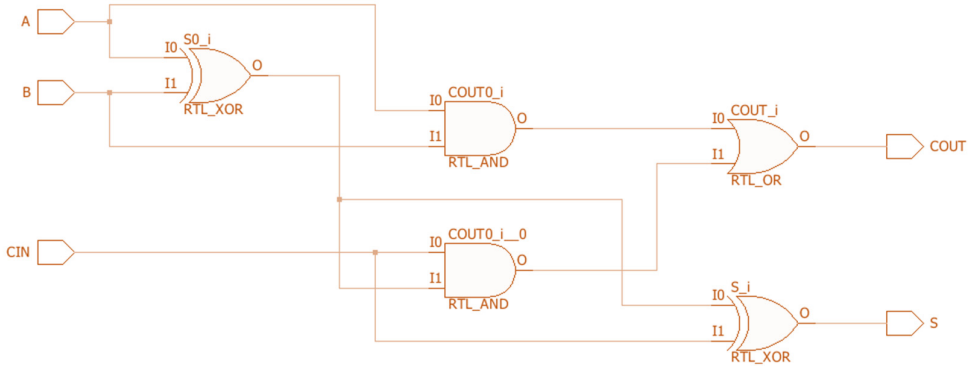
Verilog skeleton code for the one-bit-full adder:

```
module my_full_adder(input A, B, CIN, output S, COUT);

    assign S =
    assign COUT =

endmodule
```

RTL schematic for the one-bit full adder:



TWO-BIT FULL ADDER:

By cascading one-bit full adder blocks, the one-bit adder can be reused and parallel adders that add multiple bits can be created through the structural modelling method. A two-bit ripple-carry adder is illustrated in ***Figure 2.3***.

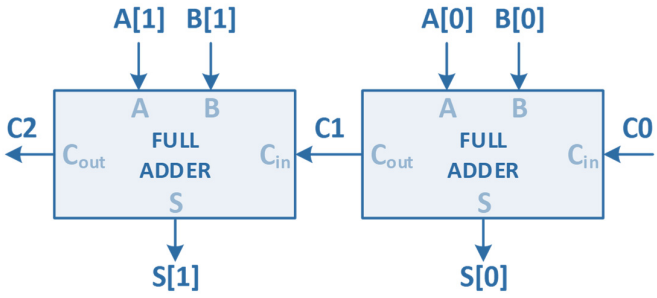


Figure 2.3: *Functional block diagram of the two-bit ripple-carry adder*

With the code for a one-bit full adder, a new module is created and two full adder blocks (fa0, fa1) are instantiated. By specifying the inputs and outputs to these blocks, the connection **C1** between them is made. Note that the order of signals during instantiation should respect the order in which they were declared in the one-bit full adder module **my_full_adder**.

This approach to hardware description is called structural modelling, whereby a more abstract module (for example, **my_2_bit_adder**) is built from simpler components describing gate-level hardware (such as **my_full_adder**).

Verilog code for two-bit ripple-carry adder, using structural modelling:

```
module my_2_bit_adder(input [1:0] A, input [1:0] B, input C0,
                      output [1:0] S, output C2);

    wire C1;

    my_full_adder fa0 (A[0], B[0], C0, S[0], C1);
    my_full_adder fa1 (A[1], B[1], C1, S[1], C2);

endmodule
```

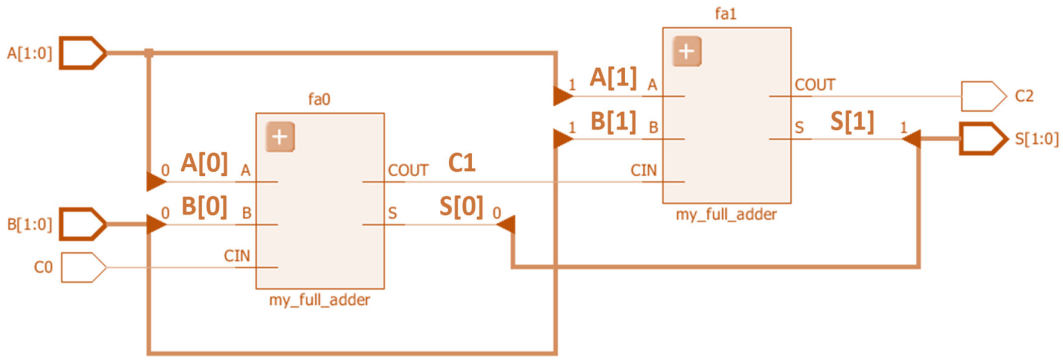
[Note] Two-bit port declaration for A, B, S:

Instead of having multiple input and output ports (A1, A0, B1, B0, S1, S0), multi-bit vector ports are defined.

Example: `input [5:0] apple`

Input port name is **apple**, with size of 6 bits. apple[5] refers to the MSB, apple[0] refers to the LSB.

RTL schematic for the two-bit ripple-carry adder:



FOUR-BIT FULL ADDER:

The functional block diagram of a four-bit ripple-carry adder is shown in ***Figure 2.4***.

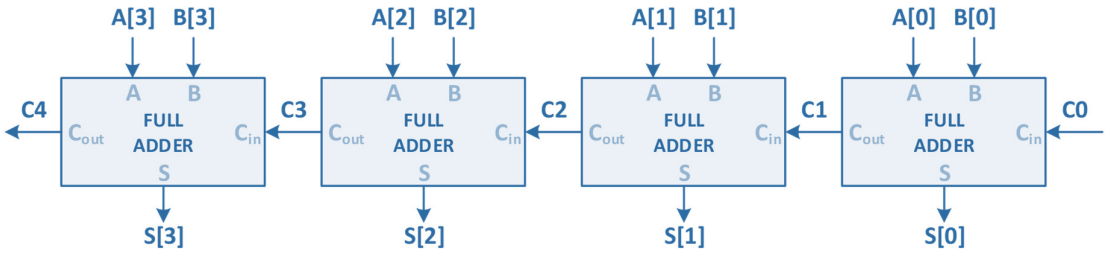


Figure 2.4: *Functional block diagram of a four-bit ripple-carry adder*

UNDERSTANDING | TASK 2

Start by adding a new design source for the four-bit full adder.

1. By using the structural modelling method, design a four-bit ripple-carry adder.
2. Generate the RTL schematic and check that connections between the blocks are correct.
3. Simulate your code with the following three sets of input values, and check that the simulation outputs are correct:

A:		0	0	1	1	A:		1	0	1	1	A:		1	1	1	1
B:	+	0	0	1	1	B:	+	0	1	1	1	B:	+	1	1	1	1
		□	□	□	□			□	□	□	□			□	□	□	□

[Note] Brief guidelines for multi-bit vector ports in the testbench:

- The port size should be indicated when declaring the signals. Inputs to the module being tested are declared using **reg**, whereas outputs from the module being tested are declared using **wire**:
  `reg [3:0] A; wire [3:0] S;`

- The parameters for the module being tested do not need the port size of the signals:
  `my_4_bit_adder module_alias (A, B, CARRY_IN, S, CARRY_OUT);`

- The testbench stimuli for multi-bit vector ports can be written as:
  `A = 4'b0011; B = 4'b0011; CARRY_IN = 1'b0;`

4. Synthesise and implement your code on the FPGA, using appropriate switches and LEDs on the Basys 3 development board to represent the inputs and outputs.

This task is considered completed and understood if you have the following items related to the four-bit full adder:

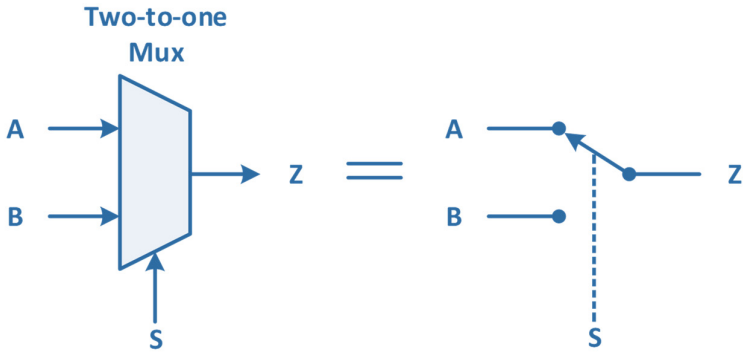
- The RTL schematic of your design (item 2 of this task)
- The simulation waveform results of the three testbench stimuli (item 3 of this task)
- The four-bit ripple-carry adder on the Basys 3 development board (item 4 of this task)

UNDERSTANDING | TASK 3

Instead of using four one-bit adder blocks, can you think of an alternative way (still using structural modelling) in creating the four-bit ripple-carry adder? Consider doing the same things as indicated in **UNDERSTANDING | TASK 2** by using such alternative way. This task is meant as practice for you to improve your Vivado skills and Verilog understanding, and will not be explained.

1-BIT TWO-TO-ONE MULTIPLEXER (POST-LAB NON-GRADED – NO SUBMISSION FOR THIS):

A multiplexer (MUX) is a combinational circuit that connects one of its input signals to the output, based on the control signal. A simple 1-bit two-to-one mux, with inputs **A**, **B**, control signal **S**, and output **Z**, is illustrated as a functional block diagram, together with its simplified truth table, in **Figure 2.5.**



S	Z
0	A
1	B

Figure 2.5: *Functional block diagram and truth table of a 1-bit two-to-one multiplexer*

UNDERSTANDING | TASK 4

A quick way to implement the Verilog code for a 1-bit two-to-one multiplexer is using the conditional syntax:

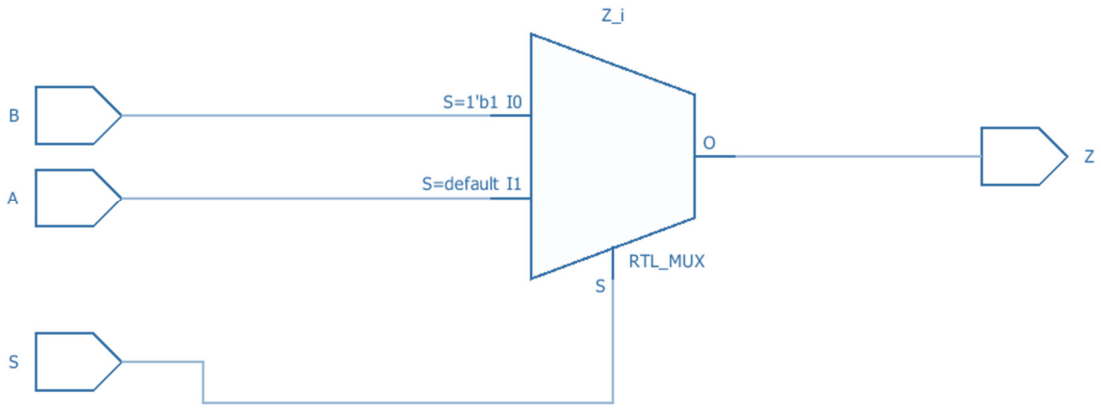
condition ? expression1 : expression2;

Notice in the schematic, how the code is automatically recognised as a MUX.

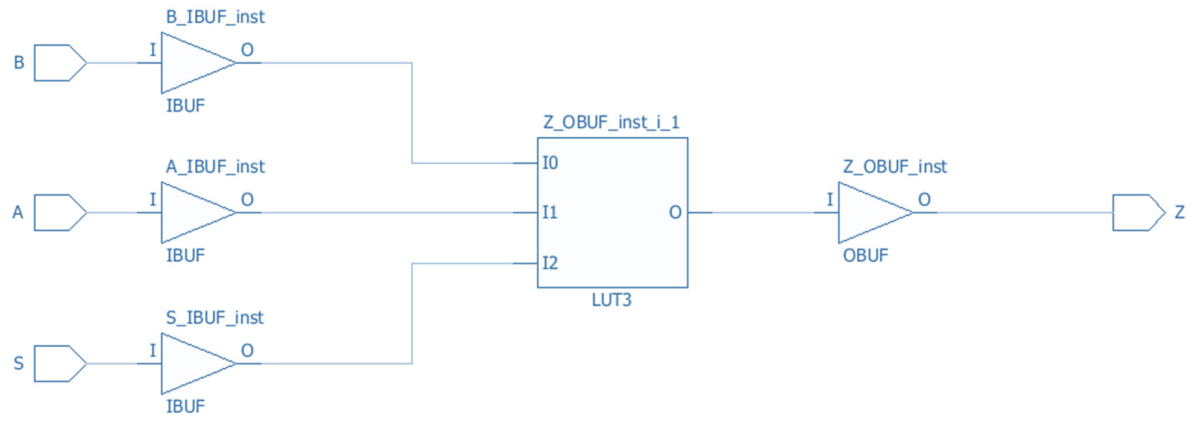
Verilog code for 1-bit two-to-one mux, using the dataflow method

```
module my_2_to_1_mux (input A, B, S, output Z);
    assign Z = S ? B : A; // assign B to Z if S = 1 or assign A to Z if S = 0;
endmodule
```

RTL schematic for the 1-bit two-to-one mux



Synthesised design schematic for the 1-bit two-to-one mux



Fill in the truth table for the **LUT3**, as extracted from the synthesised design schematic for the 1-bit two-to-one mux:

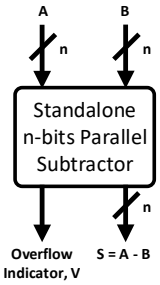
Explain how the truth table for the **LUT3** matches that of the truth table indicated in **Figure 2.5**:

GRADED POST-LAB ASSIGNMENT – THE STANDALONE SUBTRACTOR:

ASSIGNMENT

When your program starts, regardless of the switches SW0 to SW15 and leds LD0 to LD15, it is required for the seven segment displays to show the character as required from the previous lab 1 graded assignment. The anodes that are required to be enabled are also as indicated in that lab.

Then, based on your student matriculation number, you are required to create an n-bit parallel subtractor with overflow indicator (Henceforth, simply called the n-bit parallel subtractor), by combining several n-bit parallel adders. The overflow indicator is a one-bit value that indicates whether the result S is correctly represented in that specific n-bit number system. The n-bit parallel subtractor will be a standalone device, with no other subtractors connected to it and no other subtractors to connect to. The block diagram is shown below:



The RTL schematics of the n-bit parallel subtractor will need to be produced, the system simulated, and finally implemented on the Basys 3 development board.

REQUIREMENT BASED ON YOUR STUDENT MATRICULATION NUMBER

Based on the **second** rightmost numerical digit of your student matriculation number, create the following n-bit parallel adders:

Second rightmost numerical digit of your student matriculation number	Required n-bit parallel adders. Each one of these two n-bits parallel adders must be made up of multiple 1-bit adders	
0	2-bit parallel adder	3-bit parallel adder
1	3-bit parallel adder	2-bit parallel adder
2	2-bit parallel adder	4-bit parallel adder
3	4-bit parallel adder	2-bit parallel adder
4	3-bit parallel adder	4-bit parallel adder
5	4-bit parallel adder	3-bit parallel adder
6	3-bit parallel adder	5-bit parallel adder
7	5-bit parallel adder	3-bit parallel adder
8	2-bit parallel adder	5-bit parallel adder
9	5-bit parallel adder	2-bit parallel adder

After doing so, **make use of both n-bit parallel adders** to create your n-bit parallel subtractor, based on the **second** rightmost numerical digit of your student matriculation number. If required, you may assume that the user will not input any carry-in value to the n-bit parallel subtractor.

The bits given to the subtractor must be divided between the two n-bit parallel adders in the following manner:

Second rightmost numerical digit of your student matriculation number	**Most significant bits of the subtractor** must be given to the following adder	**Least significant bits of the subtractor** must be given to the following adder
0	2-bit parallel adder	3-bit parallel adder
1	3-bit parallel adder	2-bit parallel adder
2	2-bit parallel adder	4-bit parallel adder
3	4-bit parallel adder	2-bit parallel adder
4	3-bit parallel adder	4-bit parallel adder
5	4-bit parallel adder	3-bit parallel adder
6	3-bit parallel adder	5-bit parallel adder
7	5-bit parallel adder	3-bit parallel adder
8	2-bit parallel adder	5-bit parallel adder
9	5-bit parallel adder	2-bit parallel adder

Furthermore, it is compulsory to use the specified complement representation of the binary values, as indicated in the table below:

Second rightmost numerical digit of your student matriculation number	Required n-bit parallel subtractor
0	5-bit subtractor. Bits are in **2's complement**
2	6-bit subtractor. Bits are in **2's complement**
4	7-bit subtractor. Bits are in **2's complement**
6	8-bit subtractor. Bits are in **2's complement**
8	7-bit subtractor. Bits are in **2's complement**
1	5-bit subtractor. Bits are in **1's complement**
3	6-bit subtractor. Bits are in **1's complement**
5	7-bit subtractor. Bits are in **1's complement**
7	8-bit subtractor. Bits are in **1's complement**
9	7-bit subtractor. Bits are in **1's complement**

Example 1: If a student has matriculation number A1234567N, the second rightmost numerical digit is '6'. Thus, the student is required to create an 8-bit parallel subtractor, whereby all the bits are considered to be in 2's complement representation. That 8-bit subtractor must consist, at minimum, of these two parallel adders: A 3-bit parallel adder for the most significant bits, and a 5-bit parallel adder for the least significant bits.

Example 2: If a student has matriculation number A6543210Y, the second rightmost numerical digit is '1'. Thus, the student is required to create a 5-bit parallel subtractor, whereby all the bits are considered to be in 1's complement representation. That 5-bit subtractor must consist, at minimum, of these two parallel adders: A 3-bit parallel adder for the most significant bits, and a 2-bit parallel adder for the least significant bits.

SIMULATION REQUIREMENT:

You are also required to simulate any five unique test cases as chosen by you, for your n-bit subtractor circuit, to verify that the outputs, S and V, are as desired. If the number of unique test cases is less than five, full marks will not be achievable.

A screenshot (PrintScreen) of the simulation waveform pattern from the Vivado simulation window must be obtained, and then pasted on a 1-page landscape page. Marks are only given if the simulation waveforms are clear, and **all the five values** are **clearly visible in binary representations**.

RTL ANALYSIS SCHEMATIC REQUIREMENT:

A screenshot (PrintScreen) of the RTL analysis schematic from Vivado must be obtained, and pasted on a 1-page landscape page. You are not allowed to do any editing to the RTL analysis schematic screenshot.

For marks to be awarded, the following conditions must be met for the RTL analysis schematics (The images being shown here is for a 9-bit subtractor system, where a 4-bit parallel adder was used for the 4 most significant bits, and a 5-bit parallel adder was used for the 5 least significant bits):

(1) None of the modules are expanded (That is, screenshot the updated and properly zoomed schematics directly after clicking on RTL Analysis -> Schematics). Furthermore, **a minimum of two n-bit parallel adder modules** (Based on your second rightmost numerical digit of your student matriculation number) **must be seen without any modules in the schematics being expanded.**

(2) All inputs of the subtractor must be clear, including the numerical values between the square brackets. For example:

(3) All outputs of the subtractor must be clear, including the numerical values between the square brackets. For example:

(4) All inputs to, and outputs from, the n-bit parallel adder modules must be clear, including the numerical values between the square brackets. For example, in a 9-bit subtractor, there are at least two n-bit parallel adders (Based on your second rightmost numerical digit of your student matriculation number) being used:

DOCUMENT UPLOAD REQUIREMENTS:

(1) Your name and matriculation number on the first page of the document.
(2) The screenshot (PrintScreen) of the simulation waveform pattern from the Vivado simulation window on the first page of the document.
(3) The screenshot (PrintScreen) of the RTL analysis schematic from Vivado on the second page of the document.

Print the two pages landscape document as a **single PDF** for LumiNUS upload. The PDF file **must follow the naming template** indicated in the LumiNUS submission instruction at the end of this lab manual.

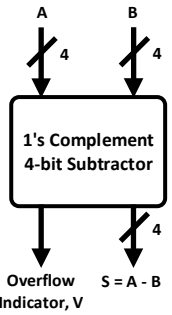
EXAMPLE OF OUTPUTS FOR A 4-BIT PARALLEL SUBTRACTOR

Assume that the two inputs to the subtractor are A and B. The output from the subtractor is sum S and overflow indicator V. In this example, we assume all the inputs and output S are 4 bits.

Since $A - B = A + (-B)$, by adding A to $-B$, the answer to $A - B$ can be obtained. The bits for A,B and S are either in 1's complement, or 2's complement, depending on your matriculation number as set out in the requirement table earlier.

Examples on the expected output S and V, for some input values of A and B

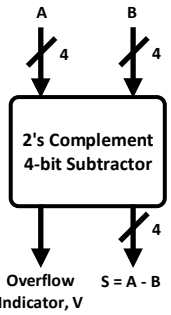
One's Complement



A	B	S	V
0101 (+5)	0001 (+1)	0100 (+4)	0
0101 (+5)	1110 (−1)	0110 (+6)	0
1110 (−1)	0101 (+5)	1001 (−6)	0
1110 (−1)	1010 (−5)	0100 (+4)	0

The overflow, V, is 0 here because the result S can correctly be represented in 1's complement in the 4-bit system

Two's Complement



A	B	S	V
0101 (+5)	0001 (+1)	0100 (+4)	0
0101 (+5)	1111 (−1)	0110 (+6)	0
1111 (−1)	0101 (+5)	1010 (−6)	0
1111 (−1)	1011 (−5)	0100 (+4)	0

The overflow, V, is 0 here because the result S can correctly be represented in 2's complement in the 4-bit system

FURTHER REQUIREMENTS AND RESTRICTIONS: OPERATORS, SWITCHES AND LEDS

- **It is compulsory to use the following switches to represent inputs A and B of the n-bit parallel subtractor:**
  - The input A must use consecutive switches on the Basys 3 Development board, with the **least significant bit A[0] linked to SW0**. Similarly, A[1] should be linked to SW1, A[2] to SW2, and so on.
  - The input B must use consecutive switches on the Basys 3 Development board, with the **least significant bit B[0] linked to SW8**. Similarly, B[1] should be linked to SW9, B[2] to SW10, and so on.
  - **Switches not used by A or B must NOT be used or linked to any other signals under any circumstances.** For example, in a 4-bit parallel subtractor, SW4 to SW7, and SW12 and SW15, should not be linked to any signals, nor used in any circumstances.
- **It is compulsory to use the following LEDs to represent output S of the n-bit parallel subtractor:**
  - The output S must use consecutive LEDs on the Basys 3 development board, with the **least significant bit S[0] linked to LD0**. Similarly, S[1] should be linked to LD1, S[2] should be linked to LD2, and so on.
  - **LD15 must be used for the overflow indicator V**
  - **LEDs not used by S must NOT be used or linked to any other signals under any circumstances.** For example, in a 4-bit parallel subtractor, LD4 to LD14, should not be linked to any signals, nor used in any circumstances.
- The addition and subtraction operators (**+**, **−**) are **not allowed** within the code.

HINT:

Review EE2026 Tutorial 2 and complete the MUX task before attempting this assignment

LUMINUS SUBMISSION INSTRUCTIONS

- Complete as much required functionalities as possible within the given deadline, and ensure that your bitstream has been successfully generated and tested on your Basys 3 development board **BEFORE** archiving your Vivado workspace for LumiNUS upload. No working bitstream is equivalent to no marks (It is best to have some working functionalities / requirements, instead of not having any bitstream at all while trying all requirements)

- It is compulsory to archive your project in a compressed form without any simulation waveforms. In the uploaded archive, the codes (.v files) are important, not the waveforms (.wdb files). **The archive size should not exceed 2 MB in size for lab 2.** Follow the instructions given in the pdf: "Archive Project in Vivado 2018.02"

- **After** following the instructions in "**Archive Project in Vivado 2018.02**", rename your project archive as indicated in the appendix of this lab manual.

- Separately from the project archive, **the single PDF document** (Simulation waveform + RTL analysis schematic of the subtractor) is to be named as indicated in the appendix of this lab manual.

- Upload to LumiNUS EE2026 -> Files -> Lab and Project - Materials and Submissions -> Lab 2 Submission

- Download your LumiNUS archive after uploading. **Unzip the project folder within, open the program, and check if you can run your bitstream correctly**. No project files and no working bitstream is equivalent to losing all marks

- The LumiNUS upload must be completed by **Monday 15th February 2021, 12:00 P.M. (Noon).** Do not plan to upload during the grace period of 2 hours

- A penalty of 25% applies for late submissions of up to 1 week.

- The late submission folder closes 1 week after the original deadline. **Late submissions are not accepted and not graded if a submission is found within the on-time folder, or if grading has already started on an earlier submitted file**. The late submission folder will be located at: LumiNUS EE2026 -> Files -> Lab and Project - Materials and Submissions -> Lab 2 Submission (Late Submission)

Plagiarism is penalised with a 100% penalty for all SOURCES and RECIPIENTS

All past and future submissions, and marks, will be reviewed in greater detail, for any person found to have plagiarised

ALL THE SUBMISSION INSTRUCTIONS LISTED ABOVE WILL AFFECT YOUR GRADES!

GRADING PROCESS

- During subsequent lab sessions, our graders will be providing you updates on the grading of your submission

- Submissions not following all the ***LUMINUS SUBMISSION INSTRUCTIONS*** (listed above) will not be graded immediately, and will instead be reviewed towards the end of the semester. **You will not be able to see your results during the labs in such situations**

APPENDIX (COMPULSORY renaming before just LumiNUS upload):

It is **compulsory to rename your project archive and PDF report**, just before the LumiNUS upload, as listed in the table below. Do not change any other part of the naming. Simply **copy** the naming from the table below, and **paste** it while renaming your project archive and report. Penalties will be incurred if your submission cannot be found according to the exact naming template below.

Archive Naming	Report Naming
L2_Tue_PM_Aaron Chan Siang Joo_426_Archive	L2_Tue_PM_Aaron Chan Siang Joo_426_Report
L2_Tue_AM_Aditi Chadha_898_Archive	L2_Tue_AM_Aditi Chadha_898_Report
L2_Tue_PM_Aiden Thaw Aung Kham Th_186_Archive	L2_Tue_PM_Aiden Thaw Aung Kham Th_186_Report
L2_Tue_AM_Alvin Lim Jun_284_Archive	L2_Tue_AM_Alvin Lim Jun_284_Report
L2_Mon_PM_Alvin Pang Zi Xiong_475_Archive	L2_Mon_PM_Alvin Pang Zi Xiong_475_Report
L2_Tue_PM_Ameer Khalid_328_Archive	L2_Tue_PM_Ameer Khalid_328_Report
L2_Tue_PM_Anderson Leong Ke Sheng_152_Archive	L2_Tue_PM_Anderson Leong Ke Sheng_152_Report
L2_Tue_PM_Andy Chua Xun Ze_384_Archive	L2_Tue_PM_Andy Chua Xun Ze_384_Report
L2_Tue_PM_ANG JIA JUN DARYL_485_Archive	L2_Tue_PM_ANG JIA JUN DARYL_485_Report
L2_Mon_PM_Ang Qi Xuan_052_Archive	L2_Mon_PM_Ang Qi Xuan_052_Report
L2_Tue_AM_Ang Yong Siang Alwin_771_Archive	L2_Tue_AM_Ang Yong Siang Alwin_771_Report
L2_Tue_PM_Anna Zhang Runyu_999_Archive	L2_Tue_PM_Anna Zhang Runyu_999_Report
L2_Tue_AM_Antriksh Verma_149_Archive	L2_Tue_AM_Antriksh Verma_149_Report
L2_Tue_AM_Anvitha Rajaram_434_Archive	L2_Tue_AM_Anvitha Rajaram_434_Report
L2_Tue_PM_Ariel Ong Xing Er_560_Archive	L2_Tue_PM_Ariel Ong Xing Er_560_Report
L2_Tue_AM_Bellakka Krishnamurthy Pr_862_Archive	L2_Tue_AM_Bellakka Krishnamurthy Pr_862_Report
L2_Tue_AM_Boo Qian Wei Adeline_207_Archive	L2_Tue_AM_Boo Qian Wei Adeline_207_Report
L2_Tue_AM_Braden Teo Wei Ren_238_Archive	L2_Tue_AM_Braden Teo Wei Ren_238_Report
L2_Tue_AM_Brendan Lau Siew Zhi_596_Archive	L2_Tue_AM_Brendan Lau Siew Zhi_596_Report
L2_Tue_AM_Bryan Elmer Mulijono_447_Archive	L2_Tue_AM_Bryan Elmer Mulijono_447_Report
L2_Tue_AM_Bryan Wong Hong Liang_051_Archive	L2_Tue_AM_Bryan Wong Hong Liang_051_Report
L2_Tue_PM_Bui Quang Huy_362_Archive	L2_Tue_PM_Bui Quang Huy_362_Report
L2_Tue_AM_Chai Zong Lun_784_Archive	L2_Tue_AM_Chai Zong Lun_784_Report
L2_Tue_AM_Chan Keng Jit_501_Archive	L2_Tue_AM_Chan Keng Jit_501_Report
L2_Tue_PM_Chan Yew Kun_985_Archive	L2_Tue_PM_Chan Yew Kun_985_Report
L2_Thu_PM_Chan Zhao Yong_518_Archive	L2_Thu_PM_Chan Zhao Yong_518_Report
L2_Tue_PM_Chan Zhi Jie Ryan_415_Archive	L2_Tue_PM_Chan Zhi Jie Ryan_415_Report
L2_Tue_PM_Chen Hsin_602_Archive	L2_Tue_PM_Chen Hsin_602_Report
L2_Tue_AM_CHEN SILIN_445_Archive	L2_Tue_AM_CHEN SILIN_445_Report
L2_Tue_PM_CHEN YUHAN_520_Archive	L2_Tue_PM_CHEN YUHAN_520_Report
L2_Tue_AM_Cheng Siyuan_728_Archive	L2_Tue_AM_Cheng Siyuan_728_Report
L2_Tue_AM_Chew Yi Jie_632_Archive	L2_Tue_AM_Chew Yi Jie_632_Report
L2_Wed_PM_Chia Shao Xian_447_Archive	L2_Wed_PM_Chia Shao Xian_447_Report
L2_Tue_PM_Chong Jia An_190_Archive	L2_Tue_PM_Chong Jia An_190_Report
L2_Thu_AM_Chong Xuan Liang_171_Archive	L2_Thu_AM_Chong Xuan Liang_171_Report
L2_Thu_AM_Christopher Nge Jing Qi_145_Archive	L2_Thu_AM_Christopher Nge Jing Qi_145_Report
L2_Thu_AM_Christopher TzeWen Langt_265_Archive	L2_Thu_AM_Christopher TzeWen Langt_265_Report
L2_Tue_PM_CHUA WAN NING_189_Archive	L2_Tue_PM_CHUA WAN NING_189_Report
L2_Thu_AM_Chua Xiong Wei_484_Archive	L2_Thu_AM_Chua Xiong Wei_484_Report
L2_Wed_PM_Chun Min Gyu_249_Archive	L2_Wed_PM_Chun Min Gyu_249_Report
L2_Tue_PM_Chung Ying Qiao Winnie_324_Archive	L2_Tue_PM_Chung Ying Qiao Winnie_324_Report
L2_Thu_AM_Conrad Ephraim Wee Cher J_123_Archive	L2_Thu_AM_Conrad Ephraim Wee Cher J_123_Report
L2_Tue_PM_Cordell Chan Yi Hng_253_Archive	L2_Tue_PM_Cordell Chan Yi Hng_253_Report
L2_Thu_AM_CUI MINJING_441_Archive	L2_Thu_AM_CUI MINJING_441_Report
L2_Tue_PM_Cui Xinyu_116_Archive	L2_Tue_PM_Cui Xinyu_116_Report
L2_Thu_AM_Damien Lim Yu Hao_933_Archive	L2_Thu_AM_Damien Lim Yu Hao_933_Report
L2_Thu_AM_Darren Khoo Kah Weng_516_Archive	L2_Thu_AM_Darren Khoo Kah Weng_516_Report
L2_Tue_PM_Darryl See_317_Archive	L2_Tue_PM_Darryl See_317_Report
L2_Wed_PM_Desmond Eng Kian Wee_095_Archive	L2_Wed_PM_Desmond Eng Kian Wee_095_Report
L2_Tue_PM_Donovan Sim Jing Yi_402_Archive	L2_Tue_PM_Donovan Sim Jing Yi_402_Report
L2_Tue_PM_Du Yantang_744_Archive	L2_Tue_PM_Du Yantang_744_Report
L2_Thu_AM_Edly Irsyad B Elham_555_Archive	L2_Thu_AM_Edly Irsyad B Elham_555_Report
L2_Thu_AM_Elumalai Oviya Dharshini_353_Archive	L2_Thu_AM_Elumalai Oviya Dharshini_353_Report
L2_Thu_AM_Eric Bryan_789_Archive	L2_Thu_AM_Eric Bryan_789_Report
L2_Thu_AM_Eugene Chong Zhi Liang_525_Archive	L2_Thu_AM_Eugene Chong Zhi Liang_525_Report
L2_Thu_AM_Fan Shixi_848_Archive	L2_Thu_AM_Fan Shixi_848_Report
L2_Thu_AM_FOONG XIN YU_018_Archive	L2_Thu_AM_FOONG XIN YU_018_Report
L2_Tue_PM_Fu Zhehui_218_Archive	L2_Tue_PM_Fu Zhehui_218_Report
L2_Thu_AM_Gavien Pat Wei Zhuo_185_Archive	L2_Thu_AM_Gavien Pat Wei Zhuo_185_Report
L2_Tue_AM_GOH KAI YAO BRYAN_690_Archive	L2_Tue_AM_GOH KAI YAO BRYAN_690_Report
L2_Tue_PM_Goh Shao Quan_422_Archive	L2_Tue_PM_Goh Shao Quan_422_Report
L2_Tue_PM_GOH SHAU HUI GEORGE_353_Archive	L2_Tue_PM_GOH SHAU HUI GEORGE_353_Report
L2_Tue_PM_Goh Wei Yang_254_Archive	L2_Tue_PM_Goh Wei Yang_254_Report

L2_Tue_PM_Gu Jianqiang_514_Archive	L2_Tue_PM_Gu Jianqiang_514_Report
L2_Tue_PM_Guan Dinghe_736_Archive	L2_Tue_PM_Guan Dinghe_736_Report
L2_Wed_PM_Han Si Yuan_050_Archive	L2_Wed_PM_Han Si Yuan_050_Report
L2_Tue_PM_Hemanth Bangalore Sriniva_135_Archive	L2_Tue_PM_Hemanth Bangalore Sriniva_135_Report
L2_Tue_PM_Ho Shu Jun_198_Archive	L2_Tue_PM_Ho Shu Jun_198_Report
L2_Thu_AM_Ho Zhen Hong_014_Archive	L2_Thu_AM_Ho Zhen Hong_014_Report
L2_Thu_AM_Hoang Trong Tan_425_Archive	L2_Thu_AM_Hoang Trong Tan_425_Report
L2_Thu_AM_HOE JUN LEONG_182_Archive	L2_Thu_AM_HOE JUN LEONG_182_Report
L2_Tue_PM_Hong Xingwen_861_Archive	L2_Tue_PM_Hong Xingwen_861_Report
L2_Thu_AM_Hossan Goh Xuan Rong_833_Archive	L2_Thu_AM_Hossan Goh Xuan Rong_833_Report
L2_Tue_PM_How Teck Wei_391_Archive	L2_Tue_PM_How Teck Wei_391_Report
L2_Thu_AM_HU JIALUN_521_Archive	L2_Thu_AM_HU JIALUN_521_Report
L2_Thu_AM_Hu Xuefei_885_Archive	L2_Thu_AM_Hu Xuefei_885_Report
L2_Thu_AM_Huang Che Yen_597_Archive	L2_Thu_AM_Huang Che Yen_597_Report
L2_Mon_PM_HUANG HAOFENG_936_Archive	L2_Mon_PM_HUANG HAOFENG_936_Report
L2_Tue_PM_Huang Shanshan_622_Archive	L2_Tue_PM_Huang Shanshan_622_Report
L2_Tue_PM_HUANG YUJING_485_Archive	L2_Tue_PM_HUANG YUJING_485_Report
L2_Thu_AM_Ian Wang Ee En_227_Archive	L2_Thu_AM_Ian Wang Ee En_227_Report
L2_Tue_PM_Imperial Edward Justin Ja_356_Archive	L2_Tue_PM_Imperial Edward Justin Ja_356_Report
L2_Thu_AM_Ishaan Maunil Vyas_479_Archive	L2_Thu_AM_Ishaan Maunil Vyas_479_Report
L2_Thu_AM_Izdiyad Farhan B Zuri_407_Archive	L2_Thu_AM_Izdiyad Farhan B Zuri_407_Report
L2_Mon_PM_Jared Cheang_192_Archive	L2_Mon_PM_Jared Cheang_192_Report
L2_Tue_PM_Jareth Tan Eu Quan_240_Archive	L2_Tue_PM_Jareth Tan Eu Quan_240_Report
L2_Tue_PM_Jason Ong Meng Lee_174_Archive	L2_Tue_PM_Jason Ong Meng Lee_174_Report
L2_Tue_PM_Jasshan Kumeresh_503_Archive	L2_Tue_PM_Jasshan Kumeresh_503_Report
L2_Tue_PM_Jeremiah Jiang_139_Archive	L2_Tue_PM_Jeremiah Jiang_139_Report
L2_Tue_PM_Jeremiah Ong Ray_551_Archive	L2_Tue_PM_Jeremiah Ong Ray_551_Report
L2_Tue_PM_Jeremy Goh Liang Yi_393_Archive	L2_Tue_PM_Jeremy Goh Liang Yi_393_Report
L2_Mon_PM_JIANG QIXIONG_698_Archive	L2_Mon_PM_JIANG QIXIONG_698_Report
L2_Thu_AM_Jiang Xing Kai_564_Archive	L2_Thu_AM_Jiang Xing Kai_564_Report
L2_Tue_AM_Jin Minyue_069_Archive	L2_Tue_AM_Jin Minyue_069_Report
L2_Wed_PM_JIN YIXUAN_976_Archive	L2_Wed_PM_JIN YIXUAN_976_Report
L2_Thu_AM_Joanne Wong Wei Yin_527_Archive	L2_Thu_AM_Joanne Wong Wei Yin_527_Report
L2_Thu_AM_Joel Matthew Chiam Zhi Qi_250_Archive	L2_Thu_AM_Joel Matthew Chiam Zhi Qi_250_Report
L2_Thu_AM_Jon Lim Yong Kiat_782_Archive	L2_Thu_AM_Jon Lim Yong Kiat_782_Report
L2_Thu_AM_Jonathan Mui Koy Kit_534_Archive	L2_Thu_AM_Jonathan Mui Koy Kit_534_Report
L2_Thu_AM_Joshua Harsha Dass_714_Archive	L2_Thu_AM_Joshua Harsha Dass_714_Report
L2_Thu_AM_Justin Fidelis Wong Jun W_326_Archive	L2_Thu_AM_Justin Fidelis Wong Jun W_326_Report
L2_Thu_AM_Kairos Koh Jia Jun_149_Archive	L2_Thu_AM_Kairos Koh Jia Jun_149_Report
L2_Thu_AM_Keh Wen Yang Rachel_249_Archive	L2_Thu_AM_Keh Wen Yang Rachel_249_Report
L2_Thu_PM_Kevinaldi Dwiastajulio Hu_912_Archive	L2_Thu_PM_Kevinaldi Dwiastajulio Hu_912_Report
L2_Thu_AM_Khoo Jia Le Isaac_733_Archive	L2_Thu_AM_Khoo Jia Le Isaac_733_Report
L2_Thu_PM_Khor Sheng Hou_443_Archive	L2_Thu_PM_Khor Sheng Hou_443_Report
L2_Thu_AM_Kishor Kumar Haribaskar_481_Archive	L2_Thu_AM_Kishor Kumar Haribaskar_481_Report
L2_Tue_AM_Koh Meng Kiat Kenneth_512_Archive	L2_Tue_AM_Koh Meng Kiat Kenneth_512_Report
L2_Thu_AM_Koh Qianqi_746_Archive	L2_Thu_AM_Koh Qianqi_746_Report
L2_Thu_PM_Koh Qin Ruo_055_Archive	L2_Thu_PM_Koh Qin Ruo_055_Report
L2_Thu_PM_Koh Ruizhe Jerome_429_Archive	L2_Thu_PM_Koh Ruizhe Jerome_429_Report
L2_Thu_AM_Kom Xing Yuan_993_Archive	L2_Thu_AM_Kom Xing Yuan_993_Report
L2_Thu_AM_Kong Dak Nam_171_Archive	L2_Thu_AM_Kong Dak Nam_171_Report
L2_Tue_PM_Koo Wei De_133_Archive	L2_Tue_PM_Koo Wei De_133_Report
L2_Thu_PM_Krishna R R_900_Archive	L2_Thu_PM_Krishna R R_900_Report
L2_Thu_AM_Kum Wing Ho_725_Archive	L2_Thu_AM_Kum Wing Ho_725_Report
L2_Thu_AM_Kumaravel Vignesh_585_Archive	L2_Thu_AM_Kumaravel Vignesh_585_Report
L2_Thu_AM_Kwok Xiu Sheng Theodore_118_Archive	L2_Thu_AM_Kwok Xiu Sheng Theodore_118_Report
L2_Thu_AM_Kwong Zhi Qian_569_Archive	L2_Thu_AM_Kwong Zhi Qian_569_Report
L2_Thu_AM_Lam Junyu William_903_Archive	L2_Thu_AM_Lam Junyu William_903_Report
L2_Thu_AM_LAM KAI WEN JONATHAN_213_Archive	L2_Thu_AM_LAM KAI WEN JONATHAN_213_Report
L2_Thu_PM_Lau Miang Puang Glennard_207_Archive	L2_Thu_PM_Lau Miang Puang Glennard_207_Report
L2_Tue_AM_Lee An Sheng_263_Archive	L2_Tue_AM_Lee An Sheng_263_Report
L2_Tue_AM_Lee Cheok Feng_743_Archive	L2_Tue_AM_Lee Cheok Feng_743_Report
L2_Thu_PM_Lee Hung Tien_965_Archive	L2_Thu_PM_Lee Hung Tien_965_Report
L2_Thu_PM_Lee Jia Jun_423_Archive	L2_Thu_PM_Lee Jia Jun_423_Report
L2_Thu_PM_Lee Jing Rui Evan_399_Archive	L2_Thu_PM_Lee Jing Rui Evan_399_Report
L2_Wed_PM_Lee Jun Wen_466_Archive	L2_Wed_PM_Lee Jun Wen_466_Report
L2_Tue_AM_LEE KENG YONG JOSHUA_644_Archive	L2_Tue_AM_LEE KENG YONG JOSHUA_644_Report
L2_Tue_AM_Lee Qi An_644_Archive	L2_Tue_AM_Lee Qi An_644_Report
L2_Thu_PM_Lee ShiAn Matthew_324_Archive	L2_Thu_PM_Lee ShiAn Matthew_324_Report
L2_Tue_AM_Lee Sungmin_490_Archive	L2_Tue_AM_Lee Sungmin_490_Report
L2_Tue_PM_Lee Sze Ern Jeremy_510_Archive	L2_Tue_PM_Lee Sze Ern Jeremy_510_Report
L2_Tue_AM_Lee Yi Kai_550_Archive	L2_Tue_AM_Lee Yi Kai_550_Report
L2_Thu_PM_Lee YuHsueh_639_Archive	L2_Thu_PM_Lee YuHsueh_639_Report

L2_Tue_PM_LEONARD CHUA ZHONG QI_873_Archive	L2_Tue_PM_LEONARD CHUA ZHONG QI_873_Report
L2_Thu_PM_Leong Kah Choong_455_Archive	L2_Thu_PM_Leong Kah Choong_455_Report
L2_Tue_AM_Leow Yuan Yang_574_Archive	L2_Tue_AM_Leow Yuan Yang_574_Report
L2_Thu_PM_Leroy Ong Nai Kiat_506_Archive	L2_Thu_PM_Leroy Ong Nai Kiat_506_Report
L2_Thu_PM_Li Huanda_101_Archive	L2_Thu_PM_Li Huanda_101_Report
L2_Tue_AM_Li Xi Yuan_926_Archive	L2_Tue_AM_Li Xi Yuan_926_Report
L2_Tue_AM_Liang Yuzhao_802_Archive	L2_Tue_AM_Liang Yuzhao_802_Report
L2_Wed_PM_LIM BING SEN_580_Archive	L2_Wed_PM_LIM BING SEN_580_Report
L2_Thu_AM_LIM CHANG QUAN THADDEUS_210_Archive	L2_Thu_AM_LIM CHANG QUAN THADDEUS_210_Report
L2_Thu_PM_Lim Jia Sheng Jackson_596_Archive	L2_Thu_PM_Lim Jia Sheng Jackson_596_Report
L2_Tue_AM_Lim Kay Yun_244_Archive	L2_Tue_AM_Lim Kay Yun_244_Report
L2_Tue_AM_Lim Shyun Yin_063_Archive	L2_Tue_AM_Lim Shyun Yin_063_Report
L2_Thu_PM_Lim Wen Jie_382_Archive	L2_Thu_PM_Lim Wen Jie_382_Report
L2_Thu_PM_Liu Danfeng_777_Archive	L2_Thu_PM_Liu Danfeng_777_Report
L2_Thu_PM_Liu Ruijun_371_Archive	L2_Thu_PM_Liu Ruijun_371_Report
L2_Tue_AM_LIU ZEHANG_491_Archive	L2_Tue_AM_LIU ZEHANG_491_Report
L2_Wed_PM_LIU ZHIYANG_653_Archive	L2_Wed_PM_LIU ZHIYANG_653_Report
L2_Thu_PM_Loo Keng Leong_408_Archive	L2_Thu_PM_Loo Keng Leong_408_Report
L2_Tue_AM_LOW ZHEN WEI JERRELL_516_Archive	L2_Tue_AM_LOW ZHEN WEI JERRELL_516_Report
L2_Thu_PM_Lu Jingguang_319_Archive	L2_Thu_PM_Lu Jingguang_319_Report
L2_Tue_AM_Lu Sicheng_634_Archive	L2_Tue_AM_Lu Sicheng_634_Report
L2_Tue_PM_LU ZONGHAN_452_Archive	L2_Tue_PM_LU ZONGHAN_452_Report
L2_Tue_PM_MA XUDONG_493_Archive	L2_Tue_PM_MA XUDONG_493_Report
L2_Tue_AM_Ma Zijian_828_Archive	L2_Tue_AM_Ma Zijian_828_Report
L2_Tue_AM_Madhan Selvapandian_482_Archive	L2_Tue_AM_Madhan Selvapandian_482_Report
L2_Thu_PM_Madheswaran Niveytha_465_Archive	L2_Thu_PM_Madheswaran Niveytha_465_Report
L2_Tue_AM_Mah Yuan Jie Alvin_500_Archive	L2_Tue_AM_Mah Yuan Jie Alvin_500_Report
L2_Tue_AM_Mahadevan Svetha_108_Archive	L2_Tue_AM_Mahadevan Svetha_108_Report
L2_Tue_AM_Mahadevan Swati_107_Archive	L2_Tue_AM_Mahadevan Swati_107_Report
L2_Thu_PM_Marcus Goh Xuan De_355_Archive	L2_Thu_PM_Marcus Goh Xuan De_355_Report
L2_Thu_PM_Marcus Lim Sheng Jie_408_Archive	L2_Thu_PM_Marcus Lim Sheng Jie_408_Report
L2_Tue_AM_Marcus Ong Yih_404_Archive	L2_Tue_AM_Marcus Ong Yih_404_Report
L2_Tue_AM_Mathur Aayush_581_Archive	L2_Tue_AM_Mathur Aayush_581_Report
L2_Tue_AM_Mayank Panjiyara_763_Archive	L2_Tue_AM_Mayank Panjiyara_763_Report
L2_Thu_PM_Mehedi Hasan Salim_436_Archive	L2_Thu_PM_Mehedi Hasan Salim_436_Report
L2_Thu_PM_Mohamed Faez Bin Shahlan_297_Archive	L2_Thu_PM_Mohamed Faez Bin Shahlan_297_Report
L2_Tue_AM_Mohammad Shoib Memon Loya_487_Archive	L2_Tue_AM_Mohammad Shoib Memon Loya_487_Report
L2_Thu_PM_Muhammad Aizat Bin Rahim_437_Archive	L2_Thu_PM_Muhammad Aizat Bin Rahim_437_Report
L2_Tue_AM_Muhammad Ashraf B Mohamad_432_Archive	L2_Tue_AM_Muhammad Ashraf B Mohamad_432_Report
L2_Thu_PM_MUHAMMAD HAZIM BIN ABDULL_633_Archive	L2_Thu_PM_MUHAMMAD HAZIM BIN ABDULL_633_Report
L2_Wed_PM_Muhammad Jaish Bin Jamalu_287_Archive	L2_Wed_PM_Muhammad Jaish Bin Jamalu_287_Report
L2_Tue_AM_Mun Le Zong_172_Archive	L2_Tue_AM_Mun Le Zong_172_Report
L2_Thu_PM_Nan Song_102_Archive	L2_Thu_PM_Nan Song_102_Report
L2_Tue_AM_Ng Andre_973_Archive	L2_Tue_AM_Ng Andre_973_Report
L2_Tue_AM_Ng Cheng Yang Titus_478_Archive	L2_Tue_AM_Ng Cheng Yang Titus_478_Report
L2_Thu_PM_Ng Jin Loong Jeremy_395_Archive	L2_Thu_PM_Ng Jin Loong Jeremy_395_Report
L2_Thu_PM_Ng Qi Hao_420_Archive	L2_Thu_PM_Ng Qi Hao_420_Report
L2_Thu_PM_Ng Xinyi_545_Archive	L2_Thu_PM_Ng Xinyi_545_Report
L2_Tue_AM_Ngoi Hui Wen Vanessa_471_Archive	L2_Tue_AM_Ngoi Hui Wen Vanessa_471_Report
L2_Tue_AM_Nguyen Minh Tuan_389_Archive	L2_Tue_AM_Nguyen Minh Tuan_389_Report
L2_Mon_PM_Nguyen Van Binh_453_Archive	L2_Mon_PM_Nguyen Van Binh_453_Report
L2_Thu_PM_Nigel Loh Weien_416_Archive	L2_Thu_PM_Nigel Loh Weien_416_Report
L2_Mon_PM_Nigel Ng_444_Archive	L2_Mon_PM_Nigel Ng_444_Report
L2_Mon_PM_Nishant Rai_182_Archive	L2_Mon_PM_Nishant Rai_182_Report
L2_Thu_PM_Oh Qi Ren_441_Archive	L2_Thu_PM_Oh Qi Ren_441_Report
L2_Tue_PM_Ong Chor Yew_460_Archive	L2_Tue_PM_Ong Chor Yew_460_Report
L2_Thu_PM_Ong Jun Giat_205_Archive	L2_Thu_PM_Ong Jun Giat_205_Report
L2_Thu_AM_Ong Siying Falicia_566_Archive	L2_Thu_AM_Ong Siying Falicia_566_Report
L2_Thu_PM_Ong Yew Yong Adrian_401_Archive	L2_Thu_PM_Ong Yew Yong Adrian_401_Report
L2_Thu_PM_Owng Kai Leng Sally_331_Archive	L2_Thu_PM_Owng Kai Leng Sally_331_Report
L2_Thu_PM_Pang Kai Lin_036_Archive	L2_Thu_PM_Pang Kai Lin_036_Report
L2_Thu_PM_Pang Kai Yi_236_Archive	L2_Thu_PM_Pang Kai Yi_236_Report
L2_Wed_PM_Pang Qi Wei Jenna_685_Archive	L2_Wed_PM_Pang Qi Wei Jenna_685_Report
L2_Mon_PM_Paramita Tejasvi_194_Archive	L2_Mon_PM_Paramita Tejasvi_194_Report
L2_Thu_PM_Peh Li Yan_267_Archive	L2_Thu_PM_Peh Li Yan_267_Report
L2_Mon_PM_PENG FEI_518_Archive	L2_Mon_PM_PENG FEI_518_Report
L2_Tue_AM_Peng Yanjia_877_Archive	L2_Tue_AM_Peng Yanjia_877_Report
L2_Thu_PM_Phoon Pei Zhen_744_Archive	L2_Thu_PM_Phoon Pei Zhen_744_Report
L2_Thu_PM_Phua Keng Wee_706_Archive	L2_Thu_PM_Phua Keng Wee_706_Report
L2_Thu_PM_Phuah Yong Chen Keith_360_Archive	L2_Thu_PM_Phuah Yong Chen Keith_360_Report
L2_Tue_AM_Pichanon Rattanadilok Na _545_Archive	L2_Tue_AM_Pichanon Rattanadilok Na _545_Report
L2_Wed_PM_Pojcharapol Leenukiat_642_Archive	L2_Wed_PM_Pojcharapol Leenukiat_642_Report

L2_Wed_PM_Poon Jeun Lek_202_Archive	L2_Wed_PM_Poon Jeun Lek_202_Report
L2_Tue_AM_Pow Zhi Xiang_942_Archive	L2_Tue_AM_Pow Zhi Xiang_942_Report
L2_Wed_PM_Pradhan Rachit Manish_230_Archive	L2_Wed_PM_Pradhan Rachit Manish_230_Report
L2_Tue_AM_Pranav Venkatram_200_Archive	L2_Tue_AM_Pranav Venkatram_200_Report
L2_Wed_PM_Qi Tian Cong_442_Archive	L2_Wed_PM_Qi Tian Cong_442_Report
L2_Tue_AM_Ramalingam Saravanamani_586_Archive	L2_Tue_AM_Ramalingam Saravanamani_586_Report
L2_Tue_AM_Ravindiran Rakesh_010_Archive	L2_Tue_AM_Ravindiran Rakesh_010_Report
L2_Thu_AM_Rebecca Chua_171_Archive	L2_Thu_AM_Rebecca Chua_171_Report
L2_Mon_PM_REN TIANLE_446_Archive	L2_Mon_PM_REN TIANLE_446_Report
L2_Thu_AM_Renzo Rivera Canare_502_Archive	L2_Thu_AM_Renzo Rivera Canare_502_Report
L2_Wed_PM_Reuel Teo Lu Wei_435_Archive	L2_Wed_PM_Reuel Teo Lu Wei_435_Report
L2_Thu_AM_Richard Willie_368_Archive	L2_Thu_AM_Richard Willie_368_Report
L2_Thu_AM_Roycius Lim Yuanwei_060_Archive	L2_Thu_AM_Roycius Lim Yuanwei_060_Report
L2_Tue_PM_Samuel Ong Wei Chuan_462_Archive	L2_Tue_PM_Samuel Ong Wei Chuan_462_Report
L2_Wed_PM_Se Sean_140_Archive	L2_Wed_PM_Se Sean_140_Report
L2_Thu_AM_See Jian Hui_737_Archive	L2_Thu_AM_See Jian Hui_737_Report
L2_Mon_PM_Seet Ting Yang Irvin_608_Archive	L2_Mon_PM_Seet Ting Yang Irvin_608_Report
L2_Mon_PM_Seetoh Yit Ching_154_Archive	L2_Mon_PM_Seetoh Yit Ching_154_Report
L2_Mon_PM_Seo Gimin_442_Archive	L2_Mon_PM_Seo Gimin_442_Report
L2_Wed_PM_Seth Teng Shann_419_Archive	L2_Wed_PM_Seth Teng Shann_419_Report
L2_Mon_PM_Shao Yurui_111_Archive	L2_Mon_PM_Shao Yurui_111_Report
L2_Wed_PM_Shawn Chang_151_Archive	L2_Wed_PM_Shawn Chang_151_Report
L2_Wed_PM_Shreshth Sarda_424_Archive	L2_Wed_PM_Shreshth Sarda_424_Report
L2_Mon_PM_Shyam Ganesh Jayagopi_484_Archive	L2_Mon_PM_Shyam Ganesh Jayagopi_484_Report
L2_Wed_PM_Sidharth Premnath_502_Archive	L2_Wed_PM_Sidharth Premnath_502_Report
L2_Thu_AM_Siew Yang Zhi_331_Archive	L2_Thu_AM_Siew Yang Zhi_331_Report
L2_Wed_PM_Sim Le Yee Beatrice_769_Archive	L2_Wed_PM_Sim Le Yee Beatrice_769_Report
L2_Thu_PM_Sin Ren Xiang_865_Archive	L2_Thu_PM_Sin Ren Xiang_865_Report
L2_Wed_PM_Sivakumar Yogarajan_505_Archive	L2_Wed_PM_Sivakumar Yogarajan_505_Report
L2_Wed_PM_Song Chenan_797_Archive	L2_Wed_PM_Song Chenan_797_Report
L2_Wed_PM_Song Min Kyu_226_Archive	L2_Wed_PM_Song Min Kyu_226_Report
L2_Mon_PM_Sridharan Arvind Srinivas_477_Archive	L2_Mon_PM_Sridharan Arvind Srinivas_477_Report
L2_Mon_PM_Sthitipragyan Samal_664_Archive	L2_Mon_PM_Sthitipragyan Samal_664_Report
L2_Mon_PM_Sun Jiale_853_Archive	L2_Mon_PM_Sun Jiale_853_Report
L2_Thu_PM_SUN JIAWEI_496_Archive	L2_Thu_PM_SUN JIAWEI_496_Report
L2_Mon_PM_SWAMINATHAN VARUN_281_Archive	L2_Mon_PM_SWAMINATHAN VARUN_281_Report
L2_Mon_PM_Swann Tet Aung_552_Archive	L2_Mon_PM_Swann Tet Aung_552_Report
L2_Wed_PM_Tan Haoxuan_934_Archive	L2_Wed_PM_Tan Haoxuan_934_Report
L2_Mon_PM_Tan Hui En_373_Archive	L2_Mon_PM_Tan Hui En_373_Report
L2_Mon_PM_Tan Jun Heng Daren Justin_331_Archive	L2_Mon_PM_Tan Jun Heng Daren Justin_331_Report
L2_Mon_PM_Tan Kah Heng_677_Archive	L2_Mon_PM_Tan Kah Heng_677_Report
L2_Mon_PM_Tan Le Yi_071_Archive	L2_Mon_PM_Tan Le Yi_071_Report
L2_Wed_PM_Tan Lindsey_197_Archive	L2_Wed_PM_Tan Lindsey_197_Report
L2_Wed_PM_Tan Qi Xian Keith_397_Archive	L2_Wed_PM_Tan Qi Xian Keith_397_Report
L2_Mon_PM_Tan Rui Yang_472_Archive	L2_Mon_PM_Tan Rui Yang_472_Report
L2_Wed_PM_Tan Tze Yeong_970_Archive	L2_Wed_PM_Tan Tze Yeong_970_Report
L2_Wed_PM_Tan Wei Li_336_Archive	L2_Wed_PM_Tan Wei Li_336_Report
L2_Mon_PM_Tan Xing Jie_747_Archive	L2_Mon_PM_Tan Xing Jie_747_Report
L2_Wed_PM_Tan Yong Zheng_261_Archive	L2_Wed_PM_Tan Yong Zheng_261_Report
L2_Mon_PM_Tang Zehou_210_Archive	L2_Mon_PM_Tang Zehou_210_Report
L2_Mon_PM_Tay Weida_027_Archive	L2_Mon_PM_Tay Weida_027_Report
L2_Mon_PM_Tay Yi Heng Atticus_994_Archive	L2_Mon_PM_Tay Yi Heng Atticus_994_Report
L2_Mon_PM_Teh Jiewen_520_Archive	L2_Mon_PM_Teh Jiewen_520_Report
L2_Wed_PM_Teh ZiChun_328_Archive	L2_Wed_PM_Teh ZiChun_328_Report
L2_Mon_PM_Teng Yi Shiong_647_Archive	L2_Mon_PM_Teng Yi Shiong_647_Report
L2_Mon_PM_Teo Ziyi Ivy_117_Archive	L2_Mon_PM_Teo Ziyi Ivy_117_Report
L2_Wed_PM_Tham Yang Tze Xavier_256_Archive	L2_Wed_PM_Tham Yang Tze Xavier_256_Report
L2_Thu_PM_TIAN ZHENYU_467_Archive	L2_Thu_PM_TIAN ZHENYU_467_Report
L2_Wed_PM_Tiang Zhang Quan Xavier_446_Archive	L2_Wed_PM_Tiang Zhang Quan Xavier_446_Report
L2_Wed_PM_Tie Zhou Peng_264_Archive	L2_Wed_PM_Tie Zhou Peng_264_Report
L2_Wed_PM_Toh Yi Cheng_421_Archive	L2_Wed_PM_Toh Yi Cheng_421_Report
L2_Mon_PM_Toh Yi Zhi_086_Archive	L2_Mon_PM_Toh Yi Zhi_086_Report
L2_Mon_PM_Tran Nhan Duc Anh_358_Archive	L2_Mon_PM_Tran Nhan Duc Anh_358_Report
L2_Wed_PM_Tran Thi Phuong Thao_438_Archive	L2_Wed_PM_Tran Thi Phuong Thao_438_Report
L2_Wed_PM_Varun Agarwal_605_Archive	L2_Wed_PM_Varun Agarwal_605_Report
L2_Mon_PM_VIKAS HARLANI_376_Archive	L2_Mon_PM_VIKAS HARLANI_376_Report
L2_Mon_PM_Vishal Jeyaram_224_Archive	L2_Mon_PM_Vishal Jeyaram_224_Report
L2_Wed_PM_Wan Haocheng_780_Archive	L2_Wed_PM_Wan Haocheng_780_Report
L2_Wed_PM_Wang Wenxuan_649_Archive	L2_Wed_PM_Wang Wenxuan_649_Report
L2_Thu_PM_WANG YUDA_443_Archive	L2_Thu_PM_WANG YUDA_443_Report
L2_Mon_PM_Wang Zhao Yu Edward_953_Archive	L2_Mon_PM_Wang Zhao Yu Edward_953_Report
L2_Mon_PM_Wang Zhihuang_682_Archive	L2_Mon_PM_Wang Zhihuang_682_Report

L2_Wed_PM_Wang Zichen_951_Archive	L2_Wed_PM_Wang Zichen_951_Report
L2_Wed_PM_Wang Zihan_361_Archive	L2_Wed_PM_Wang Zihan_361_Report
L2_Wed_PM_Wang Zixi_445_Archive	L2_Wed_PM_Wang Zixi_445_Report
L2_Mon_PM_William Wahyudi_230_Archive	L2_Mon_PM_William Wahyudi_230_Report
L2_Tue_AM_Wong Jun Lin_077_Archive	L2_Tue_AM_Wong Jun Lin_077_Report
L2_Mon_PM_Wong Tze Shan Samantha_672_Archive	L2_Mon_PM_Wong Tze Shan Samantha_672_Report
L2_Mon_PM_Wong Zi Xin Avellin_073_Archive	L2_Mon_PM_Wong Zi Xin Avellin_073_Report
L2_Mon_PM_Woo Bo Tuan_153_Archive	L2_Mon_PM_Woo Bo Tuan_153_Report
L2_Thu_PM_WU HAO HSUAN_635_Archive	L2_Thu_PM_WU HAO HSUAN_635_Report
L2_Mon_PM_Wu Luoyu_894_Archive	L2_Mon_PM_Wu Luoyu_894_Report
L2_Wed_PM_WU YUWEI_472_Archive	L2_Wed_PM_WU YUWEI_472_Report
L2_Wed_PM_XIAO JUNTIAN_497_Archive	L2_Wed_PM_XIAO JUNTIAN_497_Report
L2_Wed_PM_Xu Yuxing_183_Archive	L2_Wed_PM_Xu Yuxing_183_Report
L2_Wed_PM_Xue Yuxuan_250_Archive	L2_Wed_PM_Xue Yuxuan_250_Report
L2_Mon_PM_Yam Jin Ee Dmitri_974_Archive	L2_Mon_PM_Yam Jin Ee Dmitri_974_Report
L2_Tue_AM_Yang Zikun_313_Archive	L2_Tue_AM_Yang Zikun_313_Report
L2_Mon_PM_Yap Joon Siong_925_Archive	L2_Mon_PM_Yap Joon Siong_925_Report
L2_Mon_PM_YAP WEI XUAN_997_Archive	L2_Mon_PM_YAP WEI XUAN_997_Report
L2_Thu_PM_Yap Zhan Wei_455_Archive	L2_Thu_PM_Yap Zhan Wei_455_Report
L2_Mon_PM_Yeat Nai Jie_613_Archive	L2_Mon_PM_Yeat Nai Jie_613_Report
L2_Wed_PM_Yeo Shi Heng_390_Archive	L2_Wed_PM_Yeo Shi Heng_390_Report
L2_Mon_PM_Yeo Wei Hng_075_Archive	L2_Mon_PM_Yeo Wei Hng_075_Report
L2_Mon_PM_Yeo Zi Hao Edwin_710_Archive	L2_Mon_PM_Yeo Zi Hao Edwin_710_Report
L2_Mon_PM_YIP WAYNE_998_Archive	L2_Mon_PM_YIP WAYNE_998_Report
L2_Wed_PM_YU HAIHONG_470_Archive	L2_Wed_PM_YU HAIHONG_470_Report
L2_Thu_AM_Yue Junfeng_802_Archive	L2_Thu_AM_Yue Junfeng_802_Report
L2_Wed_PM_Yuk Yeon Soo_243_Archive	L2_Wed_PM_Yuk Yeon Soo_243_Report
L2_Mon_PM_Zeng Jiexiong_052_Archive	L2_Mon_PM_Zeng Jiexiong_052_Report
L2_Thu_AM_ZHANG HAOYU_783_Archive	L2_Thu_AM_ZHANG HAOYU_783_Report
L2_Mon_PM_ZHAO LUOYUANG_466_Archive	L2_Mon_PM_ZHAO LUOYUANG_466_Report
L2_Wed_PM_Zhao Yibo_863_Archive	L2_Wed_PM_Zhao Yibo_863_Report
L2_Wed_PM_Zhao Ziqi_275_Archive	L2_Wed_PM_Zhao Ziqi_275_Report
L2_Mon_PM_ZHONG XINGHAN_468_Archive	L2_Mon_PM_ZHONG XINGHAN_468_Report
L2_Mon_PM_ZHOU CHENGXU_492_Archive	L2_Mon_PM_ZHOU CHENGXU_492_Report
L2_Wed_PM_ZHOU YUHAN_530_Archive	L2_Wed_PM_ZHOU YUHAN_530_Report
L2_Wed_PM_Zhu Shaohan Steven_193_Archive	L2_Wed_PM_Zhu Shaohan Steven_193_Report
L2_Mon_PM_Zhuang Jianning_277_Archive	L2_Mon_PM_Zhuang Jianning_277_Report
L2_Tue_PM_Zubin Jain_990_Archive	L2_Tue_PM_Zubin Jain_990_Report