Tutorial 9 Questions (Part 2)

Finite State Machine Design

1. Implement a mod-4 counter with the count sequence 1, 2, 4, 8, 1… as a finite state machine with two D Flip-flops and additional gates.

   (i) Design a mod-4 counter with the count sequence 0, 1, 2, 3, 0… using D flip-flops.
   (ii) Develop the truth table for a combinational circuit that converts 0, 1, 2, 3, 0… to 1, 2, 4, 8, 1….
   (iii) Combine the circuits from (i) and (ii) together.
   (iv) How does this circuit differ from T8Q2?

2. A finite state machine's output **Q** depends on the value of an input signal X in the *current* and *previous clock cycles*, i.e., $\mathbf{X_t}$ and $\mathbf{X_{t-1}}$ as specified below:

$\mathbf{X_t}$	$\mathbf{X_{t-1}}$	$\mathbf{Q^+}$
0	0	$\overline{Q}$
0	1	1
1	0	0
1	1	Q

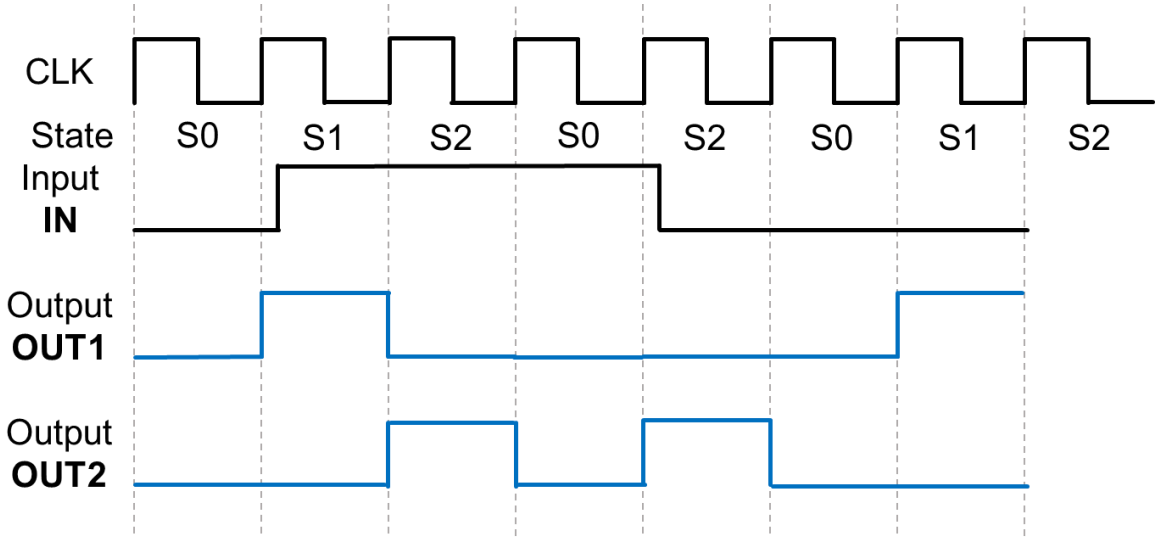
   Design the finite state machine using (a) D flip-flops and (b) J-K flip-flops. Does one design need more components than the other? Why?

Q3. For the finite state machine with the timing diagram shown in the figure below:

(i) Identify the input & output signals of the machine.

(ii) Construct the state transition diagram.

(iii) Based on (ii), fill in the next state table and output logic table below.



Next State Table

Current State	Inputs	Next State
S	**IN**	**S+**
S0	0	S1

Output Logic Table

Current State	Outputs	
S	**OUT1**	**OUT2**
S0	0	0

Q4. Given the state transition diagram of a state machine shown in Figure (a) below,

(i) Identify the input & output signals of the machine.

(ii) Complete the corresponding timing diagram in Figure (b),

(iii) Based on (ii), fill in the next state and output logic table below.

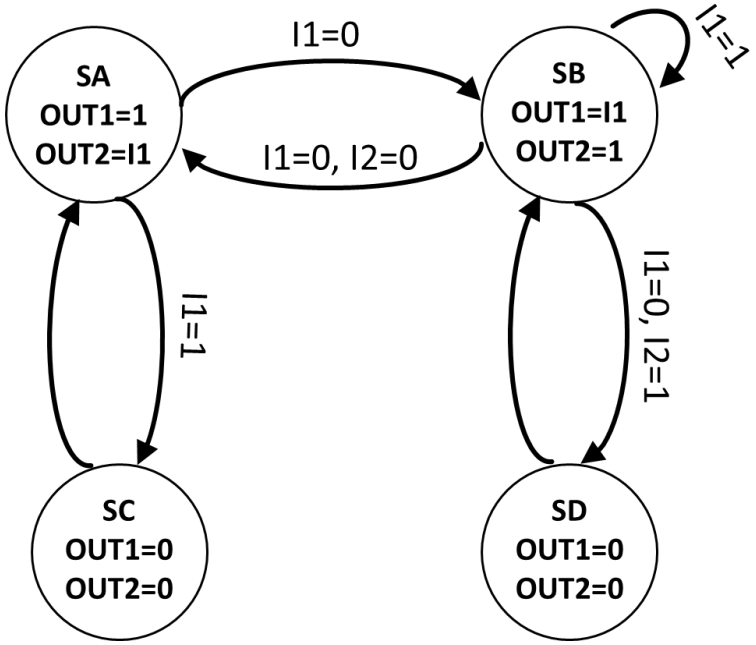


Figure (a)

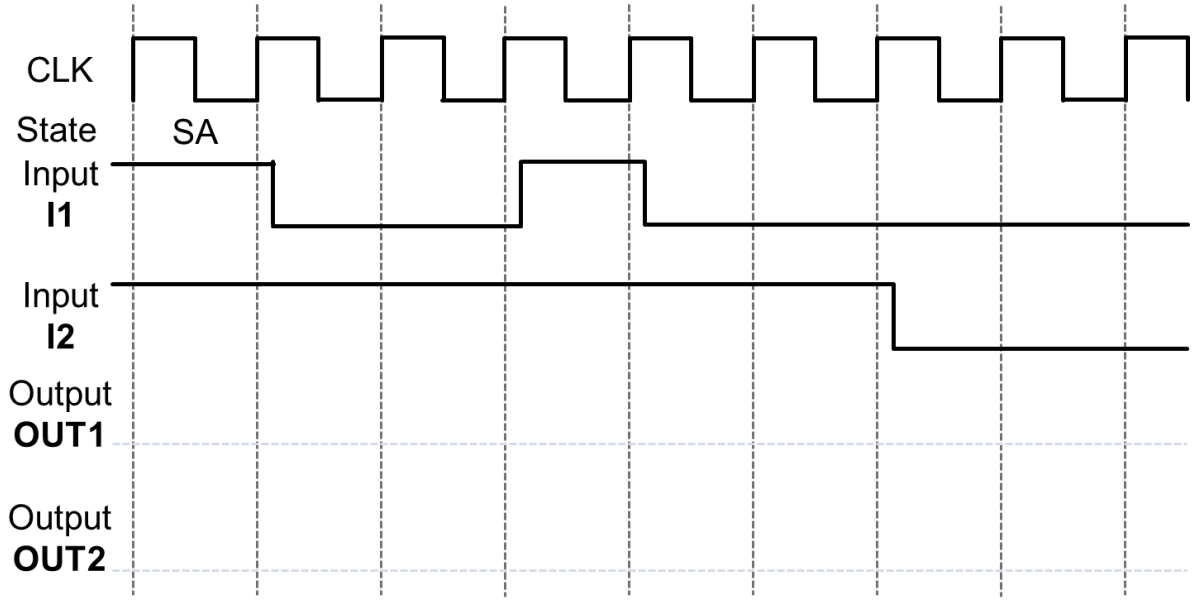


Figure (b)

Next State Table

Current State	Inputs		Next State
S	**I1**	**I2**	**S+**

Output Logic Table

Current State	Outputs	
S	**OUT1**	**OUT2**