Tutorial 7 Questions (Part 2)

Verilog Modeling

Check that the syntax of your programs is correct by using the Xilinx Vivado tool!

1. Data encryption schemes are commonly used to secure data privacy. Write a Verilog program for a *digital decrypter* which has a 5-bit input, DATA_IN of the form "$C_2O_1C_1O_0C_0$" where the operation applied to the three bit data "$C_2C_1C_0$" to produce the 3-bit output DATA_OUT depends on the two bits "O_1O_0"as shown in the table below.

"O_1O_0"	**DATA_OUT**
"00"	"$C_2C_1C_0$"
"01"	"$C_0C_2C_1$"
"10"	"$C_1C_0C_2$"
"11"	"$\overline{C_2}\,\overline{C_1}\,\overline{C_0}$"

2. A machine receives two 3-bit unsigned inputs **X**, **Y** and outputs a 6-bit unsigned output **Z** where **Z** is the product of **X** and **Y**. Write a Verilog program that implements this machine *without* using the multiplication operator.

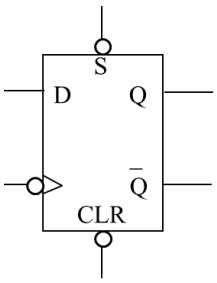
Hint: Use the shift and add method to perform multiplication i.e.

```
      1 0 1
X     0 1 1
-------------
      1 0 1
    1 0 1
  0 0 0
-------------
  0 0 1 1 1 1
```

Note that the addition operation can be performed as follows:
c <= a + b; *where a, b & c are standard logic vectors of the same length.*

3. The 74'74B is an integrated circuit containing negative-edge triggered D flip-flops with synchronous set and asynchronous reset inputs. The D flip-flop receives four 1-bit input signals, **D**, **CLK**, **S**, **CLR** and produces two 1-bit output signals, **Q** and **QB**. Write a Verilog program that implements the D flip-flop according to the characteristic table shown below.

CLK	CLR	S	D	Q^+
X	0	X	X	0
↓	1	0	X	1
↓	1	1	0	0
↓	1	1	1	1

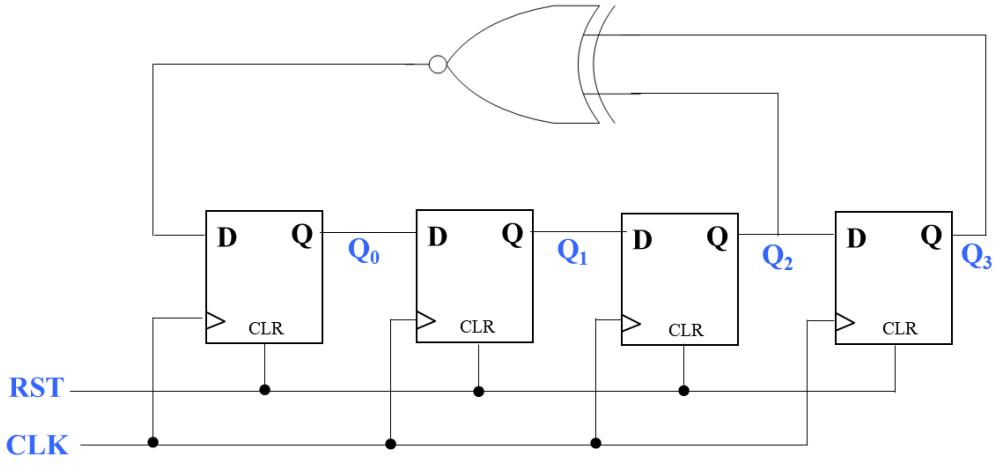


4. The circuit as shown below is a linear feedback shift register (LFSR), commonly used as a Random Number Generator in hardware implementations.

The input bit to the chain of FFs is a function of its previous output. LFSRs are able to generate pseudo-random bit sequences which also have applications in games, cryptography, bit-error-rate measurements to wireless communication systems.

The LFSR below receives two 1-bit inputs, CLK and RST and generates a 4-bit output Q. The RST signal sets the output of the LFSR to 4'b000 asynchronously when enabled.

The D flip-flops used are positive-edge triggered with asynchronous active high clear.



Write a Verilog program that implements the LFSR according to the circuit above. Simulate / work out the operation of the circuit to work out the bit sequence of Q.