Tutorial 8 (SOLUTIONS)

NOTE THAT THERE ARE OTHER POSSIBLE SOLUTIONS TOO…

Question 1

A	B	Q	Q^+
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

(i): Characteristic Table

Q	Q^+	D
0	0	0
0	1	1
1	0	0
1	1	1

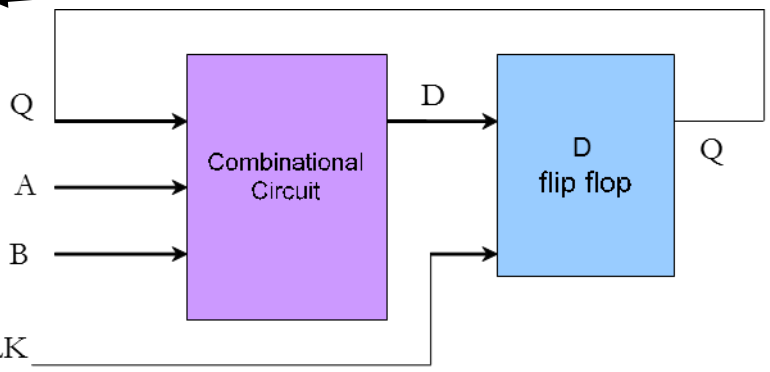
Excitation Table

A	B	Q	Q^+	D
0	0	0	1	1
0	0	1	1	1
0	1	0	0	0
0	1	1	1	1
1	0	0	1	1
1	0	1	0	0
1	1	0	0	0
1	1	1	0	0

Combined Table

A	B	Q	D
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

(iii): Combinational circuit truth table

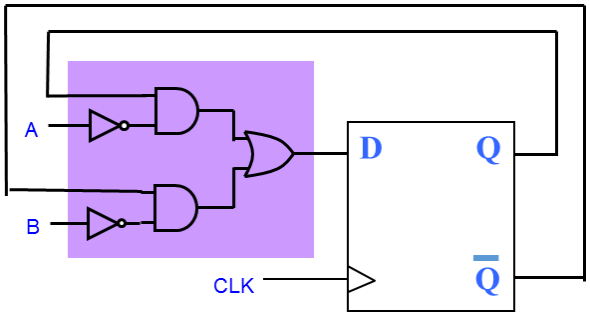


(ii): Functional Block Diagram

e: Use Karnaugh Maps to find logic expressions for D

$$D = \overline{B}\overline{Q} + \overline{A}Q$$

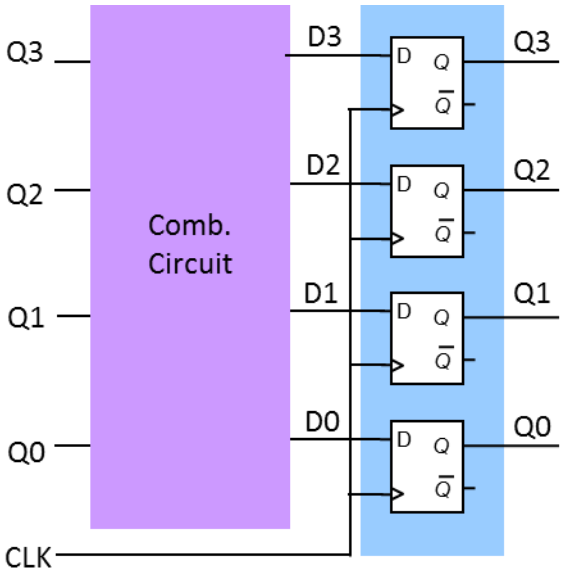
AB \ Q	0	1
00	1	1
01	0	1
11	0	0
10	1	0

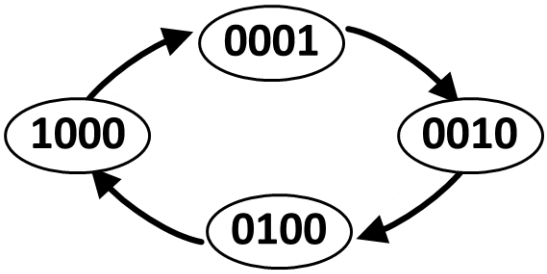



```
module abff (input clk, a, b, output reg q);
wire d;
always @ (posedge clk) begin
        q <=d;
end
assign d = (~b & ~q) | (~a & q);
endmodule
```

Question 2

1) Functional Block Diagram





2) Next State Table

Current State				Next State			
Q3	**Q2**	**Q1**	**Q0**	**Q3+/D3**	**Q2+/D2**	**Q1+/D1**	**Q0+/D0**
0	0	0	1	0	0	1	0
0	0	1	0	0	1	0	0
0	1	0	0	1	0	0	0
1	0	0	0	0	0	0	1
Other States				X	X	X	X

3) Combinational Circuit

Q3+ Kmap

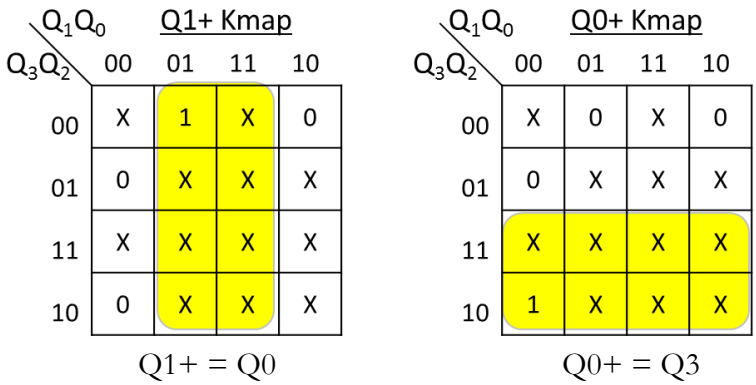
Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	X	0	X	0
01	1	X	X	X
11	X	X	X	X
10	0	X	X	X

Q3+ = D3 = Q2

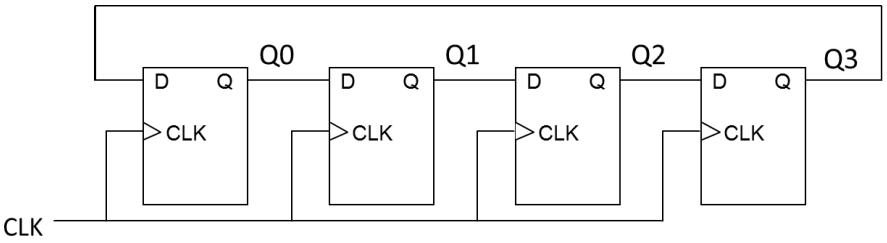
Q2+ Kmap

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	X	0	X	1
01	0	X	X	X
11	X	X	X	X
10	0	X	X	X

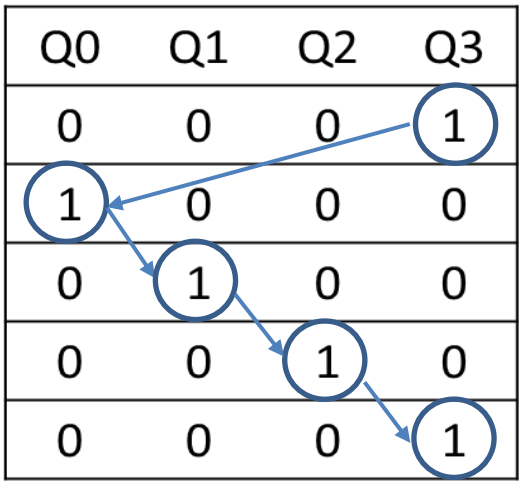
Q2+ = Q1



4) Circuit Realization



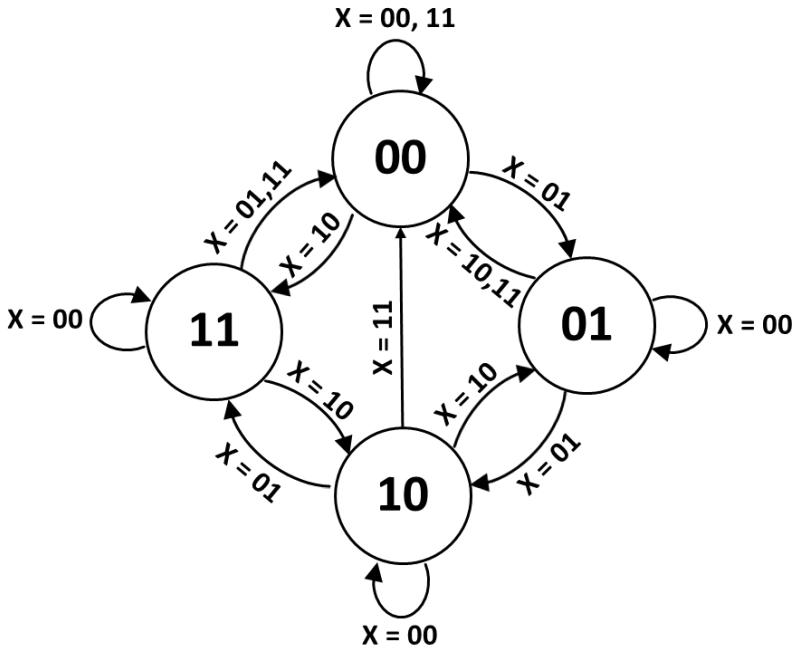
As can be seen above, the circuit realization does not require any additional logic gates. Due to the way the flip flops are connected, the bits in the counter *shift* to the right every active clock edge. This circuit is also known as a ring counter, or a shift register (where the last stage connected to the first). The operation is illustrated as below.



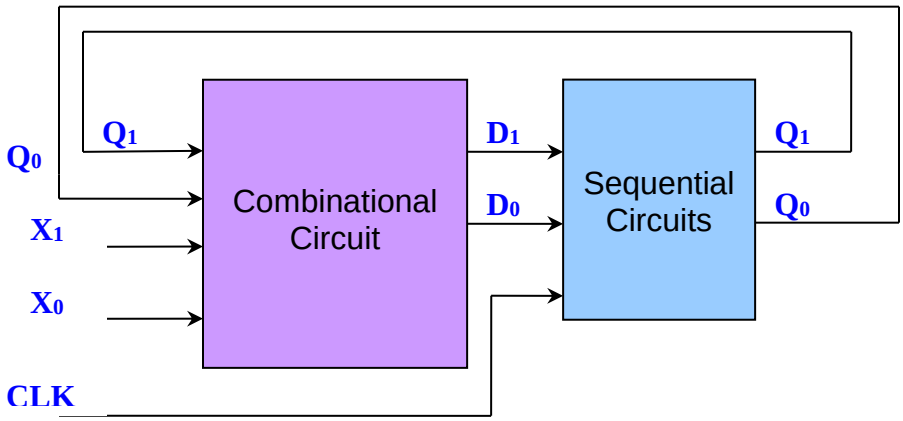
Due to the simple circuit, a tradeoff is that the counter needs to be initialized to a value of 0001, 0010, 0100 or 1000 in order to operate correctly. If the counter is initialized to other values instead (for example 0000), it would not behave as a 1,2,4,8… counter.

Question 3

State Diagram



4 mode 2-bit counter



The next state table is:

X_1	X_0	Q_1	Q_0	Q_1^+ /D_1	Q_0^+ /D_0
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	1	0
0	0	1	1	1	1
0	1	0	0	0	1
0	1	0	1	1	0
0	1	1	0	1	1
0	1	1	1	0	0
1	0	0	0	1	1
1	0	0	1	0	0
1	0	1	0	0	1
1	0	1	1	1	0
1	1	0	0	0	0
1	1	0	1	0	0
1	1	1	0	0	0
1	1	1	1	0	0

X_1X_0 \ Q_1Q_0	00	01	11	10
00	0	1	1	0
01	1	0	0	1
11	0	0	0	0
10	1	0	0	1

$$D_0 = Q_0\overline{X_1}\,\overline{X_0} + \overline{X_1}X_0\overline{Q_0} + X_1\overline{X_0}\,\overline{Q_0}$$

X_1X_0 \ Q_1Q_0	00	01	11	10
00	0	0	1	1
01	0	1	0	1
11	0	0	0	0
10	1	0	1	0

$$D_1 = \overline{Q_1}Q_0\,\overline{X_1}\,X_0 + \overline{Q_1}\,\overline{Q_0}\;X_1\overline{X_0} + \overline{X_1}Q_1\overline{Q_0} + Q_1Q_0\overline{X_0}$$