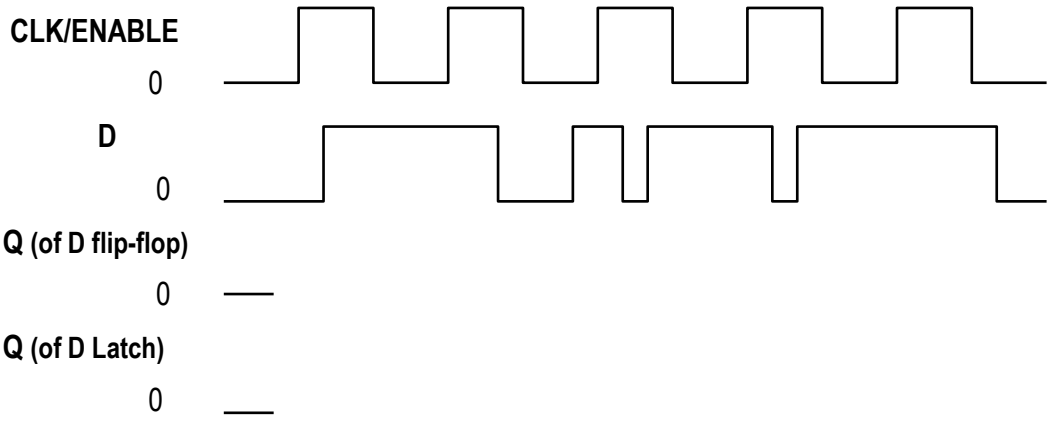
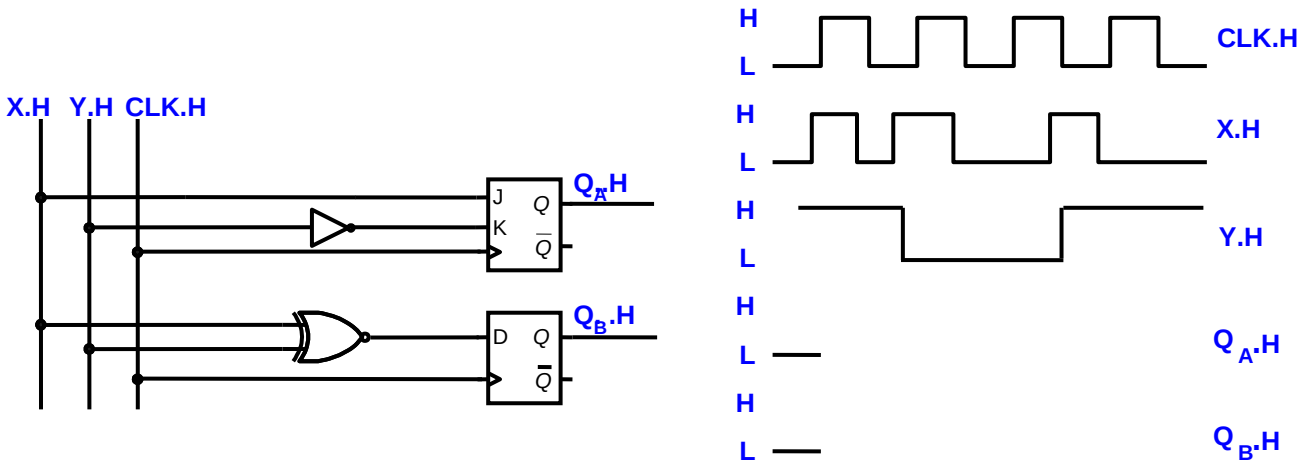
Tutorial 6 Questions

Flip Flops

Q1. The D and CLK/ENABLE input waveforms shown below are applied to a negative-edge triggered D flip-flop & a D Latch. Clearly draw the output Q waveforms of the devices and neglect all propagation delays.

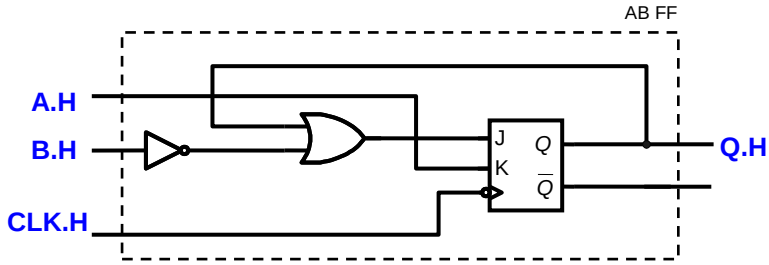


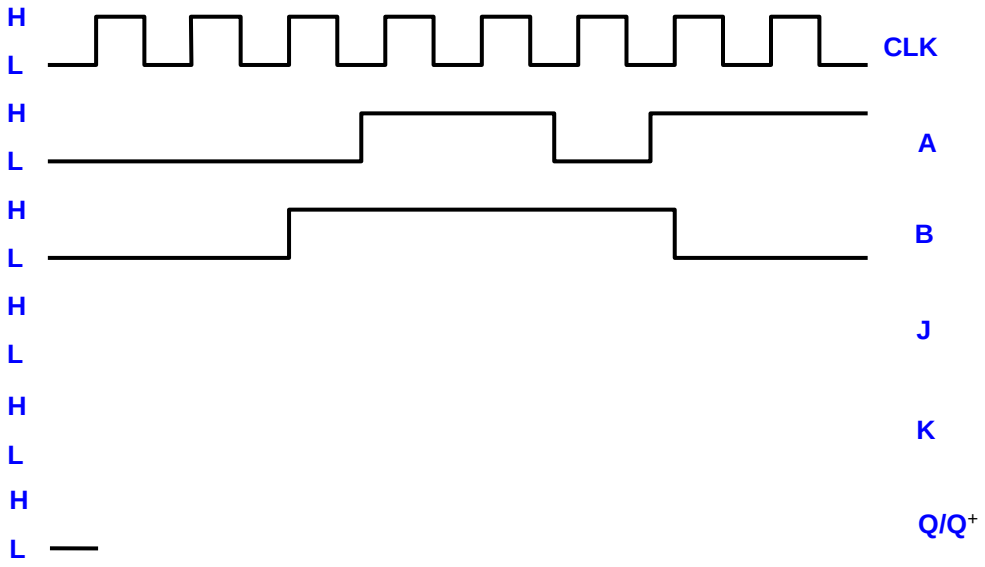
Q2. Given the circuit diagram below, complete the timing diagram below by filling in Q_A and Q_B. Include the propagation delays tp_{HL} and tp_{LH}.



Q3. (a) Given the circuit diagram below, complete the timing diagram below by filling in J, K and Q. Neglect all propagation delays in this question.

(b) If the circuit below represents a type of AB flip flop, fill in its characteristic table and condensed characteristic table below.





A	B	Q	Q^+

A	B	Q^+

Characteristic Table

Condensed Characteristic Table