Mo, Jianqiao

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EDUCATION

Graduate - Tandon School of Engineering, New York University Sep 2020-Present

- PhD in Electrical Engineering, Advised by Prof. Brandon Reagen
- GPA: 3.963/4.0

Undergraduate - School of Electronic Science and Engineering, Nanjing University Sep 2016-Jul 2020

- Bachelor of Science in Electronic Information Science and Technology
- The Elite Electrical Engineer Program
- GPA: 4.57/5.0 (91.4/100); Ranking: 3rd / 71

PUBLICATIONS

- Meiqi Wang, **Jianqiao Mo**, Jun Lin, Zhongfeng Wang, and Li Du, "DynExit: Dynamic Early-Exit Strategy for Deep Residual Networks", *2019 IEEE Workshop on Signal Processing Systems (SiPS)*, Oct 2019
  - Best Paper Award (the first prize)

RESEARCH EXPERIENCES

BAAHL | New York University | Research Assistant

Advisors: Assistant Professor Brandon Reagen

Research on secure two-party computation and in-memory computation: Sep 2020-Present

- In-memory computation is the technique of running computer calculations entirely in computer memory. It is used to solve the latency of data movement.
- Garbled circuits (GC) are a protocol for secure two-party computation. It is applied as an essential protocol for non-linear computation.
- A GC compiler and an accelerator will be proposed toward the challenges above.

ICAIS Lab | Nanjing University | Research Assistant

Advisors: Professor Zhongfeng Wang, Associate Professor Jun Lin, ESE of NJU

Research on Early Exit Mechanism of deep network: Mar 2019-Mar 2020

- Early-Exit mechanism (BranchyNet): accelerate inference, reduce latency and cut down energy cost.
- DynExit: Applied a dynamic loss-weight modification strategy for BranchyNet to adaptively modify the ratios of different exit branches and find a trade-off between accuracy and cost.
- Achieved remarkable performance on CIFAR-100/ImageNet dataset: we achieved standard or better performance compared to the state-of-the-art approaches at 43.6% FLOPs reduction.
- Developed an architecture to speed up the dynamic Early-Exit Strategy, which was evaluated on Xilinx Zynq-7000 ZC706 development board.
- Paper accepted by 2019 IEEE SiPS (Best Paper Award, the first prize).

Electronic Design Competition | Electrotechnics Center, NJU | Captain Aug 2017

Advisors: Associate Prof. Jianjun Zhuang, Associate Prof. Jian Gao, ESE of NJU

- Designing a Ball & Plate Apparatus based on PID fuzzy control system.
- Processed the image signal on Raspberry-Pi with Python.
- Completed the 4-days competition and received 2nd prize in Jiangsu Province, China.

AWARDS & HONORS

The Honor Graduate (*Nanjing University*)	Apr 2020
The China Merchants Bank Scholarship	Oct 2019
The Samsung Scholarship	Dec 2018
Outstanding Youth League Member Paragon	May 2018
Outstanding Student Leader of Nanjing University	Jan 2018
The Student Fund Promoting Ambassador of Nanjing University	Jan 2018-Jun 2018
The People's Scholarship (*Nanjing University*)	Nov 2017
The National Scholarship	Nov 2017
National Electronic Design Competition, the Second Prize (*Jiangsu Province*)	Sep 2017

WORKING EXPERIENCE & EXPERIMENT PROJECTS

Jiangsu Changjiang Electronics Technology Co., Ltd | Wuxi, Jiangsu Province | Trainee Jul 2018-Aug 2018

Advisors: Prof. Yugang Zhou, ESE of NJU

- Visited the JCET as an internship member of The Electronic Engineering Elite Program, Nanjing University
- Went through the whole assembly line in the chip packaging and testing workshop

Experiments of AM Circuits Dec 2018

- Implement an Amplitude Modulation (AM) transmitter and receiver system on circuit board

Fundamentals of Hardware Design (Experiment) Jun 2019

- Coded with Verilog, designed an 8-bit RISC-CPU and accomplished the task of verification

ACTIVITIES

Student Union | Academic Department | School of ESE, Nanjing University Sep 2016-Jun 2017

- Member of Academical Department

PROFESSIONAL SKILLS

- Programming Languages: C/C++, Matlab, Python, Assembly language, Verilog
- TOEFL MyBest™ Scores: 105/120 (Listening: 28, Reading: 28, Speaking: 23, Writing: 26)