

Yihan Pang

Email: pyihan1@vt.edu

EDUCATION

M.S. Computer Engineering;

8/2016 - 9/2019

Virginia Polytechnic Institute and State University, Blacksburg, VA

Advisor: Dr. Binoy Ravindran

Thesis: *Leveraging Processor-diversity for Improved Performance in Heterogeneous-ISA Systems*

GPA 3.81/4.0

B.S. Computer Engineering; Minor: Math, Cybersecurity

8/2011 - 12/2015

Virginia Polytechnic Institute and State University, Blacksburg, VA

GPA 3.78/4.0 Rank: 7

PUBLICATION

“Quantifying Memory Underutilization in HPC Systems and Using it to Improve Performance via Architecture Support.”

G. Panwar*, D. Zhang*, **Yihan Pang***, M. Dahshan, N. DeBardeleben, B. Ravindran, and X. Jian (* first co-authors).

In *Proc. of the 52nd annual IEEE/ACM international symposium on Microarchitecture (MICRO-52)*, October 2019

“Cross-ISA execution of SIMD regions for improved performance.”

Yihan Pang, Robert Lyrly, and Binoy Ravindran.

In *Proc. of the 12th ACM International Conference on Systems and Storage (SYSTOR 2019)*, June 2019.

EXPERIENCE

Graduate Research Assistant

July. 2018 - Oct. 2019

High-performance, Energy-efficient, Assured

Blacksburg, VA

Processing (HEAP) Lab

Supervised by Dr. Xun Jian and Dr. Binoy Ravindran

- Quantified memory underutilization problem in HPC Systems
- Designed and developed architectural and OS support to boost microarchitecture performance through better memory utilization

Graduate Research Assistant

Aug. 2016 - Oct. 2019

System Software Research Group (SSRG)

Blacksburg, VA

Supervised by Dr. Binoy Ravindran

Popcorn Linux Project

- Explored potential performance benefits in heterogeneous systems with diversity in processor designs
- Designed SIMD extension migration support (compiler(LLVM) and kernel modifications(Linux)) for Instruction Set Architecture (ISA)-diverse multi/many-core architectures
- Enhanced existing profile-guided optimization techniques in LLVM to adjust for Instruction Set Architecture (ISA)-diverse multi/many-core architectures
- Developed a scheduler to improve system performance by leveraging processor-affinity

Graduate Teaching Assistant

Aug. 2016 - May. 2017

ECE Dept at Virginia Tech

Blacksburg, VA

Teaching assistant for ECE 4534 Embedded System Design

Supervised over 100 students in their senior capstone class over two semesters

Summer Intern

Bank of China Head Office

Interned in the Investment Banking and Asset Management Department

- Developed program that analyzes investor location patterns
- Assisted in developing and implementing a mathematical model that predicts primary market return based on regression analysis

Jun. 2016 - Aug. 2016

Beijing, China

Undergraduate Research Assistant

ECE Dept at VT and Lockheed-Martin

Supervised by Lockheed-Martin Fellow Dr. Richard N. Pedersen

FPGA-based Switch Circuit Project

- Analyzed advanced switching circuits implemented in FPGAs
- Investigated techniques for optimizing Benes-Clos Networks
- Designed and implemented three variations of Benes-Clos Network
- Evaluated theoretical and empirical results

Aug. 2015 - May. 2016

Blacksburg, VA

Undergraduate Teaching Assistant

ECE Dept at Virginia Tech

Teaching assistant for ECE 4534 Embedded System Design

- Assisted in redesigning the class
- Designed milestone modules for future students
- Created prototype final deliverable for demonstrations

Aug. 2015 - Dec. 2015

Blacksburg, VA

Undergraduate Research Assistant

ECE Dept at Virginia Tech

Supervised by Dr. Cameron D. Patterson and William T. Baumann

TAIGA Project

- Designed and developed lab modules that exploited vulnerabilities in embedded system's camera module and system's configuration channel

June. 2015 - Aug. 2015

Blacksburg, VA

HONORS & AWARDS**Full Tuition Scholarship**, Virginia Tech**Dean's List**, Virginia Tech

2016-2019

2011-2015

SKILLS**Programming Languages:** C, C++, Bash, Python, Assembly, Java.**Software Frameworks:** LLVM, Gem5, DRAMSim2, Ramulator