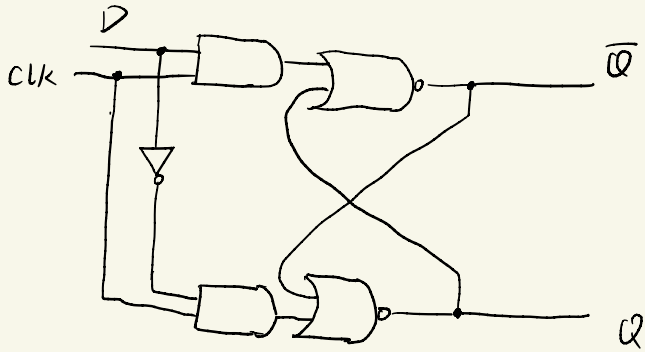
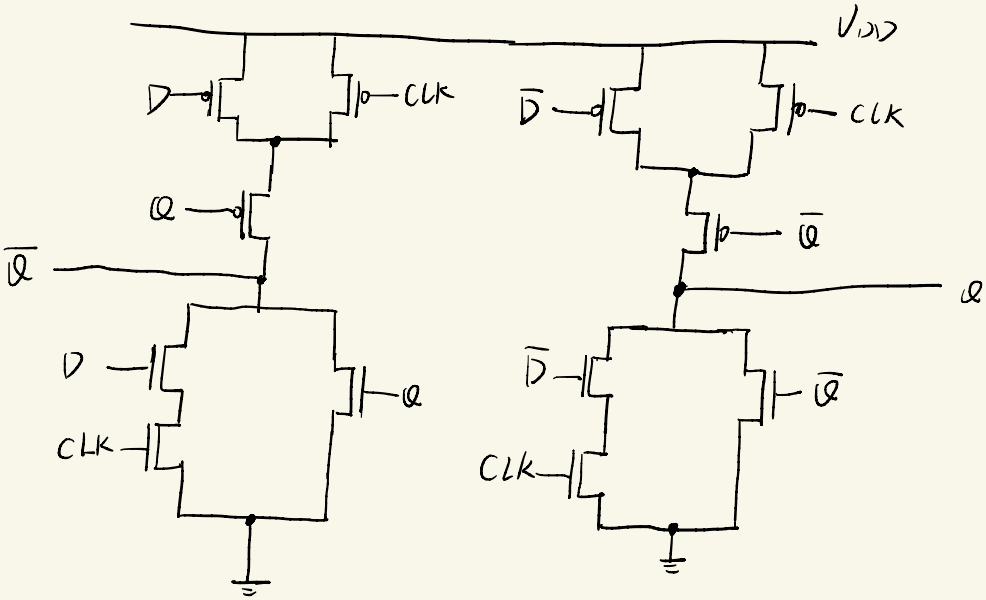
B.8.1

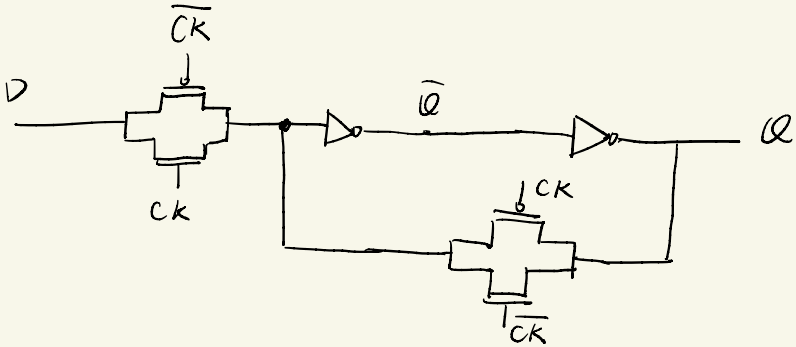
D latch:

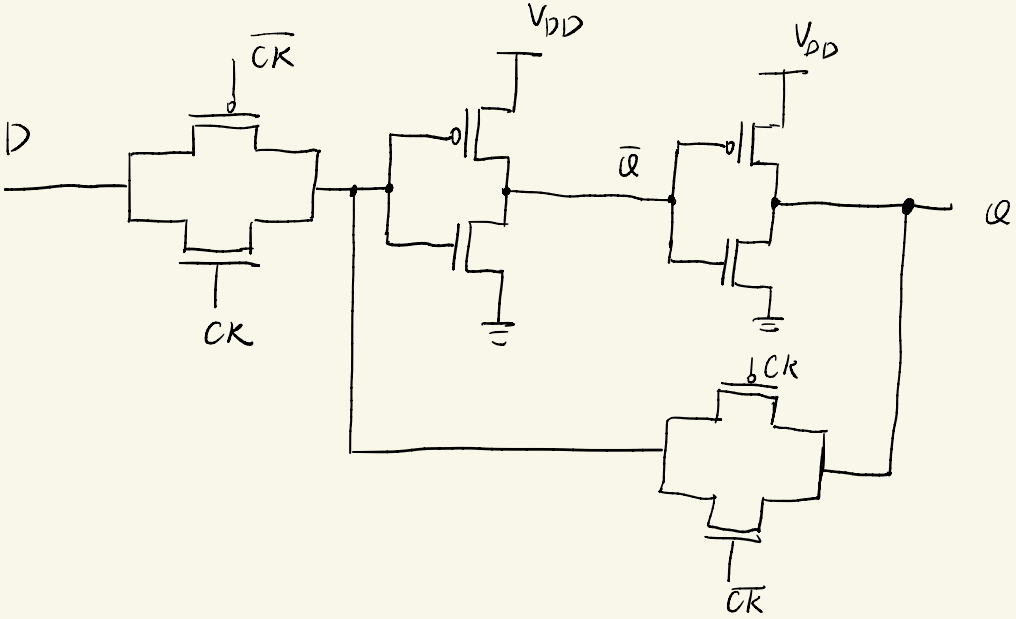


(1) AOI

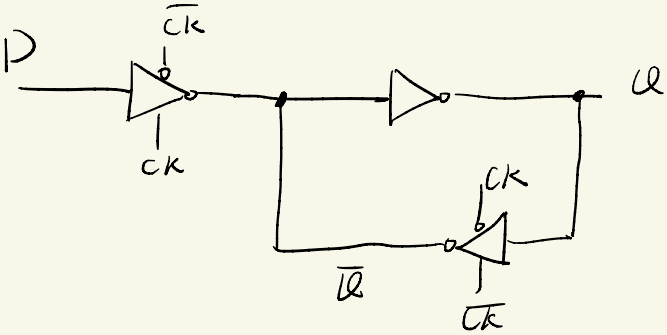


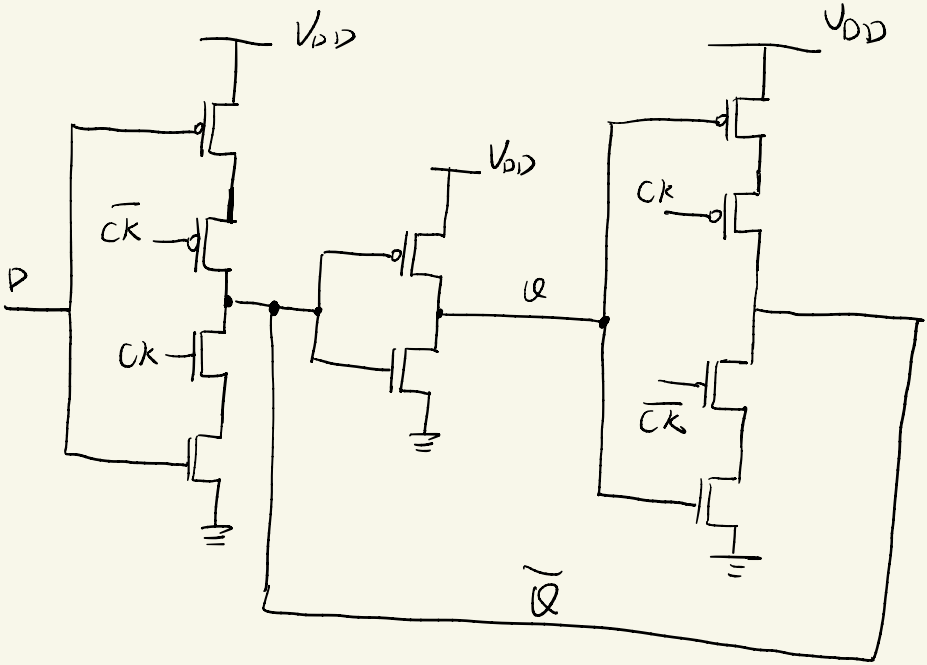
(2) 传输门



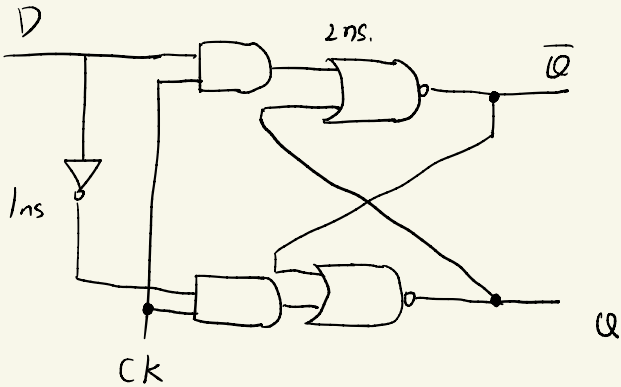

$\overline{CK}$
V_{DD}
V_{DD}
D
$\overline{Q}$
Q
CK
CK
$\overline{CK}$

(3) 三态门

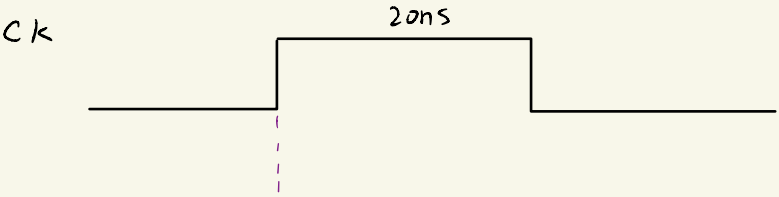

$\overline{CK}$
D
Q
CK
CK
$\overline{Q}$
$\overline{CK}$

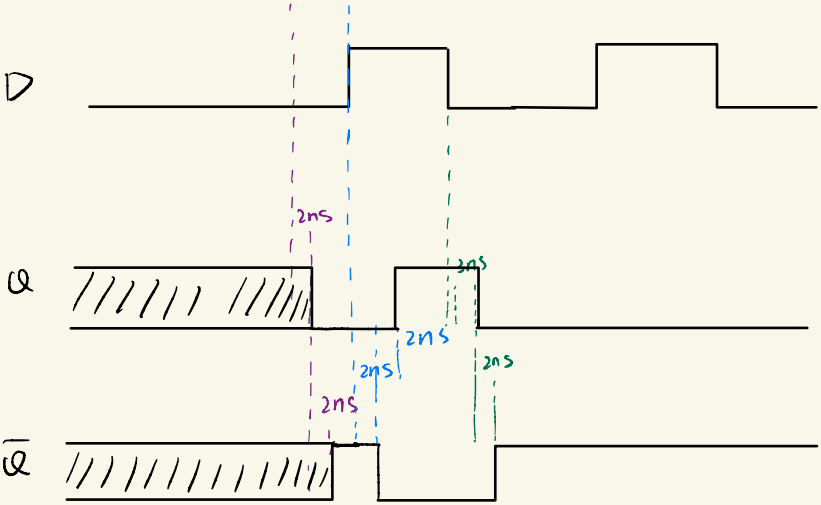


13 8.2



CK 是 25MHz. $T = \frac{1}{25\times10^6} = 0.04\times10^{-6} = 40\,ns$

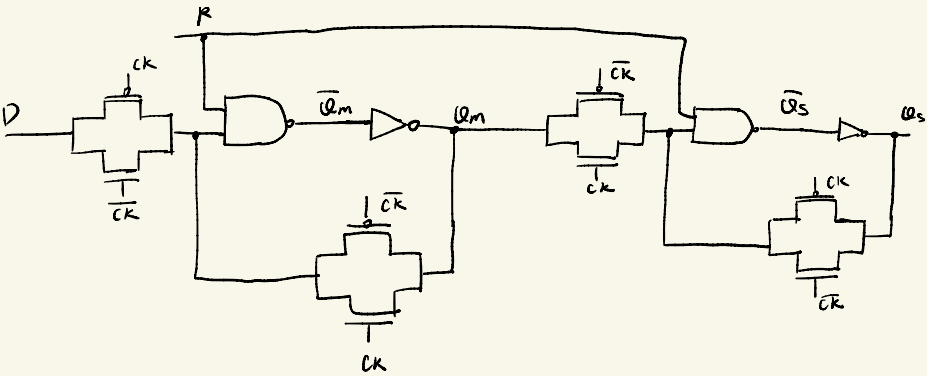




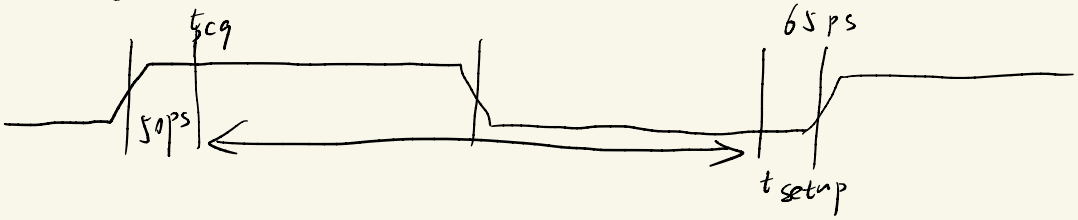
D 传到 Q 最大的延时是 4ns

传到 $\overline{Q}$ 最大的延时是 5ns

13.8.3



B.8.4 (a)



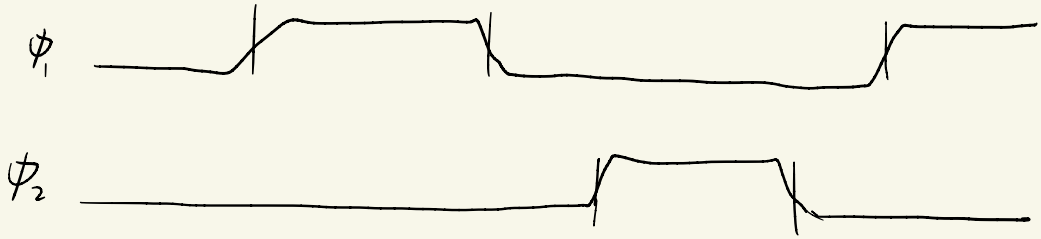
最大组合逻辑时 $500 - 50 - 65 = 385ps$.

$(T_c - t_{cq} - t_{setup} \geq t_{cd})$

$30ps = t_{hold} \leq t_{ccq} + t_{cd} = 35ps + t_{cd}$. 总成立

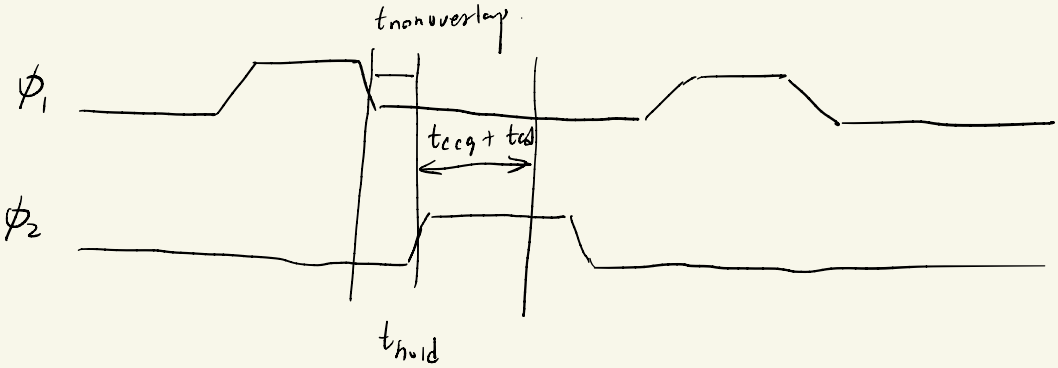
最小组合逻辑时 $t_{cd} \geq 0ps$ 即可

(b)



最大组合逻辑时 $T_c \geq t_{pd} + t_{pdq_1} + t_{pdq_2}$

$t_{pd} \leq 500 - 2 \times 40 = 420ps$.



最小组合逻辑时 $t_{hold} \le t_{nonoverlap} + t_{ccq} + t_{cd}$

$t_{cd} \ge t_{hold} - t_{nonoverlap} - t_{ccq} = 30 - 50$

$t_{cd} \ge 0ps$ 即可

有偏斜条件下: $t_{skew} = 50ps$

(a) $t_{pd} \le T_c - (t_{setup} + t_{skew}) - t_{pcq} = 500 - 50 - 65 - 50 = 335ps$

以上为最大组合延时.

最小组合延时:

$t_{hold} + t_{skew} \le t_{ccq} + t_{cd}$

$t_{cd} \ge t_{hold} + t_{skew} - t_{ccq} = 30 + 50 - 35 = 45ps$

(b) 最大组合延时: 时钟偏斜不影响两相D锁存器的最大组合延时

仍为: 420ps

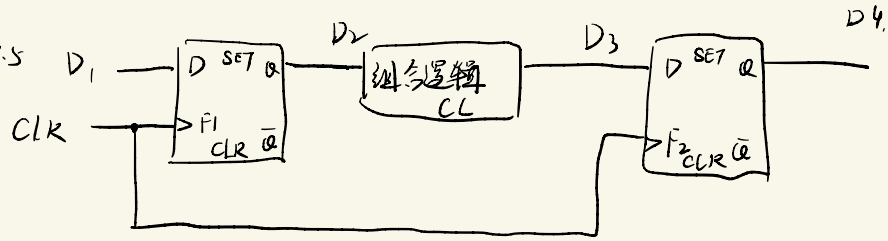
最小组合延时:

$$t_{hold} + t_{skew} \le t_{nonoverlap} + t_{ccq} + t_{cd}$$

$$t_{cd} \ge t_{hold} + t_{skew} - t_{nonoverlap} - t_{ccq}$$

$$t_{cd} \ge 30 + 50 - 0 - 35 = 45\,ps$$

B. 8.5



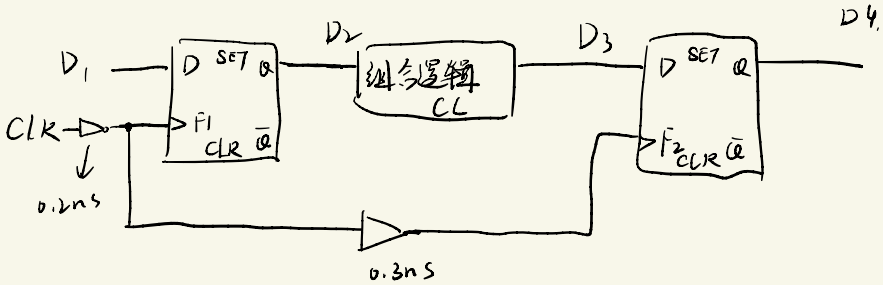
$t_{setup} = 0.3ns$. $t_{cq} = 0.4ns$. $t_{pcd} = 3.3ns$.

$$t_{setup} + t_{cq} + t_{pcd} \le T_c$$

$$T_c \ge 4ns$$

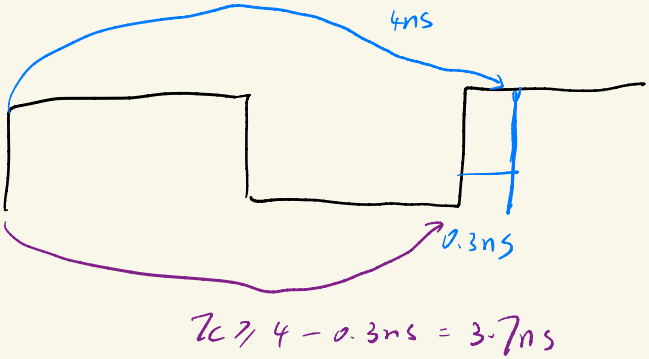
如果可以拆分, $t_{pcd} = 1.8ns$

$$T_c \ge 2.5ns$$

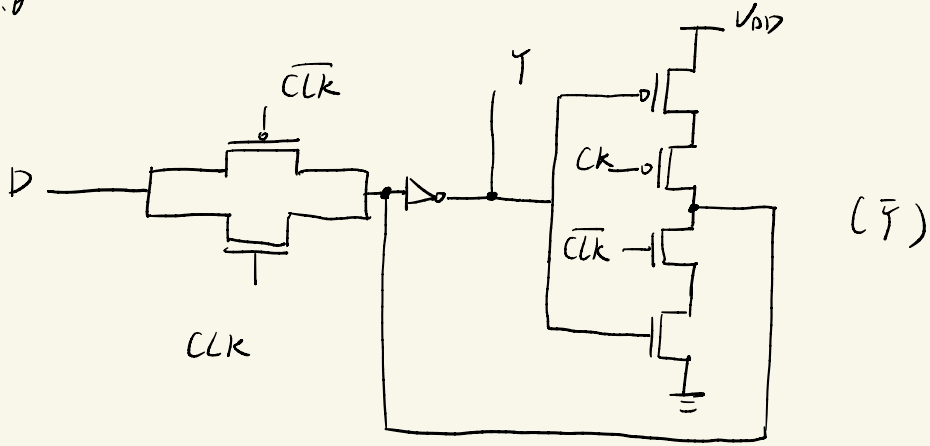


$T_c \geq t_{setup} + t_{pcd} + t_{cq} - 0.3ns$

$T_c \geq 3.7ns$



B.8.b



是个 D latch