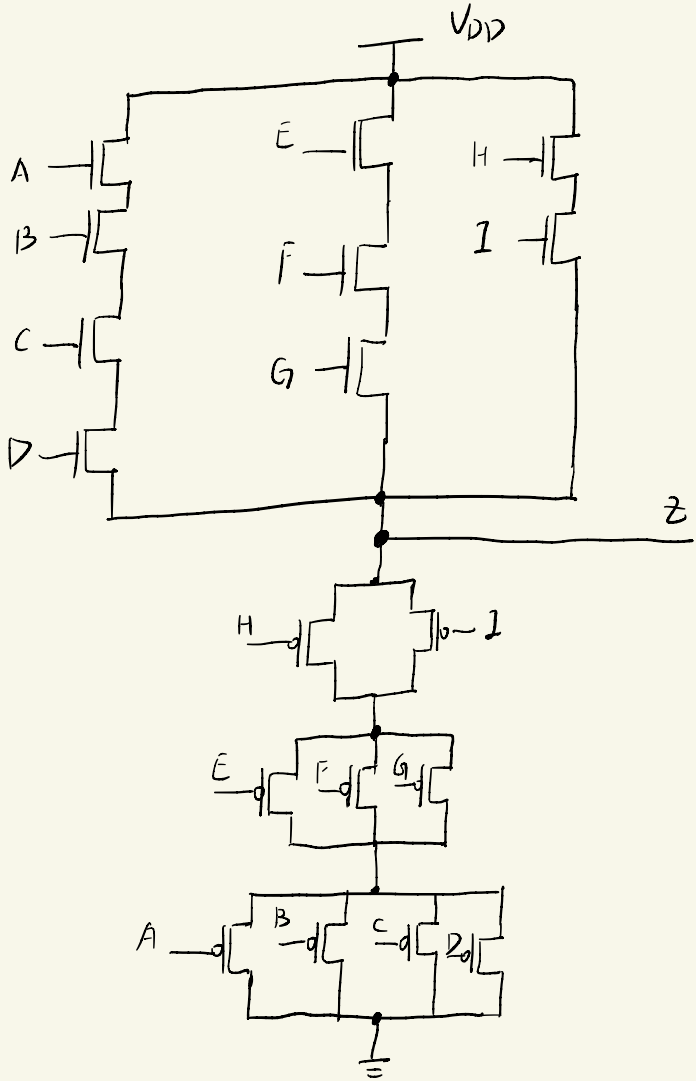
9.2 OAI432 $Z = \overline{(A+B+C+D)(E+F+G)(H+I)}$

A、E、H 为高电平：$C_{ox} = 22mF/m^2$ $k_n' = 102\mu A/V^2$

$k_p' = 51.6\mu A/V^2$ $V_{Tn,0} = 0.48V$ $V_{Tp,0} = -0.46V$

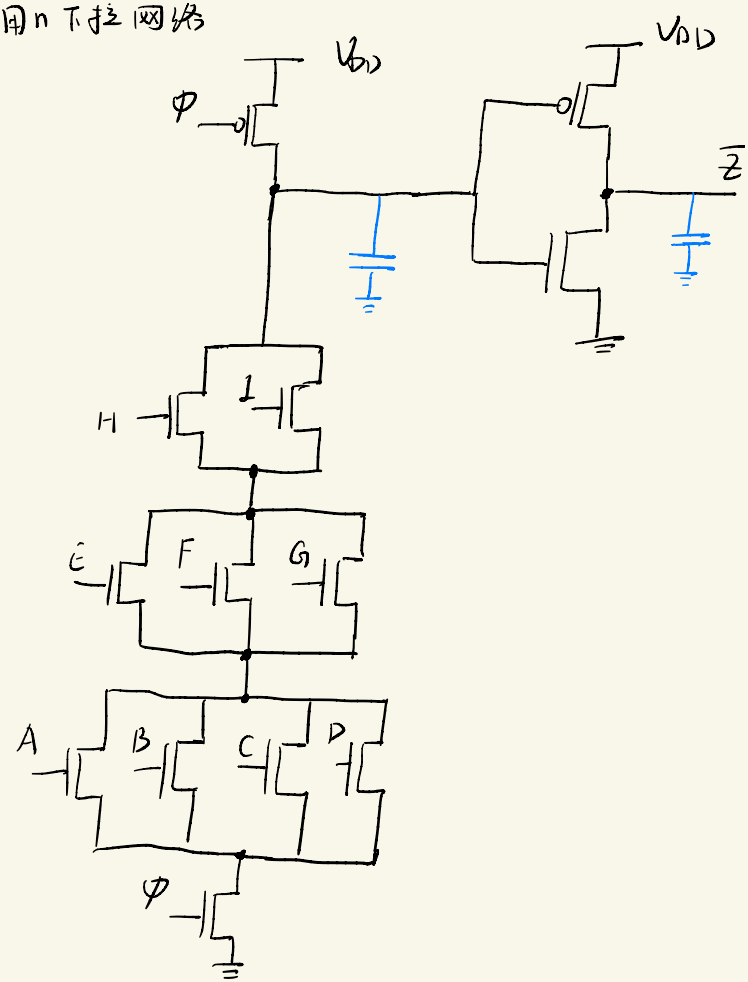
$E_{cn}L_n = 0.4V$ $E_{cp}L_p = 1.8V$

a.



b. $\overline{Z} = (A+B+C+D)(E+F+G)(H+I)$

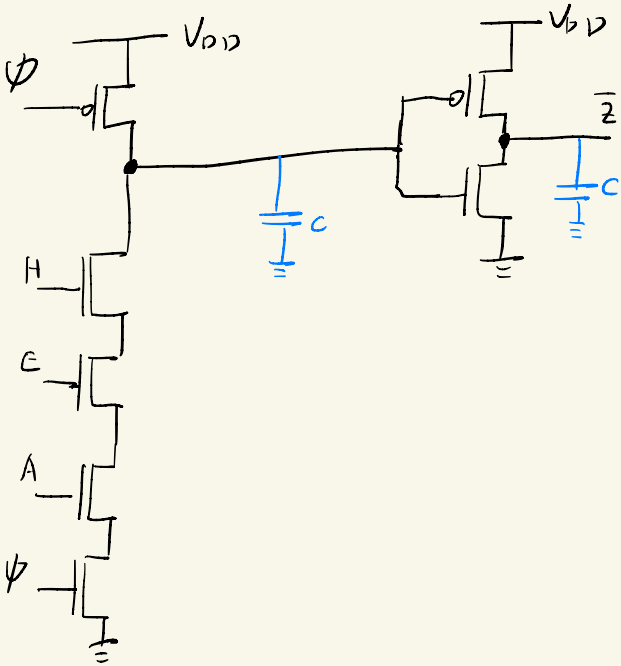
使用n下拉网络



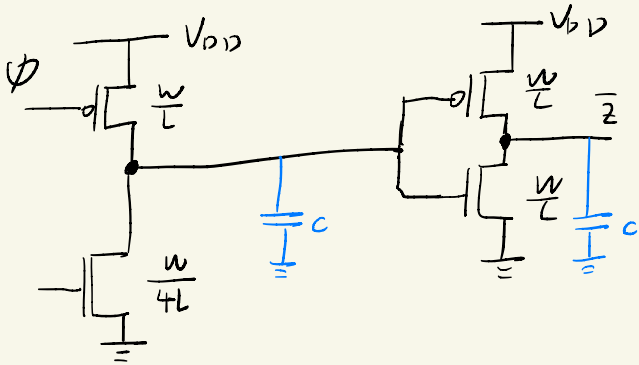
c. $\frac{W}{L} = \frac{1}{0.065}$

忽略 B、C、D F G I

上图简化为:

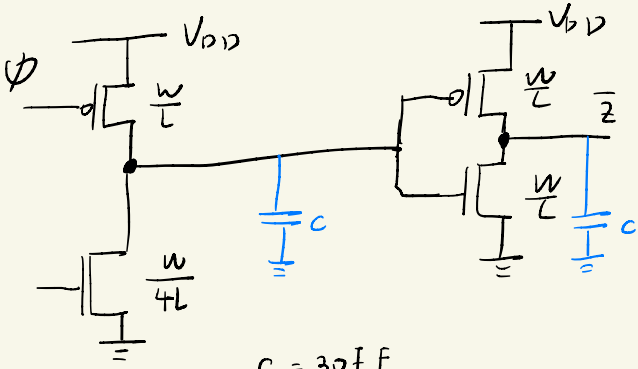


可以将下方4个 nmos 等效为 1个



$\frac{W}{L} = \frac{1}{0.065}$ $\frac{W}{4L} = \frac{1}{0.26}$

d.



$C = 30fF$

对于长沟道条件:

$$t_{pHL} = \frac{C_{load}\,\Delta V}{I_{average,\,fall}}$$

$$I_{average,fall} = \frac{1}{2}\left(I_1 (V_{in}=V_{dd},\ V_{out}=1.2V) + I_2 (V_{in}=V_{dd},\ V_{out}=0.6V)\right)$$

$V_{in} = V_{dd}$, $V_{out} = 1.2V$

$V_{DS} = 1.2V$ $V_{GS} - V_{TH} = 1.2 - 0 - 0.48 = 0.72V$

nmos 工作于饱和区

$$I_1 = \frac{1}{2}\mu_n C_{ox} \frac{W}{4L} (V_{GS}-V_{TH})^2$$

$$= \frac{1}{2} k'_n \cdot \frac{W}{4L} (V_{GS}-V_{TH})^2$$

$$= 1.01686 \times 10^{-4}\ A$$

$V_{out} = 0.6V$时 2个子 线性区

$$I_2 = \frac{1}{2}\mu_n C_{ox}\frac{W}{4L}\left(2(V_{GS}-V_{TN})V_{DS} - V_{DS}^2\right)$$

$$= \frac{1}{2}k_n'\frac{W}{4L}\left(2(V_{GS}-V_{TN})V_{DS} - V_{DS}^2\right)$$

$$= 9.886\times10^{-5}A$$

$$I_{average,fall} \approx 1\times10^{-4}A$$

$$t_{pHL} = \frac{C_{load}\Delta V}{I_{average,fall}} = \frac{30\times10^{-15}\times0.6}{1\times10^{-4}} = 18\times10^{-11} = 0.18\ ns$$

$$t_{pLH} = \frac{C_{load}\Delta V}{I_{average\ rise}}$$

$$I_{average,rise} = \frac{1}{2}\left(I_1(V_{in}=0\ V,\ V_{out}=0\ V) + I_2(V_{in}=0\ V + V_{out}=0.6V)\right)$$

$V_{out} = 0V.$ $\quad V_{DS} = -1.2V$ $\quad V_{GS}-V_{TN} = 0-1.2+0.46 = -0.74V$

$V_{DS} < V_{GS}-V_{TN}.$

pmos 2 饱和区

$$I_1 = \frac{1}{2}k_p'\frac{W}{L}(V_{GS}-V_{TN})^2$$

$$= 2.17355\times10^{-4}A$$

$V_{out} = 0.6V \quad V_{DS} = -0.6V > V_{GS} - V_{TH}$

PMOS 工作于线性区

$$I_2 = \frac{1}{2} k_p' \frac{W}{L} \left(2(V_{GS} - V_{TH}) V_{DS} - V_{DS}^2 \right)$$

$$= 2.09575 \times 10^{-4} A$$

$$I_{average.rise} = 2.13465 \times 10^{-4} A$$

$$t_{PLH} = \frac{C_{load} \Delta V}{I_{average.rise}} = \frac{30 \times 10^{-15} \times 0.6}{2.13465 \times 10^{-4}} = 8.4322957 \times 10^{-11} s$$

$$= 0.084323 ns$$

总延时大约是 $t_{PHL} + t_{PLH} = 0.264323 ns$

对于短沟道条件：

计算 t_{PHL} 时 $I_1' = I_1 \cdot \frac{1}{1 + \frac{V_{GS} - V_{TH}}{E_{cn} L_n}} = 3.63164 \times 10^{-5} A$

$$I_2' = I_2 \cdot \frac{1}{1 + \frac{V_{DS}}{E_{cn} L_n}} = 3.9544 \times 10^{-5} A$$

$$I_{average.fall} = 3.79302 \times 10^{-5} A$$

$$t_{PHL} = \frac{30 \times 10^{-15} \times 0.6}{3.79302 \times 10^{-5}} = 4.74559 \times 10^{-10} s = 0.474559 ns$$

计算 2pLH时

$$L_1' = L_1 \frac{1}{1 + \frac{V_{SD}}{E_{cp} L_p}} = 1.30413 \times 10^{-4} A$$

$$L_2' = L_2 \frac{1}{1 - \frac{V_{GS} - V_{Tp}}{E_{cp} L_p}} = 1.485 \times 10^{-4} A$$

$$I_{average.rise} = 1.39465 \times 10^{-4} A$$

$$2pLH = \frac{C_{load} \Delta U}{I_{average.rise}} = \frac{30 \times 10^{-15} \times 0.6}{1.39465 \times 10^{-4}} = 1.29 \times 10^{-10} s$$

$$= 0.129 ns$$

总延时为 $2pHL + 2pLH = 0.603559 ns$

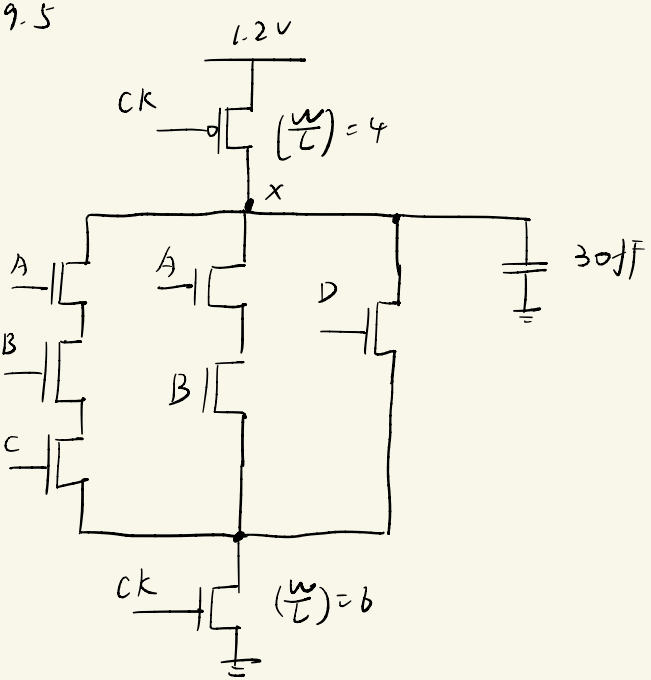
9.3 电荷共享是指在动态电路中，当后一级导通时，前一级的输出（寄生）电容上的电荷会有一部分分到下一级的输入电容上，导致前一级的电容电荷减少，电压降低，从而可能引发逻辑错误

解决方案：① 减小反相器逻辑阈值电压，使输出不因电荷减少，电压降低而发生错误

② 使用前对所有的中间节点进行预充电

③ 在动态 CMOS 门输出端加一个弱上拉能力的 PMOS

9.5

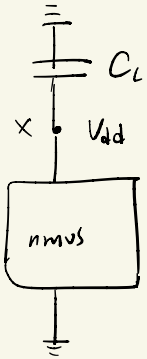


将 X 预充至 V_{DD}.　　nMOS $\frac{W}{L} = 20$.　　A、B、D → 1.2V　　C → 0V

时钟脉冲上升后，求 X 降低到 0.8V_{DD} 的时间.

$\gamma = 0$ $\quad V_{T0} = 0.48V$ $\quad k_n' = 102\mu A/V^2$ $\quad E_{cn}L_n = 0.4$

下拉等效 $\left(\frac{W}{L}\right)_{eq} = \dfrac{\left(\frac{20}{2}+20\right)\times 6}{\frac{20}{2}+20+6} = \dfrac{30\times 6}{36} = 5$



$$-I = C_L \frac{dV_{out}}{dt}$$

$$-dt = C_L \frac{1}{I} dV_{out}$$

$$-\int_0^t dt = C_L \int_{V_{dd}}^{0.8V_{dd}} \frac{dV_{out}}{\frac{1}{2}k_n'\left(\frac{W}{L}\right)_{eq}(V_{in}-V_{tn})^2}$$

$$t = C_L \cdot \frac{0.2V_{dd}}{\frac{1}{2}k_n'\left(\frac{W}{L}\right)_{eq}\cdot(V_{in}-V_{tn})^2}$$

$$t = \frac{0.2\times 1.2\times 30\times 10^{-15}}{\frac{1}{2}\times 102\times 10^{-6}\times 5\times (1.2-0.48)^2} = 5.446623\times 10^{-11}s$$

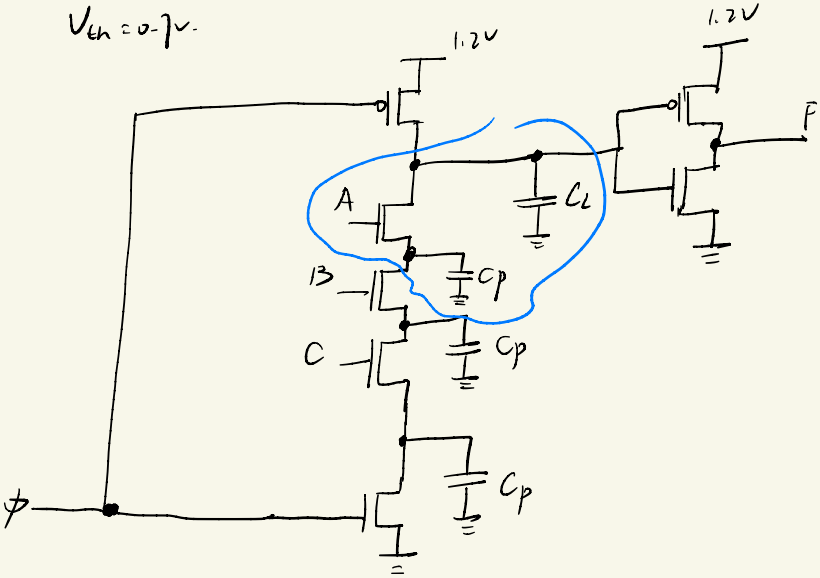
$$= 0.05446623\ ns$$

9.6. 预充电: $\phi = LO$ 逻辑门输入总为LO

$\phi = HI$ 可能产生由低到高的转换

在定值时间 $A = HI$, $B = LO$, $C = LO$ 电荷共享会使反相器输入电压下降

$V_{th} = 0.7V$



$$V_{dd} C_L = V_{in}(C_L + C_p)$$

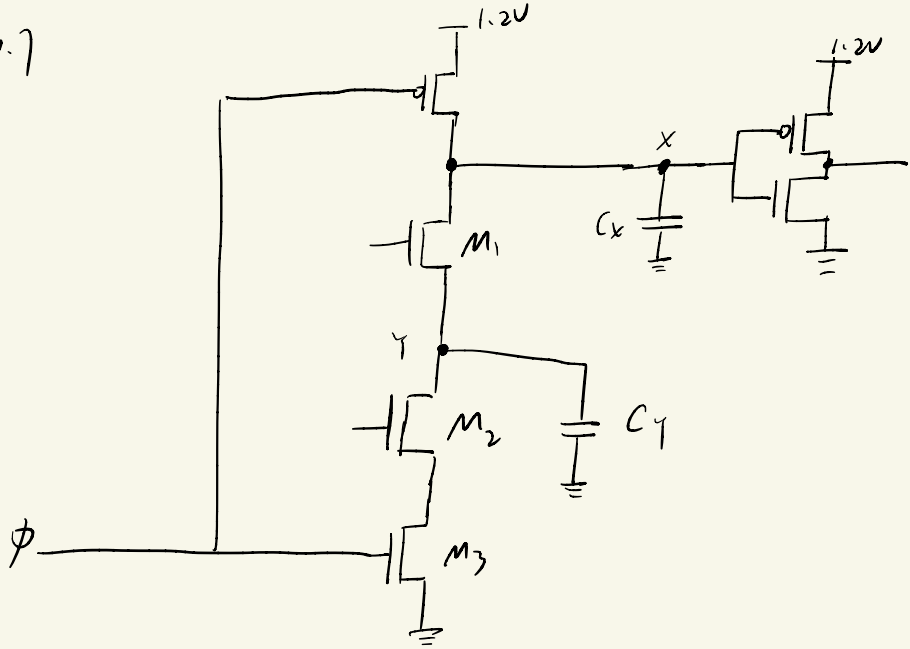
$$V_{in} = \frac{V_{dd} C_L}{C_L + C_p} \geq 0.7V$$

$$\frac{1.2}{1 + \frac{C_p}{C_L}} \geq 0.7$$

$$1 + \frac{C_p}{C_L} \leq \frac{1.2}{0.7} = \frac{12}{7}$$

$$\frac{C_p}{C_L} \leq \frac{5}{7} = 0.7142857$$

9.7



a: $C_X = C_Y$. V_X 预充到 1.2V.

电荷共享对 V_X 的影响

C_X 与 C_Y 发生电荷共享时会将 V_X 电压拉低.

导致反相器输入电压降低

M_2 栅压固定为 0V 时. 在完全预充电后. 完成电荷共享.

$$C_Y V_Y + 1.2C_X = V_X(C_X + C_Y)$$

$$V_X = \frac{C_Y V_Y + 1.2C_X}{C_X + C_Y} \xrightarrow{C_X = C_Y} \frac{V_Y + 1.2}{2}$$

b、即要求 $V_x \geq V_{th}$ $\qquad k_R = \frac{k_n}{k_p} = ?$

长沟道：$V_{th} = \dfrac{V_{T0,N} + \sqrt{\frac{1}{k_R}}\left(V_{DD} - |V_{T0,p}|\right)}{1+\sqrt{\frac{1}{k_R}}} \leq \dfrac{V_T + 1.2}{2}$

$$\frac{0.45 + \sqrt{\frac{1}{k_R}}\,(1.2 - 0.45)}{1+\sqrt{\frac{1}{k_R}}} \leq \frac{V_T}{2} + 0.6$$

$$0.45 + \sqrt{\frac{1}{k_R}}\cdot 0.75 \leq \frac{V_T}{2} + 0.6 + \left(\frac{V_T}{2} + 0.6\right)\sqrt{\frac{1}{k_R}}$$

$$-0.15 - \frac{V_T}{2} \leq \sqrt{\frac{1}{k_R}}\left(\frac{V_T}{2} - 0.15\right)$$

$$\sqrt{\frac{1}{k_R}}\,(0.3 - V_T) \leq V_T + 0.3$$

① $0 \leq V_T \leq 0.3V$ 时，

$$\sqrt{\frac{1}{k_R}} \leq \frac{0.3 + V_T}{0.3 - V_T}$$

$$k_R \geq \left(\frac{0.3 - V_T}{0.3 + V_T}\right)^2$$

② $V_T > 0.3V$ 时

$$k_R \leq \left(\frac{0.3 - V_T}{0.3 + V_T}\right)^2$$

令 $f(x) = \left(\dfrac{0.3 - x}{0.3 + x}\right)^2 = \left(\dfrac{0.3 + x - 2x}{0.3 + x}\right)^2 = \left(1 - \dfrac{2}{\frac{0.3}{x} + 1}\right)^2$

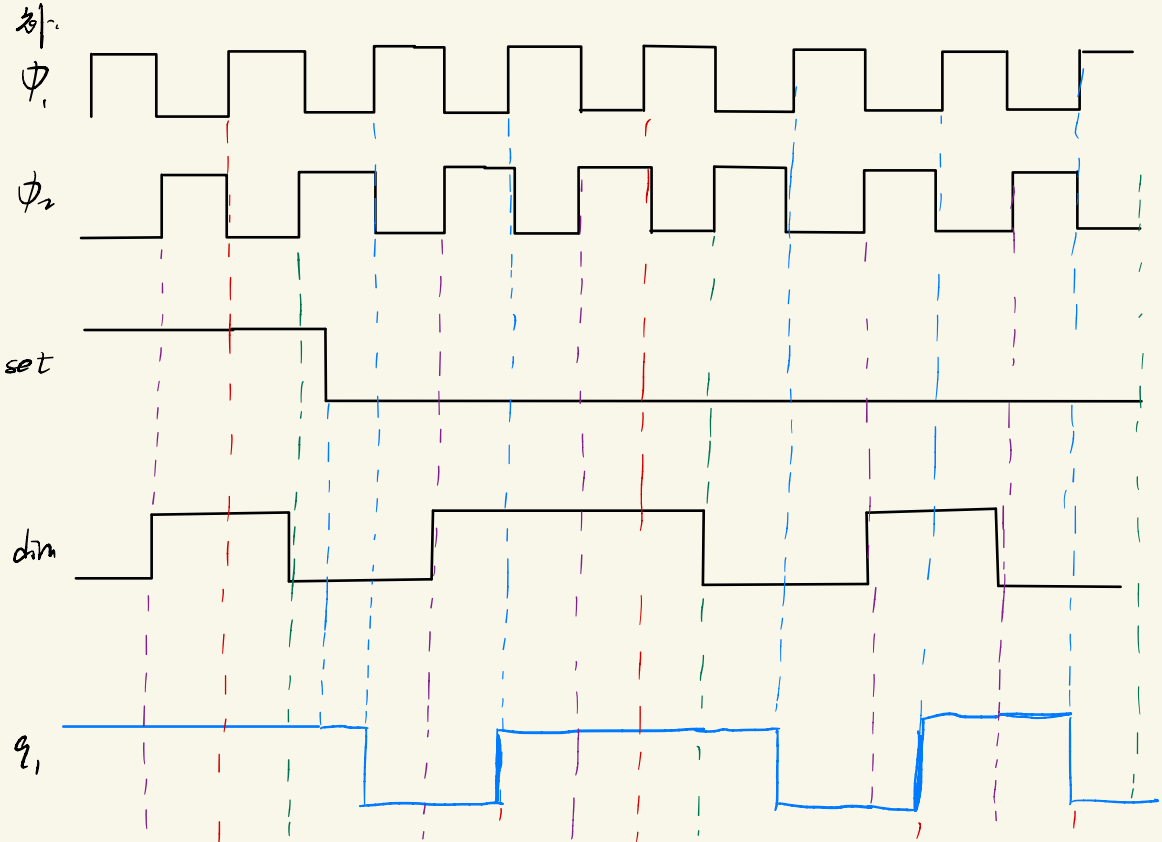
$x>0$时 $f(x)$ 减函数

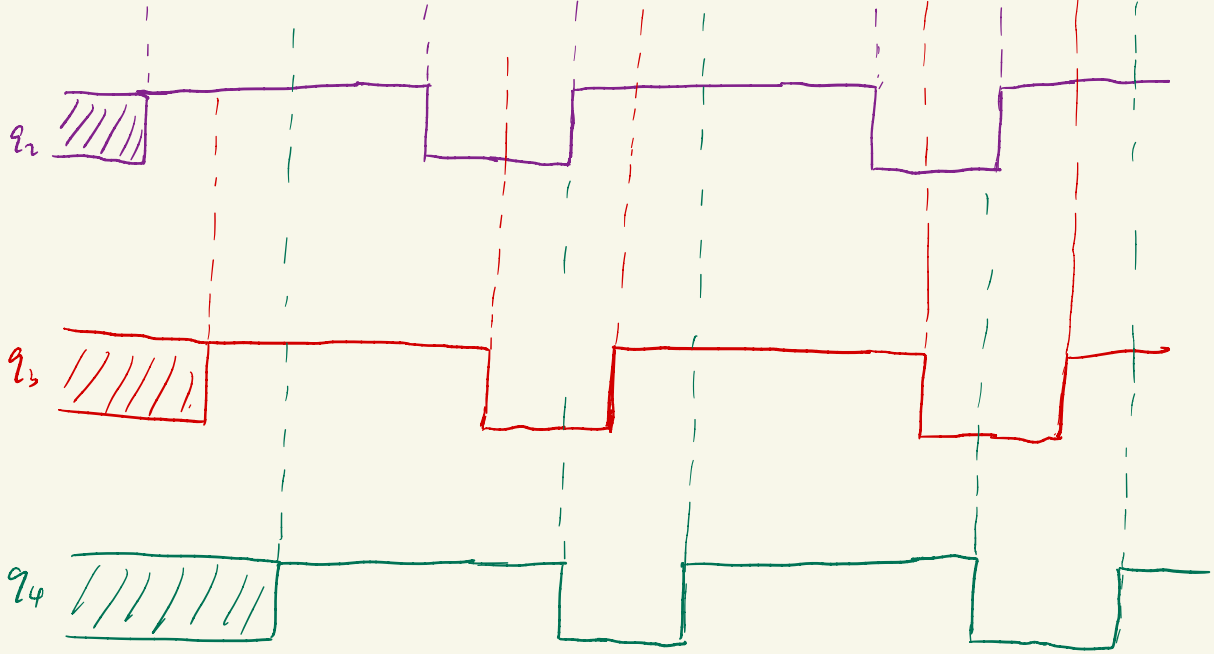
$$k_R \geq \left(\frac{0.3-V_T}{0.3+V_T}\right)^2_{max} \xrightarrow{V_T=0} 1$$

$k_R \leq 0$ （错误情况）

$k_R \geq 1$

$$\frac{k_n}{k_p} \geq 1$$




q_2
q_3
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