Wenhao Jia

Electrical Engineering, Princeton University
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Education	*Ph.D.*, Electrical Engineering, Princeton University	May 2014 (expected)
	M.A., Electrical Engineering, Princeton University	January 2011

- Thesis Summary: My thesis uses statistical analysis and design techniques to improve the usability of massively parallel systems such as GPUs.
- Thesis Advisors: Margaret Martonosi (Princeton) and Kelly A. Shaw (Richmond)

	B.S., Electrical Engineering, Tsinghua University	July 2008

- Thesis Title: A CMOS-based 2.4–5 GHz Linear Power Amplifier

Academic Honors	First-year Graduate Fellowship, Princeton University	2008
	Outstanding Graduate Award, Tsinghua University	2008
	First-class Overall Excellence Awards, Tsinghua University	2005 and 2006

Publications

MRPB: Memory Request Prioritization for Massively Parallel Processors
Wenhao Jia, Kelly A. Shaw, and Margaret Martonosi
The 20th International Symposium on High Performance Computer Architecture (HPCA 2014)

Starchart: Hardware and Software Optimization Using Recursive Partitioning Regression Trees
Wenhao Jia, Kelly A. Shaw, and Margaret Martonosi
The 22nd International Conference on Parallel Architectures and Compilation Techniques (PACT 2013)

Characterizing and Improving the Use of Demand-Fetched Caches in GPUs
Wenhao Jia, Kelly A. Shaw, and Margaret Martonosi
The 26th International Conference on Supercomputing (ICS 2012)

Stargazer: Automated Regression-Based GPU Design Space Exploration
Wenhao Jia, Kelly A. Shaw, and Margaret Martonosi
The 2012 International Symposium on Performance Analysis of Systems and Software (ISPASS 2012)

Experience

Research Assistant — Since 2009
Princeton University, Princeton, NJ

- My thesis work focuses on improving the programmability and performance of highly-parallel accelerators such as GPUs. In particular, my work has resulted in two released automated statistical tools—Starchart and Stargazer—which allow users to explore the GPU software and hardware design space in an efficient and systematic manner; real-system validation suggests these tools open up the possibility of using high-level statistical knowledge to guide future heterogeneous system design processes. In addition, I have also characterized and improved GPU caches, showing that adapting conventional microarchitectural components to suit GPU characteristics such as the massive thread count is crucial for improving their utility in future systems.

- My other work has dealt with writing LLVM compiler passes to estimate and speed up critical paths of multi-threaded CPU programs.

Software Engineering Intern   Summer 2011
Google Inc., Mountain View, CA
- Investigated how to use GCC to emit hardware-specific x86 assembly code for AMD and Intel CPUs to achieve platform-aware performance tuning.

Research Intern   Summer 2010
IBM T.J. Watson Research Center, Hawthorne, NY
- Parallelized and optimized a hierarchical tree-building algorithm using the X10 programming language in a distributed OpenMP-based environment.

Professional Activities

Reviewer
- International Symposium on High Performance Computer Architecture (HPCA)
- ACM Transactions on Architecture and Code Optimization (TACO)
- International Symposium on Microarchitecture (MICRO)

Submission Co-Chair   2013
- The 40th International Symposium on Computer Architecture (ISCA 2013)

Teaching Assistant   2009
- Computer Architecture, ELE/COS 475, Princeton University

Student Researcher
- Center for Future Architectures Research (C-FAR)
- Gigascale Systems Research Center (GSRC)
- Intel Science and Technology Center for Cloud Computing (ISTC-CC)

Student Member
- Association for Computing Machinery (ACM)
- Institute of Electrical and Electronics Engineers (IEEE)

Software Releases

Starchart
Statistical Tuning via Automatically- and Recursively-Constructed, Hierarchically-Applied Regression Trees
http://www.princeton.edu/~wjia/starchart

Stargazer
STAtistical Regression-based GPU Architecture analyZER
http://www.princeton.edu/~wjia/stargazer

Additional Skills

Programming in C/C++, Python, Java, R, MATLAB, CUDA, and OpenCL
Compiler development for LLVM and GCC
Experience with statistical regression analysis and machine learning techniques
Experience with VLSI and FPGA design tools