CSci 402 - Operating Systems

Final Exam (PM Section)

Spring 2020

(3:00pm - 3:40pm, Wednesday, May 13)

Instructor: Bill Cheng

Teaching Assistant: (N/A)

(This exam is closed book, closed notes, closed everything.
No "cheat sheet" allowed.
No calculators, cell phones, or any electronic gadgets.)

Time: 40 minutes

_____
Name (please print)

Total: 32 points

_____
Signature

Instructions

1. This is the first page of your exam. The previous page is a title page and does not have a page number. Please write and sign your name on this sheet *now*.
2. Read problem descriptions carefully. You may not receive any credit if you answer the wrong question. Furthermore, if a problem says *"in N words or less"*, use that as a hint that N words or less are expected in the answer (your answer can be longer if you want). Please note that points may get *deducted* if you put in wrong stuff in your answer.
3. If a question doesn't say `weenix`, please do not give `weenix`-specific answers.
4. Write answers to all problems on the exam itself. If you are taking the exam *remotely* and if you need additional space, please ask for additional sheets and only write on one side since they need to be fax'ed.
5. Show all work (if applicable). If you cannot finish a problem, your written work will help us to give you partial credit. We may not give full credit for answers only (i.e., for answers that do not show any work). Grading can only be based on what you wrote and cannot be based on what's on your mind when you wrote your answers.
6. Please do *not* just draw pictures to answer questions (unless you are specifically asked to draw pictures). Pictures will not be considered for grading unless they are clearly explained with words, equations, and/or formulas.
7. For problems that have multiple parts, please clearly *label* which part you are providing answers for.
8. Please ignore minor spelling and grammatical errors. They do not make an answer invalid or incorrect.
9. During the exam, please only ask questions to *clarify* problems. Questions such as "would it be okay if I answer it this way" will not be answered (unless it can be answered to the whole class). Also, you are suppose to know the definitions and abbreviations/acronyms of *all technical terms*. We cannot "clarify" them for you. We also will **not** answer any clarification-type question for multiple choice problems since that would often give answers away.
10. Unless otherwise specified and stated explicitly, multiple choice questions have one or more correct answers. You will get points for selecting correct ones and you will lose points for selecting wrong ones.
11. When we grade your exam, we must assume that you wrote what you meant and you meant what you wrote. So, please write your answers accordingly.

(Q1) (2 points) Which of the following statements are correct about the basic (two-level) virtual memory scheme where a virtual address is divided into a virtual page number (say 20 bits) and an offset (say 12 bits) on a 32-bit machine?

(1) during the lifetime of a user process, the mapping of virtual pages to physical pages stays the same
(2) a physical address is obtained by adding a physical page number with the 12-bit offset
(3) an entry in a page table contains a 20-bit physical page number no matter how much physical memory is present
(4) when performing a virtual to physical address translation, the least-significant 12-bits of the virtual address (i.e., the offset) must equal to the least-significant 12-bits of the translated address
(5) the virtual page number is just an index into a page table which has 2^{20} entries

Answer (just give numbers): 4,5 4,5是对的，slides 336页

(Q2) (2 points) Which of the following statements are correct about the **NOR** vs. **NAND** flash memory technologies?

(1) a NOR flash is not page-erasable but only block-erasable
(2) for a NOR flash, you can read/write individual bytes
(3) a NAND flash is page-addressable
(4) for a NAND flash, you can read/write individual bytes
(5) none of the above is correct

Answer (just give numbers): 2,3 2，3是对的，slides684页

(Q3) (2 points) Which of the following statements are correct about **undo journaling** and **redo journaling**?

(1) in redo journaling, you record "after images" in the log
(2) in undo journaling, you record "after images" in the log
(3) in redo journaling, you record "before images" in the log
(4) in undo journaling, you record "before images" in the log
(5) you record the same information into the log no matter if you are using undo journaling or redo journaling

Answer (just give numbers): 1,4 1，4是对的，slides617页

(Q4) (2 points) Which of the following statements are correct about using the **multi-level feedback queue** to schedule both interactive and non-interactive jobs?

(1) if a thread blocks before using up a full time slice, you should try to decrease its priority
(2) if a thread uses a full time slice, you should try to increase its priority
(3) if a thread blocks before using up a full time slice, you should try to increase its priority
(4) if a thread uses a full time slice, you should try to decrease its priority
(5) none of the above is correct

Answer (just give numbers): 4 4是对的，slides846页

(Q5) (2 points) Which of the following statements are correct about using **base and bounds** registers in a **segmented virtual memory** scheme?

(1) the base and bounds scheme can be extended to provide the ability to map an entire file or part of it into a memory segment
(2) the base and bounds scheme can be extended to provide backing-store for memory segments
(3) the base and bounds scheme can be extended to provide read-only vs. read-write access control for memory segments
(4) the base and bounds scheme can be extended to provide copy-on-write for memory segments
(5) none of the above is correct

Answer (just give numbers): 2,3,4 1，2，3，4都是对的，307页开始都有讲到

(Q6) (2 points) Which of the following statements are correct about using the **aging** mechanism for a **multi-level feedback queue**?

(1) aging is not necessary since threads can never starve if you use a multi-level feedback queue
(2) aging is a way to improve throughput for a multi-level feedback queue
(3) aging is a way to solve the starvation problem for a multi-level feedback queue
(4) if aging is used, the scheduler may increase a thread's priority if the thread has not run for a long time
(5) none of the above is correct

3，4是对的，846页

Answer (just give numbers): 3,4

(Q7) (2 points) Which of the following statements are correct about **linear page tables**?

(1) to translate a virtual address to a physical address in a linear page table requires the use of two page tables
(2) in a linear page table scheme, all page table entries in all page tables contains a virtual page number
(3) in a linear page table scheme, all page table entries in all page tables contains a physical page number
(4) in a linear page table scheme, a page table entry may contain a virtual page number while another page table entry may contain a physical page number
(5) none of the above is correct

Answer (just give numbers): 1, 4 1，4应该是对的，slides没有，在lecture19part2种里曰头讲了

(Q8) (2 points) Let's say that you have three threads A, B, and C and you are using **stride scheduling**. You have decided to give thread A 2 tickets, thread B 3 tickets, and thread C 4 ticket. The initial pass values that **you must used** for the three threads are shown below along with the "winner" of the iteration 1. Please fill out all the entries (pass values) in the table. For **iterations 2 through 5**, please write on your answer sheet the "winner" and the winning pass value of that iteration. (For example, you would write "B:2" for iteration 1 since B is the "winner" and the winning pass value is 2.) You must use the **smallest possible integer stride values** when calculating the pass values. Please note that if you get the stride values wrong, you will not get any partial credit for this problem.

itr	A	B	C
1	5	2	4
2	5	6	4
3	5	6	7
4	11	6	7
5	11	10	7

A 2 : 6
B 3 : 4
C 4 : 3

这个答案全对，
第一步：根据ticket求出stride，A：6，B：4，C：3

```
stride = 1 / ticket
```

第二步：每轮pass值里最小的胜出，pass = pass + stride，输了的pass值不变。
第三步：比较更新后的pass值。
如此循环。

(Q9) (2 points) Let's say that you have three threads A, B, and C and you are using the basic **round-robin (RR) / time-slicing** scheduler with a very small time slice. At time zero, all three threads are in the run queue and their processing times are shown in the table below. Assuming that there are no future arrivals into the run queue, please complete the table below with the "waiting time" of all three threads and the "average waiting time" (AWT) of these three threads and write the results on your answer sheet. Please make it very clear which waiting time is for which thread and which one is the AWT. For non-integer answers, you can use fractions or decimals with two digits after the decimal point. Your answer must not contain plus or multiplication symbols. You must use the definition of "waiting time" given in lectures.

	A	B	C	AWT
T (hrs)	2	7	6	-
wt (hrs)	6	15	14	11.67

答案全对
按照ABC的耗时由小到大排列计算顺序
A<C<B
WTa = 3 x 2 = 6
WTc = 2 x (6-2) + 6 = 14
WTb = 1 x (7-6) + 14 = 15
AWT = (6 + 14 + 15)/ 3 = 11.67

(Q10) (2 points) Which of the following statements are correct about **physical vs. virtual addresses** on a 32-bit machine?

(1) a user process uses physical addresses for code when it's running in the kernel and uses virtual addresses when it's running in user space
(2) a device driver uses physical addresses for both code and data
(3) a system call can be used for a user process to convert a virtual address to physical address
(4) a kernel process uses physical addresses for code when it is created and switch to use virtual addresses when it's running for the first time
(5) none of the above is correct

5是对的，slides296页

Answer (just give numbers): 5

(Q11) (2 points) Which of the following are useful approaches to **reduce page fault latency**?

(1) use a pageout daemon
(2) use a FIFO replacement policy
(3) prefetching
(4) use a larger translation lookaside buffer
(5) lazy evaluation

Answer (just give numbers): 1, 3

1，3是对的，slides410页

(Q12) (2 points) Which of the following statements are correct about the **free block list** in **S5FS**?

(1) the head and tail of the free block list in S5FS is stored in the superblock
(2) it is organized into a hash table
(3) it is organized into a doubly-linked list
(4) each node in the free block list in S5FS can contain up to 99 disk block pointers
(5) none of the above is correct

5应该是对的，265页

Answer (just give numbers): 5,

(Q13) (2 points) Which of the following statements are correct about **scheduling**?

(1) in a **multi-processor** system, **cache affinity** means that after a thread has run on a particular processor, it's beneficial to schedule it on the same processor next time it runs
(2) rate-monotonic scheduling can be used to schedule non-periodic jobs
(3) in a hard real-time system, a rate-monotonic scheduler usually performs better (i.e., schedule more jobs) than a EDF (earliest deadline first) scheduler
(4) priority inversion is not possible if all you have are kernel threads
(5) in a **multi-processor** system, to take advantage of **cache affinity**, it's better to use **one shared queue** for multiple processors because you won't have to **load balance**

1是对的，931页

Answer (just give numbers): 1,

(Q14) (2 points) Considering only **clustered hash page table** schemes and **(non-clustered) hashed page table** schemes, which of the following statements are correct?

(1) the performance of non-clustered hash page tables depends on the lengths of the hash conflict/collision resolution chains
(2) the performance of clustered hash page tables is independent of how address space is allocated
(3) clustered hash page tables would perform better if address space is truly sparsely allocated
(4) non-clustered hash page tables would perform better if contiguous virtual pages are used (such as in weenix)
(5) none of the above is correct

1，2是对的，362页

Answer (just give numbers): 1, 2,

(Q15) (2 points) Which of the following statements are correct for a **forward-mapped (multilevel) page tables** where a 32-bit virtual address is divided into a 10-bit page directory number, a 10-bit page table number, and a 12-bit offset (such as an x86 processor)?

(1) a multilevel page table scheme is preferred over the basic (two-level) page table scheme because address translation is faster
(2) the basic (two-level) page table scheme is more space efficient than the multilevel page table scheme
(3) at least two entries in a page directory table must be valid, even in weenix
(4) a page directory table is the same size as a page table
(5) a page directory table is the same size as a physical memory page

Answer (just give numbers): 3,4 这题不会

4

(Q16) (2 points) Which of the following statements are correct about using **base and bounds** registers in a **segmented virtual memory** scheme?

(1) the bounds register contains a virtual address
(2) the bounds register contains a physical address
(3) the base register contains a virtual address
(4) the base register contains a physical address
(5) none of the above is correct

Answer (just give numbers): 3, 应该选4吧，307页