JIA YU LAW

FPGA Engineer

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EXPERIENCE

Graduate Trainee, FPGA IP Software Development Engineer

Altera

Aug 2023 – Present Penang, Malaysia

- Familiar with basic FPGA development workflow such as simulation, compilation, timing analysis, hardware deployment, linting, and CDC.
- Designed appropriate IP GUI callback and information display in Quartus for better IP usability.
- Involved in the development of eCPRI & O-RAN IP design examples for Agilex 5 device family.
- Developed IP features through RTL integration.
- Maintained regression tests for IPs (simulation, compilation, timing analysis, IP upgrade, etc.).
- Authored and maintained technical documentation for knowledge transfer.
- Work with architect & microarchitect in problem solving and discussing IP architecture for next-generation device family.
- Work with DV team in bringing up functional verification through the UVM infrastructure.
- Work with the development tools team and hardware team to improve productivity and debug hardware issues.
- Provided support to customers in resolving technical issues.

Freelance Web developer

Jun 2022 – Sep 2022

- Mainly contributed as the only web developer in the development of an IoT fruit fall detection and notification system prototype. Developed and deployed a web-based user dashboard webpage which interfaces with SQL database at the backend. Also deployed a chatbot in the backend that notifies user for status update.

Industrial Trainee

Keysight Technologies

Jun 2021 – Sep 2021 Penang, Malaysia

- Development of a test automation library and proof-of-concept based on Eggplant Test Automation Tool for Keysight IoT device regulatory testing software. The library is written based on optical character recognition (OCR) and image recognition.

CERTIFICATIONS

- Advanced Verilog HDL Design Techniques by DreamCatcher Consulting
- Datapath Design by DreamCatcher Consulting
- Verilog HDL Advanced Course Completion by Intel
- Signal Tap for Intel® FPGAs Course Completion by Intel
- Graduate Engineer by Board of Engineers Malaysia (BEM)

FUN FACT

The only career experience I have in common with Jensen Huang is probably that I was a dishwasher.

SKILLS

Xilinx ISE | Altera Quartus | Verilog | VHDL | TCL scripting | PERL | Microsoft Visio | Documentation | MATLAB | Python | GitHub | Perforce | Regular expressions | IP-XACT | Raspberry Pi | HTML | CSS | JavaScript | Bootstrap | SQL | LTspice | Arduino | C/C++ | LATEX | Adobe Illustrator

EDUCATION

MEng (Hons) in Electrical and Electronic Engineering

University of Nottingham Malaysia (UNM)

2019 – 2023 Selangor, Malaysia

- Dean's Excellence Scholarship Award, 2020, 2021, 2022
- Graduated in the First Class.
- Relevant modules: HDL for Programmable Logic with Project, VLSI Design, Digital Communications, Digital Signal Processing, Advanced Control System Design, Power Networks, Power Electronic Applications and Control, Analogue Electronics, Electrical Machines, Drive Systems and Applications, Fields, Waves and Antennas, Advanced Engineering Mathematics

Foundation in Engineering

University of Nottingham Malaysia (UNM)

2018 – 2019 Selangor, Malaysia

- Dean's Excellence Scholarship Award, 2019

Malaysian Certificate of Education (SPM)

SMK Tengku Mahkota

2013 – 2017