

# User Manual

## Embedded Tegra K1 processor module



© 2015 Avionic Design GmbH  
All rights reserved

## Product information

Product: Embedded Tegra K1 processor module  
Product number: 1477-110-000  
Manufacturer: Avionic Design GmbH  
Wragekamp 10  
22397 Hamburg  
In cooperation with: NVIDIA®  
Year: 2014

## Revision history

Document number	Date	Version	Remarks
1477-011-315-01	23.06.2015	01	first release
1477-011-315-00	26.01.2015	00	Preliminary release

## Copyright

All the rights to this manual provided through this service revert to AVIONIC DESIGN GmbH.  
Any and all reproduction, modification, or publication of the guides and/or manuals either in part or their entirety without the permission of AVIONIC DESIGN GmbH is prohibited under copyright laws.

NVIDIA, the NVIDIA logo and TEGRA are trademarks and/or registered trademarks of NVIDIA Corporation.

Other company and product names may be trademarks of the respective companies with which they are associated.

The Embedded Tegra K1 products are subject to change. Please check [www.avionic-design.de](http://www.avionic-design.de) for updates.

## 1 Document Change History

Table 1: Document Change History

Version	Date	Description
Rev01	23.06.2015	<p><b>Meerkat Rev02 changes:</b></p> <ul style="list-style-type: none"> <li>• Define X5:10 as W_Disable</li> <li>• Change the VDDIO_GMI and VDDIO_BB voltage from 3.3V to 1.8V (like on Jetson). The level of the following pins are affected: <ul style="list-style-type: none"> <li>– X4:2 (GPIO_PK3)</li> <li>– X4:2 (GPIO_PK3)</li> <li>– X4:3 (GPIO_PK1)</li> <li>– X4:4 (GPIO_PI5)</li> <li>– X4:5 (GPIO_PI7)</li> <li>– X4:6 (GPIO_PH6)</li> <li>– X4:7 (GPIO_PH5)</li> <li>– X4:8 (GPIO_PK2)</li> <li>– X4:9 (BL_EN)</li> <li>– X4:10 (GPIO_PJ0)</li> <li>– X4:11 (BL_PWM)</li> <li>– X4:12 (FAN_PWM)</li> <li>– X4:14 (GPIO_PK0)</li> <li>– X4:18 (SPI4C_nCS1)</li> <li>– X4:20 (GPIO_PH3)</li> <li>– X4:22 (GPIO_PK4)</li> <li>– X4:24 (GPIO_PI2)</li> <li>– X4:35 (UART4_DEBUG_nCTS)</li> <li>– X4:36 (GPIO_PJ2)</li> <li>– X4:37 (UART4_DEBUG_TXD)</li> <li>– X4:39 (UART4_DEBUG_nRTS)</li> <li>– X4:41 (UART4_DEBUG_RXD)</li> <li>– X4:43 (GEN2_I2C_nIRQ)</li> <li>– X4:52 (HDMI_VDD_EN)</li> <li>– X5:10 (W_DISABLE)</li> <li>– X5:13 (GPIO_PO1)</li> <li>– X5:18 (GPIO_PP2)</li> <li>– X5:19 (GPIO_PO2)</li> <li>– X5:21 (SPI1A_nIRQ)</li> <li>– X5:23 (GPIO_PO3)</li> <li>– X5:27 (GPIO_PO4)</li> <li>– X5:45 (SPI1A_MISO)</li> <li>– X5:47 (SPI1A_nCS0)</li> <li>– X5:49 (SPI1A_SCK)</li> <li>– X5:51 (SPI1A_MOSI)</li> <li>– X5:53 (SPI4C_nCS0)</li> <li>– X5:55 (SPI4C_MOSI)</li> <li>– X5:57 (SPI4C_MISO)</li> <li>– X5:59 (SPI4C_SCK)</li> </ul> </li> <li>• Add possible PCIe configurations</li> <li>• Define default PCIe configuration</li> <li>• Define GEN2 as default mini PCIe socket I2C bus</li> </ul>

Version	Date	Description
		<ul style="list-style-type: none"><li>• PCB Changes for Meerkat Rev02:<ul style="list-style-type: none"><li>– add nWAKEUP_POWER pull-up (100k)</li><li>– add WAKEUP_LID pull-down (10k)</li><li>– add pull-down resistor for JTAG_TCK (100k)</li><li>– use LDO4 of the PMIC for AVDD_LVDS_PLL to support LVDS and eDP</li><li>– replace OWR with GPIO_PP0 (OWR is not supported by NVIDIA)</li><li>– add X3:42 GPIO_PBB4</li><li>– update the pinmux table (reference is the customer pinmux table from the Jetson reference board)</li></ul></li><li>• NVIDIA does not officially support SPI2D and SPI3C</li></ul>
Rev00	26.01.2015	Draft release (Initial Release)

# Contents

<b>1 Document Change History</b>	<b>2</b>
<b>2 Introduction</b>	<b>9</b>
2.1 Purpose of this manual . . . . .	9
2.2 Designated use of the COM . . . . .	9
<b>3 Properties of the COM</b>	<b>10</b>
3.1 Structure of the COM . . . . .	10
3.1.1 General overview . . . . .	10
3.1.2 Function block diagram . . . . .	12
3.2 Mechanical properties of the COM . . . . .	12
3.3 Operation parameters . . . . .	14
3.4 Power management of the COM . . . . .	15
3.4.1 Power sequence . . . . .	15
<b>4 Interfaces of the COM</b>	<b>16</b>
4.1 Tegra® K1 processor module special functions . . . . .	16
4.1.1 Signal descriptions . . . . .	17
4.2 DAP (I <sup>2</sup> S) . . . . .	18
4.2.1 Signals . . . . .	19
4.2.2 Example schematic . . . . .	20
4.2.3 Necessary layout properties . . . . .	20
4.3 eDP . . . . .	21
4.3.1 Signals . . . . .	21
4.3.2 Example schematic . . . . .	22
4.3.3 Necessary layout properties . . . . .	22
4.4 GPIO . . . . .	23
4.4.1 Signals . . . . .	23
4.4.2 Example schematic . . . . .	24
4.4.3 Necessary layout properties . . . . .	24
4.5 HDMI . . . . .	25
4.5.1 Signals . . . . .	25
4.5.2 Example schematic . . . . .	26
4.5.3 Necessary layout properties . . . . .	26
4.6 I <sup>2</sup> C . . . . .	27
4.6.1 Signals . . . . .	28
4.6.2 Example schematic . . . . .	28
4.6.3 Necessary layout properties . . . . .	28
4.7 JTAG . . . . .	29
4.7.1 Signals . . . . .	29
4.7.2 Example schematic . . . . .	29
4.7.3 Necessary layout properties . . . . .	29
4.8 MIPI CSI . . . . .	29
4.8.1 Signals . . . . .	30
4.8.2 Example schematic . . . . .	31
4.8.3 Necessary layout properties . . . . .	31
4.9 MIPI DSI . . . . .	32
4.9.1 Signals . . . . .	33
4.9.2 Example schematic . . . . .	33
4.9.3 Necessary layout properties . . . . .	33

4.10 PCIe . . . . .	35
4.10.1 Signals . . . . .	35
4.10.2 Example schematic . . . . .	37
4.10.3 Necessary layout properties . . . . .	37
4.11 SATA . . . . .	38
4.11.1 Signals . . . . .	39
4.11.2 Example schematic . . . . .	39
4.11.3 Necessary layout properties . . . . .	40
4.12 SD/MMC (SDIO) . . . . .	40
4.12.1 Signals . . . . .	41
4.12.2 Example schematic . . . . .	42
4.12.3 Necessary layout properties . . . . .	42
4.13 S/PDIF . . . . .	43
4.13.1 Signals . . . . .	44
4.13.2 Example schematic . . . . .	44
4.13.3 Necessary layout properties . . . . .	44
4.14 SPI . . . . .	44
4.14.1 Signals . . . . .	45
4.14.2 Example schematic . . . . .	46
4.14.3 Necessary layout properties . . . . .	46
4.15 UART . . . . .	46
4.15.1 Signals . . . . .	47
4.15.2 Example schematic . . . . .	47
4.15.3 Necessary layout properties . . . . .	47
4.16 USB (HSIC) . . . . .	48
4.16.1 Signals . . . . .	49
4.16.2 Example schematic . . . . .	50
4.16.3 Necessary layout properties . . . . .	50
<b>5 Software</b> . . . . .	<b>53</b>
5.1 BCT . . . . .	53
5.2 Bootloader . . . . .	53
5.3 Using tegra-u-boot-flasher-scripts . . . . .	53
5.3.1 Build cross-compiling toolchain . . . . .	54
5.3.2 Checkout required sources and utilities . . . . .	54
5.3.3 Build required utilities . . . . .	55
5.3.4 Build u-boot . . . . .	55
5.3.5 Flash u-boot to System . . . . .	55
<b>6 Pinout List</b> . . . . .	<b>56</b>
6.1 Connector overview . . . . .	56
6.2 Connector pinout and pin-muxing . . . . .	56
<b>7 Reference documents</b> . . . . .	<b>72</b>
<b>8 Contact</b> . . . . .	<b>73</b>

## List of Figures

3.1	Top view of the Tegra® K1 processor module . . . . .	11
3.2	Function block diagram of the COM . . . . .	12
3.3	Mechanical properties of the COM (top view) . . . . .	13
3.4	Mechanical properties of the COM (bottom view) . . . . .	13
3.5	Mechanical properties of the COM (heatsink mounting points) . . . . .	13
3.6	Power sequence . . . . .	16
4.1	DAP2 schematic example . . . . .	20
4.2	HDMI schematic example . . . . .	26
4.3	PCI Express schematic example . . . . .	37
4.4	Mini PCI Express socket schematic example . . . . .	37
4.5	SDMMC schematic example . . . . .	42
4.6	USB Client schematic example . . . . .	50
8.1	head office in Duvenstedt (Germany) . . . . .	73

## List of Tables

1	Document Change History . . . . .	2
2	Mechanical properties of the COM . . . . .	14
3	Absolute maximum operation conditions . . . . .	14
4	Recommended operation conditions . . . . .	15
5	Meerkat special functions . . . . .	16
6	DAP2 signals . . . . .	19
7	DAP4 signals . . . . .	19
8	DAP/I2S interface signal routing requirements . . . . .	20
9	DAP/I2S interface delays . . . . .	21
10	embedded DisplayPort (eDP) signals . . . . .	21
11	eDP (HBR2) main link signal routing requirements . . . . .	22
12	eDP (LVDS) interface delays . . . . .	23
13	1.8V GPIOs signals . . . . .	23
14	3.3V GPIOs signals . . . . .	24
15	HDMI signals . . . . .	25
16	HDMI interface signal routing requirements . . . . .	26
17	HDMI interface delays . . . . .	27
18	I <sup>2</sup> C bus-number assignment . . . . .	27
19	I <sup>2</sup> C GEN1 (1V8) signals . . . . .	28
20	I <sup>2</sup> C GEN2 (3V3) signals . . . . .	28
21	I <sup>2</sup> C CAM (1V8) signals . . . . .	28
22	HDMI DDC signals . . . . .	28
24	MIPI CSI signals . . . . .	30
25	CSI interface signal routing requirements . . . . .	31
26	CSI interface delays . . . . .	31
27	MIPI DSI signals . . . . .	33
28	DSI interface signal routing requirements . . . . .	34
29	DSI interface delays . . . . .	34
30	Possible PCIe Configurations . . . . .	35
31	PCIe: Clock and control signal mapping . . . . .	35
32	PCIe signals . . . . .	35
33	PCIe interface signal routing requirements . . . . .	37
34	PCIe interface delays . . . . .	38
35	SATA signals . . . . .	39
36	SATA interface signal routing requirements . . . . .	40
37	PCIe interface delays . . . . .	40
38	SDMMC1 (SDIO) signals . . . . .	41
39	SDMMC3 signals . . . . .	41
40	SDMMC3/1 interface signal routing requirements . . . . .	42
41	SDMMC3/1 interface delays . . . . .	43
42	S/PDIF signals . . . . .	44
43	SPI1A signals (1.8V level) . . . . .	45
44	SPI2D signals (1.8V level) . . . . .	45
45	SPI3E signals (1.8V level) . . . . .	45
46	SPI4C signals (1.8V level) . . . . .	45
47	UART1 signals (1.8V level) . . . . .	47
48	UART2 signals (1.8V level) . . . . .	47
49	UART3 signals (1.8V level) . . . . .	47
50	UART4 (DEBUG) signals (1.8V level) . . . . .	47
51	USB signals . . . . .	49

52	USB 2.0 interface signal routing requirements . . . . .	50
53	USB 3.0 interface signal routing requirements . . . . .	51
54	USB 2.0 interface delays . . . . .	52

## 2 Introduction

Tegra® K1 processor module is a platform by Avionic Design that is based on NVIDIA® Tegra® K1 technology. It defines the form factor, the pinout and the function set.

Please read all the information in this manual carefully!

If you have any questions about the Tegra® K1 processor module, please contact Avionic Design.

### 2.1 Purpose of this manual

This manual will give you information about the abilities and the interfaces of the Tegra® K1 processor module (COM). You will read about the production parameters and the operating conditions of the Tegra® K1 processor module so you will be able to operate it safely. This manual will enable you to develop a carrier that obeys the COM parameters.

This document includes an overview of the Tegra® K1 processor module, its main components and the pinout of the board connectors. You will also get information about the power management of the Tegra® K1 processor module.

You will read about the interfaces of the Tegra® K1 processor module and the properties of those interfaces.

### 2.2 Designated use of the COM

The Tegra® K1 processor module is a multimedia platform for embedded, avionic and industrial operation. Its core component is the NVIDIA® Tegra® K1 processor.

The COM supports various interfaces, like DSI, CSI, eDP, USB3.0, SATA (GEN2) and HDMI.

### 3 Properties of the COM

This chapter will give you information about the different properties of the Tegra® K1 processor module, as well as its compliance requirements and operating parameters.

#### 3.1 Structure of the COM

In this section you will receive an overview of the Tegra® K1 processor module and its main components.

##### 3.1.1 General overview

The Tegra® K1 processor module is a multimedia platform for embedded, avionic and industrial operation. It has a very high graphic performance but it consumes little power (see Section 2.6). The hardware of the Processor Module has a NVIDIA® Tegra® K1 SoC as its core component.

**The main properties of the CPU are:**

- NVIDIA® Tegra® K1 quad core:
  - ARM® Cortex™-A15 “r3” with NVIDIA 4-Plus-1™
  - FPU: ARM® NEON™
  - L1 cache:
    - \* 32 KB instruction cache for each core
    - \* 32 KB data cache for each core
  - L2 cache: 2 MB shared by all cores
  - Operation frequency: up to 2.2 GHz

**The properties of the COM memory are:**

- 2GB DDR3L (64 Bit)
- 16 GB eMMC (eMMC5.0)

**The Tegra® K1 Processor Module has a larger number of GPIOs and interfaces:**

- 2 GB DDR3
- eMMC 16 GB (eMMC5.0)
- up to 2 x4 MIPI CSI
- up to 2 x4 MIPI DSI
- 1x eDP
- up to 5 PCIe lanes

- 2x standard USB 2.0 hosts
- 1x HSIC (shared with USB1)
- 1x standard USB 2.0 client (configurable as host)
- up to 2x USB 3.0 hosts
- 1x standard SATA
- 1x standard SDMMC (4 bit)
- 1x standard SDMMC/SDIO (4 bit)
- 2x DAP (I2S/PCM)
- 1x Debug UART
- 3x UART
- 2x standard I2C (1x 3.3 V and 1x 1.8 V)
- 4x SPI
- 8x 1.8V GPIOs
- 22x 3.3V GPIOs
- 1x JTAG
- 1x S/PDIF In/Out
- 1x standard HDMI 1.4b

The following figure will give you an overview of the Tegra® K1 Processor Module and its components

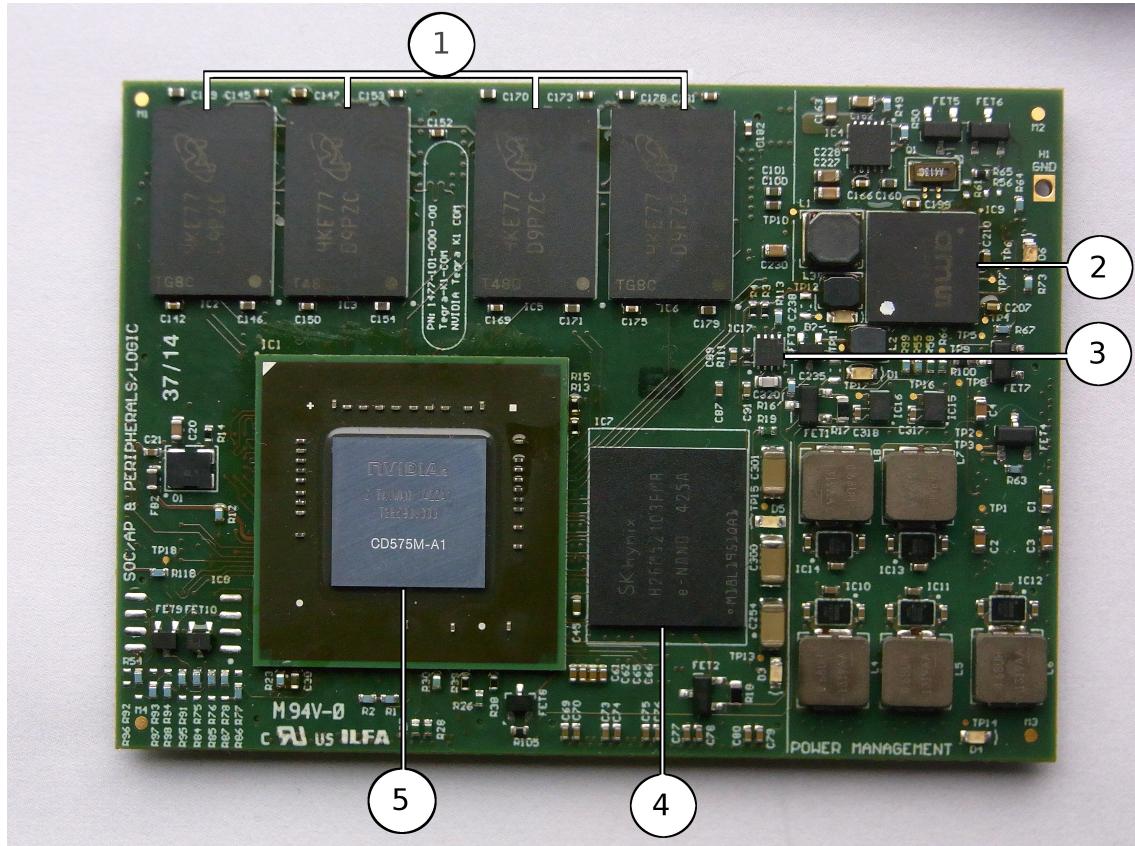


Figure 3.1: Top view of the Tegra® K1 processor module

Explanation to :

1. DDR3L
2. PMU
3. Temperature sensor
4. eMMC
5. NVIDIA® Tegra® K1 SoC

### 3.1.2 Function block diagram

Below you can find a function block diagram of the Tegra® K1 processor module.

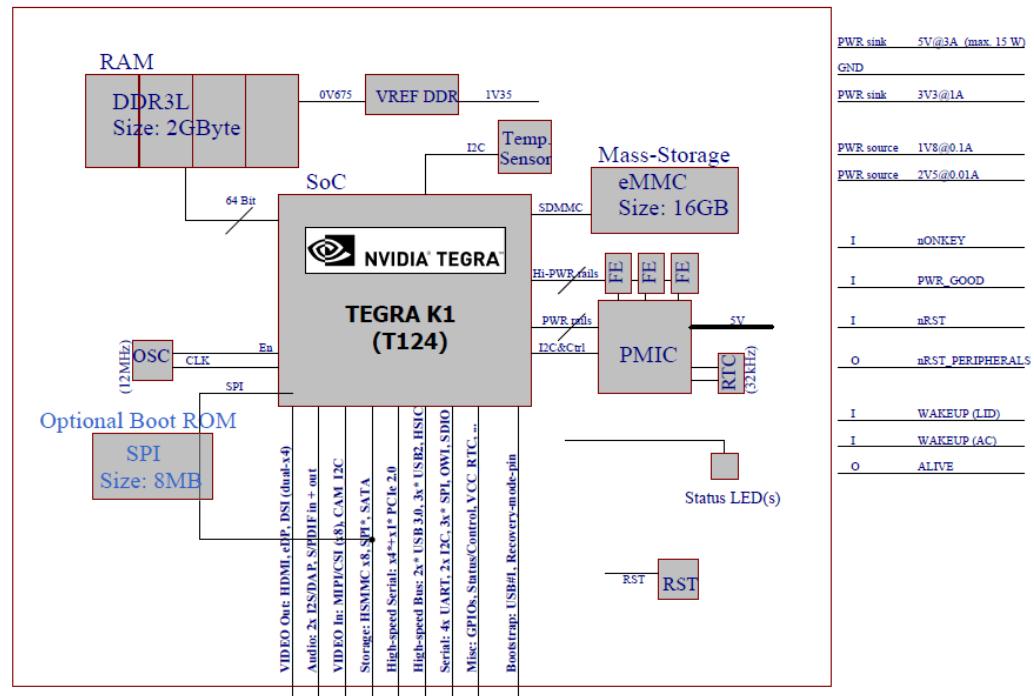


Figure 3.2: Function block diagram of the COM

### 3.2 Mechanical properties of the COM

In this section you can find information about the mechanical properties of the Tegra® K1 processor module. The diagram below shows the general layout of the processor board.

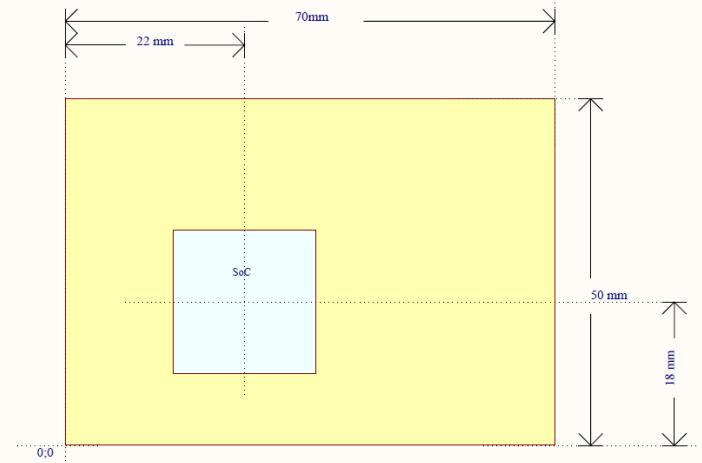


Figure 3.3: Mechanical properties of the COM (top view)

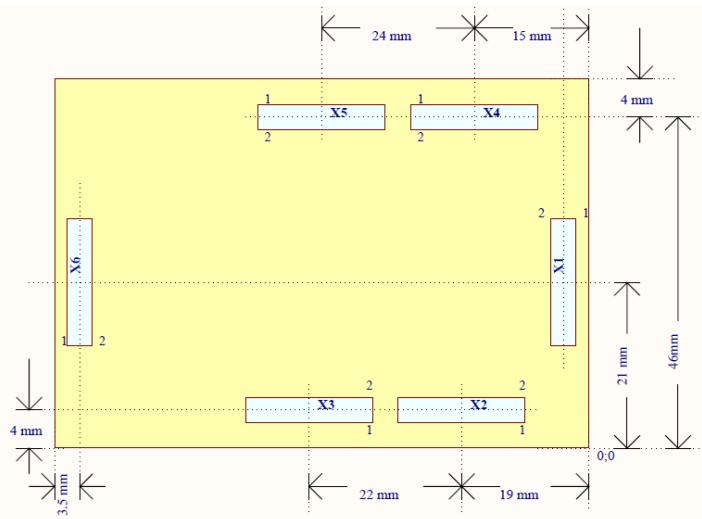


Figure 3.4: Mechanical properties of the COM (bottom view)

Hole Positions and Exemplary Cooling (from Top):

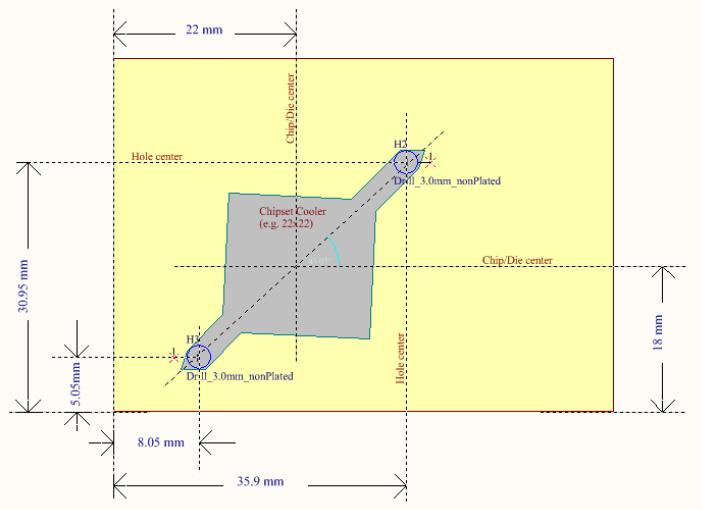


Figure 3.5: Mechanical properties of the COM (heatsink mounting points)

In the table below you can find a list of the mechanical properties of the Tegra® K1 processor module:

Table 2: Mechanical properties of the COM

Parameter	Properties
Size of the COM	70 x 50 mm
Size of the NVIDIA® Tegra™ 3 SoC	23 x 23 mm
Total PCB height	5.70 mm
Maximum stacking height (top)	2 mm
Maximum stacking height (bottom)	2.3
Weight	18 g
connector type	DF12(3.0)-60DP-0.5V(86)
Total pin count	360

### 3.3 Operation parameters

In this section you can find a list of the maximum operation conditions for the Tegra® K1 processor module. The module can operate under those conditions for a short time. If these operation conditions continue for an extended time, they could damage the module. You can find recommended operation conditions in Table 4.

**Please note:**

- Stress above the ranges listed in Table 3 can permanently damage the Tegra® K1 processor module!
- Operate the Tegra® K1 processor module only under the recommended operation conditions (see Table 4)!

Absolute maximum operation conditions:

Table 3: Absolute maximum operation conditions

Parameter	Explanation	Min	Max	Unit
Vmax +3V3_SYS	Main 3.3 V power supply	-0.5 V	3.63	V
Vmax +5V_SYS	Main 5 V power supply	-0.5	7.0	V
Vmax VBAT_BKUP	RTC backup battery voltage	0 V	5	V
Vmax PIN	Voltage applied to powered I/O pins	-0.5	3.63	V
Vmax USB_VBUS	USB supply voltage	-0.5 V	6.0 enabled (0.5 not enabled)	V
Operating temperature	Measured by a thermal diode	-25	105	°C
Storage temperature	-	-40	125	°C
Storage humidity	Relative humidity; in a sealed bag	-	less than 90	%

In the next table you will find the recommended operation parameters. It is safe to operate the module under these conditions.

Recommended operation conditions:

Table 4: Recommended operation conditions

Parameter	Explanation	Typical	Unit
+3V3_SYS	Main 3.3 V power supply	3.3	V
+5V_SYS	Main 5 V power supply	5	V
Vmax_PIN	Voltage applied to powered I/O pins	3.3 or 1.8	V
VBAT_BKUP	RTC backup battery voltage	3 (max 3.6)	V
USB_VBUS	USB supply voltage	5	V
Power dissipation	-	TBD	W
Operating temperature	Measured by a thermal diode	TBD	°C

## 3.4 Power management of the COM

The Tegra® K1 processor module has efficient solutions for the power management. The power-up process of the module is specified and it is necessary for the carrier board to follow these specifications so the module can power-up correctly.

### 3.4.1 Power sequence

To start the power sequence of the Tegra® K1 processor module the carrier board has to supply the +5V\_SYS and +3V3\_SYS. If both voltage are "Okay" the nPOWER\_GOOD must pulled low (pull-up agains +5V\_SYS are on the SoM). The Tegra® K1 can started by pull low the nONKEY (Power Button: pull-up on the SoM agains 2V5\_AON\_RTC) or by pull low WAKEUP\_nPOWER. After a fix delay the Tegra will release the nRESET\_PERIPH signal, this indicates that the power for the external periphery can be powered (see power sequencing). It is **necessary** that the external periphery is not powered before the nRESET\_PERIPH signal will be released. Otherwise the Tegra® K1 can be back-driven, which will produce unwanted behaviors. To autoboot the SoM see section 4.1.1. It is not necessary which power (+5V\_SYS or +3V3\_SYS) will be powered first. The best is that both voltages will powered at the same time.

After the power sequence is complete, the boot ROM passes control to the system-dependent software.

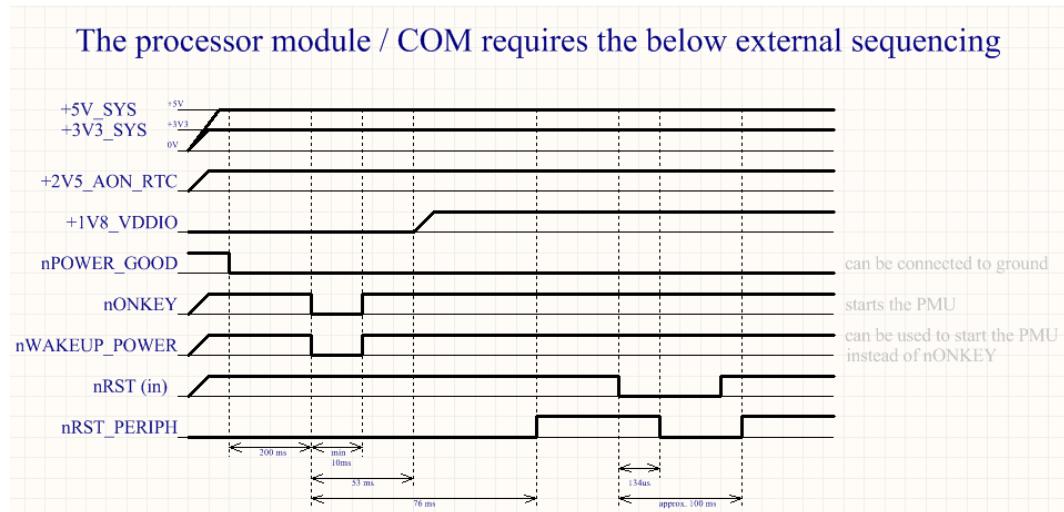


Figure 3.6: Power sequence

## 4 Interfaces of the COM

In this chapter you will find information that will help you develop a carrier board for the Tegra® K1 processor module. The COM has a larger number of interfaces and some of these have specified layout properties. When you develop your own carrier, you need to obey these properties.

This chapter will give you examples of schematics for the interfaces and it will list the signals of the interfaces.

**Please note:**

- Read all the information in this chapter carefully, when you develop a carrier board!
- If you have any questions on how to develop your own carrier board, please contact Avionic Design.

### 4.1 Tegra® K1 processor module special functions

Table 5: Meerkat special functions

Signal	Pin	Description	I/O	Comment
+2V5_AON_RTC	X6:26	Pull-up voltage	P	
USB0_ID_PMU	X6:33	TBD	I	
+1V8_VDDIO	X6:35	+1.8V power source	P	
+1V8_VDDIO	X6:36	+1.8V power source	P	
nRESET_COM	X6:37	SoM reset signal	I	(low active)
nPOWER_GOOD	X6:38	power good signal	I	(low active)
nRESET_PERIPH	X6:39	periphery reset signal	O	(low active)
+VBAT_BKUP	X6:40	PMU backup battery input	P	(2.5V - 3.6V)

Signal	Pin	Description	I/O	Comment
nONKEY	X6:41	Power button	I	
nWAKEUP_POWER	X6:43	power wakeup signal	I	(low active)
WAKEUP_LID	X6:45	LID wakeup signal	I	(high active)
FORCE_nRECOVERY	X2:51	Force to recovery mode	I	(low active)
PMU_GPIOA	X6:47	PMU GPIO	I/O	
PMU_GPIOB	X6:49	PMU GPIO	I/O	

#### 4.1.1 Signal descriptions

- **+2V5\_AON\_RTC**

This voltage rise after the PMU will be powered by the +5V\_SYS. The +5V\_SYS will be loaded after the nPOWER\_GOOD signal will be set (low active). This voltage should be used to pull the nWAKEUP\_POWER pin.

- **USB0\_ID\_PMU**

TBD

- **+1V8\_VDDIO**

The signal +1V8\_VDDIO is a power source which is powered by the PMU. The maximum current is **600 mA**.

- **nRESET\_COM**

This signal reset the PMU. It is pulled on the SoM against +2V5\_AON\_RTC (100k).

- **nPOWER\_GOOD**

The power good signal (low active) indicate that the voltages +5V\_SYS and +3V3\_SYS are okay. This signal can be connect to the power good outputs of the power supplies. Or it can also be connect to ground. This signal is pulled against +5V\_SYS (100k).

- **nRESET\_PERIPH**

This output is pulled against +1V8\_VDDIO (10k) and indicate if the Tegra is powered. The signal should be used to unload all device which are connected to the SoM, otherwise reverse supply can happen.

- **+VBAT\_BKUP**

This pin can be used for a RTC battery, but it can also be opened. The RTC backup battery can be loaded by the internal battery charger of the PMU to 2.5 V or to 3.0 V. In the power off mode the current should below 10 uA (supplier specification).

- **nONKEY**

This input can be used to start the PMU. The signal is low active and pulled on the SoM against +2V5\_AON\_RTC (220k).

- **nWAKEUP\_POWER**

This signal can also be used to start the PMU. The signal is low active and is pulled on the SoM with 100k against +2V5\_AON\_RTC.

**Autoboot:**

- if **no "Power Off Mode"** will be required, this signal can be connected to ground. In this case the PMU will be reseted instead of powered off, when a long press event is detected at the nONKEY signal.

- otherwise a reset chip should be used to generate the power on event. In this case the reset chip must generate a low level until the nPOWERGOOD is high plus minimum 210 ms.

- **WAKEUP\_LID**

This signal is high active and can be used to leave the suspend mode, when the input is configured. The suspend mode can also be leaved by the nWAKEUP\_POWER event. The signal is pulled on the SoM with 10k against ground.

- **FORCE\_nRECOVERY**

If this signal is low at the power up, the Tegra will starts in recovery mode.

- **PMU\_GPIOA**

Free usable GPIO from the PMU.

- **PMU\_GPIOB**

Free usable GPIO from the PMU.

## 4.2 DAP (I<sup>2</sup>S)

The K1 processor module support up to two I2S interfaces (DAP2 and DAP4). The I2S Controller transports streaming audio data between system memory and an audio codec. The controller supports I2S format, Left-justified Mode format, Right-justified Mode format, and DSP mode format, as defined in the Philips inter-IC-sound (I2S) bus specification. The I2S and PCM (master and slave modes) interfaces support clock rates up to 24.576 MHz.

The I2S controller supports point-to-point (P2P) serial interfaces for the I2S digital audio streams. I2S-compatible products, such as compact disc players, digital audio tape devices, digital sound processors and those with digital TV sound may be directly connected to the I2S controller. The controller also supports the PCM and telephony mode of data-transfer. Pulse-Code-Modulation (PCM) is a standard method used to digitize audio (particularly voice) patterns for transmission over digital communication channels. The Telephony mode is used to transmit and receive data to and from an external mono CODEC in a slot-based scheme of time-division multiplexing. The I2S controller supports bidirectional audio streams and can operate in half-duplex or full-duplex mode.

Features:

- Basic I2S modes to be supported (I2S, RJM, LJM, and DSP) in both Master and Slave modes
- PCM mode with short (one-bit-clock-wide) and long-fsync (two bit-clocks wide) in both master and slave modes
- NW-mode with independent slot-selection for both TX and RX
- TDM mode with flexibility in number of slots and slot(s) selection
- Capability to drive-out a High-z outside the prescribed slot for transmission
- Flow control for the external input/output stream
- Support for u-Law and A-Law compression/decompression

#### 4.2.1 Signals

Table 6: DAP2 signals

Signal	Pin	Description	I/O	Comment
DAP_MCLK1	X5:42	DAP master clock 1: External Peripheral 1 Clock: Connect to MCLK pin of the audio device if reference clock is required	O	
DAP2_DIN	X5:46	Data In. DAP pins support I2S/PCM audio. Interface can be master or slave	I	
DAP2_DOUT	X5:48	Data Out. DAP pins support I2S/PCM audio. Interface can be master or slave	O	
DAP2_FS	X5:44	Frame Sync/Word Select. DAP pins support I2S/PCM audio. Interface can be master or slave	I/O	
DAP2_SCLK	X5:50	Serial Clock/Bit Clock. DAP pins support I2S/PCM audio. Interface can be master or slave	I/O	

Table 7: DAP4 signals

Signal	Pin	Description	I/O	Comment
CLK3_OUT	X4:50	Clock 3 out: External Peripheral 3 Clock: Connect to MCLK pin of the audio device if reference clock is required Connnect to MCLK if	O	
DAP4_DIN	X4:55	Data In. DAP pins support I2S/PCM audio. Interface can be master or slave	I	
DAP4_DOUT	X4:57	Data Out. DAP pins support I2S/PCM audio. Interface can be master or slave	O	
DAP4_FS	X4:53	Frame Sync/Word Select. DAP pins support I2S/PCM audio. Interface can be master or slave	I/O	
DAP4_SCLK	X4:51	Serial Clock/Bit Clock. DAP pins support I2S/PCM audio. Interface can be master or slave	I/O	

#### 4.2.2 Example schematic

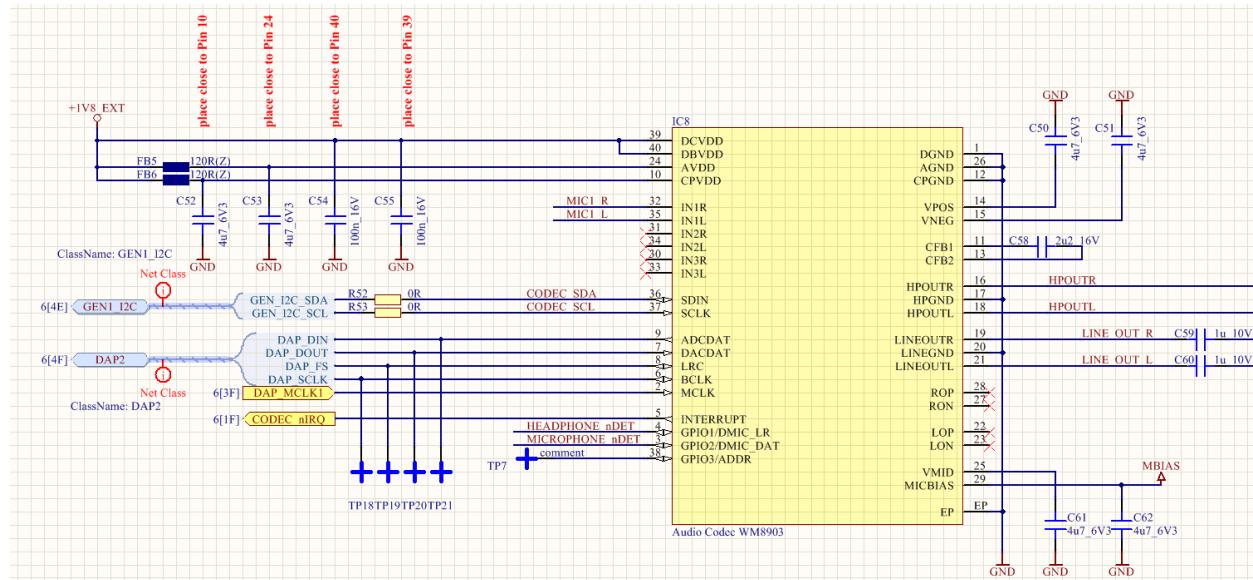


Figure 4.1: DAP2 schematic example

#### 4.2.3 Necessary layout properties

Table 8: DAP/I2S interface signal routing requirements

Parameter	Requirement	Units	Notes
Configuration / Device Organization	1	load	
Max loading	8	pF	
Topology	Point to Point		
Reference plane	GND		
Breakout region impedance	Min width / spacing		
Trace impedance	50	$\Omega$	$\pm 20\%$
Via proximity (signal to reference)	< 3.8 (24)	mm (ps)	Up to 4 signal vias can share a single GND return via
Trace spacing (Microstrip /Stripline)	2x / 2x	dielectric	
Max trace delay	3600 ( $\sim 555$ )	ps (mm)	Include Package & PCB routing delays for max trace delays parameter
Max trace delay skew between SCLK & SDATA_OUT/IN	250 ( $\sim 38$ )	ps (mm)	Include Package & PCB routing delays for max trace delay skew parameter

Table 9: DAP/I2S interface delays

Signal Name	Pkg Delay (ps)	SoM PCB delay (ps)	total delay (ps)
DAP2_DIN	69	169.5	238.5
DAP2_DOUT	61	158.9	219.9
DAP2_FS	78	200.3	278.3
DAP2_SCLK	64	110.0	174.0
DAP4_DIN	66	348.2	414.2
DAP4_DOUT	61	360.9	421.9
DAP4_FS	72	336.1	408.1
DAP4_SCLK	71	245.4	316.4

## 4.3 eDP

The Tegra K1 supports up to a 4-lane Embedded Display Port (eDP) interface. The maximum resolution supported with eDP is 3840x2160 @60fps.

- Embedded Display Port mode: interface will take in a clock frequency of 270 Mht (i.e. it will generate a 6x, 10x, and 20x high frequency clock (1.6 GHz for RBR, 2.7 GHz for HBR, and 5.4 GHz for HBR2)).

### 4.3.1 Signals

Table 10: embedded DisplayPort (eDP) signals

Signal	Pin	Description	I/O	Comment
eDP_HPD	X1:10	eDP Hot Plug detect	I/O	
eDP0_N	X1:39	eDP data lane (negative)	O	
eDP0_P	X1:37	eDP data lane (positive)	O	
eDP1_N	X1:45	eDP data lane (negative)	O	
eDP1_P	X1:43	eDP data lane (positive)	O	
eDP2_N	X1:55	eDP data lane (negative)	O	
eDP2_P	X1:57	eDP data lane (positive)	O	
eDP3_N	X1:33	eDP data lane (negative)	O	
eDP3_P	X1:31	eDP data lane (positive)	O	
LVDS_TXD3_N	X1:49	LVDS lane 3 (negative)	O	LVDS is not supported
LVDS_TXD3_P	X1:51	LVDS lane 3 (positive)	O	LVDS is not supported
DP_AUX_CH0_N		eDP Auxiliary Channel: Connect to AUX_CH_N on the display connector	O	
DP_AUX_CH0_P		eDP Auxiliary Channel: Connect to AUX_CH_P on the display connector	O	
EN_LVDS_EDP	X5:17	eDP enable signal	O	

### 4.3.2 Example schematic

Schematics follow soon

### 4.3.3 Necessary layout properties

Table 11: eDP (HBR2) main link signal routing requirements

Parameter	Requirement	Units	Notes
Max data rate (per data lane)	5.4 (HBR2) / 2.7 (HBR) / 1.62 (RBR)	Gbps	
Min UI	185 (HBR2) / 370 (HBR) / 617 (RBR)	ps	
Number of loads	1	load	
Topology			Point to Point, Differential, unidirectional
Termination	100	$\Omega$	on die at TX / RX
Max breakout PCB length	7.63	mm	
Trace impedance Diff / Single	90 / 45-60	$\Omega$	$\pm 15\%$
<b>Stripline Routing for Main Trunk</b>			
Max trace length from Tegra TX pin to connector	215 (RBR/HBR) / 165 (HBR2)	mm	Max trace delays & max trace delays skew matching must include substrate pin delays unless otherwise specified
Max propagation delay - HBR2	1137	ps	
Max number of signal vias	4 (RBR, HBR) / 2 (HBR2)		HBR2: one more test via right after AC cap OK
PCB pair-to-pair spacing	3x	dielectric height	3x of the thinner of above and below
PCB main link to AUX spacing	3x	dielectric height	3x of the thinner of above and below
Max stub length on the vias allowed			Rout below core to minimize stub length
<b>Microstrip routing for main trunk</b>			
Max trace length from Tegra TX pin to connector	215 (RBR/HBR) / 127, 152.4 (HBR2 5x, 7x spacing)	mm	Max Trace Delay & Max Trace Delay Skew matching must include substrate pin delays
Max propagation delay HBR2 (5x / 7x spacing)	750 / 900	ps	150 ps/inch delay assumption for microstrip
Max number of signal vias	4 (RBR, HBR) / 2 (HBR2)		HBR2: one more test via right after AC cap OK
PCB pair-to-pair spacing	4x (RBR/HBR) / 5x-7x (HBR2)	dielectric height	
PCB main link to AUX spacing	5x	dielectric height	
<b>Signal skews (Stripline or Mircoline)</b>			

Parameter	Requirement	Units	Notes
Max intra-pair (within pair) skew	1	ps	
Max inter-pair (pair-pair) skew	150	ps	

Table 12: eDP (LVDS) interface delays

Signal Name	Pkg Delay (ps)	SoM PCB delay (ps)	total delay (ps)
eDP0_N / (LVDS2_TX0N)	30	137.2	167.2
eDP0_P / (LVDS2_TX0P)	30	137.2	167.2
eDP1_N / (LVDS1_TX0N)	44	134.5	178.5
eDP1_P / (LVDS1_TX0P)	45	134.5	179.5
eDP2_N / (LVDS0_TX0N)	50	134.8	184.8
eDP2_P / (LVDS0_TX0P)	51	134.8	185.8
eDP3_N / (LVDS4_TX0N)	38	134.9	172.9
eDP3_P / (LVDS4_TX0P)	38	134.9	172.9
- / (LVDS3_TX0N)	46	134.5	180.5
- / (LVDS3_TX0P)	47	134.5	181.5

## 4.4 GPIO

The Tegra processor GPIO controller provides the tools for configuring each MPIO for use as software-controlled GPIO. Each GPIO is individually configurable as Output/Input/Interrupt sources with level/edge controls. The GPIO controller is divided into 8 banks. Each bank handles the GPIO functionality for up to 32 MPIOs. Within a bank, GPIOs are arranged as four ports of 8-bits each. The ports are labeled consecutively from A through Z and the AA through FF. Ports A through D are in bank 0. Ports E through H are in bank 1. There are 183 available GPIOs, but not all GPIOs are routed to the connectors. See the list below which GPIOs are available:

### 4.4.1 Signals

Table 13: 1.8V GPIOs signals

Signal	Pin	Description	I/O	Comment
GPIO_PC7	X4:43		I/O	GEN2_I2C_IRQ
GPIO_PEE2	X5:39		I/O	SATA_PWR_EN
GPIO_PH0	X4:12		I/O	FAN_PWM
GPIO_PH1	X4:52		I/O	HDMI_VDD_EN
GPIO_PH2	X4:11		I/O	BL_PWM
GPIO_PH3	X4:20		I/O	
GPIO_PH4	X4:9		I/O	BL_EN
GPIO_PH5	X4:7		I/O	
GPIO_PH6	X4:6		I/O	
GPIO_PI2	X4:24		I/O	
GPIO_PI4	X4:18		I/O	SPI4C_nCS1
GPIO_PI5	X4:4		I/O	
GPIO_PI7	X4:5		I/O	

Signal	Pin	Description	I/O	Comment
GPIO_PJ0	X4:10		I/O	
GPIO_PJ2	X4:36		I/O	
GPIO_PK0	X4:14		I/O	
GPIO_PK1	X4:3		I/O	
GPIO_PK2	X4:8		I/O	
GPIO_PK3	X4:2		I/O	
GPIO_PK4	X4:22		I/O	
GPIO_PN2	X5:41		I/O	SATA_LED
GPIO_PO1	X5:13		I/O	SPI3E_MOSI
GPIO_PO2	X5:19		I/O	SPI3E_MISO
GPIO_PO3	X5:23		I/O	SPI3E_SCK
GPIO_PO4	X5:27		I/O	SPI3E_nCS1
GPIO_PP0	X5:54		I/O	
GPIO_PP1	X5:21		I/O	SPI1A_nIRQ
GPIO_PP2	X5:18		I/O	
GPIO_PR0	X5:25		I/O	SDMMC3_VDD_EN
GPIO_PR2	X5:38		I/O	AUDIO_EN
GPIO_PR4	X5:20		I/O	
GPIO_PR5	X5:16		I/O	
GPIO_PR6	X5:29		I/O	
GPIO_PR7	X5:22		I/O	HEAD_DET
GPIO_PT0	X5:31		I/O	SOC_ALIVE
GPIO_PU1	X4:48		I/O	SDMMC1_PWR_EN
GPIO_PU5	X5:60		I/O	CODEC_nIRQ
GPIO_PW2	X5:8		I/O	
GPIO_PW3	X5:43		I/O	
GPIO_PX3	X5:36		I/O	SPI2D_nIRQ
GPIO_PX5	X5:14		I/O	GEN1_I2C_nIRQ
GPIO_PX6	X5:12		I/O	
GPIO_PX7	X5:10		I/O	

Table 14: 3.3V GPIOs signals

Signal	Pin	Description	I/O	Comment
GPIO_PK5	X5:56		I/O	SPDIF_OUT
GPIO_PK6	X5:58		I/O	SPDIF_IN

#### 4.4.2 Example schematic

No special schematics are required.

#### 4.4.3 Necessary layout properties

It is necessary that all Inputs are not powered until the Tegra is running.

## 4.5 HDMI

High-Definition Multimedia Interface (HDMI) support provides a unified method of transferring both audio and video data over a TMDS-compatible physical link to an audio/visual device. The HDMI block receives video from either display controller and audio from a separate high-definition audio (HDA) controller; it combines and transmits them as appropriate.

Features:

- High-definition Multimedia Interface (HDMI) specification 1.4b
- High-bandwidth Digital Content Protection (HDCP) system specification 1.4
- On-Chip HDCP key storage, no external SecureROM required
- TMDS (Transition Minimized Differential Signaling) PHY I/F

### 4.5.1 Signals

Table 15: HDMI signals

Signal	Pin	Description	I/O	Comment
HDMI_CEC	X1:6	HDMI Consumer Electronics Control	I/O	
HDMI_DDC_SCL	X1:4	HDMI I2C clock	O	
HDMI_DDC_SDA	X1:2	HDMI I2C data	I/O	
HDMI_INT	X1:8	HDMI interrupt. Used for Hot Plug detection	I	
HDMI_TXC_N	X1:1	Transmit clock (negative)	O	
HDMI_TXC_P	X1:3	Transmit clock (positive)	O	
HDMI_TXD0_N	X1:7	Data lane (negative)	O	
HDMI_TXD0_P	X1:9	Data lane (positive)	O	
HDMI_TXD1_N	X1:13	Data lane (negative)	O	
HDMI_TXD1_P	X1:15	Data lane (positive)	O	
HDMI_TXD2_N	X1:19	Data lane (negative)	O	
HDMI_TXD2_P	X1:21	Data lane (positive)	O	
HDMI_VDD_EN	X4:52	HDMI power enable	O	

### 4.5.2 Example schematic

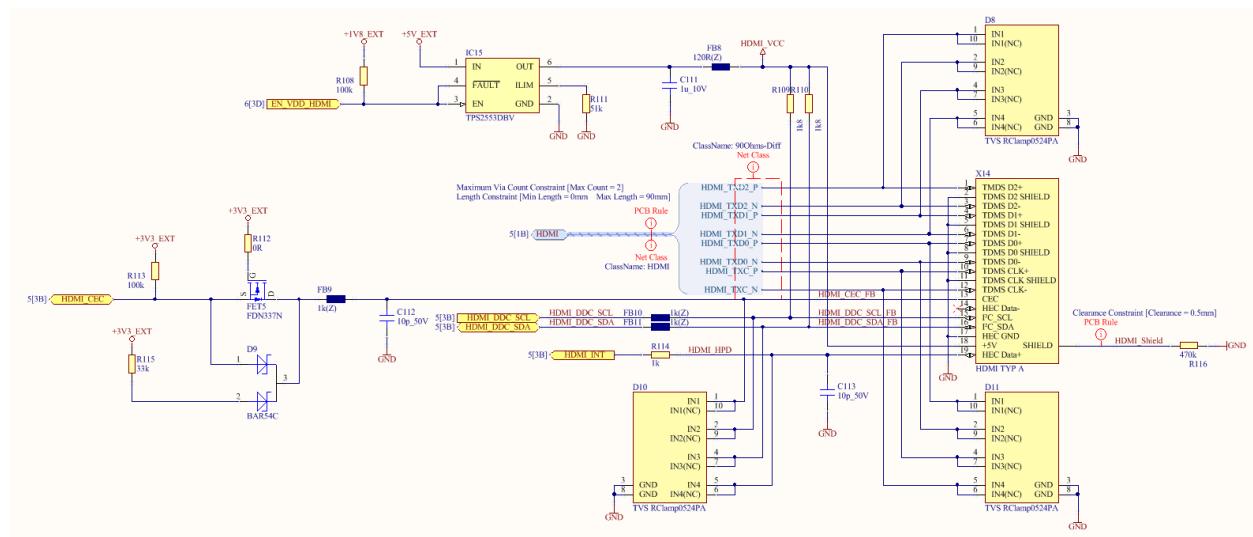


Figure 4.2: HDMI schematic example

### 4.5.3 Necessary layout properties

Table 16: HDMI interface signal routing requirements

Parameter	Requirement	Units	Notes
Max frequency	297	MHz	Data rate is ten times larger than the pixel frequency
Topology	Point to Point		
Termination	50 (At Receiver) / 500 (on-board)	$\Omega$	To 3.3V at receiver / To GND near connector
Reference plane	GND		
Max Breakout length / delay	7.62 (52.5)	mm (ps)	
Trace impedance	90 (diff pair) / 45-60 (single ended)	$\Omega$	$\pm 15\%$
Trace spacing	4x (microstrip) / 3x (stripline)	dielectric	Mircostrip routing is recommended for HDMI due to limited eye height and has longer MAX length
Max Trunk delay (297 MHz)	114 (675) (Microstrip / Stripline)	mm (ps)	Include package & PCB routing delays for Max trace delays and max trace delay skew parameters
Max Trunk delay (225 MHz)	204 (1400) (Microstrip / Stripline)	mm (ps)	Include package & PCB routing delays for Max trace delays and max trace delay skew parameters

Parameter	Requirement	Units	Notes
Max Trunk delay (16 MHz)	254 (1500) (Microstrip / Stripline)	mm (ps)	Include package & PCB routing delays for Max trace delays and max trace delay skew parameters
Max distance from ESD to connector	12.7 (87)	mm (ps)	
Max distance from signal line to ESD pad	6.35 (37.5)	mm (ps)	Keep stub connecting ESD to signal trace very short or overlay pad on signal trace.
Max intra-pair (within pair) skew	1	ps	
Max inter-pair (pair-pair) skew	150	ps	

Table 17: HDMI interface delays

Signal Name	Pkg Delay (ps)	SoM PCB delay (ps)	total delay (ps)
HDMI_TXC_N	29	182.2	211.2
HDMI_TXC_P	29	182.2	211.2
HDMI_TXD0_N	29	182.8	211.8
HDMI_TXD0_P	29	182.8	211.8
HDMI_TXD1_N	38	182.4	220.4
HDMI_TXD1_P	39	182.4	221.4
HDMI_TXD2_N	49	182.6	231.6
HDMI_TXD2_P	50	182.6	232.6

## 4.6 I<sup>2</sup>C

The Inter-Chip Communication (I2C) controller implements an I2C master and a slave controller. The I2C controller supports multiple masters and slaves in: Standard-mode (up to 100Kbit/s), Fast-mode (up to 400Kbit/s), Fast-mode plus (FM+, up to 1Mbit/s) and High-speed mode (up to 3.4Mbit/s) of operations. A general purpose I2C controller allows system expansion for I2C-based devices, such as AM/FM radio, remote LCD display, serial ADC/DAC, and serial EPROMs, as defined in the NXP Inter-IC-bus (I2C) specification. The I2C bus supports serial device communications to multiple devices. The I2C controller handles bus mastership with arbitration, clock source negotiation, speed negotiation for standard and fast devices, and 7-bit and 10-bit slave address support according to the i2c protocol and supports master and slave mode of operation.

The following table shows the our default U-Boot and Kernel I<sup>2</sup>C bus-number assignment:

Table 18: I<sup>2</sup>C bus-number assignment

Bus	Description	Comment
i2c0	GEN1_I2C	1.8V I2C bus
i2c1	GEN2_I2C	3.3V I2C bus
i2c2	CAM_I2C	1.8V I2C bus

Bus	Description	Comment
i2c3	HDMI DDC	5V tolerant I2C bus
i2c4	PWR_I2C	1.8V I2C bus (only on the SoM)

#### 4.6.1 Signals

Table 19: I<sup>2</sup>C GEN1 (1V8) signals

Signal	Pin	Description	I/O	Comment
GEN1_I2C_SCL	X5:2	GEN1 I2C clock	O	
GEN1_I2C_SDA	X5:4	GEN1 I2C data	I/O	

Table 20: I<sup>2</sup>C GEN2 (3V3) signals

Signal	Pin	Description	I/O	Comment
GEN2_I2C_SCL	X4:45	GEN2 I2C clock	O	
GEN2_I2C_SDA	X4:47	GEN2 I2C data	I/O	

Table 21: I<sup>2</sup>C CAM (1V8) signals

Signal	Pin	Description	I/O	Comment
CAM_I2C_SCL	X1:56	Camera I2C clock	O	
CAM_I2C_SDA	X1:58	Camera I2C data	I/O	

Table 22: HDMI DDC signals

Signal	Pin	Description	I/O	Comment
CAM_I2C_SCL	X1:4	HDMI DDC clock	O	
CAM_I2C_SDA	X1:2	HDMI DDC data	I/O	

#### 4.6.2 Example schematic

No special schematics are required.

#### 4.6.3 Necessary layout properties

The I2C bus lines are pulled already on the SoM.

## 4.7 JTAG

K1 series processors have an optional JTAG interface that can be used for SCAN testing or for communication with either integrated CPU.

### 4.7.1 Signals

JTAG signals

Signal	Pin	Description	I/O	Comment
JTAG_nTRST	X4:21	Test reset	I	Normal operation: Pull-down only - Do not connect to TRST pin of connector  Scan test mode: Connect to TRST_N pin of the connector  pulled with 10k to GND on the SoM
JTAG_RTCK	X4:23	Return Test reset	I	
JTAG_TCK	X4:15	Test clock	I	
JTAG_TDI	X4:19	Test data In	I	
JTAG_TDO	X4:25	Test data Out	O	
JTAG_TMS	X4:17	Test mode select	I	

### 4.7.2 Example schematic

No special schematics are required.

### 4.7.3 Necessary layout properties

no necessary layout properties

## 4.8 MIPI CSI

The Camera Serial Interface (CSI) is based on MIPI CSI 2.0 specification and implements the CSI receiver which receives data from an external camera module with a CSI transmitter. It consists of two CSI receiver interfaces so it can receive serial transmissions from two cameras.

- MIPI CSI 2.0 receiver
- Support for 3 camera sensors (any 2 can be active at the same time)
  - 1 x4 (single camera with 4 lane sensor)
  - 1 x4 + 1 x1 (one high resolution camera nad antoher front facing low resolution camera)
  - 2 x4 (dual cameras for stereo with 4 lanes for each camera)
- Supported input data formats:
  - RGB: RGB888, RGB666, RGB565, RGB555, RGB444
  - YUV: YUV422-8b, YUV420-8b (legacy), YUV420-8b, YUV444-8b
  - RAW: RAW6, RAW7, RAW8, RAW10, RAW12, RAW14
  - DPCM: user defined
  - User defined: JPEG8
  - Embedded: Embedded control information
- Supports single-shot mode
- D-PHY Modes of Operation
  - High Speed Mode - High speed differential signaling up to 1.5 Gbps; burst transmission for low power
  - Low Power Control - Single-ended 1.2 V CMOS level. Low speed signaling for handshaking.
  - Low speed signaling for data, used for escape command entry only: 20 Mbps

#### 4.8.1 Signals

Table 24: MIPI CSI signals

Signal	Pin	Description	I/O	Comment
CAM_nRST	X4:56	CAM reset	O	
CAM1_MCLK	X1:60	CAM1 master clock	O	
CAM1_PWDN	X4:54	CAM1 power down	O	
CAM2_MCLK	X1:54	CAM2 master clock	O	
CAM2_PWDN	X4:58	CAM2 power down	O	
CSI_A_CLK_N	X2:41	CSI clock (negative)	I	
CSI_A_CLK_P	X2:39	CSI clock (positive)	I	
CSI_A_D0_N	X2:27	CSI data (negative)	I/O	
CSI_A_D0_P	X2:29	CSI data (positive)	I/O	
CSI_A_D1_N	X2:35	CSI data (negative)	I/O	
CSI_A_D1_P	X2:33	CSI data (positive)	I/O	
CSI_B_D0_N	X2:21	CSI data (negative)	I/O	
CSI_B_D0_P	X2:23	CSI data (positive)	I/O	
CSI_B_D1_N	X2:17	CSI data (negative)	I/O	
CSI_B_D1_P	X2:15	CSI data (positive)	I/O	
CSI_E_CLK_N	X2:11	CSI clock (negative)	I	
CSI_E_CLK_P	X2:9	CSI clock (positive)	I	
CSI_E_D0_N	X2:3	CSI data (negative)	I/O	
CSI_E_D0_P	X2:5	CSI data (positive)	I/O	

#### 4.8.2 Example schematic

No special schematics are required.

#### 4.8.3 Necessary layout properties

Table 25: CSI interface signal routing requirements

Parameter	Requirement	Units	Notes
Max frequency / data rate (per data lane)	750 / 1500	MHz / Mbps	
Number of loads	1	load	
Max loading (per pin)	10	pF	
Reference plane	GND or PWR		If PWR, 10nF decoupling cap required for return current
Breakout region impedance	90 (diff) / 45-55 (single ended)	$\Omega$	$\pm 15\%$
Max PCB breakout delay	48	ps	
Trace impedance	90 (diff pair) / 45-55 (single ended)	$\Omega$	
Via proximity (signal to reference)	<3.8 (24)	mm (ps)	
Trace spacing	2x (microstrip / stripline)	dielectric	
Max trace delay	1620	ps	PCB routing delays for Max trace delays and max trace delay skew parameters
Max intra-pair (within pair) skew	1	ps	PCB routing delays for Max trace delays and max trace delay skew parameters
Max inter-pair (pair-pair) skew	10	ps	PCB routing delays for Max trace delays and max trace delay skew parameters

Table 26: CSI interface delays

Signal Name	Pkg Delay (ps)	SoM PCB delay (ps)	total delay (ps)
CSI_A_CLK_N	46	109.5	155.5
CSI_A_CLK_P	46	109.5	155.5
CSI_A_D0_N	81	73.8	154.8
CSI_A_D0_P	81	73.8	154.8
CSI_A_D1_N	61	94.1	155.1
CSI_A_D1_P	62	93.0	155.0
CSI_B_D0_N	78	76.4	154.4

Signal Name	Pkg Delay (ps)	SoM PCB delay (ps)	total delay (ps)
CSI_B_D0_P	79	75.5	154.5
CSI_B_D1_N	66	88.0	154.0
CSI_B_D1_P	67	87.1	154.1
CSI_E_CLK_N	67	87.4	154.4
CSI_E_CLK_P	68	86.4	154.4
CSI_E_D0_N	57	97.5	154.5
CSI_E_D0_P	58	96.5	154.5

## 4.9 MIPI DSI

The MIPI Display Serial Interface (DSI) us a serial bit-stream replacement for the parallel MIPI DPI and DBI display interface standards. DSI reduces package pin-count and I/O power consumption. DSI support enables both display controllers to connect to an external display(s) with a MIPI DSI receiver. The DSI transfers pixel data from the internal display controller to an external third-party LCD module.

Features:

- Phy Layer:
  - Start / End of transmission. Other out-of-band signaling
  - Per DSI interface: 1 Clock Lane; up to 4 data lanes
  - Supports link configuration: 1x4, 2x4
  - Supports Dual link operation in 2x4 configurations for asymmetrical/symmetrical split in both left-right side or odd-even group split schemes
  - Maximum link rate 1.5 Gbps as per MIPI D-PHY 1.1v version
  - Maximum 10 MHz LP receive rate
- Maximum resolution supported:
  - Dual link - 2x4: 3840x1920 @60Hz, 24-bpp at 1.5 Gbps per lane
  - Single link - 1x4: 2560x1440 @60Hz, 24-bpp at 1.5 Gbps per lane
- Lange Management Layer with Distributor
- Protocol Layer with Packet Constructor
- Supports MIPI DSI 1.0.1v version mandatory features
- Command Mode (one-shot) with host and/or display controller as master
- Clocks:
  - Bit clock: Serial data stream bit-rate clock
  - Byte clock: Lane management layer byte-rate clock
  - Application clock: Protocol layer byte-rate clock
- Error Detection / Correction:
  - ECC generation for packet Headers

- Checksum generation for Long Packets
- Error recovery
- High speed transmit timer
- Low power receive timer
- Turnaround acknowledge Timeout

#### 4.9.1 Signals

Table 27: MIPI DSI signals

Signal	Pin	Description	I/O	Comment
DSI_A_CLK_N	X2:46	DSI clock (negative)	O	
DSI_A_CLK_P	X2:44	DSI clock (positive)	O	
DSI_A_D0_N	X2:32	DSI bidirectional data lanes (negative)	I/O	
DSI_A_D0_P	X2:34	DSI bidirectional data lane (positive)	I/O	
DSI_A_D1_N	X2:56	DSI bidirectional data lane (negative)	I/O	
DSI_A_D1_P	X2:58	DSI bidirectional data lane (positive)	I/O	
DSI_A_D2_N	X2:40	DSI bidirectional data lane (negative)	I/O	
DSI_A_D2_P	X2:38	DSI bidirectional data lane (positive)	I/O	
DSI_A_D3_N	X2:52	DSI bidirectional data lane (negative)	I/O	
DSI_A_D3_P	X2:50	DSI bidirectional data lane (positive)	I/O	
DSI_B_CLK_N	X2:20	DSI clock (negative)	O	shared with CSI C/D
DSI_B_CLK_P	X2:22	DSI clock (positive)	O	shared with CSI C/D
DSI_B_D0_N	X2:16	DSI bidirectional data lane (negative)	I/O	shared with CSI C/D
DSI_B_D0_P	X2:14	DSI bidirectional data lane (positive)	I/O	shared with CSI C/D
DSI_B_D1_N	X2:4	DSI bidirectional data lane (negative)	I/O	shared with CSI C/D
DSI_B_D1_P	X2:2	DSI bidirectional data lane (positive)	I/O	shared with CSI C/D
DSI_B_D2_N	X2:26	DSI bidirectional data lane (negative)	I/O	shared with CSI C/D
DSI_B_D2_P	X2:28	DSI bidirectional data lane (positive)	I/O	shared with CSI C/D
DSI_B_D3_N	X2:10	DSI bidirectional data lane (negative)	I/O	shared with CSI C/D
DSI_B_D3_P	X2:8	DSI bidirectional data lane (positive)	I/O	shared with CSI C/D

#### 4.9.2 Example schematic

No special schematics are required.

#### 4.9.3 Necessary layout properties

Table 28: DSI interface signal routing requirements

Parameter	Requirement	Units	Notes
Max frequency / data rate (per data lane)	750 / 1500	MHz / Mbps	
Number of loads	1	load	
Max loading (per pin)	10	pF	
Reference plane	GND or PWR		If PWR, 10nF decoupling cap required for return current
Breakout region impedance	90 (diff) / 45-55 (single ended)	$\Omega$	$\pm 15\%$
Max PCB breakout delay	48	ps	
Trace impedance	90 (diff pair) / 45-55 (single ended)	$\Omega$	
Via proximity (signal to reference)	<3.8 (24)	mm (ps)	
Trace spacing	2x (microstrip / stripline)	dielectric	
Max trace delay	1620	ps	PCB routing delays for Max trace delays and max trace delay skew parameters
Max intra-pair (within pair) skew	1	ps	PCB routing delays for Max trace delays and max trace delay skew parameters
Max inter-pair (pair-pair) skew	10	ps	PCB routing delays for Max trace delays and max trace delay skew parameters

Table 29: DSI interface delays

Signal Name	Pkg Delay (ps)	SoM PCB delay (ps)	total delay (ps)
DSI_A_CLK_N	66	85.9	151.9
DSI_A_CLK_P	66	86.0	152.0
DSI_A_D0_N	76	76.3	152.3
DSI_A_D0_P	75	76.5	151.5
DSI_A_D1_N	50	102.0	152.0
DSI_A_D1_P	51	101.6	152.6
DSI_A_D2_N	75	77.5	152.5
DSI_A_D2_P	75	77.5	152.5
DSI_A_D3_N	56	97.6	153.6
DSI_A_D3_P	57	96.5	153.5
DSI_B_CLK_N	68	84.9	152.9
DSI_B_CLK_P	67	85.8	152.8
DSI_B_D0_N	67	85.9	152.9
DSI_B_D0_P	67	85.9	152.9
DSI_B_D1_N	47	105.7	152.7
DSI_B_D1_P	48	104.7	152.7

Signal Name	Pkg Delay (ps)	SoM PCB delay (ps)	total delay (ps)
DSI_B_D2_N	74	78.3	152.3
DSI_B_D2_P	73	79.3	152.3
DSI_B_D3_N	55	97.8	152.8
DSI_B_D3_P	55	97.0	152.8

## 4.10 PCIe

K1 series processors integrate a x4 lane bridge to enable a control path from the Tegra chip to external PCIe devices. Two PCIe Gen2 controllers (5.0 GT/s) supports up to 5 PCIe lanes (two interfaces).

Table 30: Possible PCIe Configurations

Use Case	USB3.0	PCIe	SATA	LANE0	LANE1	LANE2	LANE3	LANE4	SATA
Jetson TK1				USB_SS#0	unused	PCIe#1_0		PCIe#0_0	SATA
1	2	1 x1 & 1 x2	1	USB_SS#0	USB_SS#1	PCIe#1_0	PCIe#0_1	PCIe#0_0	SATA
2	1	1 x4	1	USB_SS#0	PCIe#0_3	PCIe#0_2	PCIe#0_1	PCIe#0_0	SATA
3	0	1 x1 & 1 x4	1	PCIe#1_0	PCIe#0_3	PCIe#0_2	PCIe#0_1	PCIe#0_0	SATA
4	1	1 x1 & 1 x4	0	PCIe#1_0	PCIe#0_3	PCIe#0_2	PCIe#0_1	PCIe#0_0	USB_SS#1

We use in our Universal-Bootloader (U-Boot) per default the configuration 1. If you require a different setup, please contact us.

The mapping of the control signals are the following:

Table 31: PCIe: Clock and control signal mapping

PCIe controller	Clock signal	Clock request signal	Reset signal
PCIe#0	PEX_CLK1	PEX_L0_nCLKREQ	PEX_L0_nRST
PCIe#1	PEX_CLK2	PEX_L1_nCLKREQ	PEX_L1_nRST

### 4.10.1 Signals

Table 32: PCIe signals

Signal	Pin	Description	I/O	Comment
PEX_CLK1_N	X3:58	PCIe clock (negative)	O	
PEX_CLK1_P	X3:60	PCIe clock (positive)	O	
PEX_CLK2_N	X3:24	PCIe clock (negative)	O	
PEX_CLK2_P	X3:22	PCIe clock (positive)	O	
PEX_L0_nCLKREQ	X3:44	PCIe clock request	I	
PEX_L0_nRST	X3:46	PCIe reset. This signal provides a reset signal to all the PCIe links. It must be asserted 100 ms after power to the PCIe slots has stabilized.	O	
PEX_L1_nCLKREQ	X3:48	PCIe clock request	I	

<b>Signal</b>	<b>Pin</b>	<b>Description</b>	<b>I/O</b>	<b>Comment</b>
PEX_L1_nRST	X3:50	PCIe reset. This signal provides a reset signal to all the PCIe links. It must be asserted 100 ms after power to the PCIe slots has stabilized.	O	
PEX_nWAKE	X3:52	PCIe Wake. This signal is used as the PCIe defined WAKE# signal. When asserted by a PCIe device, it is a request that the system power be restored. No interrupt or other consequences result from	I	
USB3_RX0_N	X3:9	PCIe receive data lane0 (negative). Shared with USB3.0	I	
USB3_RX0_P	X3:7	PCIe receive data lane0 (positive). Shared with USB3.0	I	
USB3_TX0_N	X3:1	PCIe transmit data lane0 (negative). Shared with USB3.0	O	
USB3_TX0_P	X3:3	PCIe transmit data lane0 (positive). Shared with USB3.0	O	
PEX_USB3_RX1_N	X3:19	PCIe receive data lane1 (negative). Shared with USB3.0	I	
PEX_USB3_RX1_P	X3:21	PCIe receive data lane1 (positive). Shared with USB3.0	I	
PEX_USB3_TX1_N	X3:13	PCIe transmit data lane1 (negative). Shared with USB3.0	O	
PEX_USB3_TX1_P	X3:15	PCIe transmit data lane1 (positive). Shared with USB3.0	O	
PEX_RX2_N	X3:31	PCIe receive data lane2 (negative)	I	
PEX_RX2_P	X3:33	PCIe receive data lane2 (positive)	I	
PEX_TX2_N	X3:25	PCIe transmit data lane2 (negative)	O	
PEX_TX2_P	X3:27	PCIe transmit data lane2 (positive)	O	
PEX_RX3_N	X3:45	PCIe receive data lane3 (negative)	I	
PEX_RX3_P	X3:43	PCIe receive data lane3 (positive)	I	
PEX_TX3_N	X3:37	PCIe transmit data lane3 (negative)	O	
PEX_TX3_P	X3:39	PCIe transmit data lane3 (positive)	O	
PEX_RX4_N	X3:49	PCIe receive data lane4 (negative)	I	
PEX_RX4_P	X3:51	PCIe receive data lane4 (positive)	I	
PEX_TX4_N	X3:57	PCIe transmit data lane4 (negative)	O	
PEX_TX4_P	X3:55	PCIe transmit data lane4 (positive)	O	

#### 4.10.2 Example schematic

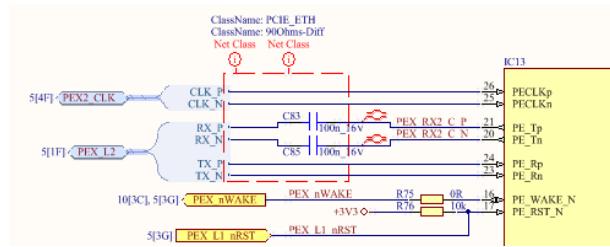


Figure 4.3: PCI Express schematic example

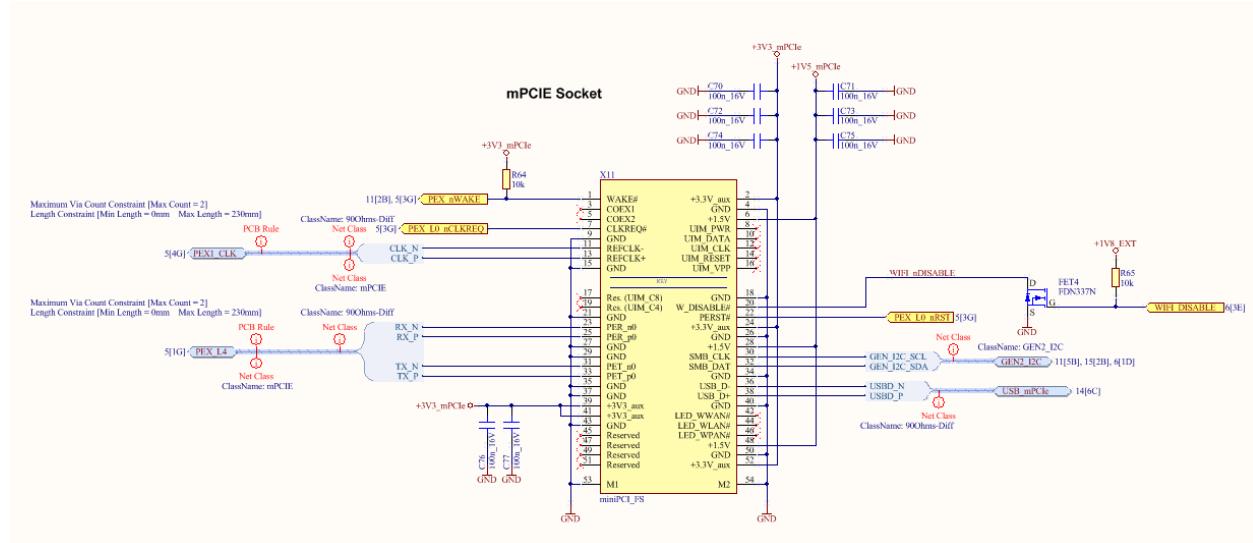


Figure 4.4: Mini PCI Express socket schematic example

#### 4.10.3 Necessary layout properties

Table 33: PCIe interface signal routing requirements

Parameter	Requirement	Units	Notes
Max frequency / UI period	5.0 / 200	Gbps / ps	2.5 GHz, half-rate architecture
Topology	Point-to-Point		Unidirectional, differential
Configuration / Device organization	1	load	
Max loading (per pin)	N/A	pF	see return loss spec in PCIe 2.0 spec
Termination	50	$\Omega$	To GND single ended for P & N
Reference plane	GND		
Breakout region Width/-line spacing	4	mils	
Breakout region pair spacing	10	mils	Maximum pair spacing of 500 mils

Parameter	Requirement	Units	Notes
Trace impedance	90 (diff pair) / 45-55 (single ended)	$\Omega$	
Pair to Pair Trace Spacing	3x (stripline) / 4x (microstrip)	dielectric	
Max trace length/delay	254 (1700)	mm (ps)	
Max intra-pair (within pair) skew	1	ps	PCB routing delays for Max trace delays and max trace delay skew parameters
Max inter-pair (pair-pair (RX-TX)) skew	600	ps	PCB routing delays for Max trace delays and max trace delay skew parameters

Table 34: PCIe interface delays

Signal Name	Pkg Delay (ps)	SoM PCB delay (ps)	total delay (ps)
PEX_CLK1_N	73	149.8	222.8
PEX_CLK1_P	72	150.5	222.5
PEX_CLK2_N	67	147.2	214.2
PEX_CLK2_P	64	149.8	213.8
USB3_RX0_N	43	145.7	188.7
USB3_RX0_P	43	145.5	188.5
USB3_TX0_N	36	146.4	182.4
USB3_TX0_P	35	147.6	182.6
PEX_USB3_RX1_N	46	136.6	182.6
PEX_USB3_RX1_P	46	136.9	182.9
PEX_USB3_TX1_N	26	147.4	173.4
PEX_USB3_TX1_P	26	147.4	173.4
PEX_RX2_N	39	159.2	198.2
PEX_RX2_P	38	160.2	198.2
PEX_TX2_N	37	142.9	179.9
PEX_TX2_P	36	143.6	179.6
PEX_RX3_N	45	147.2	192.2
PEX_RX3_P	45	147.2	192.2
PEX_TX3_N	29	165.4	194.4
PEX_TX3_P	28	166.3	194.3
PEX_RX4_N	49	145.3	194.3
PEX_RX4_P	48	146.4	194.4
PEX_TX4_N	39	168.6	207.6
PEX_TX4_P	39	168.6	207.6

## 4.11 SATA

The Serial ATA (SATA) controller enables a control path from the Tegra processor to an external SATA device. A SSD / HDD / ODD drive can be connected. Controller can support the maximum throughput of a

GEN 2 drive.

Features:

- SATA specification rev 3.1 and AHCI specification rev 1.3.1 compliant
  - Including all errata, ENC, and TP, except DHU (direct head unload)
- Device sleep feature support
  - Software initiated device sleep from slumber state only
  - Software initiated device sleep from any link states (active, partial, slumber)
  - Hardware initiated aggressive device sleep management
- Port multiplier support
  - Command based switching (CBS)
  - FIS based switching (FBS)
- Supported Cables and connectors
  - Standard internal connector
  - Internal micro connector
  - Internal slimline connector
  - mSATA connector
  - BGA SSD interface
  - Not supported: External connector (eSATA), USM, Internal LIF-SATA

#### 4.11.1 Signals

Table 35: SATA signals

table:sata

Signal	Pin	Description	I/O	Comment
SATA_L0_RX_N	X3:10	receive data lane (negative)	I	
SATA_L0_RX_P	X3:12	receive data lane (positive)	I	
SATA_L0_TX_N	X3:6	transmit data lane (negative)	O	
SATA_L0_TX_P	X3:4	transmit data lane (positive)	O	
SATA_LED	X5:41	SATA status LED	O	
SATA_PWR_EN	X5:39	SATA power enable	O	

#### 4.11.2 Example schematic

No special schematics are required.

### 4.11.3 Necessary layout properties

Table 36: SATA interface signal routing requirements

Parameter	Requirement	Units	Notes
Max frequency / UI period	3.0 / 333.3	Gbps / ps	1.5 GHz
Topology	Point-to-Point		Unidirectional, differential
Configuration / Device organization	1	load	
Max loading (per pin)	0.5	pF	
Termination	100	$\Omega$	On die termination
Reference plane	GND		
Breakout region Width/-line spacing	4	mils	
Trace impedance	90 (diff pair) / 55 (single ended)	$\Omega$	
Pair to Pair Trace Spacing	3x (stripline) / 3x (microstrip)	dielectric	
Max trace length/delay	203 (1330)	mm (ps)	Include Package & PCB routing delays for max trace delays and max trace delay skew parameters
Max intra-pair (within pair) skew	1	ps	PCB routing delays for Max trace delays and max trace delay skew parameters

Table 37: PCIe interface delays

Signal Name	Pkg Delay (ps)	SoM PCB delay (ps)	total delay (ps)
SATA_LO_RX_N	44	65.7	109.7
SATA_LO_RX_P	44	65.7	109.7
SATA_LO_TX_N	50	61.9	111.9
SATA_LO_TX_P	49	62.9	111.9

## 4.12 SD/MMC (SDIO)

The Tegra K1 has four SD/MMC controllers. The Meerkat uses SDMMC3 for an SD Card interface and SDMMC4 to interface to an eMMC device (primary boot option). SDMMC1 is available to use as SDIO. SDMMC2 is **not** routed on the Meerkat SoM.

For the SD Card and SDIO interfaces, SDMMC3 and SDMMC1 support up to UHS-1. For eMMC, SDMMC4 supports up to HS200.

#### 4.12.1 Signals

Table 38: SDMMC1 (SDIO) signals

Signal	Pin	Description	I/O	Comment
SDMMC1_PWR_EN	X4:48	SDMMC1 power enable	O	
SDMMC1_CLK	X1:50	SDMMC/SDIO clock	O	
SDMMC1_CMD	X1:52	SDMMC/SDIO command	I/O	
SDMMC1_DAT0	X1:42	SDMMC/SDIO data	I/O	
SDMMC1_DAT1	X1:44	SDMMC/SDIO data	I/O	
SDMMC1_DAT2	X1:40	SDMMC/SDIO data	I/O	
SDMMC1_DAT3	X1:48	SDMMC/SDIO data	I/O	
SDMMC1_nIRQ	X1:38	SDMMC/SDIO interrupt request	I	low active
SDMMC1_nWP	X1:46	SDMMC/SDIO write protect	O	low active

Table 39: SDMMC3 signals

Signal	Pin	Description	I/O	Comment
SDMMC3_VDD_EN	X5:25	SDMMC power enable	O	
SDMMC3_CLK	X1:30	SDMMC clock	O	
SDMMC3_CLK_LB_IN	X1:26	SDMMC clock loop back input: SDMMC3_CLK_LB_IN connects to SDMMC3_CLK_LB_OUT. Total trace length is the length of a round trip, from Tegra to connector and back.	I	
SDMMC3_CLK_LB_OUT	X1:28	SDMMC clock loop back output	O	
SDMMC3_CMD	X1:18	SDMMC command	I/O	
SDMMC3_DAT0	X1:22	SDMMC data	I/O	
SDMMC3_DAT1	X1:16	SDMMC data	I/O	
SDMMC3_DAT2	X1:20	SDMMC data	I/O	
SDMMC3_DAT3	X1:14	SDMMC data	I/O	
SDMMC3_nCD	X1:32	SDMMC card detect	O	low active
SDMMC3_nWP	X1:34	SDMMC write protect	O	low active

### 4.12.2 Example schematic

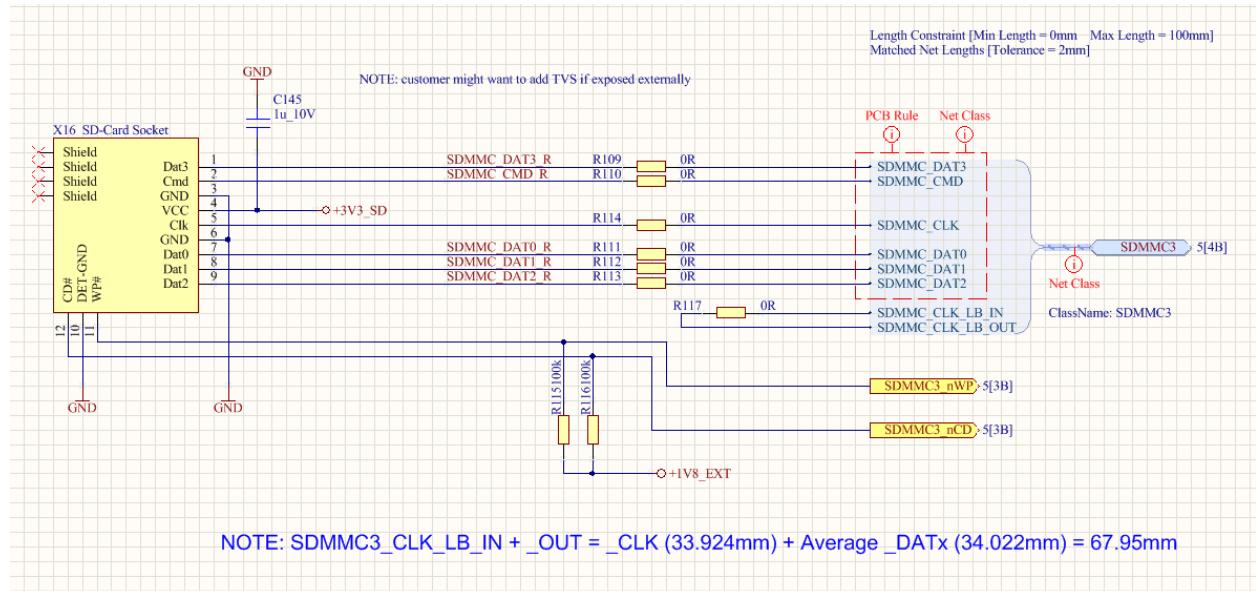


Figure 4.5: SDMMC schematic example

### 4.12.3 Necessary layout properties

Table 40: SDMMC3/1 interface signal routing requirements

Parameter	Requirement	Units	Notes
Max frequency	3.3V DS	25 (12.5) 50 (25)	MHz / (MB/s)
	HS	25 (12.5) 50 (25)	
1.8V	SDR12	100 (50)	Actual frequencies may be slightly different due to clock source/divider limitations
	SDR25	208 (104)	
	SDR50	50 (50)	
	SDR104		
	DDR50		
Topology	Point-to-Point		
Max loading (per pin)	10	pF	
Reference plane	GND or PWR		
Breakout region impedance	45-50	$\Omega$	$\pm 15\%$
Trace impedance	45-50	$\Omega$	$\pm 15\%$
Max trace delay	1100 / 745	ps	Include Package & PCB routing delays for max trace delays and max trace delay skew parameters
SDR12, SDR25, SDR50 / SDR104			

Parameter	Requirement	Units	Notes
Max trace delay skew in/between CLK & CMD/DAT  SDR12, SDR25, SDR50 / SDR104	100 / 20	ps	PCB routing delays for Max trace delays and max trace delay skew parameters
Loopback clock routing LB_OUT to LB_IN = CLK length + Average of DAT[3:0]	+/- 150	ps	PCB routing delays for Max trace delays and max trace delay skew parameters

Table 41: SDMMC3/1 interface delays

Signal Name	Pkg Delay (ps)	SoM PCB delay (ps)	total delay (ps)
SDMMC1_CLK	97	91.1	188.1
SDMMC1_CMD	86	95.8	181.8
SDMMC1_DAT0	68	103.3	171.3
SDMMC1_DAT1	68	104.1	172.1
SDMMC1_DAT2	69	103.5	172.5
SDMMC1_DAT3	90	101.2	191.2
SDMMC3_CLK	63	81.4	144.4
SDMMC3_CMD	76	69.0	145.0
SDMMC3_DAT0	74	70.1	144.1
SDMMC3_DAT1	89	73.5	162.5
SDMMC3_DAT2	77	76.5	153.5
SDMMC3_DAT3	72	81.4	153.4
SDMMC3_CLK_LB_IN	72	70.0	142.0
SDMMC3_CLK_LB_OUT	73	76.1	146.1

## 4.13 S/PDIF

The Sony/Philips Digital Interconnect Format (SPDIF) interface supports both professional and consumer applications. When used in a professional application, the interface is primarily intended to carry monophonic or stereophonic programs, at a 48 kHz sampling frequency and with a resolution of up to 24-bits per sample; it may alternatively be used to carry signals sampled at 32 kHz or 44.1 kHz. When used in a consumer application, the interface is primarily stereophonic programs with a resolution of up to 20-bits per sample.

The Interface normally carries audio data coded as other than linear PCM-coded audio samples. The interface may also carry data related to computer software or signals coded using non-linear PCM.

Features:

- Supported data formats: 16-bit, 20-bit, 24-bit, RAW and 16-bit packed
- Supported sample rates: 32, 44.1, 48, 88.2, 96, 176.4 and 192 kHz

- Flexible clock divisor for use to generate different "spdifout" data rate
- SPDIFOUT (TX)
  - 16-word data FIFO for storage of outgoing audio data
  - 4-word user FIFO for storage of outgoing user data
  - 6-word page buffer for storage of outgoing channel status

#### 4.13.1 Signals

Table 42: S/PDIF signals

Signal	Pin	Description	I/O	Comment
SPDIF_IN	X5:58	Data In	I	
SDPIF_OUT	X5:56	Data Out	O	

#### 4.13.2 Example schematic

No special schematics are required.

#### 4.13.3 Necessary layout properties

no necessary layout properties

### 4.14 SPI

The Serial Peripheral Interface (SPI) controller supports master/slave operations up to 50 MHz (50 Mbps maximal data rate). It allows a duplex, synchronous, serial communication between the controller and external peripheral devices. It consists of 4 signals, nCS (chip select), SCK (clock), MOSI (master data out and Slave data in) and MISO (master data in and Slave data out). The data is transferred on MOSI or MISO based on the data transfer direction on every SCK edge. The receiver always receives the data on the other edge of SCK.

Features:

- Independent RX FIFO and RX FIFO
- Software controlled bit-length supports packet sizes of 1 to 32 bits
- Packed mode support for bit-length of 7 (8-bit packet size) and 15 (16-bit packet size)
- nCS can be selected to be controlled by software, or it can be generated automatically by the hardware on packet boundaries

- Receive compare mode (controller listens for a specified pattern on the incoming data before receiving the data in the FIFO)
- Simultaneous receive and transmit supported
- Supports Master and Slave modes of operation

#### 4.14.1 Signals

Table 43: SPI1A signals (1.8V level)

Signal	Pin	Description	I/O	Comment
SPI1A_MISO	X5:45	Master In/Slave Out	I	
SPI1A_MOSI	X5:51	Master Out/Slave In	O	
SPI1A_nCS0	X5:47	Chip Select	O	
SPI1A_SCK	X5:49	Serial Clock	O	
SPI1A_nIRQ	X5:43	Interrupt request	I	

Table 44: SPI2D signals (1.8V level)

Signal	Pin	Description	I/O	Comment
SPI2D_MISO	X5:7	Master In/Slave Out	I	
SPI2D_MOSI	X5:3	Master Out/Slave In	O	
SPI2D_nCS0	X5:1	Chip Select	O	
SPI2D_SCK	X5:5	Serial Clock	O	
SPI2D_nIRQ	X5:36	Interrupt request	I	

Table 45: SPI3E signals (1.8V level)

Signal	Pin	Description	I/O	Comment
SPI2D_MISO	X5:19	Master In/Slave Out	I	
SPI2D_MOSI	X5:13	Master Out/Slave In	O	
SPI2D_nCS1	X5:27	Chip Select	O	
SPI2D_SCK	X5:23	Serial Clock	O	

Table 46: SPI4C signals (1.8V level)

Signal	Pin	Description	I/O	Comment
SPI4_MISO	X5:57	Master In/Slave Out	I	
SPI4_MOSI	X5:55	Master Out/Slave In	O	
SPI4_nCS0	X5:53	Chip Select	O	
SPI4_SCK	X5:59	Serial Clock	O	

**NOTE:** SPI2 and SPI3 are not officially supported from NVIDIA. You can use them on your own risk. The SPI3 interface pins will be used as GPIOs per default.

#### 4.14.2 Example schematic

No special schematics are required.

#### 4.14.3 Necessary layout properties

no necessary layout properties

### 4.15 UART

The Universal Asynchronous Receiver Transmitter (UART) controller provides serial data synchronization and data conversion (parallel-to-serial and serial-to-parallel) for both receiver and transmitter sections. Synchronization for serial data stream is accomplished by adding start and stop bits to the transmit data to form a data character. Data integrity is accomplished by attaching a parity bit to the data character. The parity bit can be checked by the receiver for any transmission bit errors.

Features:

- Synchronization for the serial data stream with start and stop bits to transmit data and form a data character
- Supports both 16450- and 16550-compatible modes. Default mode is 16450
- Device clock up to 200 MHz, baudrate of 12.5 Mbits/second
- Data integrity by attaching parity bit to the data character
- Support for word lengths from five to eight bits, an optional parity bit and one or two stop bits
- Support for modem control inputs
- DMA capability for both TX and RX
- 8-bit x 36 deep TX FIFO
- 11-bit x 36 deep RX FIFO. 3 bits of 11 bits per entry will log the RX errors in FIFO mode (break, framing and parity errors as bits 10,9,8 of fifo entry)
- Auto sense baud detection
- Timeout interrupts to indicate if the incoming stream stopped
- Priority interrupts mechanism
- Flow control support on RTS and CTS
- Internal loopback
- SIR encoding/decoding (3/16 or 4/16 baud pulse widths to transmit bit zero)

### 4.15.1 Signals

Table 47: UART1 signals (1.8V level)

Signal	Pin	Description	I/O	Comment
UART1_RXD	X5:9	UART receive	I	
UART1_TXD	X5:11	UART transmit	O	

Table 48: UART2 signals (1.8V level)

Signal	Pin	Description	I/O	Comment
UART2_nCTS	X4:34	UART Clear-to-send	I	low active
UART2_nRTS	X4:32	UART Request-to-send	O	low active
UART2_RXD	X4:28	UART receive	I	
UART2_TXD	X4:30	UART transmit	O	

Table 49: UART3 signals (1.8V level)

Signal	Pin	Description	I/O	Comment
UART3_nCTS	X4:44	UART Clear-to-send	I	low active
UART3_nRTS	X4:42	UART Request-to-send	O	low active
UART3_RXD	X4:38	UART receive	I	
UART3_TXD	X4:40	UART transmit	O	

Table 50: UART4 (DEBUG) signals (1.8V level)

Signal	Pin	Description	I/O	Comment
UART4_DEBUG_nCTS	X4:35	UART Clear-to-send	I	low active
UART4_DEBUG_nRTS	X4:39	Request-to-send	O	low active
UART4_DEBUG_RXD	X4:41	UART receive	I	
UART4_DEBUG_TXD	X4:37	UART transmit	O	

### 4.15.2 Example schematic

No special schematics are required.

### 4.15.3 Necessary layout properties

no necessary layout properties

## 4.16 USB (HSIC)

The K1 USB complex provides a mechanism to communicate with a PC and/or USB2.0 peripherals, such as keyboard, mouse, and card readers; USB3.0 peripherals, such as camera and storage devices, as a host using regular USB 3.0 ports; and to an ob-board baseband controller using ether USB HSIC or HSI interfaces. The USB complex consists of a single USB 3.0 controller and three USB 2.0 controllers. The USB 3.0 controller supports up to 2 regular USB 3.0 ports and their companion regular USB 2.0 ports. The USB 2.0 controllers support up to: 2x regular USB ports, 2x HSIC interfaces. On the K1 Meerkat SoM is only one HSIC interface (HSIC1) routed, which is shared with USB1 (USB 2.0).

Tegra USB interfaces are compliant with the following USB specifications:

- Universal Serial Bus Specification Revision 3.0
- Universal Serial Bus Specification Revision 2.0, plus the following:
  - USB Battery Charging Specification, version 1.0; Including Data Contract Detect protocol
  - Modes: Host and Device
  - Speeds: low, Full and High
- Enhanced Host Controller Interface Specification for Universal Serial Bus revision 1.0

**USB 3.0 controller** The USB 3.0 controller (XUSB) - USB 3.0 ports only operate in USB 3.0 Super Speed (SS) mode. All USB 3.0 ports share one Super Speed Bus Instance (5Gb/s bandwidth is distributed across these ports). The XUSB controller supports:

- xHCI programming model for scheduling transactions and interface management as a host that natively support USB 3.0, USB 2.0, and USB 1.1 transactions through USB 3.0 and USB 2.0 interfaces.
- Remote wakeup, wake on connect, wake on disconnect, and wake on overcurrent in all Tegra power states, including deep sleep mode.

**USB 2.0 controller** All USB 2.0 controllers support:

- USB host controller registers and data structures are compliant to Intel<sup>TM</sup>EHCI specification. The max packet size supported on any endpoint is 1024 bytes in high-speed mode, for both device and host modes
- USB legacy (USB 1.1) Full and Low speed devices without a companion USB 1.1 host controller or host controller driver software using EHCI standard data structures.

USB 2.0 Controller #1 - Supports both USB 2.0 device and USB 2.0 host operations. USB recovery is supported only with USB 2.0 port0 (USB0\_CLIENT). USB controller #1 only connects to USB 2.0 port 0, which is the primary USB 2.0 port on the Tegra devices. This controller shares the same USB 2.0 port 0 pins with the XUSB controller.

USB 2.0 Controller #2 - Can be configured to use regular USB 2.0 port 1 (USB1) or can be configured to use an HSIC interfaces that allows connection of an on-board peripheral supporting an HSIC interface to the Tegra processor. This controller shares the same USB 2.0 port 1 pins with the XUSB controller.

USB 2.0 Controller #3 - Can be configured to use regular USB 2.0 port 2 (USB2). This controller shares the same USB 2.0 port 2 pins with the XUSB controller.

#### 4.16.1 Signals

Table 51: USB signals

Signal	Pin	Description	I/O	Comment
USB0_D_N	X2:53	USB0 (OTG) data	I/O	
USB0_D_P	X2:55	USB0 (OTG) data	I/O	
USB0_ID	X2:57	USB0 (OTG) ID	I	
USB0_VBUS	X2:59	USB0 (OTG) VBUS	P	
USB_VBUS_EN0_nOC	X3:36	USB0 enable/overcurrent	I	requires pull-up against 3.3V
USB1_D_N	X3:28	USB1 data	I/O	
USB1_D_P	X3:30	USB1 data	I/O	
USB_VBUS_EN1_nOC	X3:34	USB1 enable/overcurrent	I	requires pull-up against 3.3V
USB2_D_N	X3:18	USB2 data	I/O	
USB2_D_P	X3:16	USB2 data	I/O	
USB_VBUS_EN2_nOC	X3:54	USB2 enable/overcurrent	I	requires pull-up against 3.3V
USB3_RX0_N	X3:9	USB 3.0 receive data lane (negative). Shared with PCIe.	I	
USB3_RX0_P	X3:7	USB 3.0 receive data lane (positive). Shared with PCIe.	I	
USB3_TX0_N	X3:1	USB 3.0 transmit data lane (negative). Shared with PCIe.	O	
USB3_TX0_P	X3:3	USB 3.0 transmit data lane (positive). Shared with PCIe.	O	
PEX_USB3_RX1_N	X3:19	USB 3.0 receive data lane (negative). Shared with PCIe.	I	
PEX_USB3_RX1_P	X3:21	USB 3.0 receive data lane (positive). Shared with PCIe.	I	
PEX_USB3_TX1_N	X3:13	USB 3.0 transmit data lane (negative). Shared with PCIe.	O	
PEX_USB3_TX1_P	X3:15	USB 3.0 transmit data lane (positive). Shared with PCIe.	O	

#### 4.16.2 Example schematic

The following figure shows a schematic example of a OTG-capable USB Client port:

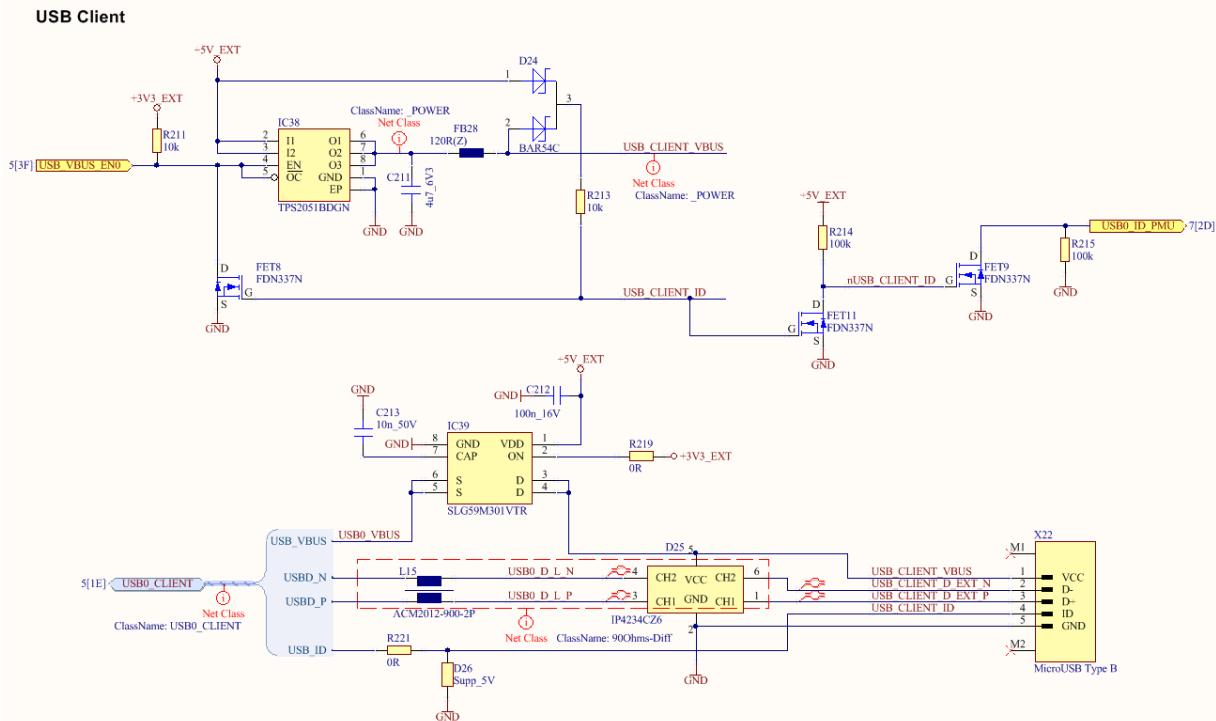


Figure 4.6: USB Client schematic example

#### 4.16.3 Necessary layout properties

Table 52: USB 2.0 interface signal routing requirements

Parameter	Requirement	Units	Notes
Max frequency (High Speed)	480 / 2083 / 240	Mbps / ns / MHz	
Max loading High Speed / Full Speed / Low Speed	10 / 150 / 600	pF	
Reference plane	GND		
Breakout region impedance	min width/spacing		
Trace impedance	90 (diff pair) / 50 (single ended)	$\Omega$	$\pm 15\%$
Via proximity (Signal to reference)	<3.8 (24)	mm (ps)	Up to 4 signal vias can share a single GND return via
Max trace delay	1280 (microstrip) / 1150 (stripline)	ps	

Parameter	Requirement	Units	Notes
Max intra-pair skew between USBx_D_P & USBx_D_N	7.5	ps	PCB routing delays for Max trace delays and max trace delay skew parameters

Table 53: USB 3.0 interface signal routing requirements

Parameter	Requirement	Units	Notes
Data rate / UI period	5.0 / 200	Gbps / ps	
Max number of loads	1	load	
Termination	90 differential	$\Omega$	On die termination TX & RX
Reference plane	GND		
Breakout region Max length	7.62	mm	4x dielectric spacing preferred
Trace impedance  Microstrip / stripline To Ref plane & capacitor pad To unrelated high-speed signals	4x / 3x 5x / 3x 5x / 4x	dielectric	
Max trace length	152	mm	Include Package & PCB routing delays for max trace delays and max trace delay skew parameters
Max PCB Via distance from BGA ball	7.62	mm	
Max intra-pair skew (RX/TX_N to RX/TX_P)	1 (0.15)	ps (mm)	PCB routing delays for Max trace delays and max trace delay skew parameters
Max intra-pair matching between subsequent discontinuities	1 (0.15)	ps (mm)	Recommended trace length matching to <1 ps before Vias or any discontinuity to minimize common mode conversion
Via placement (GND via distance)	<1x	Diff via pitch	Recommended trace length matching to <1 ps before Vias or any discontinuity to minimize common mode conversion
Max number of vias	4		
Via stub length	<0.4	mm	
AC coupling capacitor	100	nF	Discrete 0402
AC coupling capacitor location	<8 (53)	mm (ps)	

Table 54: USB 2.0 interface delays

Signal Name	Pkg Delay (ps)	SoM PCB delay (ps)	total delay (ps)
USB0_D_N	73	75.5	148.5
USB0_D_P	72	75.5	147.5
USB1_D_N	67	156.8	223.8
USB1_D_P	64	157.4	221.4
USB2_D_N	43	125.9	168.9
USB2_D_P	43	126.1	169.1

For the USB 3.0 interface delays take a look on table 34 (PCIe interface delays).

## 5 Software

This chapter contains information about the BCT and the Bootloader.

### 5.1 BCT

The BCT is a nvidia specific format, which contains initialisation data for the Tegra processor. Most importantly it includes the initial configuration for the memory controller, which is required to set timings matching the connected DDR memory modules. As those timings depend on chip characteristics as well as PCB layout data they differ between boards. Avionic Design provides a BCT file for the Meerkat processor module that is independent of the carrier board, and which can be used for flashing the Meerkat modules.

The BCT files are flashed onto the processor along with the bootloader files using the nvidia tegrarcm tool. Nvidia provides a set of helper utilities called "tegra-uboot-flasher-scripts" which ease the process of building BCT and bootloader and flashing them onto the module. BCT is a binary format which is generated using the nvidia tool called "cbootimage", which compiles clear text BCT configuration files into BCT files.

### 5.2 Bootloader

Once the Tegra has read the BCT it jumps to the initial load address from which it should load a bootloader. There are two bootloaders available for the Tegra K1:

#### **fastboot (deprecated):**

Fastboot is a minimalistic bootloader which is available in a special nvidia version supporting the Tegra K1. This was the default for early software releases but shall not be used for new projects anymore.

#### **u-boot:**

The u-boot bootloader is the default bootloader for Tegra K1 running a mainline or L4T linux system. u-boot is an open source project (<http://www.denx.de/wiki/U-Boot>) and widely used as bootloader on embedded systems, especially on ARM processors. Avionic Design has added support for the Meerkat processor module as well as the Avionic Design Evaluation Carrier to u-boot, and provides the source code on github.

### 5.3 Using **tegra-uboot-flasher-scripts**

The **tegra-uboot-flasher-scripts** can be used to build a u-boot image, generate the BCT file and flash them to a Avionic Design Evaluation Carrier equipped with a Meerkat processor module. The following steps show how to use **tegra-uboot-flasher** scripts for an Avionic Design Evaluation Carrier.

### 5.3.1 Build cross-compiling toolchain

In order to build the bootloader, you need a cross-compilation toolchain for armv7l as a prerequisite. If you already have a toolchain for the target, you can just set the environment variable CROSS\_COMPILE and skip this step. Otherwise, you may build a toolchain using the buildroot-based BSP for Meerkat from Avionic Design. The BSP has the form of a *buildroot external*. Get the BSP sources by running:

```
$ git clone https://github.com/avionic-design/buildroot-external-ad.git
```

Then follow the instructions in the file buildroot-external-ad/README to build the toolchain.

Then point the environment variable CROSS\_COMPILE to that toolchain. Assuming your buildroot root directory is \$BR\_ROOT (insert absolute path here) and you have built the BSP resp. the BSP toolchain there using the commandline

```
make O=build/meerkat-rootfs [toolchain]
```

as described in the buildroot-external-ad README, then do

```
export CROSS_COMPILE=$BR_ROOT/build/meerkat-rootfs/host/usr/bin/arm-buildroot-linux-gnueabihf-
```

If you have chosen a different directory for O=... when building the BSP, adapt accordingly.

### 5.3.2 Checkout required sources and utilities

1. Enter working-directory:

```
# mkdir -p ~/dev/tegra-linux  
# export BUILD_DIR=~/dev/tegra-linux  
# cd $BUILD_DIR
```

2. Checkout tegra-uboot-flasher-scripts from github:

```
# git clone --branch tk1/master https://github.com/avionic-design/tegra-uboot-flasher-scripts.git
```

3. Checkout helper repositories:

```
# git clone https://github.com/NVIDIA/cbootimage.git  
# git clone https://github.com/NVIDIA/tegrarcm.git  
# git clone https://git.kernel.org/pub/scm/utils/dtc/dtc.git
```

4. Checkout configuration repositories:

```
# git clone https://github.com/avionic-design/cbootimage-configs.git
```

5. Checkout u-boot

```
# git clone --branch tk1/master https://github.com/avionic-design/u-boot.git
```

### 5.3.3 Build required utilities

```
# cd $BUILD_DIR/tegra-uboot-flasher-scripts  
# ./build-tools
```

### 5.3.4 Build u-boot

Make sure that the environment variable CROSS\_COMPILE is correctly set.

```
# cd $BUILD_DIR/tegra-uboot-flasher-scripts  
# ./build --boards kein-baseboard build
```

### 5.3.5 Flash u-boot to System

1. Connect the USB debug port of the baseboard to your host PC
2. Put the carrier into recovery mode
3. Make sure that the carrier was detected on the USB host by running

```
# lsusb | grep NVidia
```

Output should look like this:

```
Bus 001 Device 011: ID 0955:7140 NVidia Corp.
```

Bus number and device may be different on your system.

4. Flash u-boot onto the system:

```
# sudo ./tegra-uboot-flasher flash kein-baseboard
```

## 6 Pinout List

In this section you will find a list of pinouts for all the connectors of the Tegra® K1 processor module towards a carrier board.

### 6.1 Connector overview

### 6.2 Connector pinout and pin-muxing

Pin	Net Name	GPIO	Tegra Ball Name	Tegra Pin Name	SF10	SF11	SF12	SF13	Power Rail	Pin State	Note
X1:1	HDMI_TXC_N	-	HDMI_TXCN	AF5	HDMI_TXCN	-	-	-	avdd_hdmi (3.3V)	-	
X1:2	HDMI_DDC_SDA	GPIO3_PV.05	DDC_SDA	AC8	I2C4_DAT	-	-	-	vddio_lv (3.3V)	z	
X1:3	HDMI_TXC_P	-	HDMI_TXCP	AF6	HDMI_TXCP	-	-	-	avdd_hdmi (3.3V)	-	
X1:4	HDMI_DDC_SCL	GPIO3_PV.04	DDC_SCL	AC7	I2C4_CLK	-	-	-	vddio_lv (3.3V)	z	
X1:5	Ground										
X1:6	HDMI_CEC	GPIO3_PEE.03	HDMI_CEC	AD7	CEC	-	-	-	vddio_lv (3.3V)	z	
X1:7	HDMI_TXD0_N	-	HDMI_TXD0N	AD5	HDMI_TXD0N	-	-	-	avdd_hdmi (3.3V)	-	
X1:8	HDMI_INT	GPIO3_PN.07	HDMI_INT	AC3	-	-	-	-	vddio_lv (3.3V)	pd	
X1:9	HDMI_TXD0_P	-	HDMI_TXD0P	AD6	HDMI_TXD0P	-	-	-	avdd_hdmi (3.3V)	-	
X1:10	eDP_HPD	GPIO3_PFF.00	DP_HPD	AC2	DP_HPD	-	-	-	vddio_lv (3.3V)	z	
X1:11	Ground										
X1:12	Ground										
X1:13	HDMI_TXD1_N	-	HDMI_TXD1N	AD4	HDMI_TXD1N	-	-	-	avdd_hdmi (3.3V)	-	
X1:14	SDMMC3_DAT3	GPIO3_PB.04	SDMMC3_DAT3	G1	SDMMC3_DAT3	-	-	-	vddio_sdmmc3 (1.8V-3.3V)	pu	
X1:15	HDMI_TXD1_P	-	HDMI_TXD1P	AD3	HDMI_TXD1P	-	-	-	avdd_hdmi (3.3V)	-	

Pin	Net Name	GPIO	Tegra Ball Name	Tegra Pin Name	SFI0	SFI1	SFI2	SFI3	Power Rail	Pin State	Note
X1:16	SDMMC3_DAT1	GPIO3_PB.06	SDMMC3_DAT1	H1	SDMMC3_DAT1	-	-	-	vddio_sdmmc3 (1.8V-3.3V)	pu	
X1:17	Ground										
X1:18	SDMMC3_CMD	GPIO3_PA.07	SDMMC3_CMD	F2	SDMMC3_CMD	-	-	-	vddio_sdmmc3 (1.8V-3.3V)	pu	
X1:19	HDMI_TXD2_N	-	HDMI_TXD2N	AD2	HDMI_TXD2N	-	-	-	avdd_hdmi (3.3V)	-	
X1:20	SDMMC3_DAT2	GPIO3_PB.05	SDMMC3_DAT2	F1	SDMMC3_DAT2	-	-	-	vddio_sdmmc3 (1.8V-3.3V)	pu	
X1:21	HDMI_TXD2_P	-	HDMI_TXD2P	AD1	HDMI_TXD2P	-	-	-	avdd_hdmi (3.3V)	-	
X1:22	SDMMC3_DAT0	GPIO3_PB.07	SDMMC3_DAT0	H2	SDMMC3_DAT0	-	-	-	vddio_sdmmc3 (1.8V-3.3V)	pu	
X1:23	Ground										
X1:24	Ground										
X1:25	DP_AUX_P	-	DP_AUX_CH0_P	AC6	I2C6_CLK	-	-	-	vddio_hv (3.3V)	z	
X1:26	SDMMC3_CLK_LB_IN	GPIO3_PEE.05	SDMMC3_CLK_LB_IN	F3	SDMMC3_CLK_LB_IN	-	-	-	vddio_sdmmc3 (1.8V-3.3V)	pd	
X1:27	DP_AUX_N	-	DP_AUX_CH0_N	AC5	I2C6_DAT	-	-	-	vddio_hv (3.3V)	z	
X1:28	SDMMC3_CLK_LB_OUT	GPIO3_PEE.04	SDMMC3_CLK_LB_OUT	F4	SDMMC3_CLK_LB_OUT	-	-	-	vddio_sdmmc3 (1.8V-3.3V)	z	
X1:29	Ground										
X1:30	SDMMC3_CLK	GPIO3_PA.06	SDMMC3_CLK	F5	SDMMC3_CLK	-	-	-	vddio_sdmmc3 (1.8V-3.3V)	pd	
X1:31	eDP3_P	-	LVDS0_TXD4P	AF4	LVDS0_TXD4P	-	-	-	avdd_lvds0_io (1.05V)	-	
X1:32	SDMMC3_nCD	GPIO3_PV.02	SDMMC3_CD_N	V24	SDMMC3_CD_N	-	-	-	vddio_sys (1.8V)	pu	
X1:33	eDP3_N	-	LVDS0_TXD4N	AF3	LVDS0_TXD4N	-	-	-	avdd_lvds0_io (1.05V)	-	
X1:34	SDMMC3_nWP	GPIO3_PQ.04	KB_COL4	AF28	-	-	-	SDMMC3_WP_N	-	vddio_sys (1.8V)	pu
X1:35	Ground										
X1:36	Ground										
X1:37	eDP0_P	-	LVDS0_TXD2P	AG6	LVDS0_TXD2P	-	-	-	avdd_lvds0_io (1.05V)	-	
X1:38	SDMMC1_nIRQ	GPIO3_PCC.05	CLK2_REQ	L4	-	-	-	-	vddio_sdmmc1 (1.8V)	z	

Pin	Net Name	GPIO	Tegra Ball Name	Tegra Pin Name	SFI0	SFI1	SFI2	SFI3	Power Rail	Pin State	Note
X1:39	eDP0_N	-	LVDS0_TXD2N	AG5	LVDS0_TXD2N	-	-	-	avdd_lvds0_io (1.05V)	-	
X1:40	SDMMC1_DAT2	GPIO3_PY.05	SDMMC1_DAT2	L1	SDMMC1_DAT2	-	-	-	vddio_sdmmc1 (1.8V)	pu	
X1:41	Ground										
X1:42	SDMMC1_DAT0	GPIO3_PY.07	SDMMC1_DAT0	L2	SDMMC1_DAT0	-	-	-	vddio_sdmmc1 (1.8V)	pu	
X1:43	eDP1_P	-	LVDS0_TXD1P	AG4	LVDS0_TXD1P	-	-	-	avdd_lvds0_io (1.05V)	-	
X1:44	SDMMC1_DAT1	GPIO3_PY.06	SDMMC1_DAT1	L3	SDMMC1_DAT1	-	-	-	vddio_sdmmc1 (1.8V)	pu	
X1:45	eDP1_N	-	LVDS0_TXD1N	AG3	LVDS0_TXD1N	-	-	-	avdd_lvds0_io (1.05V)	-	
X1:46	SDMMC1_nWP	GPIO3_PV.03	SDMMC1_WP_N	L5	SDMMC1_WP_N	-	-	-	vddio_sdmmc1 (1.8V)	pu	
X1:47	Ground										
X1:48	SDMMC1_DAT3	GPIO3_PY.04	SDMMC1_DAT3	J8	SDMMC1_DAT3	-	-	-	vddio_sdmmc1 (1.8V)	pu	
X1:49	LVDS_TXD3_N	-	LVDS0_TXD3N	AG1	LVDS0_TXD3N	-	-	-	avdd_lvds0_io (1.05V)	-	
X1:50	SDMMC1_CLK	GPIO3_PZ.00	SDMMC1_CLK	L7	SDMMC1_CLK	-	-	-	vddio_sdmmc1 (1.8V)	pd	
X1:51	LVDS_TXD3_P	-	LVDS0_TXD3P	AG2	LVDS0_TXD3P	-	-	-	avdd_lvds0_io (1.05V)	-	
X1:52	SDMMC1_CMD	GPIO3_PZ.01	SDMMC1_CMD	L8	SDMMC1_CMD	-	-	-	vddio_sdmmc1 (1.8V)	pu	
X1:53	Ground										
X1:54	CAM2_MCLK	GPIO3_PBB.00	GPIO_PBB0	AK5	-	-	-	vimclk2_alt3	vddio_cam (1.8V)	pd	
X1:55	eDP2_N	-	LVDS0_TXD0N	AJ2	LVDS0_TXD0N	-	-	-	avdd_lvds0_io (1.05V)	-	
X1:56	CAM_I2C_SCL	GPIO3_PBB.01	CAM_I2C_SCL	AF8	-	I2C3_CLK	-	-	vddio_cam (1.8V)	z	
X1:57	eDP2_P	-	LVDS0_TXD0P	AJ3	LVDS0_TXD0P	-	-	-	avdd_lvds0_io (1.05V)	-	
X1:58	CAM_I2C_SDA	GPIO3_PBB.02	CAM_I2C_SDA	AG8	-	I2C3_DAT	-	-	vddio_cam (1.8V)	z	
X1:59	Ground										

Pin	Net Name	GPIO	Tegra Ball Name	Tegra Pin Name	SFI0	SFI1	SFI2	SFI3	Power Rail	Pin State	Note
X1:60	CAM1_MCLK	GPIO3_PCC.00	CAM_MCLK	AL5	-	-	vimelk_alt3	-	vddio_cam (1.8V)	pu	
X2:1	Ground										
X2:2	DSI_B_D1_P	-	DSI_B_D1_P	AD12	DSI_B_D1_P	-	-	-	avdd_dsi_csi (1.2V)	-	
X2:3	CSI_E_D0_N	-	CSI_E_D0_N	AF9	CSI_E_D0_N	-	-	-	avdd_dsi_csi (1.2V)	-	
X2:4	DSI_B_D1_N	-	DSI_B_D1_N	AE12	DSI_B_D1_N	-	-	-	avdd_dsi_csi (1.2V)	-	
X2:5	CSI_E_D0_P	-	CSI_E_D0_P	AG9	CSI_E_D0_P	-	-	-	avdd_dsi_csi (1.2V)	-	
X2:6	Ground										
X2:7	Ground										
X2:8	DSI_B_D3_P	-	DSI_B_D3_P	AG12	DSI_B_D3_P	-	-	-	avdd_dsi_csi (1.2V)	-	
X2:9	CSI_E_CLK_P	-	CSI_E_CLK_P	AH8	CSI_E_CLK_P	-	-	-	avdd_dsi_csi (1.2V)	-	
X2:10	DSI_B_D3_N	-	DSI_B_D3_N	AF12	DSI_B_D3_N	-	-	-	avdd_dsi_csi (1.2V)	-	
X2:11	CSI_E_CLK_N	-	CSI_E_CLK_N	AJ8	CSI_E_CLK_N	-	-	-	avdd_dsi_csi (1.2V)	-	
X2:12	Ground										
X2:13	Ground										
X2:14	DSI_B_D0_P	-	DSI_B_D0_P	AJ12	DSI_B_D0_P	-	-	-	avdd_dsi_csi (1.2V)	-	
X2:15	CSI_B_D1_P	-	CSI_B_D1_P	AH9	CSI_B_D1_P	-	-	-	avdd_dsi_csi (1.2V)	-	
X2:16	DSI_B_D0_N	-	DSI_B_D0_N	AH12	DSI_B_D0_N	-	-	-	avdd_dsi_csi (1.2V)	-	
X2:17	CSI_B_D1_N	-	CSI_B_D1_N	AJ9	CSI_B_D1_N	-	-	-	avdd_dsi_csi (1.2V)	-	
X2:18	Ground										
X2:19	Ground										
X2:20	DSI_B_CLK_N	-	DSI_B_CLK_N	AJ11	DSI_B_CLK_N	-	-	-	avdd_dsi_csi (1.2V)	-	
X2:21	CSI_B_D0_N	-	CSI_B_D0_N	AK8	CSI_B_D0_N	-	-	-	avdd_dsi_csi (1.2V)	-	

Pin	Net Name	GPIO	Tegra Ball Name	Tegra Pin Name	SFI0	SFI1	SFI2	SFI3	Power Rail	Pin State	Note
X2:22	DSI_B_CLK_P	-	DSI_B_CLK_P	AH11	DSI_B_CLK_P	-	-	-	avdd_dsi_csi (1.2V)	-	
X2:23	CSI_B_D0_P	-	CSI_B_D0_P	AL8	CSI_B_D0_P	-	-	-	avdd_dsi_csi (1.2V)	-	
X2:24	Ground										
X2:25	Ground										
X2:26	DSI_B_D2_N	-	DSI_B_D2_N	AL12	DSI_B_D2_N	-	-	-	avdd_dsi_csi (1.2V)	-	
X2:27	CSI_A_D0_N	-	CSI_A_D0_N	AK9	CSI_A_D0_N	-	-	-	avdd_dsi_csi (1.2V)	-	
X2:28	DSI_B_D2_P	-	DSI_B_D2_P	AK12	DSI_B_D2_P	-	-	-	avdd_dsi_csi (1.2V)	-	
X2:29	CSI_A_D0_P	-	CSI_A_D0_P	AL9	CSI_A_D0_P	-	-	-	avdd_dsi_csi (1.2V)	-	
X2:30	Ground										
X2:31	Ground										
X2:32	DSI_A_D0_N	-	DSI_A_D0_N	AK11	DSI_A_D0_N	-	-	-	avdd_dsi_csi (1.2V)	-	
X2:33	CSI_A_D1_P	-	CSI_A_D1_P	AD9	CSI_A_D1_P	-	-	-	avdd_dsi_csi (1.2V)	-	
X2:34	DSI_A_D0_P	-	DSI_A_D0_P	AL11	DSI_A_D0_P	-	-	-	avdd_dsi_csi (1.2V)	-	
X2:35	CSI_A_D1_N	-	CSI_A_D1_N	AE9	CSI_A_D1_N	-	-	-	avdd_dsi_csi (1.2V)	-	
X2:36	Ground										
X2:37	Ground										
X2:38	DSI_A_D2_P	-	DSI_A_D2_P	AK15	DSI_A_D2_P	-	-	-	avdd_dsi_csi (1.2V)	-	
X2:39	CSI_A_CLK_P	-	CSI_A_CLK_P	AD11	CSI_A_CLK_P	-	-	-	avdd_dsi_csi (1.2V)	-	
X2:40	DSI_A_D2_N	-	DSI_A_D2_N	AL15	DSI_A_D2_N	-	-	-	avdd_dsi_csi (1.2V)	-	
X2:41	CSI_A_CLK_N	-	CSI_A_CLK_N	AE11	CSI_A_CLK_N	-	-	-	avdd_dsi_csi (1.2V)	-	
X2:42	Ground										
X2:43	Ground										
X2:44	DSI_A_CLK_P	-	DSI_A_CLK_P	AH14	DSI_A_CLK_P	-	-	-	avdd_dsi_csi (1.2V)	-	

Pin	Net Name	GPIO	Tegra Ball Name	Tegra Pin Name	SFI0	SFI1	SFI2	SFI3	Power Rail	Pin State	Note
X2:45	HSIC1_DATA	-	HSIC1_DATA	AF18	HSIC1_DATA	-	-	-	vddio_hsic (1.2V)	-	
X2:46	DSI_A_CLK_N	-	DSI_A_CLK_N	AJ14	DSI_A_CLK_N	-	-	-	avdd_dsi_csi (1.2V)	-	
X2:47	HSIC1_STROBE	-	HSIC1_STROBE	AE18	HSIC1_STROBE	-	-	-	vddio_hsic (1.2V)	-	
X2:48	Ground										
X2:49	Ground										
X2:50	DSI_A_D3_P	-	DSI_A_D3_P	AF14	DSI_A_D3_P	-	-	-	avdd_dsi_csi (1.2V)	-	
X2:51	FORCE_nRECOVERY	GPIO3_PI01	GPIO_PI1	AA6	-	-	-	-	vddio_gmi (1.8V)	pu	Pull-Up on SoM against 3.3V
X2:52	DSI_A_D3_N	-	DSI_A_D3_N	AG14	DSI_A_D3_N	-	-	-	avdd_dsi_csi (1.2V)	-	
X2:53	USB0_D_N	-	USB0_DN	AH20	USB0_DN	-	-	-	avdd_usb (3.3V)	-	
X2:54	Ground										
X2:55	USB0_D_P	-	USB0_DP	AJ20	USB0_DP	-	-	-	avdd_usb (3.3V)	-	
X2:56	DSI_A_D1_N	-	DSI_A_D1_N	AD14	DSI_A_D1_N	-	-	-	avdd_dsi_csi (1.2V)	-	
X2:57	USB0_ID	-	USB0_ID	AK20	USB0_ID	-	-	-	avdd_usb (3.3V)	-	
X2:58	DSI_A_D1_P	-	DSI_A_D1_P	AE14	DSI_A_D1_P	-	-	-	avdd_dsi_csi (1.2V)	-	
X2:59	USB0_VBUS	-	USB0_VBUS	AL20	USB0_VBUS	-	-	-	avdd_usb (3.3V)	-	
X2:60	Ground										
X3:1	USB3_TX0_N	-	USB3_TX0N	AJ21	USB3_TX0N	-	-	-	dvddio_pex (1.05V)	-	
X3:2	Ground										
X3:3	USB3_TX0_P	-	USB3_TX0P	AH21	USB3_TX0P	-	-	-	dvddio_pex (1.05V)	-	
X3:4	SATA_L0_TX_P	-	SATA_L0_TXP	AL27	SATA_L0_TXP	-	-	-	vddio_sata (1.05V)	-	
X3:5	Ground										
X3:6	SATA_L0_TX_N	-	SATA_L0_TXN	AK27	SATA_L0_TXN	-	-	-	vddio_sata (1.05V)	-	
X3:7	USB3_RX0_P	-	USB3_RX0P	AK21	USB3_RX0P	-	-	-	dvddio_pex (1.05V)	-	
X3:8	Ground										

Pin	Net Name	GPIO	Tegra Ball Name	Tegra Pin Name	SFI0	SFI1	SFI2	SFI3	Power Rail	Pin State	Note
X3:9	USB3_RX0_N	-	USB3_RX0N	AL21	USB3_RX0N	-	-	-	dvddio_pex (1.05V)	-	
X3:10	SATA_L0_RX_N	-	SATA_L0_RXN	AH27	SATA_L0_RXN	-	-	-	vddio_sata (1.05V)	-	
X3:11	Ground										
X3:12	SATA_L0_RX_P	-	SATA_L0_RXP	AJ27	SATA_L0_RXP	-	-	-	vddio_sata (1.05V)	-	
X3:13	PEX_USB3_TX1_N	-	PEX_USB3_TX1N	AG21	PEX_USB3_TX1N	-	-	-	dvddio_pex (1.05V)	-	
X3:14	Ground										
X3:15	PEX_USB3_TX1_P	-	PEX_USB3_TX1P	AF21	PEX_USB3_TX1P	-	-	-	dvddio_pex (1.05V)	-	
X3:16	USB2_D_P	-	USB2_DP	AD20	USB2_DP				avdd_usb (3.3V)	-	
X3:17	Ground										
X3:18	USB2_D_N	-	USB2_DN	AE20	USB2_DN	-	-	-	avdd_usb (3.3V)	-	
X3:19	PEX_USB3_RX1_N	-	PEX_USB3_RX1N	AL23	PEX_USB3_RX1N	-	-	-	dvddio_pex (1.05V)	-	
X3:20	Ground										
X3:21	PEX_USB3_RX1_P	-	PEX_USB3_RX1P	AK23	PEX_USB3_RX1P	-	-	-	dvddio_pex (1.05V)	-	
X3:22	PEX_CLK2_P	-	PEX_CLK2P	AC26	PEX_CLK_OUT_2_P	-	-	-	vddio_pex_ctl (3.3V)	0	
X3:23	Ground										
X3:24	PEX_CLK2_N	-	PEX_CLK2N	AC27	PEX_CLK_OUT_2_N	-	-	-	vddio_pex_ctl (3.3V)	0	
X3:25	PEX_TX2_N	-	PEX_TX2N	AJ23	PEX_TX2N	-	-	-	dvddio_pex (1.05V)	-	
X3:26	Ground										
X3:27	PEX_TX2_P	-	PEX_TX2P	AH23	PEX_TX2P	-	-	-	dvddio_pex (1.05V)	-	
X3:28	USB1_D_N	-	USB1_DN	AF20	USB1_DN	-	-	-	avdd_usb (3.3V)	-	
X3:29	Ground										
X3:30	USB1_D_P	-	USB1_DP	AG20	USB1_DP	-	-	-	avdd_usb (3.3V)	-	
X3:31	PEX_RX2_N	-	PEX_RX2N	AE21	PEX_RX2N	-	-	-	dvddio_pex (1.05V)	-	
X3:32	Ground										

Pin	Net Name	GPIO	Tegra Ball Name	Tegra Pin Name	SFI0	SFI1	SFI2	SFI3	Power Rail	Pin State	Note
X3:33	PEX_RX2_P	-	PEX_RX2P	AD21	PEX_RX2P	-	-	-	dvddio_pex (1.05V)	-	
X3:34	USB_VBUS_EN1_nOC	GPIO3_PN.05	USB_VBUS_EN1	AC1	usb_vbus_en1	-	-	-	vddio_hv (3.3V)	0	
X3:35	Ground										
X3:36	USB_VBUS_EN0_nOC	GPIO3_PN.04	USB_VBUS_EN0	AB1	usb_vbus_en0	-	-	-	vddio_hv (3.3V)	0	
X3:37	PEX_TX3_N	-	PEX_TX3N	AG23	PEX_TX3N	-	-	-	dvddio_pex (1.05V)	-	
X3:38	Ground										
X3:39	PEX_TX3_P	-	PEX_TX3P	AF23	PEX_TX3P	-	-	-	dvddio_pex (1.05V)	-	
X3:40	unconnected										
X3:41	Ground										
X3:42	GPIO_PBB4	GPIO3_PBB.04	GPIO_PBB4	AH6	VGP4	-	-	-	vddio_cam (1.8V)		
X3:43	PEX_RX3_P	-	PEX_RX3P	AL24	PEX_RX3P	-	-	-	dvddio_pex (1.05V)	-	
X3:44	PEX_L0_nCLKREQ	GPIO3_PDD.02	PEX_L0_CLKREQ_N	AK29	pe0_clkreq_l	-	-	-	vddio_pex_ctl (3.3V)	z	
X3:45	PEX_RX3_N	-	PEX_RX3N	AK24	PEX_RX3N	-	-	-	dvddio_pex (1.05V)	-	
X3:46	PEX_L0_nRST	GPIO3_PDD.01	PEX_L0_RST_N	AJ29	pe0_rst_l	-	-	-	vddio_pex_ctl (3.3V)	z	
X3:47	Ground										
X3:48	PEX_L1_nCLKREQ	GPIO3_PDD.06	PEX_L1_CLKREQ_N	AJ30	pe1_clkreq_l	-	-	-	vddio_pex_ctl (3.3V)	z	
X3:49	PEX_RX4_N	-	PEX_RX4N	AL26	PEX_RX4N	-	-	-	dvddio_pex (1.05V)	-	
X3:50	PEX_L1_nRST	GPIO3_PDD.05	PEX_L1_RST_N	AJ31	pe1_rst_l	-	-	-	vddio_pex_ctl (3.3V)	z	
X3:51	PEX_RX4_P	-	PEX_RX4P	AK26	PEX_RX4P	-	-	-	dvddio_pex (1.05V)	-	
X3:52	PEX_nWAKE	GPIO3_PDD.03	PEX_WAKE_N	AG28	pe_wake_l	-	-	-	vddio_pex_ctl (3.3V)	z	
X3:53	Ground										
X3:54	USB_VBUS_EN2_nOC	GPIO3_PFF.01	USB_VBUS_EN2	AG29	usb_vbus_en2	-	-	-	vddio_pex_ctl (3.3V)	0	
X3:55	PEX_TX4_P	-	PEX_TX4P	AJ26	PEX_TX4P	-	-	-	dvddio_pex (1.05V)	-	

Pin	Net Name	GPIO	Tegra Ball Name	Tegra Pin Name	SFI0	SFI1	SFI2	SFI3	Power Rail	Pin State	Note
X3:56	Ground										
X3:57	PEX_TX4_N	-	PEX_TX4N	AH26	PEX_TX4N	-	-	-	vddio_pex (1.05V)	-	
X3:58	PEX_CLK1_N	-	PEX_CLK1N	AG26	PEX_CLK_OUT_1_N	-	-	-	vddio_pex_ctl (3.3V)	0	
X3:59	Ground										
X3:60	PEX_CLK1_P	-	PEX_CLK1P	AF26	PEX_CLK_OUT_1_P	-	-	-	vddio_pex_ctl (3.3V)	0	
X4:1	Ground										
X4:2	GPIO_PK3	GPIO3_PK.03	GPIO_PK3	R2	SDMMC2A_DAT4	tracectl	-	-	vddio_gmi (1.8V)	pu	
X4:3	GPIO_PK1	GPIO3_PK.01	GPIO_PK1	R3	SDMMC2A_CLK	traceclk	-	-	vddio_gmi (1.8V)	pd	
X4:4	GPIO_PI5	GPIO3_PI.05	GPIO_PI5	U7	SDMMC2A_DAT1	-	-	-	vddio_gmi (1.8V)	pu	
X4:5	GPIO_PI7	GPIO3_PI.07	GPIO_PI7	Y4	-	tracedata7	-	DTV_ERR_PSYNC	vddio_gmi (1.8V)	pu	
X4:6	GPIO_PH6	GPIO3_PH.06	GPIO_PH6	U8	SDMMC2A_DAT3	tracedata3	-	DTV_DATA	vddio_gmi (1.8V)	pu	
X4:7	GPIO_PH5	GPIO3_PH.05	GPIO_PH5	R4	SDMMC2A_DAT2	-	-	-	vddio_gmi (1.8V)	pd	
X4:8	GPIO_PK2	GPIO3_PK.02	GPIO_PK2	Y1	-	-	-	-	vddio_gmi (1.8V)	pu	
X4:9	BL_EN	GPIO3_PH.04	GPIO_PH4	R5	SDMMC2A_DAT0	-	-	-	vddio_gmi (1.8V)	pu	
X4:10	GPIO_PJ0	GPIO3_PJ.00	GPIO_PJ0	U6	-	-	-	-	vddio_gmi (1.8V)	pu	
X4:11	BL_PWM	GPIO3_PH.02	GPIO_PH2	AA4	PM3_PWM2	-	-	-	vddio_gmi (1.8V)	pd	
X4:12	FAN_PWM	GPIO3_PH.00	GPIO_PH0	Y6	PM3_PWM0	tracedata2	-	DTV_VALID	vddio_gmi (1.8V)	pd	
X4:13	Ground										
X4:14	GPIO_PK0	GPIO3_PK.00	GPIO_PK0	AA1	-	-	-	soc_therm_oc3_n	vddio_gmi (1.8V)	pu	
X4:15	JTAG_TCK	-	JTAG_TCK	H6	JTAG_TCK	-	-	-	vddio_sys_2 (1.8V)	-	
X4:16	Ground										
X4:17	JTAG_TMS	-	JTAG_TMS	J5	JTAG_TMS	-	-	-	vddio_sys_2 (1.8V)	pu	

Pin	Net Name	GPIO	Tegra Ball Name	Tegra Pin Name	SFI0	SFI1	SFI2	SFI3	Power Rail	Pin State	Note
X4:18	SPI4C_nCS1	GPIO3_PI.04	GPIO_PI4	Y9	SPI4C_CS1	tracedata6	-	-	vddio_gmi (1.8V)	pd	
X4:19	JTAG_TDI	-	JTAG_TDI	H5	JTAG_TDI	-	-	-	vddio_sys_2 (1.8V)	pu	
X4:20	GPIO_PH3	GPIO3_PH.03	GPIO_PH3	V8	PM3_PWM3	-	-	-	vddio_gmi (1.8V)	pd	
X4:21	JTAG_nTRST	-	JTAG_TRST_N	H4	JTAG_TRST_N	-	-	-	vddio_sys_2 (1.8V)	pd	
X4:22	GPIO_PK4	GPIO3_PK.04	GPIO_PK4	T1	SDMMC2A_DAT5	-	-	-	vddio_gmi (1.8V)	pu	
X4:23	JTAG_RTCK	-	JTAG_RTCK	J2	JTAG_RTCK	-	-	-	vddio_sys_2 (1.8V)	pu	
X4:24	GPIO_PI2	GPIO3_PI.02	GPIO_PI2	V1	SDMMC2A_DAT6	tracedata5	-	-	vddio_gmi (1.8V)	pu	
X4:25	JTAG_TDO	-	JTAG_TDO	J1	JTAG_TDO	-	-	-	vddio_sys_2 (1.8V)	0	
X4:26	Ground										
X4:27	unconnected										
X4:28	UART2_RXD	GPIO3_PC.03	UART2_RXD	L9	IR3_RXD	-	-	-	vddio_uart (1.8V)	pu	
X4:29	Ground										
X4:30	UART2_TXD	GPIO3_PC.02	UART2_TXD	M8	IR3_TXD	-	-	-	vddio_uart (1.8V)	pu	
X4:31	unconnected										
X4:32	UART2_nRTS	GPIO3_PJ.06	UART2_RTS_N	P4	-	UB3_RTS	-	-	vddio_uart (1.8V)	pu	
X4:33	Ground										
X4:34	UART2_nCTS	GPIO3_PJ.05	UART2_CTS_N	M1	-	UB3_CTS	-	-	vddio_uart (1.8V)	pu	
X4:35	UART4_DEBUG_nCTS	GPIO3_PB.01	GPIO_PB1	V9	UD3_CTS	-	-	-	vddio_gmi (1.8V)	z	
X4:36	GPIO_PJ2	GPIO3_PJ.02	GPIO_PJ2	W1	-	-	-	soc_therm_oc4_n	vddio_gmi (1.8V)	pu	
X4:37	UART4_DEBUG_RXD	GPIO3_PJ.07	GPIO_PJ7	V4	UD3_RXD	-	-	-	vddio_gmi (1.8V)	z	
X4:38	UART3_RXD	GPIO3_PW.07	UART3_RXD	M3	UC3_RXD	-	-	-	vddio_uart (1.8V)	pu	
X4:39	UART4_DEBUG_nRTS	GPIO3_PK.07	GPIO_PK7	V5	UD3_RTS	-	-	-	vddio_gmi (1.8V)	z	

Pin	Net Name	GPIO	Tegra Ball Name	Tegra Pin Name	SFI0	SFI1	SFI2	SFI3	Power Rail	Pin State	Note
X4:40	UART3_TXD	GPIO3_PW.06	UART3_TXD	M2	UC3_TXD	-	-	-	vddio_uart (1.8V)	pu	
X4:41	UART4_DEBUG_RXD	GPIO3_PB.00	GPIO_PB0	U4	UD3_RXD	-	-	-	vddio_gmi (1.8V)	z	
X4:42	UART3_nRTS	GPIO3_PC.00	UART3_RTS_N	R9	UC3_RTS	-	-	-	vddio_uart (1.8V)	pu	
X4:43	GEN2_I2C_nIRQ	GPIO3_PC.07	GPIO_PC7	U1	-	-	-	-	vddio_gmi (1.8V)	pu	
X4:44	UART3_nCTS	GPIO3_PA.01	UART3_CTS_N	R8	UC3_CTS	-	-	-	vddio_uart (1.8V)	pu	
X4:45	GEN2_I2C_SCL	GPIO3_PT.05	GEN2_I2C_SCL	Y2	I2C2_CLK	-	-	-	vddio_gmi (3.3V)	z	
X4:46	Ground										
X4:47	GEN2_I2C_SDA	GPIO3_PT.06	GEN2_I2C_SDA	AA2	I2C2_DAT	-	-	-	vddio_gmi (3.3V)	z	
X4:48	SDMMC1_PWR_EN	GPIO3_PU.01	GPIO_PU1	P2	-	UA3_RXD	-	-	vddio_uart (1.8V)	z	
X4:49	Ground										
X4:50	CLK3_OUT	GPIO3_PEE.00	CLK3_OUT	P7	experiph3_clk	-	-	-	vddio_uart (1.8V)	z	
X4:51	DAP4_SCLK	GPIO3_PP.07	DAP4_SCLK	N1	I2S3_SCLK	-	-	-	vddio_uart (1.8V)	pd	
X4:52	HDMI_VDD_EN	GPIO3_PH.01	GPIO_PH1	U3	PM3_PWM1	-	-	-	vddio_gmi (1.8V)	pd	
X4:53	DAP4_FS	GPIO3_PP.04	DAP4_FS	P1	I2S3_LRCK	-	-	-	vddio_uart (1.8V)	pd	
X4:54	CAM1_PWDN	GPIO3_PBB.05	GPIO_PBB5	AH5	VGP5	-	-	-	vddio_cam (1.8V)	pd	
X4:55	DAP4_DIN	GPIO3_PP.05	DAP4_DIN	P3	I2S3_SDATA_IN	-	-	-	vddio_uart (1.8V)	pd	
X4:56	CAM_nRST	GPIO3_PBB.03	GPIO_PBB3	AK6	VGP3	-	-	-	vddio_cam (1.8V)	pd	
X4:57	DAP4_DOUT	GPIO3_PP.06	DAP4_DOUT	P5	I2S3_SDATA_OUT	-	-	-	vddio_uart (1.8V)	pd	
X4:58	CAM2_PWDN	GPIO3_PBB.06	GPIO_PBB6	AL6	-	-	-	-	vddio_cam (1.8V)	pd	
X4:59	Ground										
X4:60	BOOT_SEC										Pull-Down on SoM against GND

Pin	Net Name	GPIO	Tegra Ball Name	Tegra Pin Name	SFI0	SFI1	SFI2	SFI3	Power Rail	Pin State	Note
X5:1	SPI2D_nCS0	GPIO3_PS.05	KB_ROW13	AF29	-	-	SPI2D_nCS0 <sup>1</sup>	-	vddio_sys (1.8V)	pd	
X5:2	GEN1_I2C_SCL	GPIO3_PC.04	GEN1_I2C_SCL	P6	I2C1_CLK	-	-	-	vddio_uart (1.8V)	z	
X5:3	SPI2D_MOSI	GPIO3_PQ.00	KB_COL0	AD30	-	-	SPI2D_DOUT <sup>(1)</sup>	-	vddio_sys (1.8V)	pu	
X5:4	GEN1_I2C_SDA	GPIO3_PC.05	GEN1_I2C_SDA	M6	I2C1_DAT	-	-	-	vddio_uart (1.8V)	z	
X5:5	SPI2D_SCK	GPIO3_PS.06	KB_ROW14	AC30	-	-	SPI2D_SCK <sup>(1)</sup>	-	vddio_sys (1.8V)	pd	
X5:6	Ground										
X5:7	SPI2D_MISO	GPIO3_PQ.01	KB_COL1	AC28	-	-	SPI2D_DIN <sup>(1)</sup>	-	vddio_sys (1.8V)	pu	
X5:8	GPIO_PW2	GPIO3_PW.02	GPIO_W2_AUD	M28	-	-	-	-	vddio_audio (1.8V)	pu	
X5:9	UART1_RXD	GPIO3_PS.02	KB_ROW10	AA31	-	-	-	UA3_RXD	vddio_sys (1.8V)	pd	
X5:10	W_DISABLE	GPIO3_PX.07	GPIO_X7_AUD	P28	-	-	-	-	vddio_audio (1.8V)	pd	
X5:11	UART1_TXD	GPIO3_PS.01	KB_ROW9	AA28	-	-	-	UA3_TXD	vddio_sys (1.8V)	pd	
X5:12	GPIO_PX6	GPIO3_PX.06	GPIO_X6_AUD	N31	-	-	-	-	vddio_audio (1.8V)	pu	
X5:13	GPIO_PO1	GPIO3_PO.01	ULPI_DATA0	AF15	SPI3E_DOUT <sup>(1)</sup>	-	-	-	vddio_bb (1.8V)	pu	
X5:14	GEN1_I2C_nIRQ	GPIO3_PX.05	GPIO_X5_AUD	R31	-	-	-	-	vddio_audio (1.8V)	pu	
X5:15	Ground										
X5:16	GPIO_PR5	GPIO3_PR.05	KB_ROW5	Y31	-	-	-	-	vddio_sys (1.8V)	pd	
X5:17	EN_LVDS_EDP	GPIO4									AS3722 PMU Pin B3
X5:18	GPIO_PP2	GPIO3_PP.02	DAP3_DOUT	AE17	I2S2_SDATA_OUT	-	-	-	vddio_bb (1.8V)	pd	
X5:19	GPIO_PO2	GPIO3_PO.02	ULPI_DATA1	AH15	SPI3E_DIN <sup>(1)</sup>	-	-	-	vddio_bb (1.8V)	pu	
X5:20	GPIO_PR4	GPIO3_PR.04	KB_ROW4	Y29	-	-	-	-	vddio_sys (1.8V)	pd	
X5:21	SPI1A_nIRQ	GPIO3_PP.01	DAP3_DIN	AF17	I2S2_SDATA_IN	-	-	-	vddio_bb (1.8V)	pd	
X5:22	HEAD_DET	GPIO3_PR.07	KB_ROW7	Y30	-	-	-	-	vddio_sys (1.8V)	pd	
X5:23	GPIO_PO3	GPIO3_PO.03	ULPI_DATA2	AD17	SPI3E_SCK <sup>(1)</sup>	-	-	-	vddio_bb (1.8V)	pu	
X5:24	Ground										
X5:25	SDMMC3_VDD_EN	GPIO3_PR.00	KB_ROW0	W31	-	-	-	-	vddio_sys (1.8V)	pd	
X5:26	unconnected										
X5:27	GPIO_PO4	GPIO3_PO.04	ULPI_DATA3	AJ15	SPI3E_CS1 <sup>(1)</sup>	-	-	-	vddio_bb (1.8V)	pu	

Pin	Net Name	GPIO	Tegra Ball Name	Tegra Pin Name	SFI0	SFI1	SFI2	SFI3	Power Rail	Pin State	Note
X5:28	unconnected										
X5:29	GPIO_PR6	GPIO3_PR.06	KB_ROW6	AB31	-	-	DCA_LSPII	-	vddio_sys (1.8V)	pd	
X5:30	unconnected										
X5:31	SOC_ALIVE	GPIO3_PT.00	KB_ROW16	AA26	-	-	-	-	vddio_sys (1.8V)	pd	
X5:32	unconnected										
X5:33	Ground										
X5:34	unconnected										
X5:35	unconnected										
X5:36	SPI2D_nIRQ	GPIO3_PX.03	GPIO_X3_AUD	M30	-	-	-	-	vddio_audio (1.8V)	pu	
X5:37	Ground										
X5:38	AUDIO_EN	GPIO3_PR.02	KB_ROW2	AF30	-	-	-	-	vddio_sys (1.8V)	pd	
X5:39	SATA_PWR_EN	GPIO3_PEE.02	DAP_MCLK1_REQ	M31	-	-	SATA_DEV_SLP	-	vddio_audio (1.8V)	pd	
X5:40	Ground										
X5:41	SATA_LED	GPIO3_PN.02	DAP1_DOUT	L28	I2S0_SDATA_OUT	-	-	-	vddio_audio (1.8V)	pd	
X5:42	DAP_MCLK1	GPIO3_PW.04	DAP_MCLK1	L29	extperiph1_clk	-	-	-	vddio_audio (1.8V)	pd	
X5:43	GPIO_PW3	GPIO3_PW.03	GPIO_W3_AUD	J30	-	-	-	-	vddio_audio (1.8V)	pu	
X5:44	DAP2_FS	GPIO3_PA.02	DAP2_FS	R30	I2S1_LRCK	-	-	-	vddio_audio (1.8V)	pd	
X5:45	SPI1A_MISO	GPIO3_PY.01	ULPI_DIR	AL18	SPI1A_DIN	-	-	-	vddio_bb (1.8V)	z	
X5:46	DAP2_DIN	GPIO3_PA.04	DAP2_DIN	L30	I2S1_SDAT_IN	-	-	-	vddio_audio (1.8V)	pd	
X5:47	SPI1A_nCS0	GPIO3_PY.03	ULPI_STP	AL16	SPI1A_CS0	-	-	-	vddio_bb (1.8V)	z	
X5:48	DAP2_DOUT	GPIO3_PA.05	DAP2_DOUT	J29	I2S1_SDAT_OUT	-	-	-	vddio_audio (1.8V)	pd	
X5:49	SPI1A_SCK	GPIO3_PY.02	ULPI_NXT	AG15	SPI1A_SCK	-	-	-	vddio_bb (1.8V)	z	
X5:50	DAP2_SCLK	GPIO3_PA.03	DAP2_SCLK	M29	I2S1_SCLK	-	-	-	vddio_audio (1.8V)	pd	
X5:51	SPI1A_MOSI	GPIO3_PY.00	ULPI_CLK	AK17	SPI1A_DOUT	-	-	-	vddio_bb (1.8V)	z	
X5:52	Ground										

Pin	Net Name	GPIO	Tegra Ball Name	Tegra Pin Name	SFI0	SFI1	SFI2	SFI3	Power Rail	Pin State	Note
X5:53	SPI4C_nCS0	GPIO3_PI.03	GPIO_PI3	V7	-	-	-	SPI4C_CS0	vddio_gmi (1.8V)	pu	
X5:54	GPIO_PP0	GPIO3_PP.00	DAP3_FS	AE15	I2S2_LRCK	-	-	-	vddio_bb (1.8V)	pd	
X5:55	SPI4C_MOSI	GPIO3_PG.06	GPIO_PG6	Y8	-	-	-	SPI4C_DOUT	vddio_gmi (1.8V)	z	
X5:56	SPDIF_OUT	GPIO3_PK.05	SPDIF_OUT	AC4	SPDIF_OUT	-	-	-	vddio_hv (3.3V)	pu	
X5:57	SPI4C_MISO	GPIO3_PG.07	GPIO_PG7	V3	-	-	-	SPI4C_DIN	vddio_gmi (1.8V)	z	
X5:58	SPDIF_IN	GPIO3_PK.06	SPDIF_IN	AA8	SPDIF_IN	-	-	-	vddio_hv (3.3V)	pd	
X5:59	SPI4C_SCK	GPIO3_PG.05	GPIO_PG5	AA3	-	-	-	SPI4C_SCK	vddio_gmi (1.8V)	z	
X5:60	CODEC_nIRQ	GPIO3_PU.05	GPIO_PU5	M4	-	-	-	-	vddio_uart (1.8V)	z	
X6:1	Ground										
X6:2	Ground										
X6:3	Ground										
X6:4	Ground										
X6:5	Ground										
X6:6	Ground										
X6:7	Ground										
X6:8	Ground										
X6:9	Ground										
X6:10	Ground										
X6:11	+5V_SYS										
X6:12	+5V_SYS										
X6:13	+5V_SYS										
X6:14	+5V_SYS										
X6:15	+5V_SYS										
X6:16	+5V_SYS										
X6:17	+5V_SYS										
X6:18	+5V_SYS										
X6:19	+5V_SYS										
X6:20	+5V_SYS										

Pin	Net Name	GPIO	Tegra Ball Name	Tegra Pin Name	SFI0	SFI1	SFI2	SFI3	Power Rail	Pin State	Note
X6:21	+5V_SYS										
X6:22	+5V_SYS										
X6:23	+5V_SYS										
X6:24	+5V_SYS										
X6:25	+5V_SYS										
X6:26	+2V5_AON_RTC										AS3722 PMU H2
X6:27	Ground										
X6:28	Ground										
X6:29	Ground										
X6:30	Ground										
X6:31	Ground										
X6:32	Ground										
X6:33	USB0_ID_PMU										AS3722 PMU B11
X6:34	unconnected										
X6:35	+1V8_VDDIO										
X6:36	+1V8_VDDIO										
X6:37	nRESET_COM										Pull-Up on SoM against 2.5V
X6:38	nPOWER_GOOD										Pull-Up on SoM against 5V
X6:39	nRESET_PERIPH										Pull-Up on SoM against 1.8V
X6:40	+VBAT_BKUP										RTC Batterie Voltage
X6:41	nONKEY										Pull-Up on SoM against 2.5V
X6:42	+3V3_SYS										
X6:43	nWAKEUP_POWER										pull-up required on carrier against +2V5_AON_RTC
X6:44	+3V3_SYS										
X6:45	WAKEUP_LID										pull-down required on carrier
X6:46	+3V3_SYS										

Pin	Net Name	GPIO	Tegra Ball Name	Tegra Pin Name	SFI0	SFI1	SFI2	SFI3	Power Rail	Pin State	Note
X6:47	PMU_GPIOA										AS3722 PMU GPIO
X6:48	+3V3_SYS										
X6:49	PMU_GPIOB										AS3722 PMU GPIO
X6:50	+3V3_SYS										
X6:51	Ground										
X6:52	Ground										
X6:53	Ground										
X6:54	Ground										
X6:55	Ground										
X6:56	Ground										
X6:57	Ground										
X6:58	Ground										
X6:59	Ground										
X6:60	Ground										

<sup>1</sup>NVIDIA does not officially support these interfaces. You can use them on your own risk.

## 7 Reference documents

In the following chapter, you can find a list of documents that will provide you with more information on the processor module and the carrier.

You can find information about the Tegra® K1 SoC on their website:

<https://developer.nvidia.com/>

Technical Reference Manual (TRM) for Tegra® K1 processor module

**Please note:**

To access the TRM, you need to follow these steps:

1. Be registered on the NVIDIA® Developer website
2. Apply for the Tegra™ Registered Developer Program through your account settings.

## 8 Contact



Figure 8.1: head office in Duvenstedt (Germany)

If you have any questions about the Tegra® K1 processor module, you can contact us at:

Avionic Design GmbH  
Wragekamp 10  
22397 Hamburg  
Germany

Fon: +49 40-88187-0  
Fax: +49 40-88187-150  
E-Mail: [info@avionic-design.de](mailto:info@avionic-design.de)

[www.avionic-design.de](http://www.avionic-design.de)