MT7621AN mother board

Oolite V8.0 Dev V1.0.3 Spec

Specification Version 1.0.3

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May 26, 2018

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Revision	Date	Contents of Revision Change	Remark
1.0.1	2017-05-24	First release	
1.0.2	2017-05-26	Add block Diagram	
1.0.3	2018-05-26	New Version	

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1 INTRODUTION

The OoliteV8.0 Dev board is the mother board for the OoliteV8.0 which intergrates MT7621AN Soc，DDR2, SPI Flash in one 50*50mm core board. The OoliteV8.0 Dev lateset version can provide full function extension delivered from core board including:

One USB 3.0 Superspeed PORT and One USB 2.0 Highspeed PORT.

Two SATA 3.0 PORTS supporting 2.5' or 3.5' HDD ,SDD as well

Three PCIE SLOTS supporting "WiFi PCIE Card "or "4G PCIE Card"

Five PORTS GbE which features switch function

Others：

One USB hub on Dev Board providing three PCIE SLOTts full USB 2.0 function

One SD-XC Bus expands TF Card supporting or nand flash supporting（reseverd）

One Series hearder plugs up to 56pins (position number :J9) providing RGMII, I2C, UART,JTAG function or GPIOS usage.

Two 5V 2A Power modules on board which increases one more than last version

Three 3.3V 2A Power modules on board which increase two more than last version

Attention&notes:

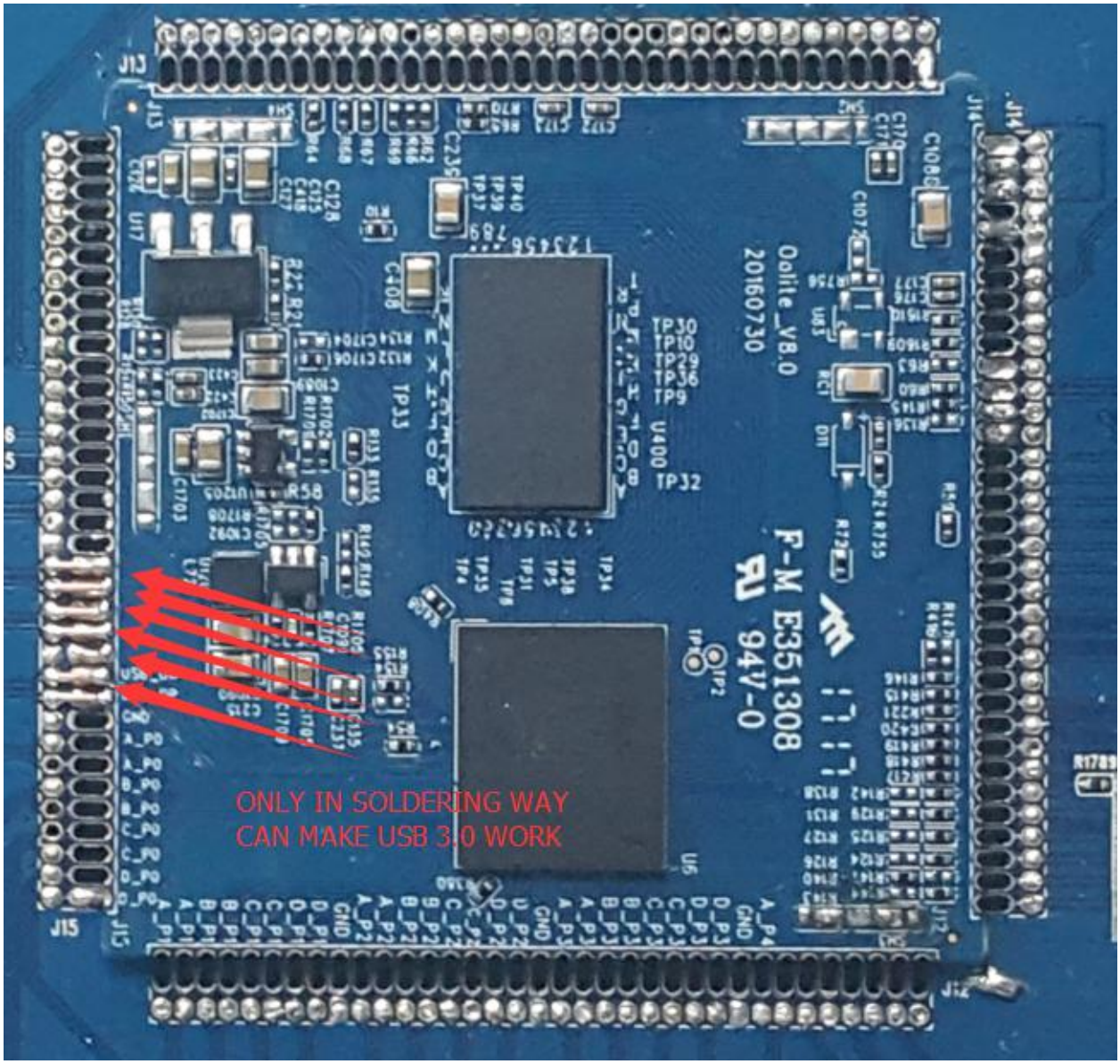
1.USB 3.0 Superspeed port can only work on USB 2.0 BUS even one USB 3.0 device attached when V8.0 core board assembled on V8.0 DEV board by steel pin Connection。

The reason is that steel pin connection instead of stamp hole soldering will cause Signal Integrity problem ，resulting in USB device can only work on USB 2.0 BUS.

However, if USB 3.0 function is required. we strongly suggest that core board soldering on mother board directly and make the related tests in factory for shipment.

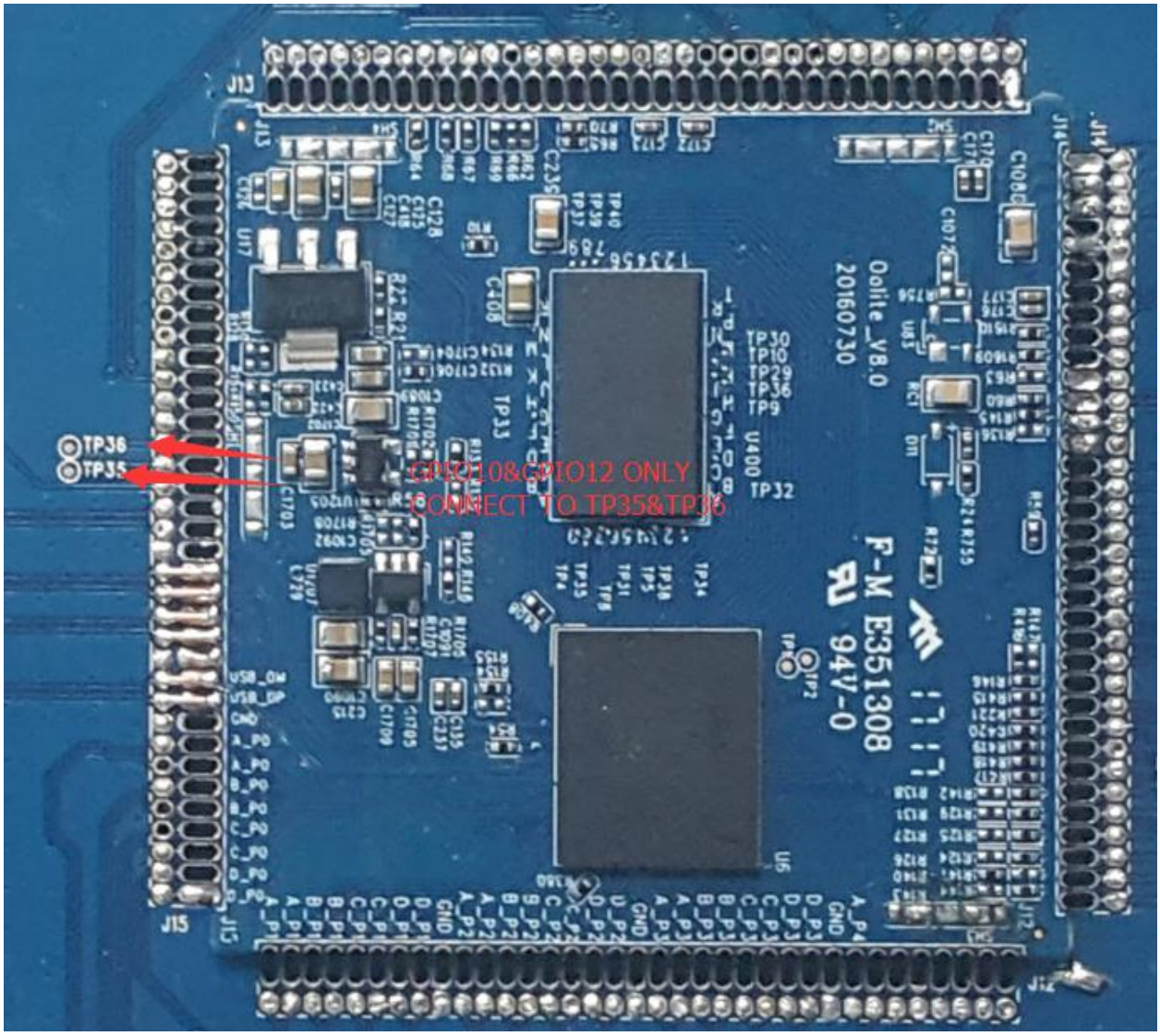
Soldering actions about core board and mother board out of factory can result in USB 3.0 function failure.

Shown as picture following:


ONLY IN SOLDERING WAY
CAN MAKE USB 3.0 WORK
F-M E351308
94V-0
Oolite_V8.0
20160730

2.TP35&TP36 on DEV board should have been connect to J9 (position number)for GPIOS extension .But they(GPIO12&GPIO10) did only connect to TP35&TP36 only for simplicity.

Shown as picture following:



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3.One PCIE SLOT and SATA chip co-use one PCIE bus by resistor jumping.

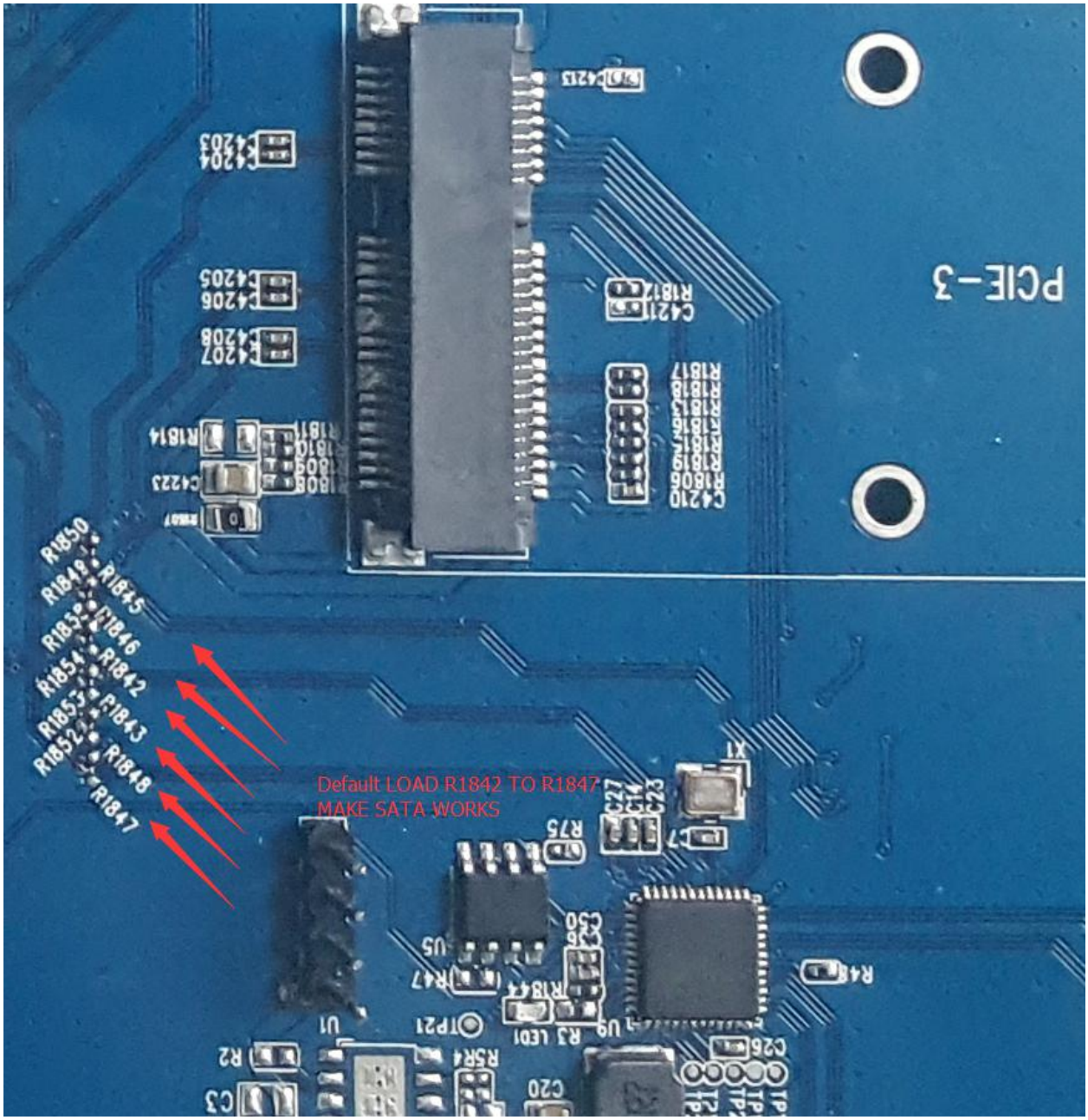
R1842,R1843,R1844, R1845,R1846,R1847,R1848 Load ,

R1849,R1850,R1852,R1853,R1854,R1855,R1812 NC make the SATA function work.(default)

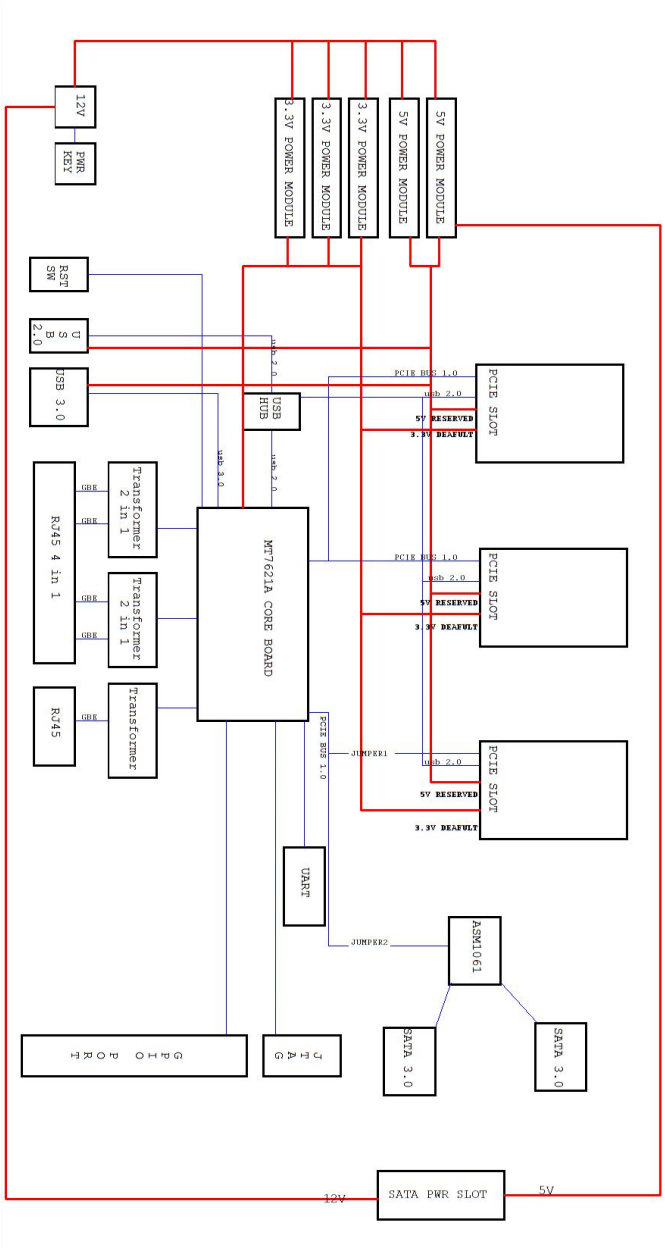
R1849,R1850,R1852,R1853,R1854,R1855,R1812 Load ,

R1842,R1843,R1844, R1845,R1846,R1847,R1848 NC make the PCIE-3 function work.

Shown as picture following:

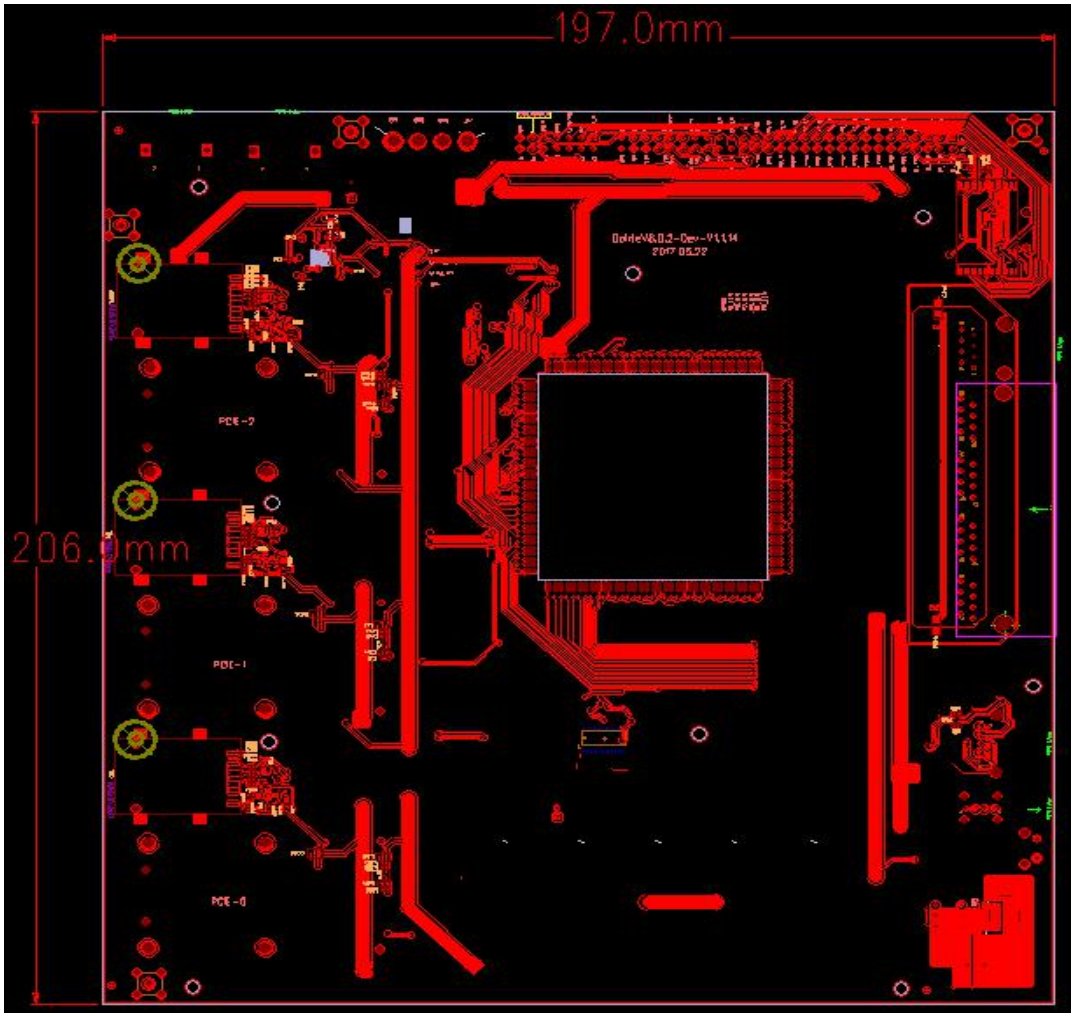

PCIE-3
Default LOAD R1842 TO R1847
MAKE SATA WORKS

2 BLOCK DIAGRAM



3 MECHANICAL

Dimensions (mm)	Length	Width	Height
	206 (Tolerance:±0.2mm)	197 (Tolerance:±0.2mm)	15 (Tolerance:±0.2mm)



4 PICTURES

5 PINS DESCRIPTION

Pin NO.	Function	Description
1	ESW_TXVN_D_P4	Gigabit Port4_D-
2	ESW_TXVP_D_P4	Gigabit Port4_D+
3	ESW_TXVN_C_P4	Gigabit Port4_C-
4	ESW_TXVP_C_P4	Gigabit Port4_C+
5	ESW_TXVN_B_P4	Gigabit Port4_B-
6	ESW_TXVP_B_P4	Gigabit Port4_B+
7	ESW_TXVN_A_P4	Gigabit Port4_A-
8	ESW_TXVP_A_P4	Gigabit Port4_A+
9	GND	Ground
10	ESW_TXVN_D_P3	Gigabit Port3_D-
11	ESW_TXVP_D_P3	Gigabit Port3_D+
12	ESW_TXVN_C_P3	Gigabit Port3_C-
13	ESW_TXVP_C_P3	Gigabit Port3_C+
14	ESW_TXVN_B_P3	Gigabit Port3_B-
15	ESW_TXVP_B_P3	Gigabit Port3_B+
16	ESW_TXVN_A_P3	Gigabit Port3_A-
17	ESW_TXVP_A_P3	Gigabit Port3_A+
18	GND	Ground
19	ESW_TXVN_D_P2	Gigabit Port2_D-
20	ESW_TXVP_D_P2	Gigabit Port2_D+
21	ESW_TXVN_C_P2	Gigabit Port2_C-
22	ESW_TXVP_C_P2	Gigabit Port2_C+
23	ESW_TXVN_B_P2	Gigabit Port2_B-
24	ESW_TXVP_B_P2	Gigabit Port2_B+
25	ESW_TXVN_A_P2	Gigabit Port2_A-
26	ESW_TXVP_A_P2	Gigabit Port2_A+
27	GND	Ground
28	ESW_TXVN_D_P1	Gigabit Port1_D-
29	ESW_TXVP_D_P1	Gigabit Port1_D+
30	ESW_TXVN_C_P1	Gigabit Port1_C-
31	ESW_TXVP_C_P1	Gigabit Port1_C+

32	ESW_TXVN_B_P1	Gigabit Port1_B-
33	ESW_TXVP_B_P1	Gigabit Por1_B+
34	ESW_TXVN_A_P1	Gigabit Port1_A-
35	ESW_TXVP_A_P1	Gigabit Por1_A+
36	ESW_TXVN_D_P0	Port #0 MDI Transceivers
37	ESW_TXVP_D_P0	Port #0 MDI Transceivers
38	ESW_TXVN_C_P0	Port #0 MDI Transceivers
39	ESW_TXVP_C_P0	Port #0 MDI Transceivers
40	ESW_TXVN_B_P0	Port #0 MDI Transceivers
41	ESW_TXVP_B_P0	Port #0 MDI Transceivers
42	ESW_TXVN_A_P0	Port #0 MDI Transceivers
43	ESW_TXVP_A_P0	Port #0 MDI Transceivers
44	GND	Ground
45	USB_DP	SB Port0 HS/FS/LS data pin Data+ (USB3.0)
46	USB_DM	USB Port0 HS/FS/LS data pin Data- (USB3.0)
47	GND	Ground
48	SSUSB_RXP	USB Port0 SS data pin RX+ (USB3.0)
49	SSUSB_RXN	USB Port0 SS data pin RX+-(USB3.0)
50	SSUSB_TXN	USB Port0 SS data pin TX- (USB3.0)
51	SSUSB_TXP	USB Port0 SS data pin TX+ (USB3.0)
52	GND	Ground
53	USB_DP_1P	USB Port1 data pin Data+ (USB2.0)
54	USB_DM_1P	USB Port1 data pin Data- (USB2.0)
55	RXD3	UART RX Data
56	MT6605_INT(TP35)	UART RX Data
57	MT6605_IRQ(TP36)	UART Clear To Send
58	CTS3_N	UART Clear To Send
59	RTS2_N	UART Request To Send
60	TXD3	UART TX Data
61	GND	Ground
62	ND_CLE	NAND Flash Command Latch Enable
63	ND_WE_N	NAND Flash Write Enable
64	ND_WP	NAND Flash Write Protect
65	ND_ALE	NAND Flash ALE Latch Enable
66	ND_CS_N	NAND Flash Chip Select
67	ND_RE_N	NAND Flash Read Enable
68	ND_RB_N	NAND Flash Ready/Busy
69	ND_D0	NAND Flash Data0
70	ND_D1	NAND Flash Data1

71	ND_D2	NAND Flash Data2
72	ND_D3	NAND Flash Data3
73	ND_D4	NAND Flash Data4
74	ND_D5	NAND Flash Data5
75	ND_D6	NAND Flash Data6
76	ND_D7	NAND Flash Data7
77	TXD2	UART TX Data/GPIO11
78	JTCLK	JTAG Clock
79	JTRST_N	JTAG Target Reset
80	JTDI	JTAG Data Input
81	JTDO	JTAG Data Output
82	DINT	JTAG NO
83	JTMS	JTAG Mode Select
84	RTS3	UATT Request To Send/GPIO05
85	WPS	WPS
86	PERST_N	PCIE
87	PCIE_TX0_P	PCIE0_TX+
88	PCIE_TX0_M	PCIE0_TX-
89	GND	Ground
90	PCIE_CK0_M	PCIE0_CLK-
91	PCIE_CK0_P	PCIE0_CLK+
92	PCIE_CK1_P	PCIE1_CLK+
93	PCIE_CK1_M	PCIE1_CLK-
94	GND	Ground
95	PCIE_RXN0	PCIE0_RX-
96	PCIE_RXP0	PCIE0_RX+
97	PCIE_RXN1	PCIE1_RX-
98	PCIE_RXP1	PCIE1_RX+
99	GND	Ground
100	PCIE_CK2_P	PCIE2_CLK+
101	PCIE_CK2_M	PCIE2_CLK-
102	PCIE_TX1_M	PCIE1_TX+
103	PCIE_TX1_P	PCIE1_TX-
104	PCIE_RXN2	PCIE2_RX-
105	PCIE_RXP2	PCIE2_RX+
106	3.3VD	POWER
107	3.3VD	POWER
108	3.3VD	POWER
109	GND	Ground

110	GND	Ground
111	GND	Ground
112	PCIE_TX2_P	PCIE2_TX+
113	PCIE_TX2_M	PCIE2_TX-
114	I2C_SD	I2C Data
115	I2C_SCLK	I2C Clock
116	D2DB_PORST_N	Power on reset
117	UART0_TXD	UART RX Data
118	UART0_RXD	UART TX Data
119	GND	Ground
120	GE_RXCLK	RGMII2 Rx Clock
121	GE_RXDV	RGMII2 Rx Data Valid
122	GE_RXD0	RGMII2 Rx Data bit #0
123	GE_RXD1	RGMII2 Rx Data bit #1
124	GE_RXD2	RGMII2 Rx Data bit #2
125	GE_RXD3	RGMII2 Rx Data bit #3
126	GE_TXCLK	RGMII2 Tx Clock
127	GE_TXEN	RGMII2 Tx Data Valid
128	GE_MDC	PHY Management Clock. Note: While RGMII/MII connects to external PHY, this pin is MDC. Else, it should be NC.
129	GE_MDIO	PHY Management Data. Note: While RGMII/MII connects to external PHY, this pin is MDIO. Else, it should be NC.
130	GND	Ground
131	GE_TXD0	RGMII2 Tx Data bit #0
132	GE_TXD1	RGMII2 Tx Data bit #1
133	GE_TXD2	RGMII2 Tx Data bit #2
134	GE_TXD3	RGMII2 Tx Data bit #0
135	GPIO0	GPIO0
136	ESW_P0_LED_0	Port #0 PHY LED indicators
137	ESW_P1_LED_0	Port #1PHY LED indicators
138	ESW_P2_LED_0	Port #2 PHY LED indicators
139	ESW_P3_LED_0	Port #3 PHY LED indicators
140	ESW_P4_LED_0	Port #4 PHY LED indicators