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MT7613BEN Datasheet

802.11a/n/ac Wi-Fi 2T2R Chip

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Specifications are subject to change without notice.

Document Revision History

Revision	Date	Author	Description
1.0	2018-12-05	CH Hung	Formal release
1.1	2018-12-21	CH Hung	Update 5.2 / 3.1.3
1.2	2019-01-02	CH Hung	Add 5.4 IO Control Option
1.3	2019-05-16	CH Hung	Update 1.2.4 WLAN Update 5.6 Top marking Update 4.1 Absolute maximum rating Update Figure.2 Update Table.2 and Table.3
1.4	2019-09-11	CH Hung	Update 4.2 Update Figure.2

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1 System overview

1.1 General Description

MT7613BEN is highly integrated single chip which features a low power 2x2 11a/n/ac WAVE2 5GHz band Wi-Fi subsystem. The Wi-Fi subsystem contains the 802.11a/n/ac radio, baseband, and MAC that are designed to meet both the low power and high throughput application.

1.2 Features

1.2.1 Technology and package

- 9x9 QFN 76 pins package

1.2.2 Power management and clock source

- Integrate high efficiency power management unit with single 3.3V power supply input
- Support 24,25,26 and 40MHz crystal clock with low power operation in idle mode
- Buffered clock output for co-clock with other SOC chipset

1.2.3 Platform

- 32-bit RISC MCU for Wi-Fi protocols
- Embedded SRAM/ROM
- Programmable and multiplexed GPIO pins
- PCIe device fully compliant to PCIe v2.1 specification

1.2.4 WLAN

- IEEE 802.11 a/n/ac compliant
- Support 20MHz, 40MHz, 80Mhz bandwidth in 5GHz band
- 5GHz-band 2T2R mode
  - MT7613BEN data rate up to 867Mbps
- Support MU-MIMO TX/RX
- Support STBC, LDPC, TX Beamformer and RX Beamformee
- Greenfield, mixed mode, legacy modes support
- IEEE 802.11 d/e/h/i/j/k/mc/r/v/w support
- Security support for WFA WPA/WPA2 personal, WPS2.0
- QoS support of WFA WMM, WMM PS
- Integrated LNA, PA, and T/R switch
- Optional external LNA and PA support.

1.2.5 Miscellaneous

- Integrate 8Kbit efuse to store device specific information and RF calibration data.

1.3 Block Diagram

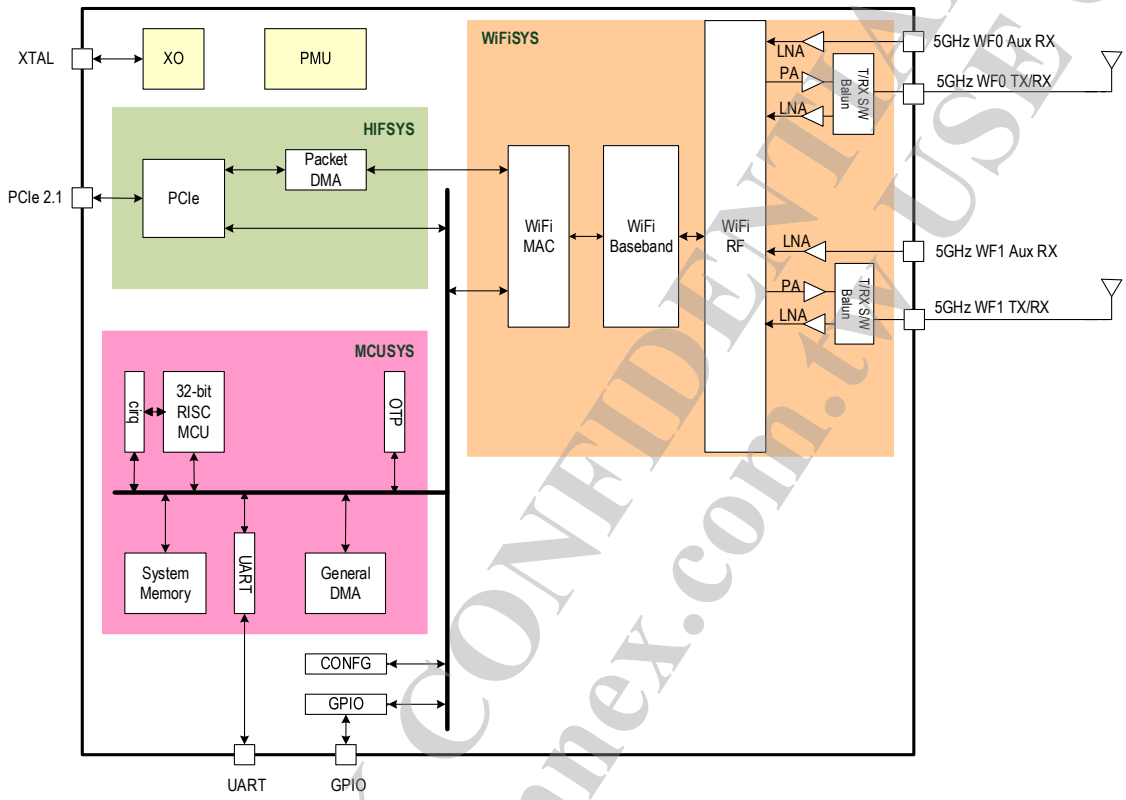


Figure 1 MT7613BEN system-on-chip block diagram

2 Functional Description

2.1 Overview

MT7613BEN is designed to support high data throughput over Wi-Fi. The host interface PCIe2.1 is integrated to provide stable bandwidth between the host platform and MT7613BEN. The clock rate of the internal bus fabric can also support the throughput the requirement. The clock rate of MCU is also configurable for different kinds of scenarios.

MT7613BEN supports low power requirement. Multiple power domains are implemented on chip. It defines a deep sleep mode, in which only the AON domain is powered on, while other OFF domains are shut off by the power switches integrated on chip. In deep sleep mode, the PMU could be further configured to be in a low power state to save the power consumption. The power, clock, and reset schemes of MT7613BEN are described in 2.2.

MT7613BEN has one CPU subsystem. There is a 32-bit RISC MCU subsystem. The CPU has its local memory. They also have common memory space for MEMORY and memory-mapped hardware engine. There are several options of clock frequency to provide the optimal performance with the best power consumption. The 32-bit RISC MCU is used to do clock control, power management, and host interface configuration. It also handles Wi-Fi MAC operations. PDMA (packet DMA) engines are integrated to support on-the-fly data buffer management. The architecture of 32-bit RISC MCU subsystem is described in 2.3.

MT7613BEN features PCIe2.1 for the host interface. The configuration and the feature set of the interface are described in 2.4.

MT7613BEN has the Wi-Fi MAC, BBP, and the RF subsystems, which provide the best-in-class radio and low power performance. The architecture of Wi-Fi subsystem is described in 2.5.

2.2 Chip architecture

The section describes the power, clock, and reset schemes in MT7613BEN.

2.2.1 Chip power plan

The external power source can be directly supplied to the Power Management Unit, digital IOs, PCIe PHY, and RF circuitry on MT7613BEN. The on-chip Power Management Unit contains 1 switching regulator and a number of LDOs. It converts the 3.3V input to other power rails.

PMU:

- 3.3V to 1.8V by PHYLDO for digital IOs and PCIe PHY circuit.
- 3.3V to 1.4V by the switching regulator (Buck converter) for CLDO and RF circuit.
- 1.4V to 1.05V by CLDO for digital circuit.

RF:

- 1.4V to lower voltages by the RF LDOs for RF circuits.

2.2.2 Chip power on sequence

The figure below shows the chip power on sequence.

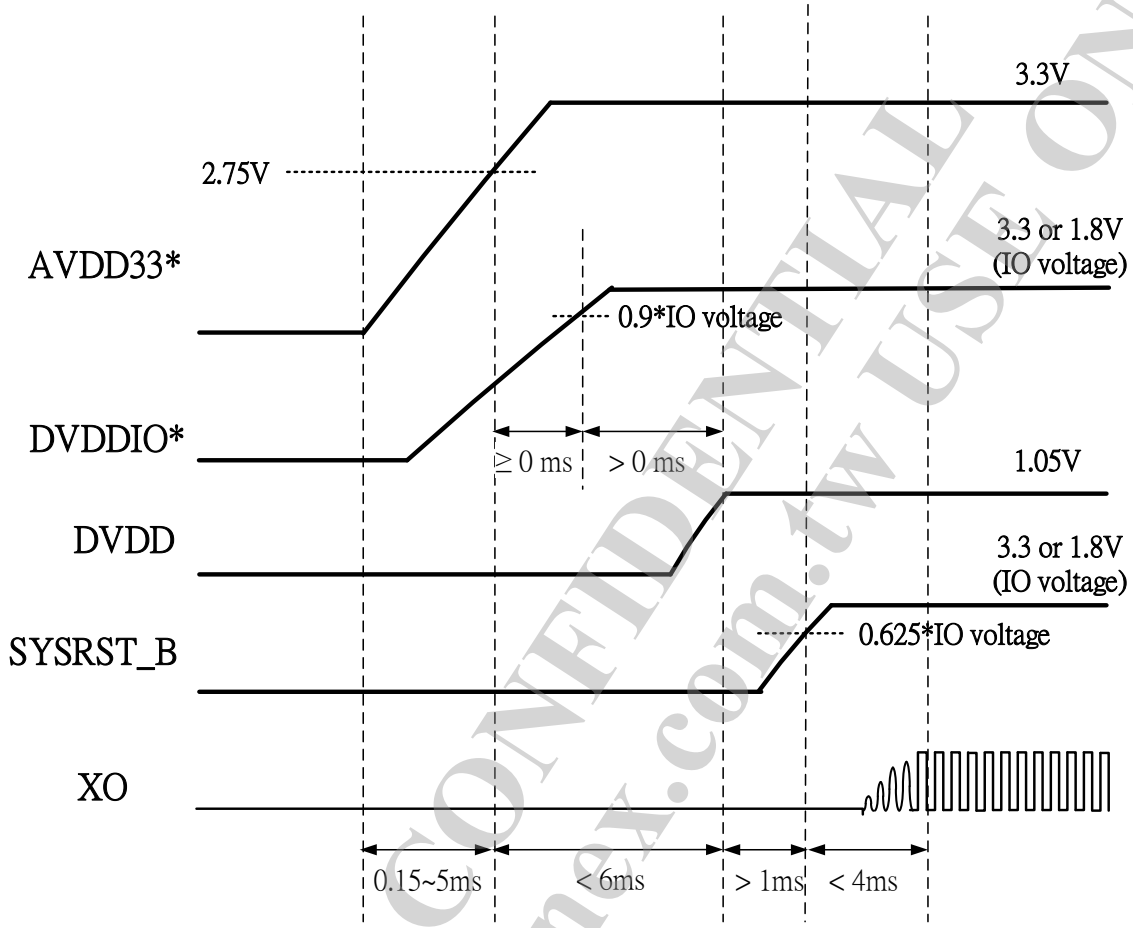


Figure 2 Chip power on sequence

2.2.3 Digital power domain

The digital circuit is separated into AON (always-on), MCU, Wi-Fi MAC, Wi-Fi baseband, and PCIe power domains. Except AON, each power domain can be turned off individually for different sleep scenarios.

2.2.4 Clock

2.2.4.1 Clock scheme

MT7613BEN connects to the crystal (XTAL) or the external clock source as the single clock source of the whole system. MT7613BEN XTAL oscillator support the XTAL frequency 24MHz, 25MHz, 26MHz and 40MHz.

2.2.5 Reset

2.2.5.1 Global reset

MT7613BEN has 3 global resets as follows:

- Cold reset by AVDD33_BUCK, AVDD33_MISC — Whole chip reset.

- System reset by SYSRST_B - Reset digital circuit, include strapping and XTAL controller.
- MCU WDT (watch-dog-timer) reset — Reset digital circuit, except strapping, PMU, and XTAL controller.

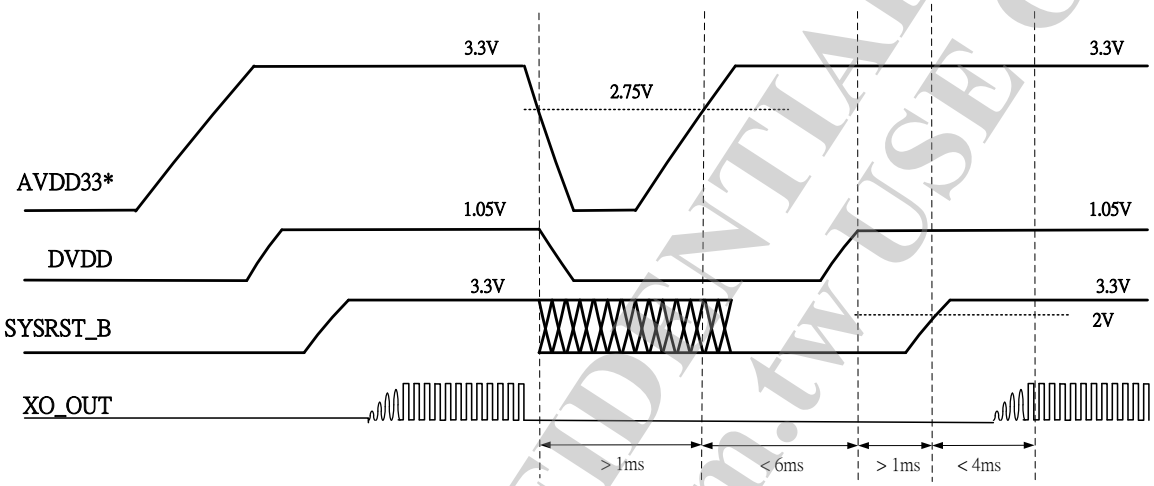


Figure 3 Cold reset sequence

2.3 32-bit RISC MCU subsystem

The 32-bit RISC MCU subsystem is built upon a multi-layer AHB bus fabric infrastructure. There is 880KB ROM and 560KB RAM in local instruction memory, and 368KB RAM in local data memory, with 1T access capability.

2.4 Host interface subsystem

2.4.1 PCIe interface

MT7613BEN supports PCI Express End Point which is fully compliant with the PCI Express Base Specification Revision 2.0. It supports PCI Express Gen1 (2.5Gbps) and PCIE Express Gen2 (5.0Gbps) differential bus speed.
MT7613BEN supports PCI Express low power operations such as ASPM L1.0, ASPM L1.CLK_PM, ASPM L1.SS (L1.1 and L1.2), and PCI PM L2 state. It also supports WAKE_N for device wakeup host scenario, as well as remote wake-up signaling.
The PCI Express interface is only used for Wi-Fi operations. The DMA ring and the data structure are controlled by the descriptor-based PDMA engine over PCI Express interface.

2.4.1.1 PERST_N

Fundamental reset is triggered when PERST_N is asserted with power already applied to the device and SYSRST_B have been asserted.

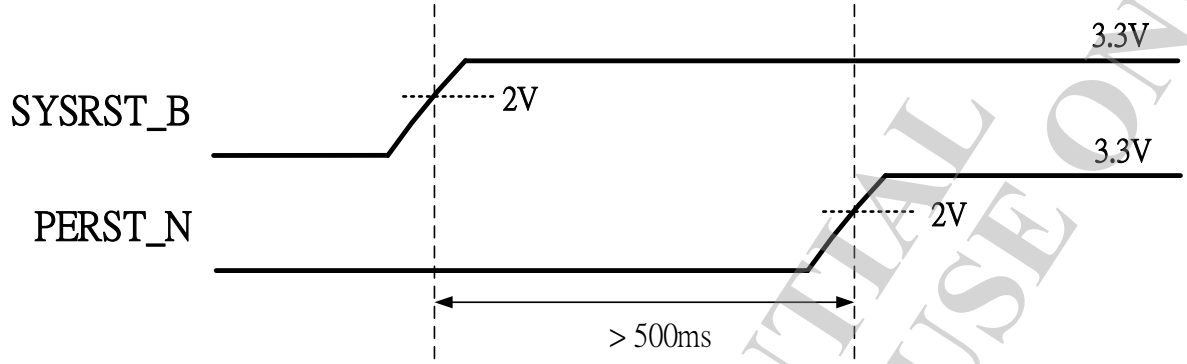


Figure 4 PERST_N sequence

2.5 Wi-Fi subsystem

2.5.1 Wi-Fi MAC

2.5.1.1 Features

Wi-Fi MAC supports the following features:

- Support all date rates of 802.11a including 6, 9, 12, 18, 24, 36, 48, and 54Mbps
- Support short GI and all data rates of 802.11n including MCS0 to MCS7
- Support 802.11ac MCS0 to MCS9
- AMPDU/AMSDU RX (de-aggregation) and TX (aggregation) support
- TX beamformer and RX beamformee
- TX rate adaptation
- TX power control
- Security
  - 64-bit WEP (WEP-40) and 128-bit WEP (WEP-104) encryption with hardware TKIP and CKIP processing
  - AES-CCMP hardware processing
  - GCMP hardware processing
- Support 2x2 and two independent 1x1 operations
- Low power beacon filtering
- Management/control frame filtering

2.5.2 WLAN Baseband

2.5.2.1 Features

Wi-Fi baseband supports the following features:

- 20/40/80 MHz channels
- VHT MCS0-9 BW20/40/80MHz with Nss=1~2
- Short Guard Interval
- Space-time block code (STBC)

- Low Density Parity check (LDPC)
- Support digital pre-distortion to enhance PA performance
- Smoothing (channel estimation) extension to MIMO case
- DFS radar detection
- Beamformer (explicit/implicit)
  - Decoded BW20/40/80 up to 2x2 BF matrix apply
- Beamformee
  - Decoded BW20/40/80 up to 4x2 MU matrix feedback
- MU-MIMO TX/RX
- Support 2x2 and two independent 1x1 operations.

2.5.3 WLAN RF

RF supports the following features:

- Integrated 5GHz PA and LNA, and T/R switch
- Integrated 5GHz Balun
- Support 5GHz external PA and LNA
- Support frequency band
  - 5150-5350MHz
  - 5470-5725MHz
  - 5725-5850MHz
  - 5850-5925MHz
- Configurable PA that provides different PA modes at different power levels for power consumption optimization

3 Radio Characteristics

3.1 Wi-Fi Radio Characteristics

3.1.1 Wi-Fi RF Block Diagram

MT7613BEN has two Wi-Fi RF ports.

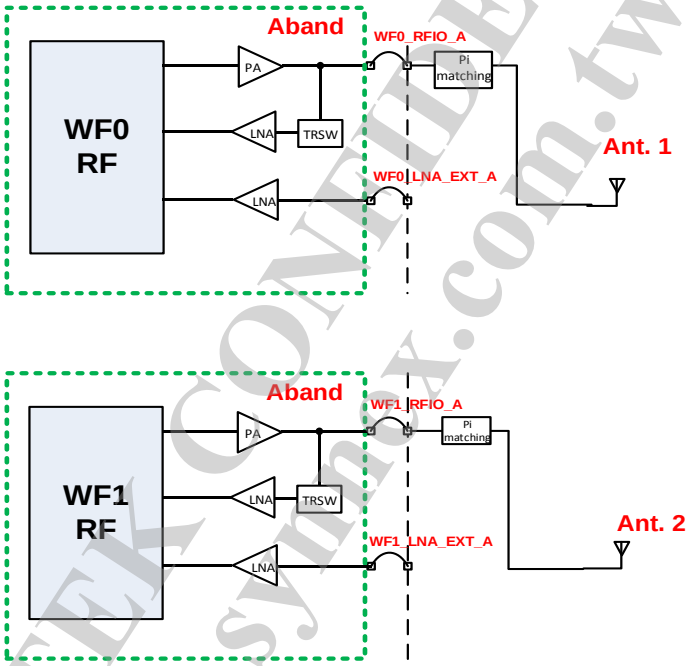


Figure 5 5GHz RF block diagram

3.1.2 Wi-Fi 5GHz band RF receiver specifications

The specification in table below is measured at the antenna port, which includes the frond-end loss.

Parameter	Description	Performance			
		MIN	TYP	MAX	Unit
Frequency range		5180	-	5825	GHz
RX sensitivity	6 Mbps OFDM	-	-93.5	-	dBm
	9 Mbps OFDM	-	-91.5	-	dBm
	12 Mbps OFDM	-	-91	-	dBm
	18 Mbps OFDM	-	-88.5	-	dBm
	24 Mbps OFDM	-	-84.5	-	dBm
	36 Mbps OFDM	-	-82	-	dBm
	48 Mbps OFDM	-	-77	-	dBm

	54 Mbps OFDM	-	-76	-	dBm
RX Sensitivity BW=20MHz VHT Mixed Mode 800ns Guard Interval Non-STBC	MCS 0	-	-93	-	dBm
	MCS 1	-	-90	-	dBm
	MCS 2	-	-88	-	dBm
	MCS 3	-	-84	-	dBm
	MCS 4	-	-81.5	-	dBm
	MCS 5	-	-77	-	dBm
	MCS 6	-	-75.5	-	dBm
	MCS 7	-	-74	-	dBm
	MCS 8	-	-69.5	-	dBm
RX Sensitivity BW=40MHz VHT Mixed Mode 800ns Guard Interval Non-STBC	MCS 0	-	-90	-	dBm
	MCS 1	-	-87	-	dBm
	MCS 2	-	-85	-	dBm
	MCS 3	-	-81	-	dBm
	MCS 4	-	-78.5	-	dBm
	MCS 5	-	-74	-	dBm
	MCS 6	-	-72.5	-	dBm
	MCS 7	-	-71	-	dBm
	MCS 8	-	-66.5	-	dBm
	MCS 9	-	-65	-	dBm
RX Sensitivity BW=80MHz VHT Mixed Mode 800ns Guard Interval Non-STBC	MCS 0	-	-86.5	-	dBm
	MCS 1	-	-83.5	-	dBm
	MCS 2	-	-81.5	-	dBm
	MCS 3	-	-77.5	-	dBm
	MCS 4	-	-75	-	dBm
	MCS 5	-	-70.5	-	dBm
	MCS 6	-	-69	-	dBm
	MCS 7	-	-67.5	-	dBm
	MCS 8	-	-63	-	dBm
	MCS 9	-	-61.5	-	dBm
Maximum Receive Level	6 Mbps OFDM	-	-10	-	dBm
	54 Mbps OFDM	-	-10	-	dBm
	MCS0	-	-10	-	dBm
	MCS7	-	-10	-	dBm
Receive Adjacent Channel Rejection (VHT20)	MCS0	-	28	-	dBm
	MCS8	-	0	-	dBm
Receive Adjacent Channel Rejection (VHT40)	MCS 0	-	27	-	dBm
	MCS 9	-	1	-	dBm
Receive Adjacent Channel Rejection (VHT80)	MCS 0	-	31	-	dBm
	MCS 9	-	12	-	dBm

Table 1 5GHz RF receiver specifications

3.1.3 Wi-Fi 5GHz band RF transmitter specifications

The specification in table below is measured at the antenna port, which includes the frond-end loss.

Parameter	Description	Performance			
		MIN	TYP	MAX	Unit
Frequency range		5180	-	5825	MHz
	6 Mbps OFDM	-	19.5	-	dBm
	54 Mbps OFDM	-	17	-	dBm

Output power at 25℃ and 3.3V with mask and EVM compliance	HT20, MCS 0	-	18.5	-	dBm
	HT20, MCS 7	-	16	-	dBm
	HT40, MCS 0	-	18.5	-	
	HT40, MCS 7	-	16	-	
	VHT80, MCS0	-	18.5	-	dBm
	VHT80, MCS9	-	15	-	dBm
Output power variation[1]	TSSI closed-loop control across all temperature range and channels and VSWR ≦1.5:1.	-2	-	2	dB
Carrier suppression		-	-	-30	dBc
Harmonic Output Power	2nd Harmonic	-	-45	-	dBm/MHz
	3nd Harmonic	-	-45	-	dBm/MHz

Note 1: VDD33 voltage is within ±5% of typical value

Table 2 5GHz RF transmitter specifications

3.2 Current Consumption

3.2.1 WLAN Current Consumption

Description	Current (average)	
	MT7613BEN	Unit
Sleep mode, radio off	61	mA
5GHz VHT80 RX Listen, 2RX	179	mA
5GHz RX Active, VHT80, MCS9, Nss=2	228	mA
5GHz TX VHT80, MCS9, Nss=2 @ 15dBm	693	mA
5GHz TX VHT80, MCS0, Nss=2 @ 18.5dBm	802	mA

Note:
[1] All result is measured provided VDD33 is 3.3V. TX power is measured at antenna port. Temperature is 25°C.
[2] Duty cycle for TX/RX measurement is 100%.
[3] The chip variation is +/- 15%.

Table 3 WLAN 5GHz Current Consumption

4 Electrical Characteristics

4.1 Absolute maximum rating

Symbol	Parameters	Maximum rating	Unit
VDD33	3.3V Supply Voltage	-0.3 to 3.63	V
VDD18	1.8V Supply Voltage	-0.3 to 1.98	V
T_{STG}	Storage Temperature	-40 to +125	°C
VESD	ESD protection (HBM)	2000	V

Table 4 Absolute maximum rating

4.2 Recommended operating range

Symbol	Rating	MIN	TYP	MAX	Unit
VDD33	3.3V Supply Voltage	2.97	3.3	3.63	V
VDD18	1.8V Supply voltage	1.7	1.8	1.9	V
$T_{AMBIENT}$	Ambient Temperature	-10	-	70	°C

Table 5 Recommended operating range

4.3 DC characteristics

The digital IO supports VDD33 or VDD18 application.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V_{IL}	Input Low Voltage	Input voltage • VDD33 • VDD18	 -0.3 -0.3	-	 VDD33*0.25 VDD18*0.35	V
V_{IH}	Input High Voltage	Input voltage • VDD33 • VDD18	 VDD33*0.625 VDD18*0.65	-	 VDD33+0.3 VDD18+0.3	V
V_{OL}	Output Low Voltage	Input voltage • VDD33 • VDD18 $\|I_{OL}\|$ = 4~16 mA	 -0.3 -0.3	-	 0.4 0.2	V
V_{OH}	Output High Voltage	Input voltage • VDD33 • VDD18 $\|I_{OH}\|$ = 4~16 mA	 VDD33-0.4 VDD18-0.2	-	 VDD33+0.3 VDD18+0.3	V
R_{PU}	Input Pull-Up Resistance	Input voltage • VDD33 • VDD18 PU=high, PD=low	 40 10	 75 50	 190 100	KΩ
R_{PD}	Input Pull-Down Resistance	Input voltage • VDD33 • VDD18 PU=low, PD=high	 40 10	 75 50	 190 100	KΩ

Table 6 DC characteristics of 3.3V application

4.4 XTAL oscillator

The table below lists the requirement for the XTAL.

Parameter	Value
Frequency	24MHz, 25MHz, 26MHz and 40MHz
Frequency stability	±10 ppm @ 25℃

Table 7 XTAL oscillator requirement

4.5 PMU Characteristics

PARAMETER	CONDITIONS	PERFORMANCE			
		MIN	TYP	MAX	Unit
Switching regulator(BUCK)					
Input voltage		2.97	3.3	3.63	V
Output voltage		1.33	1.4	1.47	V
Output current		-	-	800	mA
Quiescent current		-	150	200	uA
Efficiency	500mA load current	-	82	-	%
Over-current Shutdown	Iout=800mA	1.2*Iout	-	5*Iout	mA
Core LDO (CLDO)					
Input voltage		1.33	1.4	1.47	V
Output voltage		0.8	1.05	1.2	V
Output current		-	-	500	mA
Quiescent current		-	40	50	uA
PHY LDO					
Input voltage		2.97	3.3	3.63	V
Output voltage		1.7	1.8	1.9	V
Output current		-	-	60	mA
Quiescent current		-	40	50	uA

Table 8 PMU electrical characteristic

4.6 Thermal characteristics

Θ_{JC} assumes that all the heat is dissipated through the top of the package, while Ψ_{Jt} assumes that the heat is dissipated through the top, sides, and the bottom of the package. Thus it's suggested to use Ψ_{Jt} to estimate the junction temperature.

Symbol	Description	Performance	
		Typical	Unit
T_J	Maximum Junction Temperature (Plastic Package)	125	°C
Θ_{JA}	Junction to ambient temperature thermal resistance	22.67	°C/W
Θ_{JC}	Junction to case temperature thermal resistance	9.28	°C/W

Ψ_{Jt}	Junction to the package thermal resistance	2.12	°C/W

Note: JEDEC 51-7 system FR4 PCB size: 76.2x114.3mm (3”x4.5”), 4 layer.

Table 9 Thermal characteristics

5 Package specification

5.1 Pin Layout

MT7613BEN uses QFN package of with 9mm x 9mm dimension.

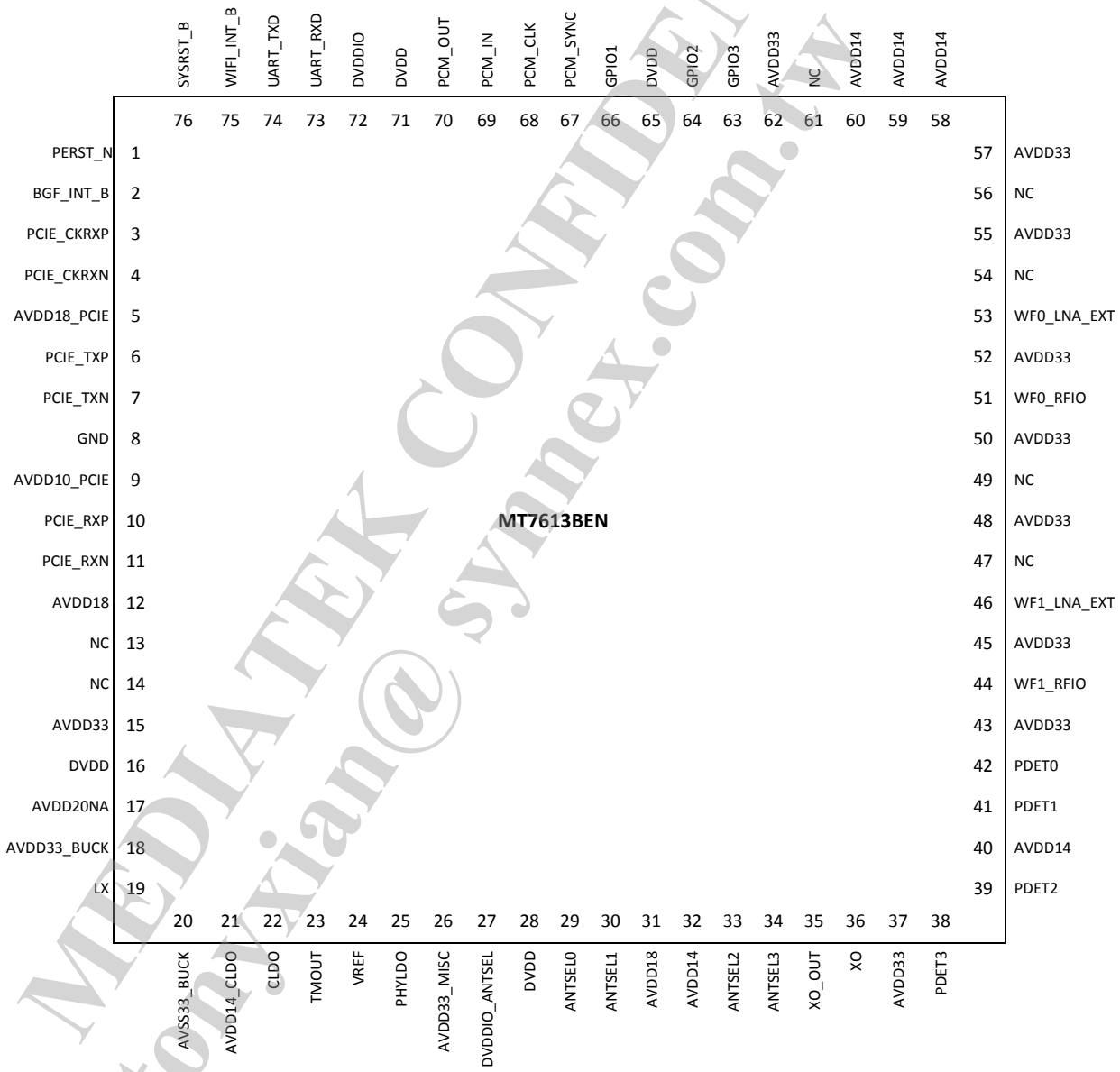


***Figure 6** MT7613BEN Pin Layout*

5.2 Pin Description

The section describes the pin functionality of MT7613BEN chip.

QFN	Pin Name	Pin description	PU/PD	I/O	Supply domain
Reset and clocks					
76	SYSRST_B	External system reset active low	PU	Input	DVDDIO
36	XO	Crystal input or external clock input	N/A	Input	AVDD33_XO
35	XO_OUT	XTAL buffered clock output	N/A	Output	
UART					
73	UART_RXD	UART receive	PU	Input	DVDDIO
74	UART_TXD	UART transmit	N/A	Output	DVDDIO
PCM					
68	PCM_CLK	PCM interface clock	PD	Input	DVDDIO
69	PCM_IN	PCM interface input data	PD	Input	DVDDIO
70	PCM_OUT	PCM interface output data	N/A	Output	DVDDIO
67	PCM_SYNC	PCM interface sync	PD	Input	DVDDIO
EPA TSSI					
42	PDET0	External PA TSSI input	N/A	Output	DVDDIO_ANTSEL
41	PDET1	External PA TSSI input	N/A	Output	DVDDIO_ANTSEL
39	PDET2	External PA TSSI input	N/A	Output	DVDDIO_ANTSEL
38	PDET3	External PA TSSI input	N/A	Output	DVDDIO_ANTSEL
Antenna Control					
29	ANTSEL0	RF switch control 0	PD	Input	DVDDIO_ANTSEL
30	ANTSEL1	RF switch control 1	PD	Input	DVDDIO_ANTSEL
33	ANTSEL2	RF switch control 2	PD	Input	DVDDIO_ANTSEL
34	ANTSEL3	RF switch control 3	N/A	Output	DVDDIO_ANTSEL
WIFI radio interface					
37,43,45,48, 50,52,55,57, 62	AVDD33	RF 3.3v power supply	N/A	Power	
32,40,58,59, 60	AVDD14	RF 1.4v power supply	N/A	Power	
31	AVDD18	RF 1.8v power supply	N/A	Power	
51	WF0_RFIO	RF a-band RF port	N/A	In/out	
44	WF1_RFIO	RF a-band RF port	N/A	In/out	
53	WF0_LNA_EXT	RF a-band RF port	N/A	In/out	

46	WF1_LNA_EXT	RF a-band RF port	N/A	In/out	
47,49,54,56, 61	NC				
PMU/BUCK					
20	AVSS33_BUCK	BUCK ground	N/A	Ground	
19	LX	BUCK output	N/A	Output	
18	AVDD33_BUCK	BUCK power supply	N/A	Input	
17	VDD20NA	BUCK internal circuit output cap	N/A	Output	
21	AVDD14_CLDO	CLDO supply	N/A	Input	
26	AVDD33_MISC	PMU supply	N/A	Input	
22	CLDO	Core LDO output	N/A	Output	
25	PHYLDO	PHY LDO 1.8V output	N/A	Output	
24	VREF		N/A	Ground	
23	TMOUT	PMU monitor	N/A	Output	
Miscellaneous					
75	WIFI_INT_B	WLAN host interrupt	PU	Input	DVDDIO
2	BGF_INT_B	host interrupt	N/A	Output	DVDDIO
1	PERST_N	PCIe functional reset	PU	Input	DVDDIO
66	GPIO1	GPIO1 in/out	PD	Input	DVDDIO
64	GPIO2	GPIO2 in/out	N/A	Output	DVDDIO
63	GPIO3	GPIO3 in/out	N/A	Output	DVDDIO
power supplies					
72	DVDDIO	Digital IO power input	N/A	Power	
27	DVDDIO_ANTSEL	Digital IO power input	N/A	Power	
16,28,65,71	DVDD	Digital CORE power input	N/A	Power	
8	GND	Ground	N/A	Ground	

Table 10 MT7613BEN common pin descriptions

PCIE interface					
5	AVDD18_PCIE	PCIe 1.8V power supply	N/A	Power	
7	PCIE_TXN	PCIe transmit differential pair	N/A	Analog	
6	PCIE_TXP	PCIe transmit differential pair	N/A	Analog	
11	PCIE_RXN	PCIe receive differential pair	N/A	Analog	
10	PCIE_RXP	PCIe receive differential pair	N/A	Analog	
9	AVDD10_PCIE	PCIe 1.05V power supply	N/A	Power	
3	PCIE_CKRXP	PCIe differential reference clock	N/A	Analog	
4	PCIE_CKRXN	PCIe differential reference clock	N/A	Analog	

15	AVDD33	3.3V power supply	N/A	Power	
14, 13	NC				
12	AVDD18	1.8V power supply	N/A	Power	

Table 11 MT7613BEN pin descriptions

5.3 Bootstrap

The section describes the bootstrap function. The chip modes are sensed from the device pin during power up. After chip reset, the pull configuration are stored in a register and determine the device operation mode.

XTAL clock mode	GPIO3	GPIO2	Description
24MHz	Pull-down	Pull-up	Uses 24MHz XTAL.
25MHz	Pull-up	Pull-down	Uses 25MHz XTAL.
26MHz	Pull-up	Pull-up	Uses 26MHz XTAL.
40MHz	Pull-down	Pull-down	Uses 26MHz XTAL.

Table 12 Bootstrap option – XTAL clock mode

Chip mode	PCM_OUT	Description
Normal mode	Pull-down(1)	Chip operates in normal mode.
Test mode	Pull-up	Chip operates in test mode.

Note 1: No external pull-down resistor is required because internal pull-down is active during power up.

Table 13 Bootstrap option – Chip mode

Pins PCM_OUT, UART_TXD, GPIO2 and GPIO3 are used for bootstrap. The system design should follow the following guideline:

- Those pins shall not be used as input functions because the signals from other device might affect the values sensed.
- Those pins shall not be used as an open-drain function because the pull-up resistor would affect the values sensed.

5.4 IO Control Option

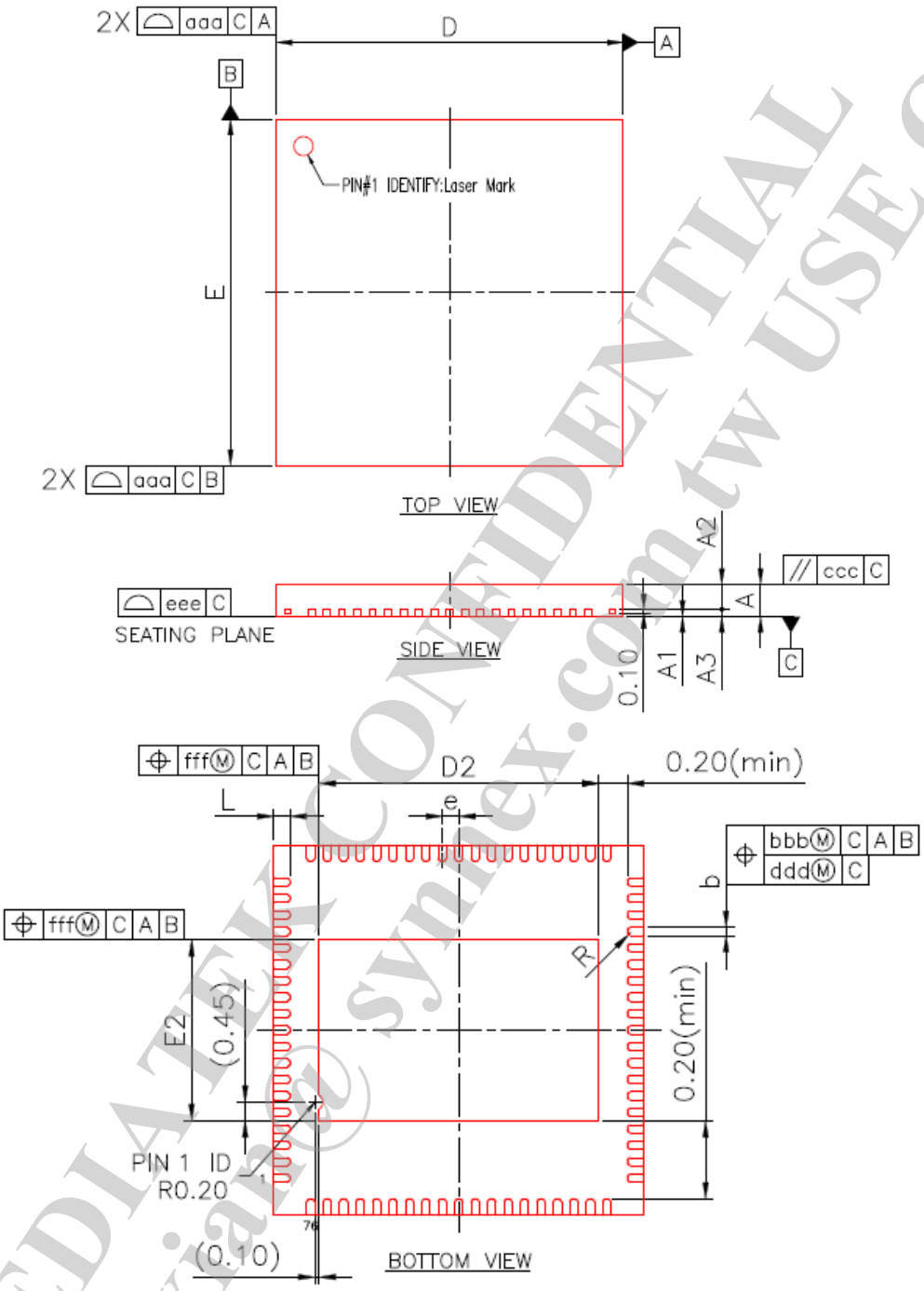
MT7613 provides 16 configurable I/O functions to support diversified applications. The IO functions can be configured through the control register PINMUX_SEL. It supports external front-end module on dual bands for high power requirement. Open drained IOs are available for WLAN LED. The most common configuration is listed in the table below.

	Function 0 (default)	Function 1	Function 2

QFN pin name	wire	dir	wire	dir	wire	dir
SYSRST_B	SYSRST_B	-	-	-	-	-
BGF_INT_B	CLK_REQ_N	I/O		O	GPIO[0]	I/O
WIFI_INT_B	WAKE_N	I/O	LED0	I/O	GPIO[1]	I/O
UART_RXD			LED1	I/O	GPIO[2]	I/O
UART_TXD			-	-	GPIO[3]	I/O
PCM_CLK			ANTSEL[8]	O	GPIO[4]	I/O
PCM_SYNC			ANTSEL[9]	O	GPIO[5]	I/O
PCM_OUT			ANTSEL[10]	O	GPIO[6]	I/O
PCM_IN			ANTSEL[11]	O	GPIO[7]	I/O
GPIO0	PERST_N	I	ANTSEL[4]	O	GPIO[8]	I/O
GPIO1			ANTSEL[5]	O	GPIO[9]	I/O
GPIO2			ANTSEL[6]	O	GPIO[10]	I/O
GPIO3			ANTSEL[7]	O	GPIO[11]	I/O
ANTSEL0 (FLASH_SPI_SO)	LED0	I/O	ANTSEL[0]	O	GPIO[12]	I/O
ANTSEL1 (FLASH_SPI_SI)	EXT_32K	I	ANTSEL[1]	O	GPIO[13]	I/O
ANTSEL2 (FLASH _SPI_CS)			ANTSEL[2]	O	GPIO[14]	I/O
ANTSEL3 (FLASH _SPI_CK)			ANTSEL[3]	O	GPIO[15]	I/O

Table 14 IO Control Option

5.5 Package information



Item		Symbol	MIN.	NOM.	MAX.
total height		A	0.80	0.85	0.90
stand off		A1	0.00	0.02	0.05
mold thickness		A2	0.60	0.65	0.70
leadframe thickness		A3		0.20 REF.	
lead width		b	0.15	0.20	0.25
package size	X	D	8.90	9.00	9.10
	Y	E	8.90	9.00	9.10
E-PAD size	X	D2	6.70	6.80	6.90
	Y	E2	4.30	4.40	4.50
lead length		L	0.30	0.40	0.50
lead pitch		e		0.40 bsc	
lead arc		R	0.075	---	---
Package profile of a surface		aaa		0.10	
Lead position		bbb		0.07	
Paralleliam		ccc		0.10	
Lead position		ddd		0.05	
Lead profile of a surface		eee		0.08	
Epad position		fff		0.10	

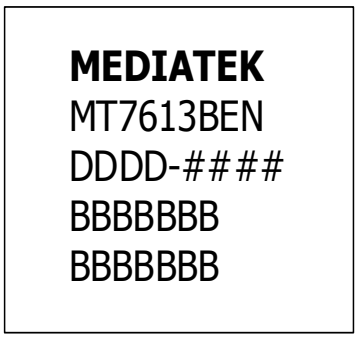
Figure 7 Package outline drawing

5.6 Ordering Information

Part number	Package	Operational temperature range
MT7613BEN	9x9x0.9 mm 76-QFN	-10~70°C

Table 15 Ordering information

5.7 Top marking




```
MT7613BEN : Part number
DDDD      : Date code
####      : Internal control code
BBBBBBB   : Lot number
```

Figure 8 MT7613BEN Top Marking

ESD CAUTION

MT7613 is ESD (electrostatic discharge) sensitive device and may be damaged with ESD or spike voltage. Although MT7613 is with built-in ESD protection circuitry, please handle with care to avoid the permanent malfunction or the performance degradation.