GAINSTRONG

Oolite V8.1_SPEC_EN

Version 1.0.0

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Revision	Date	Contents of Revision Change	Remark
1.0.0	2020-05-25	First release	

1 INTRODUTION

The Oolite V8.1 module use the MT7621DAT main chipset, and MT7603 2.4Ghz and MT7613 5.8Ghz WiFi chip are connected externally.

The MT7621DAT integrates a dual-core MIPS1004Kc (880MHz), HNAT/ HQoS/ Samba/ VPN accelerators, 5-port GbE switch, RGMII, USB3.0, USB2.0, 3xPCIe, SD-XC. The powerful CPU with rich portfolio is suitable for 802.11ac, LTE cat4/5, edge, hotspot, VPN, AC (Access Control). It can also connect to touch-panel, ZigBee/Z-Wave for Internet Service Router and Home Security Gateway.

MT7603EN is a highly integrated Wi-Fi single chip which supports 300 Mbps PHY rate. It fully complies with IEEE 802.11n and IEEE 802.11 b/g standards, offering feature-rich wireless connectivity at high standards, and delivering reliable, cost-effective throughput from an extended distance.

The MT7613BEN is a highly integrated single chip which has built in a 2*2 dual-band wireless LAN radio.It supports IEEE802.11ac draft standard and provides the highest PHY rate up to 866Mbps,offering feature-rich wireless connectivity and reliable throughput from an extended distance.

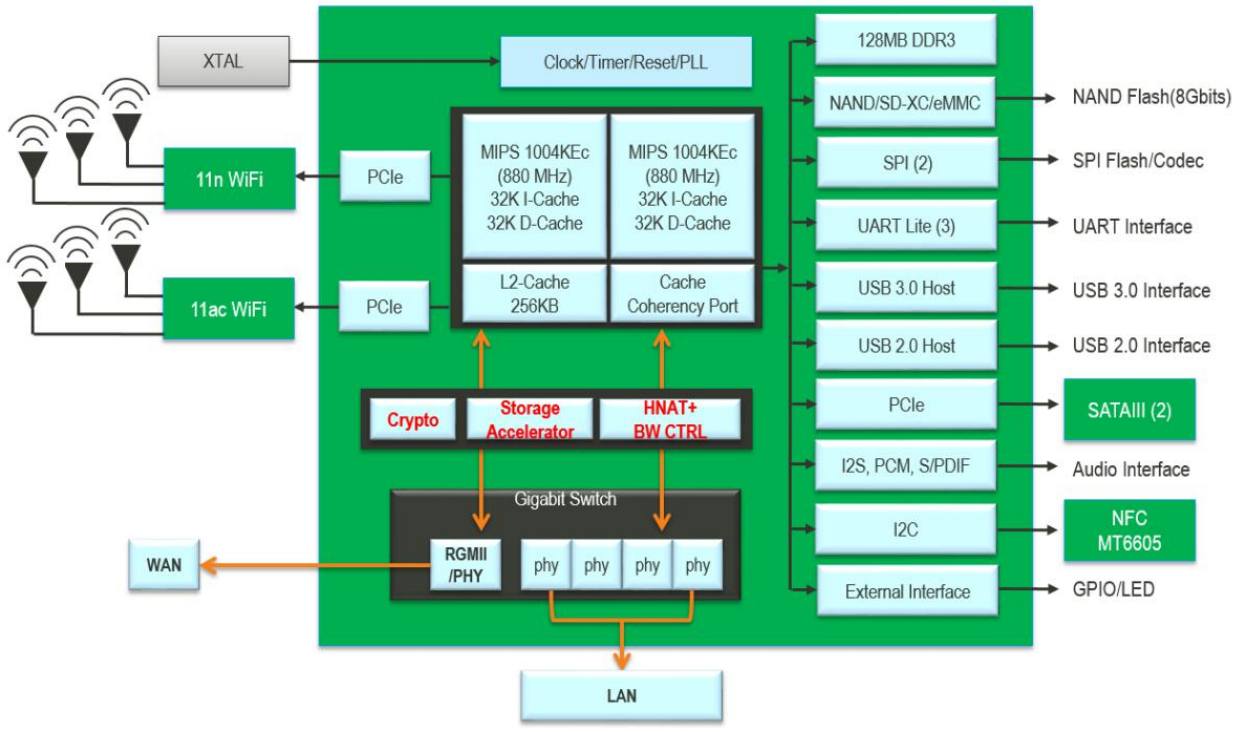
For the next generation router, MT7621DA provides several dedicated hardware engines to accelerate the NAT, QoS, Samba and VPN traffic. These accelerators relief the CPU for other upper layer applications.

Features

- MT7621DAT Embedded MIPS1004Kc (880 MHz)
- RAM: Embedded DDR3-1200 128MBytes (KGD)
- Flash:16MByte(16/32/64MByte optional)
- 5-port 10/100/1000Mbps SW/PHY
- Support 802.11b/g/n 2T2R 2.4Ghz 300Mbps ,802.11ac 2T2R 5.8Ghz 688Mbps

- 1x RGMII/MII interface
- SPI, NAND Flash, SDXC, eMMC(4 bits)
- 1x USB 3.0, 1x USB 2.0, 1x Mini-PCIe host
- I2C, SPI*2, UART lite*3, JTAG, MDC, MDIO, GPIO
- HW storage accelerator
- OpenWrt / Linux 2.6 SDK
- VoIP support (I2S, PCM) , Audio interface (SPDIF-Tx, I2S, PCM)
- Power supply voltage: 3.3V
- Antenna: 4xIPEX external Antenna(default) or use the stamp hole pins interface
- Size: 50.0mm x 50.0mm x 4.8mm

2 BLOCK DIAGRAM



3 MAIN CHIP FEATURES

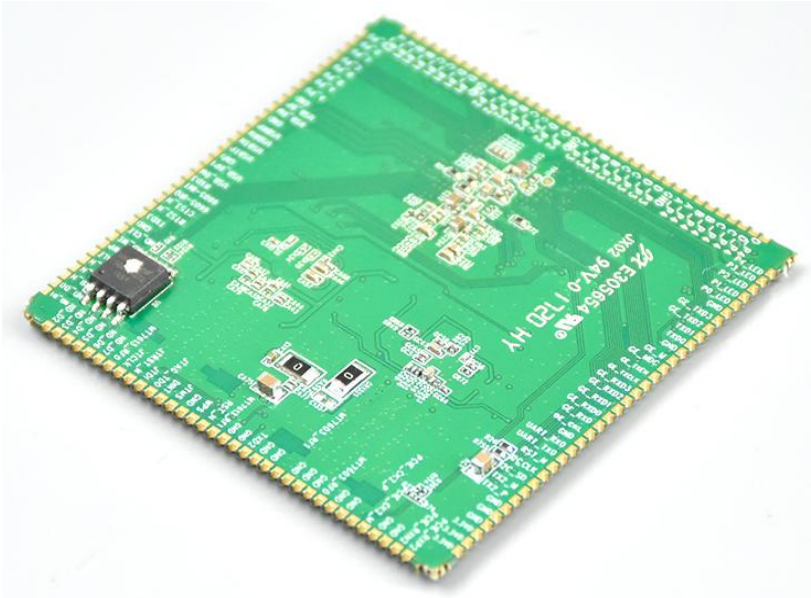
The following table covers the main features offered by the MT7621DAT. Overall, the MT7621DAT supports the requirements of a high-level AP/router, and a number of interfaces together with a large RAM capacity.

Features	MT7621DA
CPU	MIPS1004Kc (880 MHz, Dual Core)
I-Cache, D-Cache	32 KB, 32 KB
L2 Cache	256KB
HNAT/HQoS	HQoS 16 queues HNAT 2 Gbps forwarding (IPv4, IPv6 routing, DS-Lite, 6RD, 6to4)
Memory	Embedded DDR3-1200 128MB (KGD)
NAND	Small page 512-Byte (max 512 Mbit) Large page 2k-Byte (max 8 Gbit)
SPI Flash	3B addr mode (max 128 Mbit) 4B addr mode (max 512 Mbit)
SD eMMC	SD-XC class 10 (max 128 GByte) 4-bit eMMC (max 8 GByte)
PCIe	3
USB	USB3 x 1+ USB2 x 1 or USB2 x 2
Ethernet	5-port GSW + RGMII(1)
I2S	1
PCM	1
I2C	1
SPDIF-Tx	1
UART Lite	3
JTAG	1
Package	LFBGA 11.7 mm x 13.6 mm

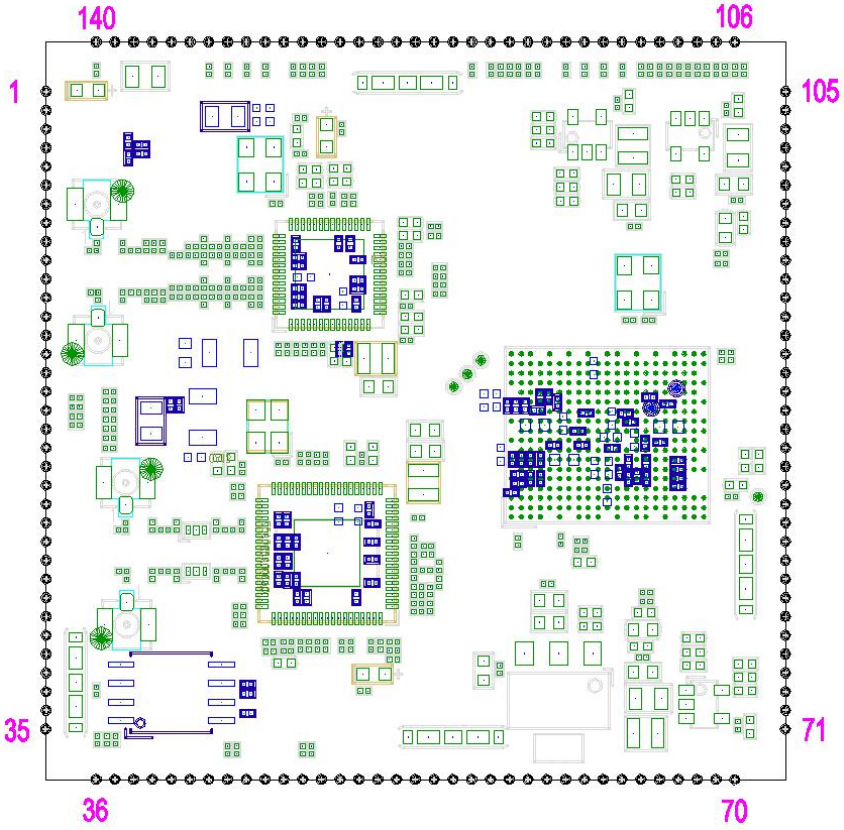
4 PICTURES

TOP:

Bottom:



5 PINS DESCRIPTION



Pin NO.	Function	Description
1	ND_D2	NAND Flash Data2
2	ND_D3	NAND Flash Data3
3	ND_D4	NAND Flash Data4
4	ND_D5	NAND Flash Data5
5	ND_D6	NAND Flash Data6
6	ND_D7	NAND Flash Data7
7	MT7613_RF0	MT7613_RF0
8	JTCLK	JTAG Clock
9	JTRST_N	JTAG Target Reset
10	JTDI	JTAG Data Input

11	EJTAG-TDO	JTAG Data Output
12	DINT	3.3V pull up
13	JTMS	JTAG Mode Select
14	RTS3_N	UART Request To Send
15	WPS	Watchdog reset
16	PERST_N	PCIE
17	MT7613_RF1	MT7613_RF1
18	GND	Ground
19	GND	Ground
20	TXD2	DRAM_TYPE
21	GND	Ground
22	GND	Ground
23	MT7603_RF1	MT7603_RF1
24	GND	Ground
25	GND	Ground
26	GND	Ground
27	MT7603_RF0	MT7603_RF0
28	GND	Ground
29	GND	Ground
30	PCIE_CK2_P	PCIE2_CLK+
31	PCIE_CK2_M	PCIE2_CLK+
32	GND	Ground
33	GND	Ground
34	PCIE_RXN2	PCIE2_RX-
35	PCIE_RXP2	PCIE2_RX+
36	ND_D1	NAND Flash Data1
37	ND_D0	NAND Flash Data0
38	ND_RB_N	NAND Flash Ready/Busy
39	ND_RE_N	NAND Flash Read Enable
40	ND_CS_N	NAND Flash Chip Select
41	ND_ALE	NAND Flash ALE Latch Enable
42	ND_WP	NAND Flash Write Protect
43	ND_WE_N	NAND Flash Write Enable

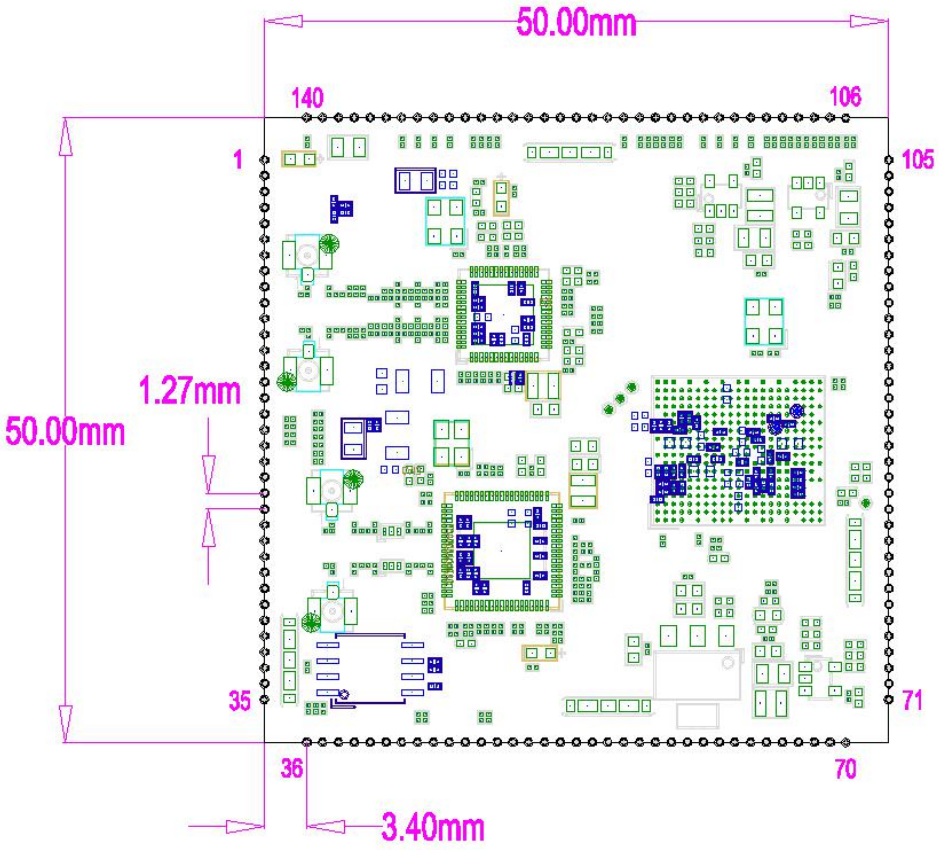
44	ND_CLE	NAND Flash Command Latch Enable
45	GND	Ground
46	TXD3	UART TX Data
47	RTS2_N	UART Request To Send
48	CTS3_N	UART Clear To Send
49	MT6605_IRQ	UART Clear To Send
50	MT6605_INT	UART RX Data
51	RXD3	UART RX Data
52	USB_DM_1P	USB Port1 data pin Data- (USB2.0)
53	USB_DP_1P	USB Port1 data pin Data+ (USB2.0)
54	GND	Ground
55	SSUSB_TXP	USB Port0 SS data pin TX+ (USB3.0)
56	SSUSB_TXN	USB Port0 SS data pin TX- (USB3.0)
57	SSUSB_RXN	USB Port0 SS data pin RX+-(USB3.0)
58	SSUSB_RXP	USB Port0 SS data pin RX+ (USB3.0)
59	GND	Ground
60	USB_DM	USB Port0 HS/FS/LS data pin Data- (USB3.0)
61	USB_DP	SB Port0 HS/FS/LS data pin Data+ (USB3.0)
62	GND	Ground
63	ESW_TXVP_A_P0	Port #0 MDI Transceivers
64	ESW_TXVN_A_P0	Port #0 MDI Transceivers
65	ESW_TXVP_B_P0	Port #0 MDI Transceivers
66	ESW_TXVN_B_P0	Port #0 MDI Transceivers
67	ESW_TXVP_C_P0	Port #0 MDI Transceivers
68	ESW_TXVN_C_P0	Port #0 MDI Transceivers
69	ESW_TXVP_D_P0	Port #0 MDI Transceivers
70	ESW_TXVN_D_P0	Port #0 MDI Transceivers
71	ESW_TXVP_A_P1	Gigabit Por1_A+
72	ESW_TXVN_A_P1	Gigabit Port1_A-
73	ESW_TXVP_B_P1	Gigabit Por1_B+
74	ESW_TXVN_B_P1	Gigabit Port1_B-
75	ESW_TXVP_C_P1	Gigabit Port1_C+
76	ESW_TXVN_C_P1	Gigabit Port1_C-

77	ESW_TXVP_D_P1	Gigabit Port1_D+
78	ESW_TXVN_D_P1	Gigabit Port1_D-
79	GND	Ground
80	ESW_TXVP_A_P2	Gigabit Port2_A+
81	ESW_TXVN_A_P2	Gigabit Port2_A-
82	ESW_TXVP_B_P2	Gigabit Port2_B+
83	ESW_TXVN_B_P2	Gigabit Port2_B-
84	ESW_TXVP_C_P2	Gigabit Port2_C+
85	ESW_TXVN_C_P2	Gigabit Port2_C-
86	ESW_TXVP_D_P2	Gigabit Port2_D+
87	ESW_TXVN_D_P2	Gigabit Port2_D-
88	GND	Ground
89	ESW_TXVP_A_P3	Gigabit Port3_A+
90	ESW_TXVN_A_P3	Gigabit Port3_A-
91	ESW_TXVP_B_P3	Gigabit Port3_B+
92	ESW_TXVN_B_P3	Gigabit Port3_B-
93	ESW_TXVP_C_P3	Gigabit Port3_C+
94	ESW_TXVN_C_P3	Gigabit Port3_C-
95	PESW_TXVP_D_P3	Gigabit Port3_D+
96	ESW_TXVN_D_P3	Gigabit Port3_D-
97	GND	Ground
98	ESW_TXVP_A_P4	Gigabit Port4_A+
99	ESW_TXVN_A_P4	Gigabit Port4_A-
100	ESW_TXVP_B_P4	Gigabit Port4_B+
101	ESW_TXVN_B_P4	Gigabit Port4_B-
102	ESW_TXVP_C_P4	Gigabit Port4_C+
103	ESW_TXVN_C_P4	Gigabit Port4_C-
104	ESW_TXVP_D_P4	Gigabit Port4_D+
105	ESW_TXVN_D_P4	Gigabit Port4_D-
106	ESW_P4_LED_0	Port #4 PHY LED indicators
107	ESW_P3_LED_0	Port #3 PHY LED indicators
108	ESW_P2_LED_0	Port #2 PHY LED indicators
109	ESW_P1_LED_0	Port #1PHY LED indicators

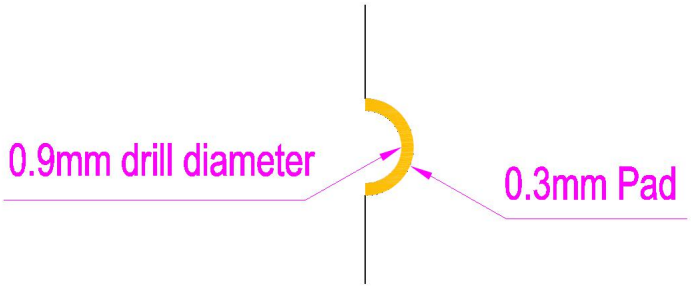
110	ESW_P0_LED_0	Port #0 PHY LED indicators
111	GPIO0	GPIO#0
112	GE_TXD3	RGMII2 Tx Data bit #0
113	GE_TXD2	RGMII2 Tx Data bit #2
114	GE_TXD1	RGMII2 Tx Data bit #1
115	GE_TXD0	RGMII2 Tx Data bit #0
116	GND	Ground
117	GE_MDIO	PHY Management Data. Note: While RGMII/MII connects to external PHY, this pin is MDIO. Else, it should be NC.
118	GE_MDC	PHY Management Clock. Note: While RGMII/MII connects to external PHY, this pin is MDC. Else, it should be NC.
119	GE_TXEN	RGMII2 Tx Data Valid
120	GE_TXCLK	RGMII2 Tx Clock
121	GE_RXD3	RGMII2 Rx Data bit #3
122	GE_RXD2	RGMII2 Rx Data bit #2
123	GE_RXD1	RGMII2 Rx Data bit #1
124	GE_RXD0	RGMII2 Rx Data bit #0
125	GE_RXDV	RGMII2 Rx Data Valid
126	GE_RXCLK	RGMII2 Rx Clock
127	GND	Ground
128	UART0_RXD	UART RX Data
129	UART0_TXD	UART TX Data
130	D2DB_PORST_N	Power on reset
131	I2C_SCLK	I2C Clock
132	I2C_SD	I2C Data
133	PCIE_TX2_M	PCIE2_TX-
134	PCIE_TX2_P	PCIE2_TX+
135	GND	Ground
136	GND	Ground
137	GND	Ground
138	3.3VD	POWER
139	3.3VD	POWER
140	3.3VD	POWER

6 MECHANICAL

Dimensions (mm)	Length	Width	Height
	50.0 (Tolerance:±0.2mm)	50.0 (Tolerance:±0.2mm)	4.8 (Tolerance:±0.2mm)



Pin Size:



7 SCHEMATIC DESIGN NOTES

This part contains the schematic and PCB design notes for the customer who use the Core moudle for their own production. You can see our reference design and the MT7621DAT Spec. for more detail design information.

7.1 ANTENNA CONNECTER

By default, the RF antenna is an external IPEX antenna, which can also support direct connection to pinout,. If the RF connected to the customer’ s main boad, the RF match circuit and suitable trace should be noted.

7.2 PCIE

Mt7621DAT can support three PCIe interfaces. It has occupied two interfaces by MT7603 and MT7613. In fact, only one PCIe interface is available.

7.3 POWER

There is only one external power 3.3VDC for the Core Moudle. Other powers as 1.8VDC,1.5VDC and 1.2VDC are all generated from the Core Moudle internally.

Power consumption:

For the 3.3VDC,the main board should supply at least 2A current for the module, for security use ,the Margin should be 30% at least.

Power Ripple:

Small ripple is necessary for better performance, especially for the RF property.

The 3.3VDC ripple should be ≤50mV at idle state and ≤100mV at full load.

8 REFLOW SOLDERING TEMPERATURE CURVE

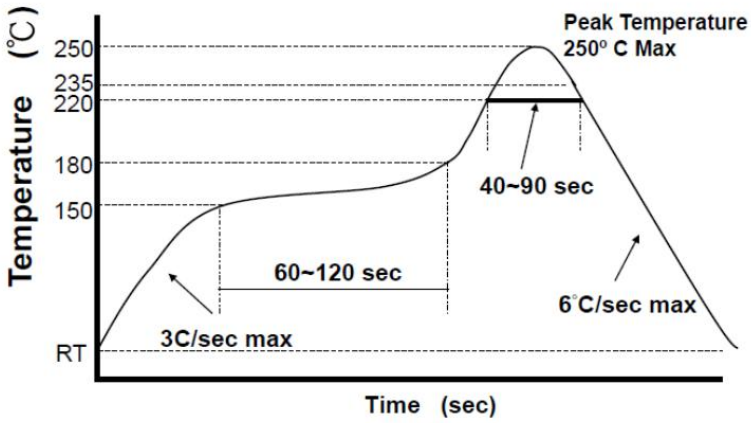


Figure 4-2 Reflow profile

Notes:

1. Reflow profile guideline is designed for SnAgCulead-free solder paste.
2. Reflow temperature is defined at the solder ball of package/or the lead of package.
3. MTK would recommend customer following the solder paste vendor's guideline to design a profile appropriate your line and products.
4. Appropriate N2 atmosphere is recommended since it would widen the process window and mitigate the risk for having solder open issues.

9 MODULE OPERATING ENVIRONMENT

Power Supply	3.3V ±5%
Operating Temperature	0℃ ~45℃
Storage Temperature	-40℃ ~ 80℃
Operating Humidity	10%~90% non-condensing
Storage Humidity	5%~90% non-condensing