NXP Semiconductors
User's Guide

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i.MX 8M Nano LPDDR4 EVK Board Hardware User's Guide

Contents

Chapter 1
Introduction

This document is the hardware user's guide for the i.MX 8M Nano LPDDR4 Evaluation Kit (EVK) based on the NXP Semiconductor's i.MX 8M Nano Applications Processor. This board is fully supported by NXP Semiconductor. This manual includes system setup and configurations, and provides detailed information on the overall design and usage of the EVK board from a hardware system perspective.

1.1 Board overview

The LPDDR4 EVK board is a platform designed to show the most commonly used features of the i.MX 8M Nano Applications Processor. The i.MX 8M Nano LPDDR4 EVK board helps developers get familiar with the processor before investing a large amount of resources in more specific designs.

Table 1 lists the features of the i.MX 8M Nano LPDDR4 EVK board.

Table 1. Board features

Processor	NXP Applications Processor	MIMX8MN6DVTJZAA
DRAM memory	Kingston 16 GB LPDDR4	C1612PC2WDGTKR-U
Mass storage	SanDisk 32 GB eMMC5.1	SDINBDG4-32G-I1
	Micron 32 MB QSPI NOR	MT25QU256ABA1EW7-0SIT
	MicroSD card connector	SD3.0 supported
Power	NXP PMIC PCA9450B + Discrete DCDC/LDO	
Camera	CSI interface (Mini-SAS connector)	
Display interface	DSI interface (Mini-SAS connector)	
Ethernet	1 GB Ethernet with RJ45 connector	
USB	Port1 is USB (2.0) Type-C connector and Port2 is used as the Power Input.	
Wi-Fi/Bluetooth	x1 on board Wi-Fi/Bluetooth module AW-CM358SM based on NXP 88W8987, 802.11a/b/g/n/ac, BT5.0	
Audio connectors	3.5 mm Stereo Line output, 2 Vrms	
	FPC connector (SAI ports) for Audio Card	
Debug connectors	JTAG (10-pin header)	
	MicroUSB for UART debug, two COM Ports for A53 and M7	
Expansion connector	40-pin dual-row Pin Header for I^2S, UART, I^2C and GPIO expansion	
I^2C connector	8-pin dual-row Pin Header for I^2C expansion	

Table continues on the next page...

Table 1. Board features (continued)

Buttons	ON/OFF, RESET
LED indicators	Power status, UART
PCB	8MNANOLPD4-CPU: 2 inch × 2.7 inch, 6-layer 8MMINI-BB: 4 inch × 4.2 inch, 8-layer
Orderable part number	8MNANOLPD4-EVK [1]

1. It consists of 8MNANOLPD4-CPU plus 8MMINI-BB. Boards not orderable separately.

1.2 Board contents

The i.MX 8M Nano LPDDR4 EVK contains the following items:

- i.MX 8M Nano LPDDR4 EVK board, assembled by two separate boards, 8MNANOLPD4-CPU (SOM Board) and 8MMINI-BB (Base Board)
- IMX-MIPI-HDMI Accessory Card, MIPI-DSI to HDMI adapter board
- USB Type-C 45W Power Delivery Supply, 5V/3A, 9V/3A, 15V/3A, 20V/2.25A supported
- Mini-SAS cable, 8" mini-SAS cable
- USB Type-C Cable, Cable – Assembly, USB 3.0, Type-C Male to Type-A Male
- USB micro-B Cable, Cable – Assembly, USB 2.0, Type-A Male to Micro-B Male
- USB Type-C to A Adapter, Adapter – USB 3.0, Type-C Male to Type-A Female
- Quick Start Guide

Chapter 2
Specifications

This section provides the detailed information about the electrical design and practical considerations on the LPDDR4 EVK board. Figure 1 describes each block in the high-level block diagram of the LPDDR4 EVK board.

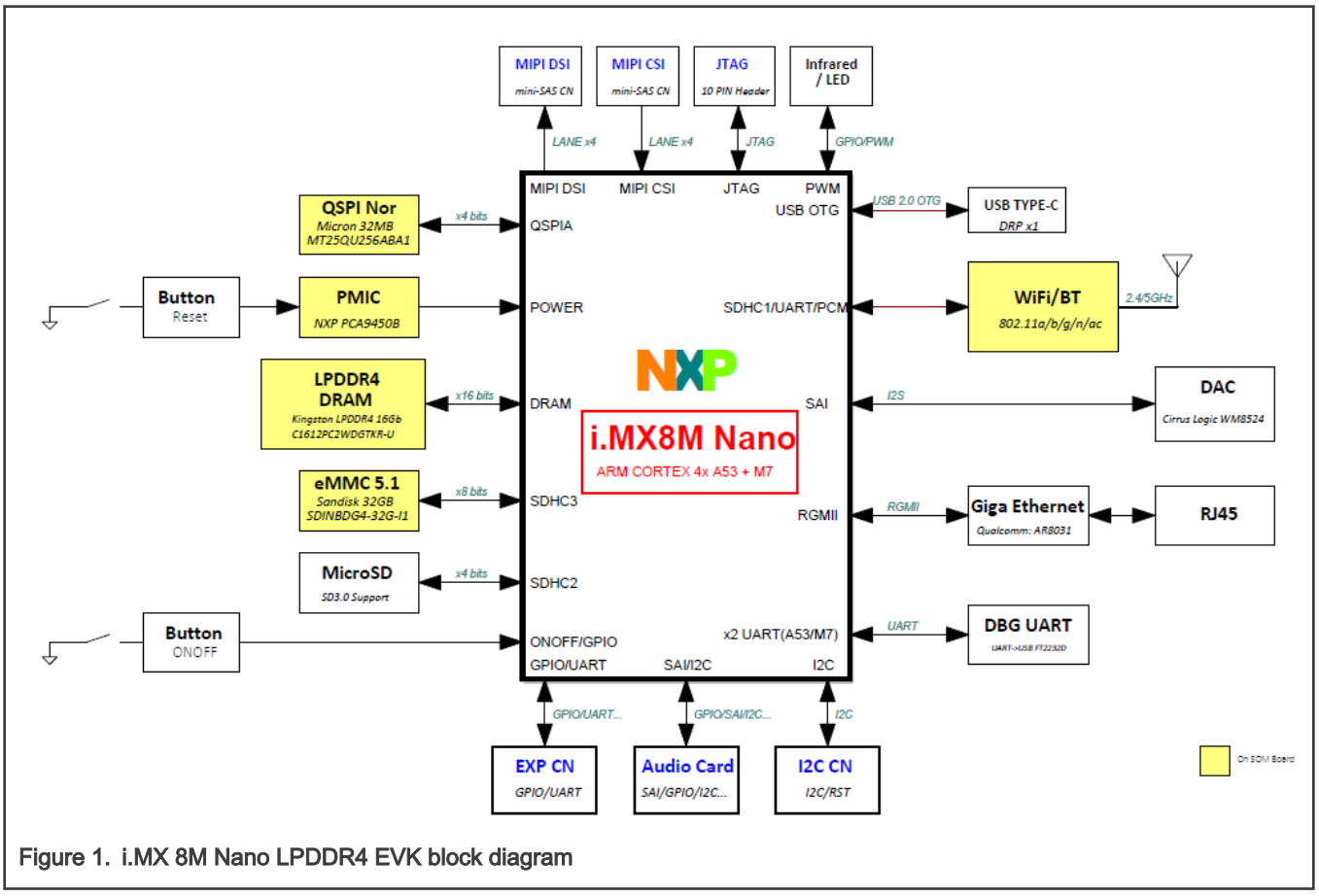

Figure 1. i.MX 8M Nano LPDDR4 EVK block diagram

Figure 2 shows the overview of the i.MX 8M Nano LPDDR4 EVK board.

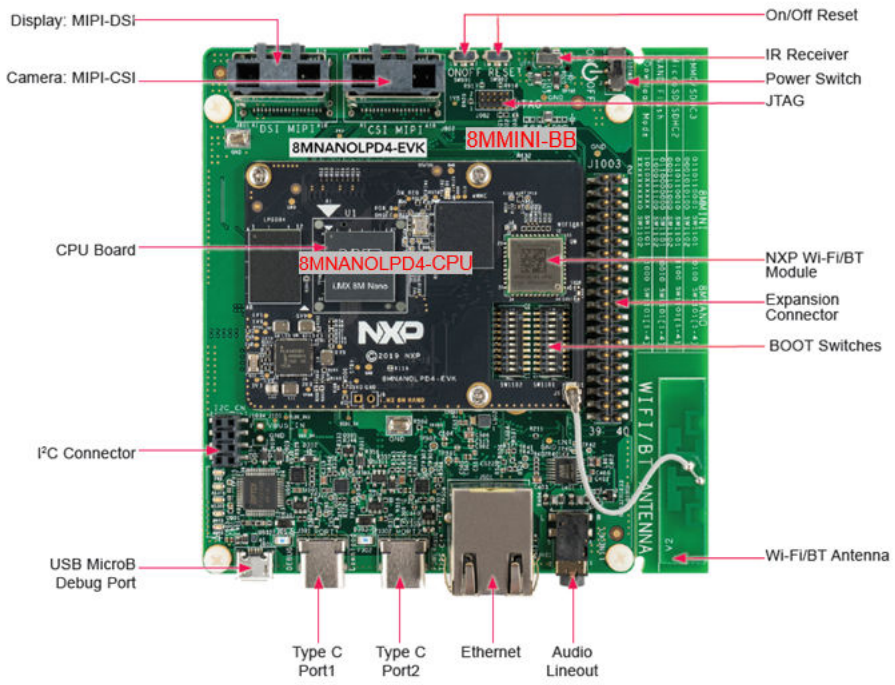

Figure 2. i.MX 8M Nano LPDDR4 EVK board overview

NOTE

Type-C Port2 is the only power supply port, and it must be always supplied for system running.

i.MX 8M Nano EVK is not a typical use case of the PD device. It is supplied by the PD charger only, but with a power switch. When the switch keeps **OFF** for more than 5.5 seconds after adapting the PD charger, the charger (Source) will repower EVK (Sink) after the system initiates the PD software. See **Section 6.5.7** in Universal Serial Bus Specification Revision 2.0. There are two ways to avoid the repower:

- The power switch must always be in the **ON** position before attaching the PD charger.
- Change the software to disable the PD function, and make it Type-C supply only.

2.1 Processor

The i.MX 8M Nano applications processors represent NXP Semiconductor's latest achievement in highly integrated multimedia-focused products offering high performance processing. These applications processors can enable the growing market of smart, secure, connected devices. The i.MX 8M Nano applications processors feature NXP's advanced implementation of the Quad ARM Cortex®-A53+ ARM Cortex®-M7 cores, which operate at speeds up to 1.5 GHz and 750 MHz respectively. Each i.MX 8M Nano device provides a 16-bit DDR3L/DDR4/LPDDR4 memory interface and other interfaces for connecting peripherals, such as MIPI LCD, MIPI Camera, WLAN, Bluetooth™, Ethernet, Digital Mic, and multi-sensors.

For more detailed information about the processor, see the datasheet and reference manual on i.MX 8M NANO.

2.2 Boot mode and boot device configurations

The i.MX 8M Nano implements a compressed boot mode decode with four BOOT_MODE pins. It can boot from the boot configuration selected on SW1101 or from the boot configuration stored on the internal eFUSE. In addition, the i.MX 8M Nano can download a program image from a USB connection when configured in the serial downloader mode. The method used to determine where the processor finds its boot information is from four dedicated BOOT MODE pins.

On the i.MX 8M Nano LPDDR4 EVK board, the default boot mode is to boot from the eMMC device. There are two additional boot devices: one QSPI Nor Flash on the CPU board and one MicroSD connector on the base board. If you set the boot device to QSPI or MicroSD, the board will boot from the device accordingly.

Table 2 shows the values used for boot selection.

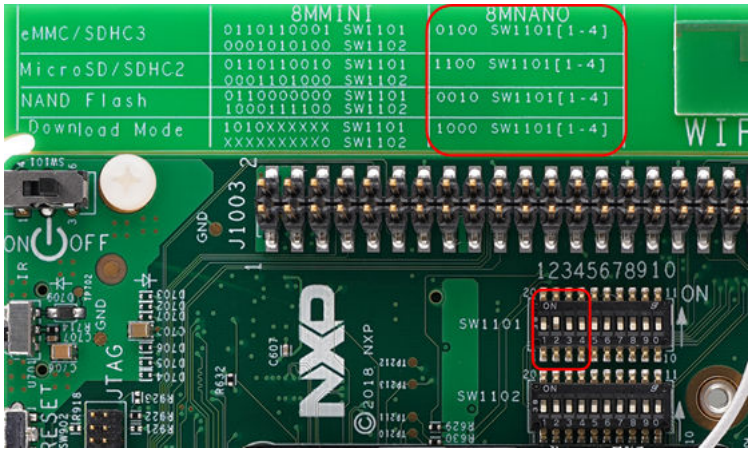

Figure 3. Boot selection

Table 2. Boot selection

BOOT_MODE3 (SW1101 pin4)	BOOT_MODE2 (SW1101 pin3)	BOOT_MODE1 (SW1101 pin2)	BOOT_MODE0 (SW1101 pin1)	Boot device
0	0	0	0	Boot from fuses
0	0	0	1	Serial downloader
0	0	1	0	eMMC/uSDHC3
0	0	1	1	MicroSD/uSDHC2
0	1	0	0	NAND Flash
0	1	1	0	QSPI 3B Read
0	1	1	1	QSPI Hyperflash 3.3 V
1	0	0	0	ecSPI Boot

NOTE

Only SW1101[1-4] are used for boot selection. The left pins of SW1101 and SW1102 are useless for i.MX 8M Nano. Either 0 or 1 is acceptable.

2.3 Power tree

There is a Type-C power supply that needs to be connected to the i.MX 8M Nano LPDDR4 EVK board at connector J302. The other powers on the EVK board are generated from PMIC and discrete devices to supply the whole system. Figure 4 shows the power tree.

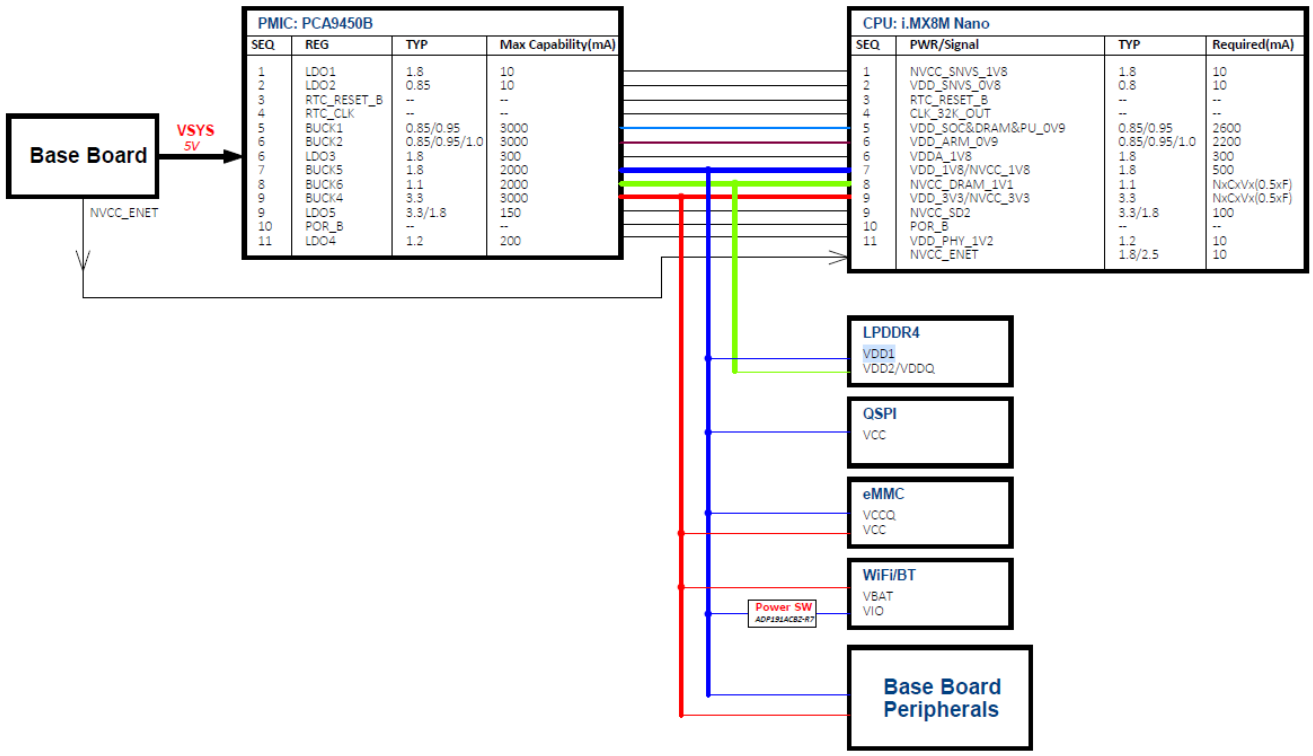

Figure 4. Power tree diagram

In Figure 4, the developer can get all the voltage supply rails used on the EVK board. When some modules are not enabled, the power supplies might be shut down by software. Table 3 lists the power rails on the board.

Table 3. Power rails

SEQ	Power rail	Regulator	Value/V
0	VSYS_5V	From baseboard	5
1	NVCC_SNVS_1V8	PCA9450B LDO1	1.8
2	VDD_SNVS_0V8	PCA9450B LDO2	0.8
3	RTC_RESET_B	PCA9450B	—
4	CLK_32K_OUT	PCA9450B	—
5	VDD_SOC_DRAM_PU_0V9	PCA9450B BUCK1	0.85/0.95[1]
6	VDD_ARM_0V9	PCA9450B BUCK2	0.85/0.95/1.0[2]
6	VDDA_1V8	PCA9450B LDO3	1.8

Table continues on the next page...

Table 3. Power rails (continued)

SEQ	Power rail	Regulator	Value/V
7	VDD_1V8/NVCC_1V8	PCA9450B BUCK5	1.8
8	NVCC_DRAM_1V1	PCA9450B BUCK6	1.1
9	VDD_3V3/NVCC_3V3	PCA9450B BUCK4	3.3
9	NVCC_SD2	PCA9450B LDO5	3.3/1.8
10	POR_B	PCA9450B	—
11	VDD_PHY_1V2	PCA9450B LDO6	1.2

1. PCA9450B BUCK1 default output voltage is 0.85 V. Software will change it to 0.95 V for overdrive mode in SPL before DDR initialization.
2. BUCK2 default output voltage is 0.85 V. Software will change it to 0.95 V for 1.4 GHz and to 1.0 V for 1.5 GHz.

2.4 LPDDR4 DRAM memory

The i.MX 8M Nano LPDDR4 EVK board has one 16 bit LPDDR4 SDRAM chip (C1612PC2WDGTKR-U) for a total of 2 GB RAM memory.

In the physical layout, the LPDDR4 chip is placed on the TOP side, the data traces are not necessarily connected to the LPDDR4 chips in sequential order, but for ease of routing, are connected as best determined by the layout and other critical traces.

The `DRAM_VREF` can be generated by i.MX 8M Nano internally, so it does not need to use external power supply and decoupling capacitors. The calibration resistors used by the LPDDR4 chips and processor are 240 Ohm 1% resistors. The differential termination resistors for DRAM Clock are one 150 ohm 1% resistor on EVK. Developers can change this value depending on simulation and test result.

2.5 eMMC memory (U4)

The eMMC memory is connected to the uSDHC3 interface of i.MX 8M Nano, and it can support up to eMMC 5.1 device. The eMMC memory is on the 8MNANOLPD4-CPU board, and the part number is SDINBDG4-32G-I1 . It is the default boot device of the EVK. The boot settings are as shown in Table 2.

2.6 QSPI Nor Flash (U5)

The QSPI memory is connected to the FlexSPI interface of i.MX 8M Nano, and it can support up to 166 MHz DDR mode device. The QSPI memory is on the 8MNANOPLPD4-CPU board, and the part number is MT25QU256ABA1EW7-0SIT. To select it as the boot device of the EVK, developers can refer to the boot settings as shown in Table 2.

2.7 SD card slot (J701)

There is one MicroSD card slot (J701) on the 8MMINI-BB board, connecting to the uSDHC2 interface of i.MX 8M Nano. This connector supports one 4-bit SD3.0 MicroSD card. To select it as the boot device of the EVK, developers can refer to the boot settings as shown in Table 2.

2.8 MIPI-CSI and MIPI-DSI connectors (J802, J801)

The i.MX 8M Nano processor supports one 4-lane MIPI-CSI and one 4-lane MIPI-DSI. The MiniSAS connectors are designed to support camera and LCD with dedicated pin definition. The connectors are as shown in Figure 2. Display and camera accessory boards are available separately. The full list can be found at i.MX 8 Series Accessory Boards.

2.9 Ethernet connector (J501)

The Ethernet subsystem of the EVK board is provided by the Qualcomm AR8031 Ethernet Transceiver (U501). The Ethernet Transceiver (or PHY) receives standard RGMII Ethernet signals from the MAC-NET core of the i.MX 8M Nano. The processor handles all Ethernet protocols at the MAC layer and above. The PHY is only responsible for the Link Layer formatting. The Ethernet connector (J501) integrates Magnetic transformer inside, so it cannot be directly connected to AR8031 (U501).

Each EVK board has a unique MAC address, which is burned into i.MX 8M Nano by Fuse. A label with the unique MAC address is placed on the connector for reference.

2.10 USB connector (J301, J302)

The i.MX 8M Nano Applications Processors contain one USB 2.0 OTG controller, with one integrated USB PHY. There are two USB Type-C connectors on the EVK board, but only Port1 can support Host and Device Mode.

J301 is connected to USB1 interface of i.MX 8M Nano, which can act as the download port of the EVK.

J302 is the power supply port of the EVK.

2.11 Wi-Fi/Bluetooth (U9)

The EVK board has a Wi-Fi/Bluetooth module AW-CM358SM on the 8MNANOLPD4-CPU board. The module is NXP 88W8987 based, contains SDIO3.0, UART, PCM interface, and can support 802.11a/b/g/n/ac, BT5.0. The 2.4G/5G antenna is stuck to the edge of the Base Board with a coaxial cable connected to the CPU Board.

2.12 Audio line output (J401)

The EVK board uses a high-quality Stereo DAC WM8524 (U401), which can support 24 bit I2S data and 192 KHz sampling rate. The Line output of WM8524 is **2Vrms**, not like common headphone output 1 Vrms. Developers must be very careful about this interface. The Line output connector (J401) is a 3.5 mm 4-pole (or TRRS) phone jack.

NOTE

The Audio Line output connector is designed for active speaker with a power amplifier. To connect it with a headphone, make sure that the headphone has volume control functionality and set the headphone's volume properly before wearing it. Do not plug in the non-volume-control headphone directly. The audio output volume may be too high for non-volume-control headphone and may damage it.

2.13 Audio card connector (J1001)

One 60-pin FPC connector (J1001) is provided on the EVK board to support audio card connection, and the developers can use the audio card to perform audio features development.

NOTE

There is no SAI1 from the i.MX 8M Nano process, so AK4458/AK4497 can't be enabled on audio card.

2.14 JTAG connector (J902)

The i.MX 8M Nano Applications Processor has four JATG signals on dedicated pins, and one HW reset input signal POR_B. Those signals are directly connected to the 10-pin 1.27 mm JTAG connector J902. The four JTAG signals used by the processor are:

- `JTAG_TCK`: TAP Clock
- `JTAG_TMS`: TAP Machine State
- `JTAG_TDI`: TAP Data In
- `JTAG_TDO`: TAP Data Out

2.15 USB-UART connector (J901)

The i.MX 8M Nano Applications Processor has four independent UART ports, UART1 - UART4. On the EVK board, UART2 is used for Cortex-A53 core and UART4 is used for Cortex-M7 core. We use a single-chip USB to dual-channel UART IC for system debugging, and the part number is FT2232D. The developers can download the driver from FTDI. After the driver for FT2232D is installed, the PC will enumerate two COM ports when the USB cable is plugged into J901. Developers can use Putty, Tera Term, Xshell, or other terminal tools. The required settings are as listed in Table 4.

Table 4. Terminal setting parameters

Data rate	115,200 baud
Data bits	8
Parity	None
Stop bits	1

2.16 Expansion connector (J1003)

One 40-pin dual-row Pin Header connector, **J1003**, is provided on the EVK board to support I^2S, UART, I2C, and GPIO connection. The developers can use the port for some specific application development.

Table 5. J1003 pin definition

No.	Net name	Description	No.	Net name	Description
1	VEXT_3V3	Power Output, 3.3 V	2	VDD_5V	Power Output, 5 V
3	I2C3_SDA_3V3	I2C3 data signal	4	VDD_5V	Power Output, 5 V
5	I2C3_SCL_3V3	I2C3 clock signal	6	GND	Ground
7	UART3_CTS	UART3 clear to send signal	8	UART3_TXD	UART3 transmit signal
9	GND	Ground	10	UART3_RXD	UART3 transmit signal
11	UART3_RTS	UART3 request to send signal	12	EXP_IO8	Expansion IO signal
13	EXP_IO9	Expansion IO signal	14	GND	Ground
15	EXP_IO10	Expansion IO signal	16	EXP_IO11	Expansion IO signal
17	VEXT_3V3	Power Output, 3.3 V	18	—	NC
19	ECSPI2_MOSI	SPI2 data signal, master output slave input	20	GND	Ground
21	ECSPI2_MISO	SPI2 data signal, master input slave output	22	—	NC
23	ECSPI2_SCLK	SPI2 clock signal	24	ECSPI2_SS0	SPI2 chip select signal
25	GND	Ground	26	—	NC

Table continues on the next page...

Table 5. J1003 pin definition (continued)

No.	Net name	Description	No.	Net name	Description
27	—	NC	28	—	NC
29	—	NC	30	GND	Ground
31	EXP_IO14	Expansion IO signal	32	EXP_IO12	Expansion IO signal
33	EXP_IO13	Expansion IO signal	34	GND	Ground
35	SAI5_RXD3	SAI5 receive data signal	36	SAI5_RXD2	SAI5 receive data signal
37	SAI5_RXD1	SAI5 receive data signal	38	SAI5_RXD0	SAI5 receive data signal
39	GND	Ground	40	SAI5_RXC	SAI5 receive clock signal

2.17 I²C connector (J1004)

One 8-pin dual-row Pin Header connector (J1004) is provided on the EVK board to support I²C connection. The developers can use the port for some specific application development.

Table 6. J1004 pin definition

No.	Net name	Description
1/2	VDD_3V3	Power Output, 3.3 V
3/4	I2C3_SCL_3V3	I²C clock signal
5/6	I2C3_SDA_3V3	I²C data signal
7/8	GND	Ground

2.18 User interface buttons

There are two user interface buttons on the EVK board.

2.18.1 Power button (SW901)

The i.MX 8M Nano Applications Processor supports the use of a button input signal to request main SoC power state changes, such as, ON or OFF, from the PMU.

The ON/OFF button can be used for debounce, OFF-to-ON time, and max timeout. Debounce is used to generate the power-off interrupt. In the ON state, if ON/OFF button is held longer than the debounce time, the power-off interrupt is generated. In the OFF state, if the ON/OFF button is held longer than the OFF-to-ON time, the state will transit from OFF to ON. Max timeout can also be the time for requesting physical power down after the ON/OFF button has been held for the defined time.

2.18.2 Reset button (SW902)

The RESET button, SW902, is directly connected to the PMIC PCA9450B. Holding the RESET button will force to reset the PMIC power outputs except `NVCC_SNVS_1V8` and `VDD_SNVS_0V8` on the EVK board. The i.MX 8M Nano applications processor will be immediately turned off and reinitiate a boot cycle from the OFF state.

2.19 User interface LED indicators

There are four LED indicators on the board. These LEDs have the following functions:

- Main power supply, D708:
  - Green: The board is powered on.
  - OFF: The board is powered off.
- System status, D1, on 8MNANOLPD4-CPU
  - Green blinking: – CPU is running well.
  - OFF: CPU is not running.
- M7 UART, D902/D903
  - D902 Green light flashing: The UART data transmitted to PC.
  - D903 Orange light flashing: The UART data received from PC.
- A53 UART, D906/D905
  - D906 Green light flashing: The UART data transmitted to PC.
  - D905 Orange light flashing: The UART data received from PC.

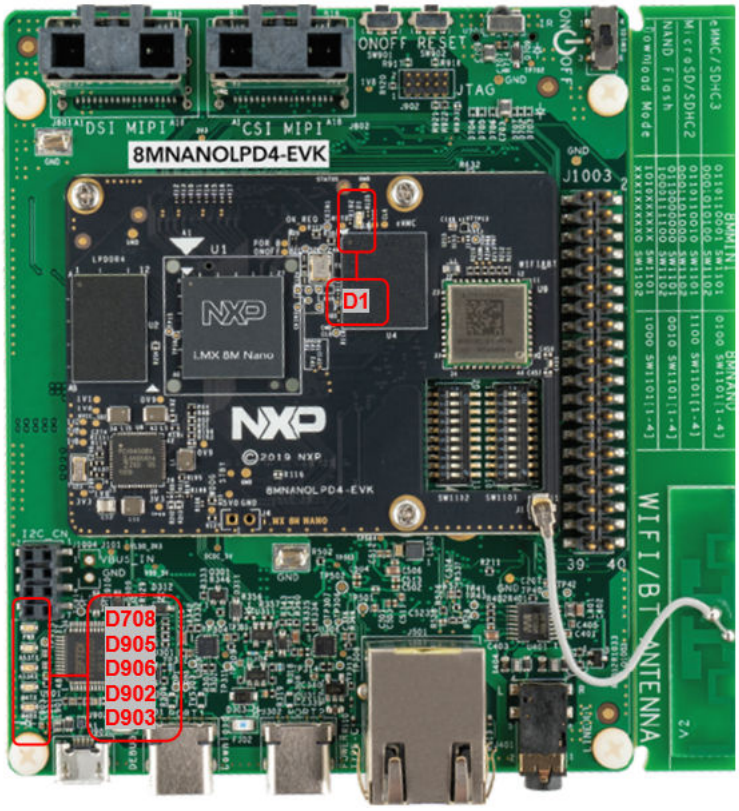

Figure 5. LED indicator

Chapter 3
PCB information

The i.MX 8M Nano LPDDR4 EVK is composed by 8MNANOLPD4-CPU and 8MMINI-BB. Table 1 lists the dimensions of the two boards. Both boards are made with standard 8-layer technology and the material is FR-4. The PCB stack-up information is shown in Table 7 and Table 8.

Table 7. 8MNANOLPD4-CPU Board stack up information

Layer	Description	Coppoer (Oz.)	Dielectric thickness (mil)
1	Signal	0.5+Plating	
	Dielectric		2.76 mil
2	GND	1	
	Dielectric		2.95 mil
3	Signal	1	
	Dielectric		25.28 mil
4	Power	1	
	Dielectric		2.95 mil
5	Power	1	
	Dielectric		2.76 mil
6	Signal	0.5+Plating	
Total thickness:	47.24(4.72/-4.72) mil		1.2 (+0.12/-0.12) MM
Material:	TU768		TU768

Table 8. 8MMINI-BB Board stack up information

Layer	Description	Coppoer (Oz.)	Dielectric thickness (mil)
1	Signal	0.5+Plating	
	Dielectric		2.77 mil
2	GND	1	
	Dielectric		4.33 mil
3	Signal	1	

Table continues on the next page...

Table 8. 8MMINI-BB Board stack up information (continued)

Layer	Description	Coppoer (Oz.)	Dielectric thickness (mil)
	Dielectric		12.89 mil
4	Power	1	
	Dielectric		11.81 mil
5	Power	1	
	Dielectric		12.89 mil
6	Signal	1	
	Dielectric		4.33 mil
7	GND	1	
	Dielectric		2.77 mil
8	Signal	0.5+Plating	
Total thickness:	62.992 (6.299/-6.299) mil		1.6 (+0.16/-0.16) MM
Material:	TU768		TU768

3.1 EVK design files

You can download the schematics, layout files, gerber files, and BOM from i.MX 8M Nano.

Chapter 4
Revision history

Table 9. Revision history

Rev.	Date	Description
0	10/2020	Initial release
1	12/2020	• Updated Power tree • Updated Table 7

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