

MISRTRONICS

# UPDATED DESIGN OF A 6 GHZ BOARD

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## UPDATED DESIGN DOCUMENT

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**8/17/2023**

*This document contains all the design steps, explanations, simulation results and design details of the RF PCB board as specified by the project owner. It includes also all the additional requirements of the project owner that have been completely done.*

## CONTENTS

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<b>1. GENERAL DESIGN TASK .....</b>	5
<b>1.1. RF Transmission Lines.....</b>	5
<b>1.2. Transmission Line Design.....</b>	6
<b>2. THE PLL FREQUENCY SYNTHESIZER .....</b>	8
<b>2.1. Given Information.....</b>	8
<b>2.2. ADF4356 Schematic Design.....</b>	10
<b>2.3. The SIT5021AI-2DE-33E-100.000000X Reference Oscillator.....</b>	11
<b>2.4. The Loop Filter .....</b>	13
<b>2.5. PLL Power Supply .....</b>	15
<b>2.5.1. Power Supply Requirements .....</b>	15
<b>2.5.2. The ADM7150.....</b>	17
<b>2.5.3. Power Supply Design .....</b>	18
<b>2.6. The PLL Schematic and Layout Design.....</b>	19
<b>2.7. Updating the PLL Schematic and Layout Design.....</b>	21
<b>3. RF TRANSMITTER.....</b>	24
<b>3.1. The I/Q MODULATOR.....</b>	24
<b>3.1.1. The Input Transmissioin lines .....</b>	27
<b>3.1.2. Coupling caoacitors from PLL to Modulator .....</b>	28
<b>3.1.3. Another Tx-Rx Layout Design .....</b>	29
<b>3.1.4. Modulator Schematic and Layout Design .....</b>	32
<b>3.2. The POWER AMPLIFIER .....</b>	33
<b>3.2.1. Power Amplifiet Schematic.....</b>	33
<b>3.2.2. Power Amplifier IC .....</b>	33
<b>3.2.3. Power Supply Requirements .....</b>	35
<b>3.2.4. Power Amplifier Schematic Drawing.....</b>	36
<b>3.2.5. The Output RF Connector .....</b>	36
<b>3.3. The TRANSMITTER LAYOUT DESIGN.....</b>	37
<b>4. RF RECEIVER .....</b>	37
<b>4.1. Given Schematic Design.....</b>	37
<b>4.2. The QPL9098TR7 LNA.....</b>	38
<b>4.3. The 2450BL15B100E BALUN Transformer .....</b>	41
<b>4.4. The ADL5380 Quadrature Demodulator .....</b>	43
<b>4.5. RECEIVER INTEGRATION .....</b>	45

<b>5. THE 5V POWER BUDGET .....</b>	47
<b>5.1. The 5V Power Supply Decision.....</b>	47
<b>6. RF PCB POWER SUPPLIES .....</b>	48
<b>7. RF PCB INTEGRATION.....</b>	50
<b>7.1. RF PCB SCHEMATIC DESIGN.....</b>	50
<b>7.2. RF PCB LAYOUT DESIGN.....</b>	52
<b>7.2.1. RF PCB LAYOUT DESIGN .....</b>	52
<b>7.3. RF PCB BILL OF MATERIALS .....</b>	55
<b>8. PROJECT OWNER'S FEEDBACK.....</b>	60
<b>9. IMPLEMENTATION OF THE OWNER'S MODIFICATIONS.....</b>	62
<b>9.1. GENERAL MECHANICAL MODIFICATIONS.....</b>	62
<b>9.2. I/Q PROCESSING CIRCUITS DESIGN.....</b>	63
<b>9.2.1. RECEIVER I/Q OUTPUT PROCESSING CIRCUITS.....</b>	63
<b>9.2.2. LIMITING AMPLIFIER DESIGN.....</b>	64
<b>9.2.3. Project Owner's Requests regarding the Rx Limiting Amplifier.....</b>	66
<b>9.3. INPUT/OUTPUT &amp; CONTROL SIGNALS.....</b>	66
<b>9.4. SCHEMATID DESIGN DRAWING OF THE RF ASSEMBLY.....</b>	70
<b>9.5. LAYOUT DESIGN DRAWING OF THE RF ASSEMBLY .....</b>	73
<b>10. NEW REQUIREMENTS OF THE PROJECT OWNER .....</b>	74
<b>A. RX down-converter Output ADL5380 • .....</b>	74
<b>B. TX Up-converter LO input ADL5375 • .....</b>	74
<b>C. TX Up-converter Data input ADL5375 • .....</b>	75
<b>D. Another Spec that I forgot to point out as well:.....</b>	76
<b>11. DESIGN AND IMPLEMENTATION OF THE REQUIRED FILTERS.....</b>	76
<b>11.1. RX downconverter Output Filters.....</b>	76
<b>11.2. Baseband LPF Design .....</b>	76
<b>11.3. RF LPF between the PLL and the Modulator.....</b>	81
<b>11.3.1. RF LPF Design.....</b>	81
<b>11.3.2. Differential LPF induction .....</b>	82
<b>11.4. Tx Up-converter Data Input Filters.....</b>	87
<b>11.5. Simulating the Single Ended LPF .....</b>	89
<b>11.6. Biasing the ADLS375-05 Modulator data inputs .....</b>	91
<b>11.7. Biasing the ADLS375-15 Modulator data inputs .....</b>	93
<b>11.8. Inserting the LPF and bias at the modulator inputs.....</b>	95
<b>12. UPDATED DESIGN .....</b>	97

<b>12.1.</b>	<b>Design with ADL5375-15 Modulator.....</b>	97
<b>12.2.</b>	<b>BOM with ADL5375-15 Modulator.....</b>	100
<b>12.3.</b>	<b>Design with ADL5375-05 Modulator.....</b>	109
<b>12.4.</b>	<b>BOM with ADL5375-05 Modulator.....</b>	112
<b>13.</b>	<b>RECOMMENDED DESIGN.....</b>	122
<b>13.1.</b>	<b>An Important Note regarding substrate thickness .....</b>	122
<b>13.2.</b>	<b>Recommended Substrate Parameters .....</b>	124
<b>13.3.</b>	<b>RECOMMENDED LAYOUT DESIGN .....</b>	125
	<b>REFERENCES.....</b>	130

# DESIGN TASK

## 1. GENERAL DESIGN TASK

It is required to design an RF Assembly consisting of a PLL Frequency Synthesizer, An RF Transmitter and an RF Receiver as shown in the following figure.

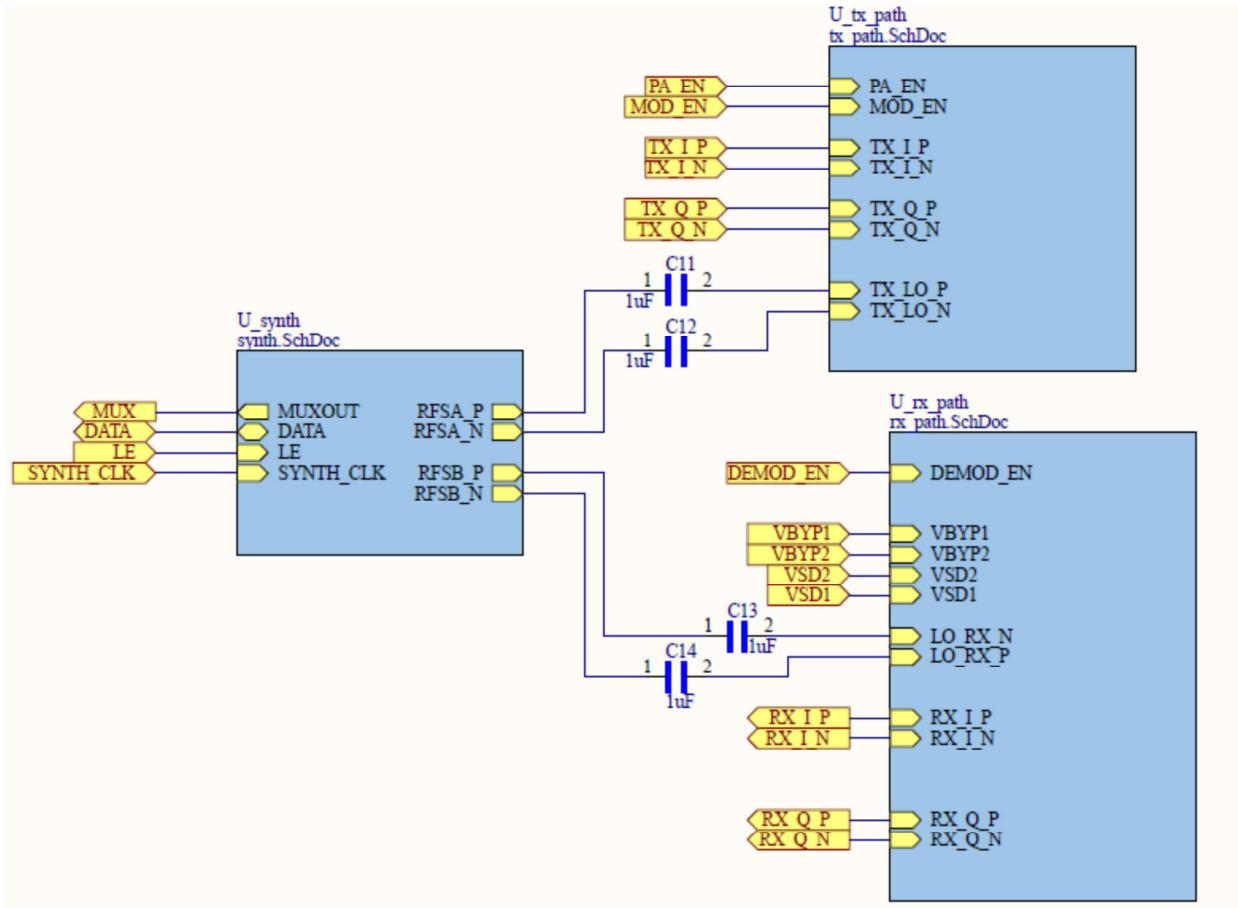


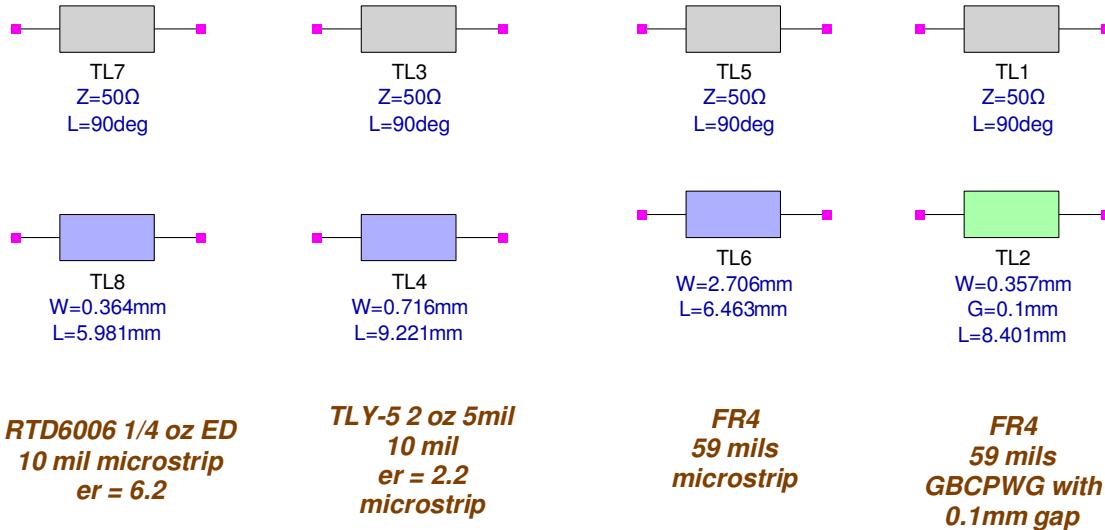
Figure 1. RF Assembly

### 1.1. RF Transmission Lines

- All the RF transmission lines should be matched to  $50 \text{ } [\Omega]$  characteristic impedance in the frequency range 5.5 to 6 GHz.
- The TL width must be  $< 0.5 \text{ mm}$  to avoid problems with the pin separations of the integrated circuits used in the design.
- Microstrip TL is preferred by the project owner than GBCPWG..
- The substrate to be used was specified by the project owner to be:
  - $\epsilon_r = 2.2$
  - height = 10 mils

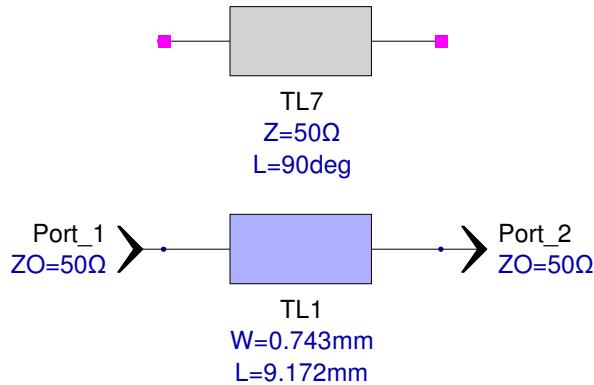
## 1.2. Transmission Line Design

- Different substrates have been assumed and the  $50 \text{ } [\Omega]$  TL dimensions for each have been calculated. The results are shown in the following figure.



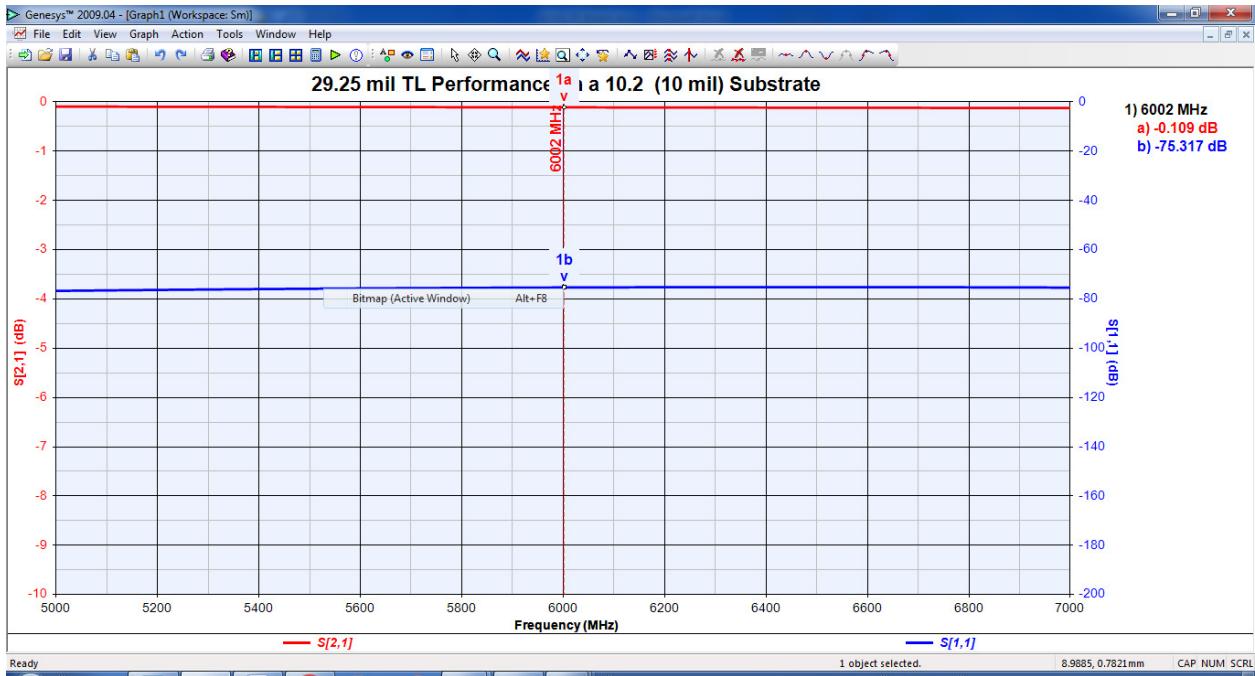
**Figure 2. TL design for different possible substrates**

- When the project owner specified a substrate with  $\epsilon_r = 2.2$  and  $h = 10$  mils, a  $50 \text{ } [\Omega]$  microstrip TL was designed for this specific substrate. It is shown in the following figure.



**Figure 3a. 50 Ohm Matched microstrip TL for the owner-specified substrate**

- The designed microstrip TL was simulated in the frequency range 5 to 7 GHz with the following results:



**Figure 3b. Frequency response of the shown 50 Ohm Matched microstrip TL**

S11 < -75 dB

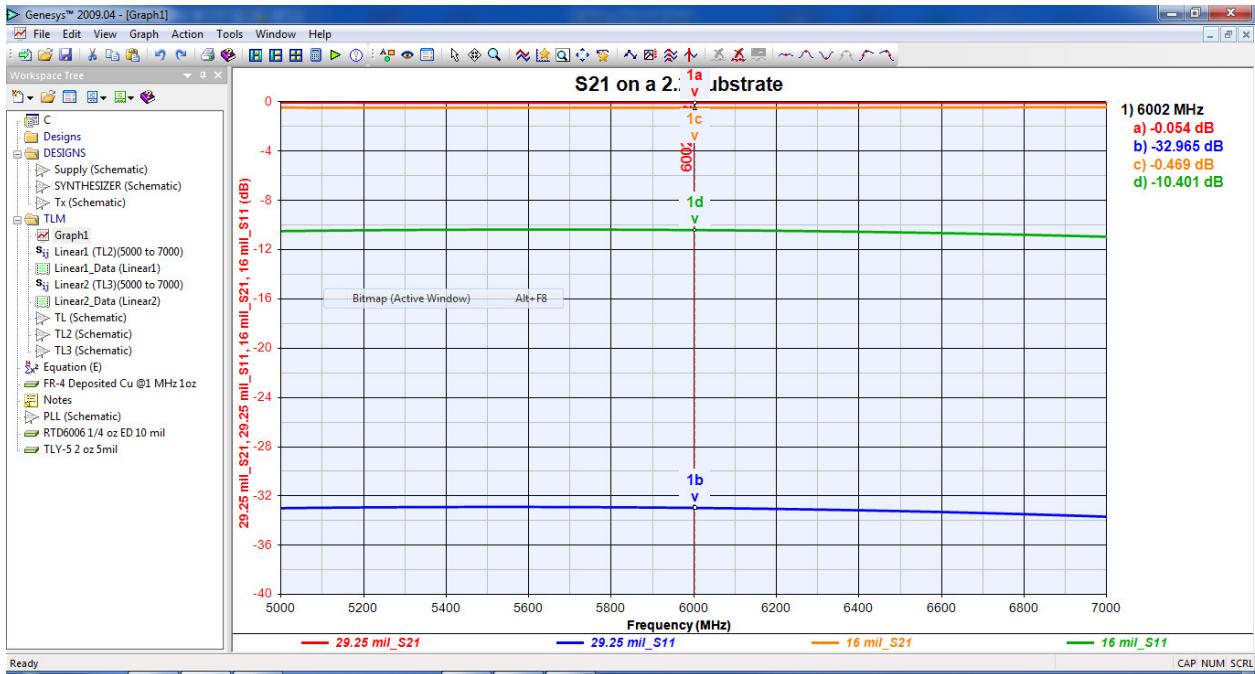
S21 > -0.11 dB

- It is well matched. But the line width is 0.743mm (29.25 mils) > 0.5mm.
- The project owner specified a TL width of 16 mils.
- A 10 mm of the 16 mils and 29.25 mil microstrip TL were simulated and compared with the following results (shown in the next figure):

S11 < -9.65 dB

S21 > -0.62 dB

- Since the return loss is of the order of the 10 dB required for acceptable matching ( $VSWR = 2$ ); the compromise can be accepted due to the restrictions posed by the project owner on the substrate to be used.
- As recommended by the project owner, the transmission lines should be as short as possible; in order to minimize RF losses that would increase otherwise; due to the relatively high insertion loss.
- When possible, tapered TL width (between 16 mils and 29.25 mils) may be used in the transition between the IC pin and the TL to enhance RF match and minimize reflection.



**Figure 3c. Frequency response comparison of 16 mil and 29.25 mil microstrip TL**

## 2. THE PLL FREQUENCY SYNTHESIZER

### 2.1. Given Information

- It is required to use the ADF4356 fractional-N / integer-N phase-locked loop (PLL) frequency synthesizers with built-in VCO and the [SIT5021AI-2DE-33E-100.000000X](#) reference oscillator with 100 MHz frequency, LVDS output and 5ppm frequency stability. Its size is 7mmx5mm; according to the part number size code “D”.
- The PLL synthesizer generates two balanced RF outputs, A and B.
- The PLL synthesizer should be controlled by an MCU via a 4-wire control bus (Enable, Clock, Data-In and Data\_Out).
- It is required to connect the given loop filter in the feedback loop of the PLL frequency synthesizer.
- The schematic design drawing of the PLL Frequency Synthesizer is shown in the following figure.

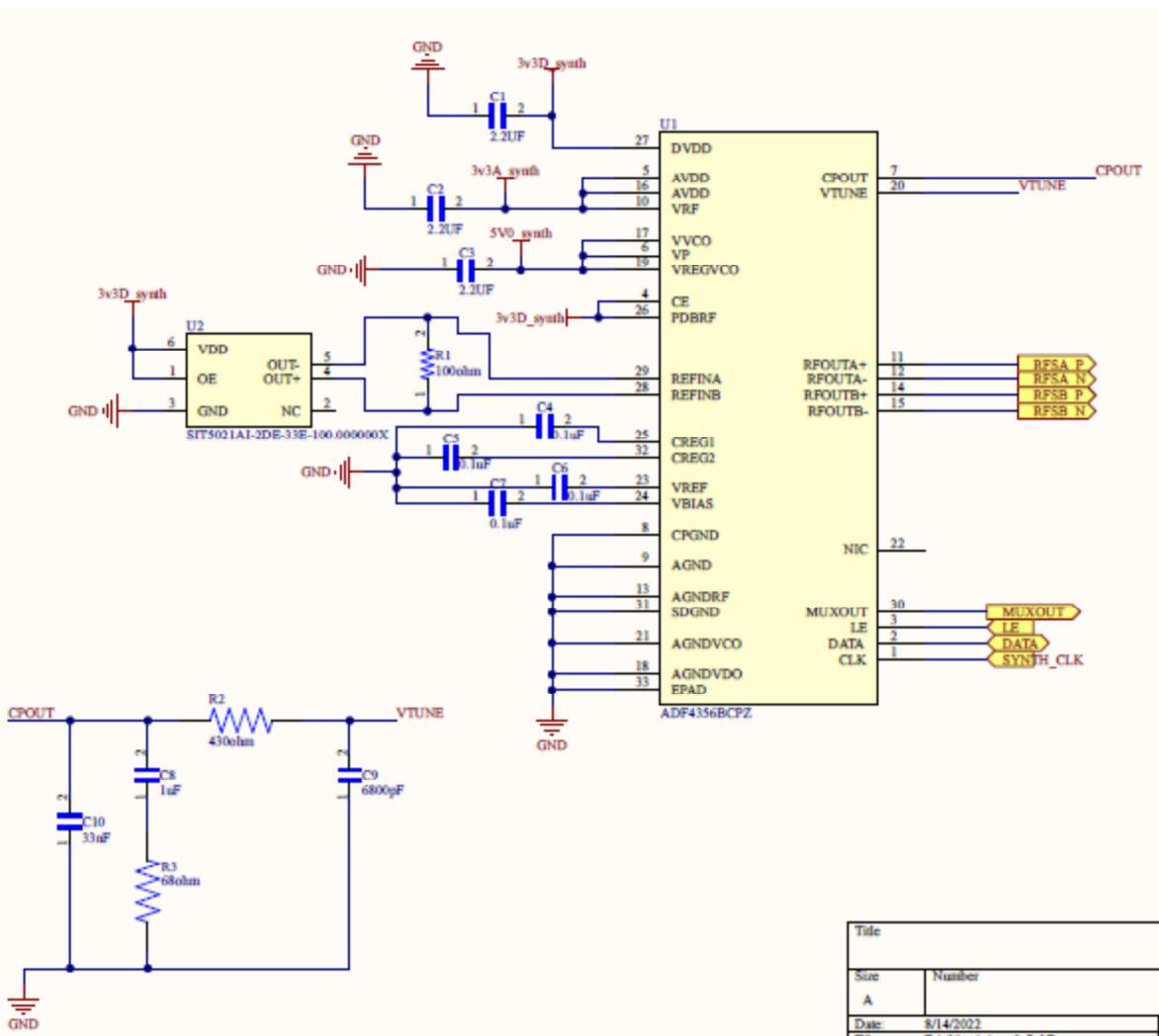
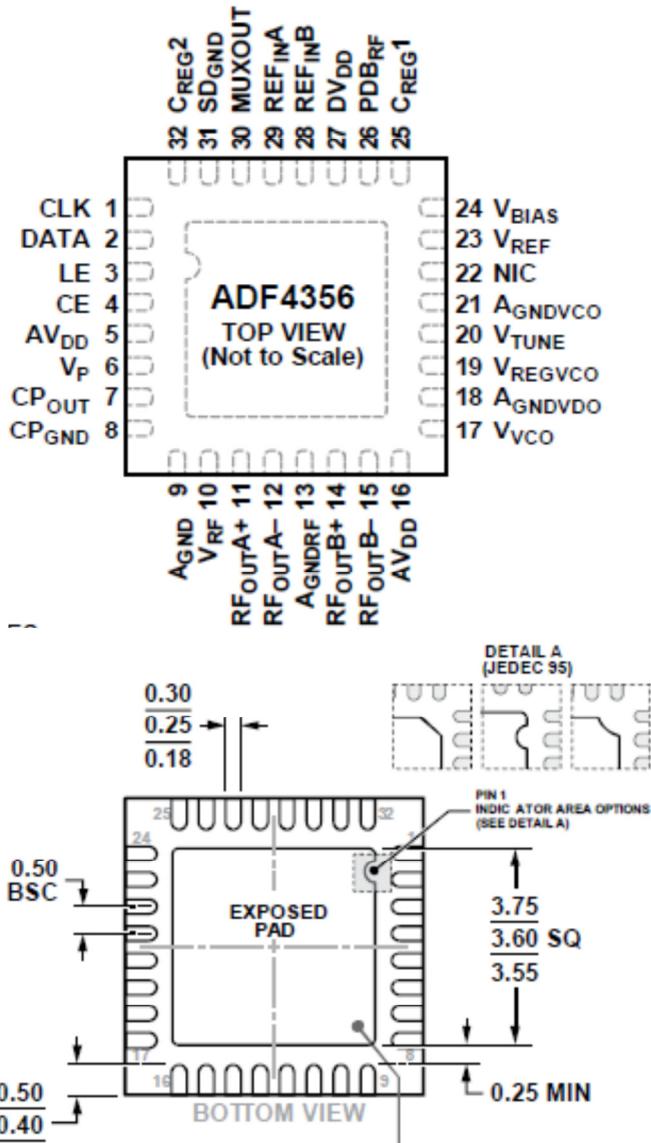


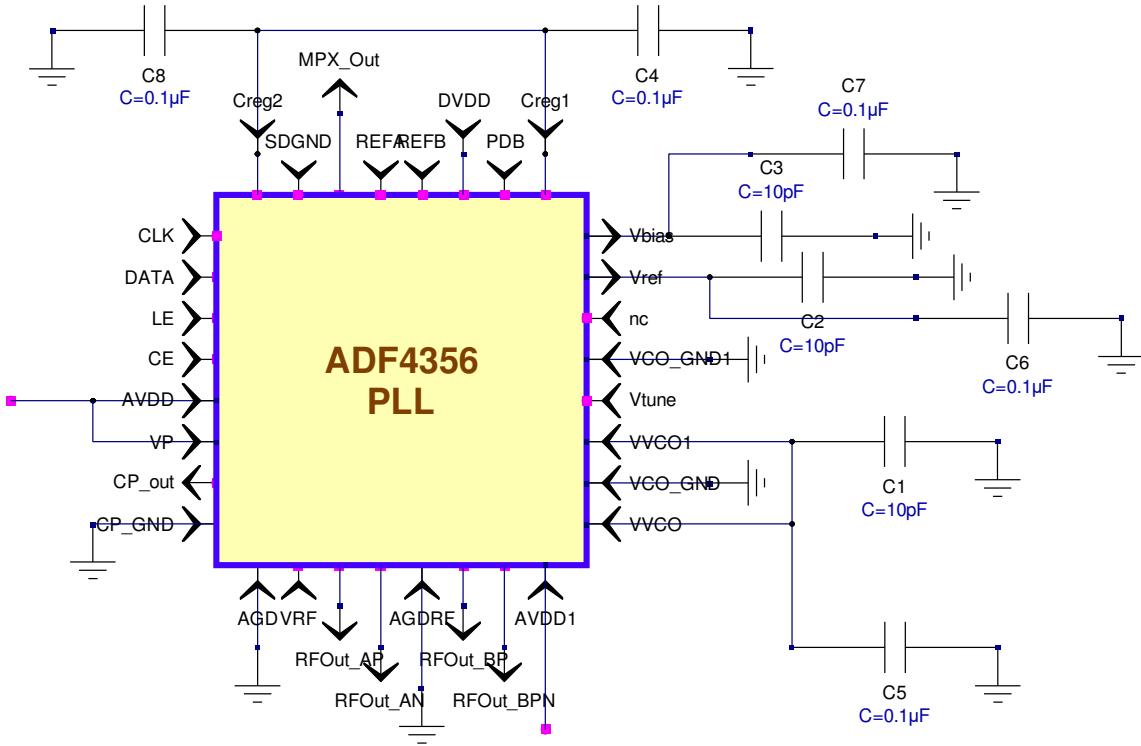
Figure 4. PLL Frequency Synthesizer



**Figure 5. The ADF4356 PLL Synthesizer**

## 2.2. ADF4356 Schematic Design

The following figure shows the preliminary schematic drawing of the ADF4356 circuit without reference oscillator and power supplies.



**Figure 6. The preliminary ADF4356 PLL Frequency Synthesizer Schematic**

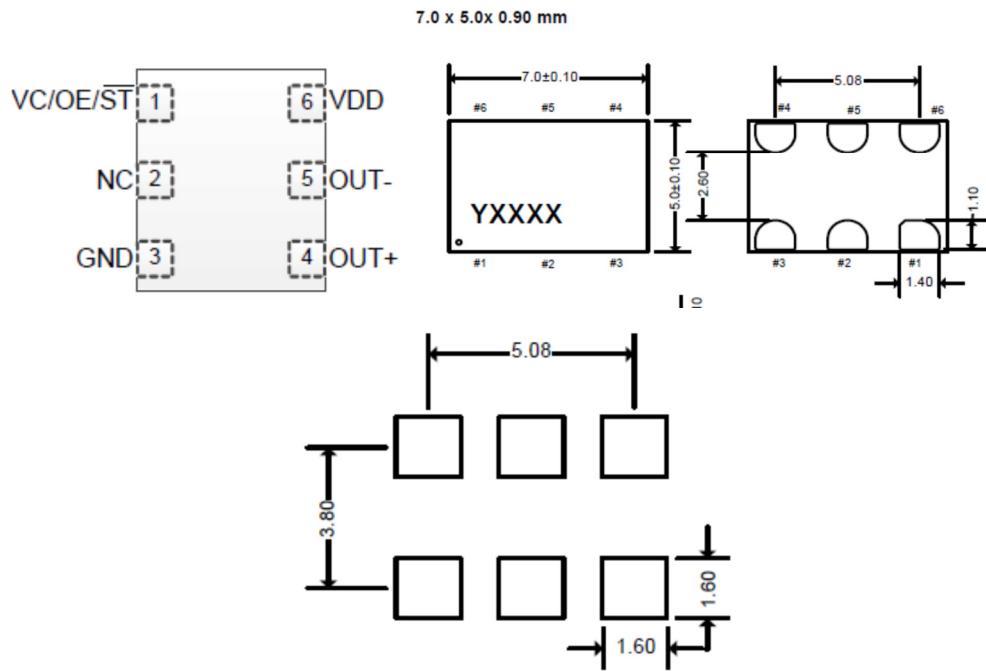
### 2.3. The SIT5021AI-2DE-33E-100.000000X Reference Oscillator

The following figure shows the SIT5021AI-2DE-33E-100.000000X reference oscillator pin configuration and layout footprint.

From the part number we can know the following:

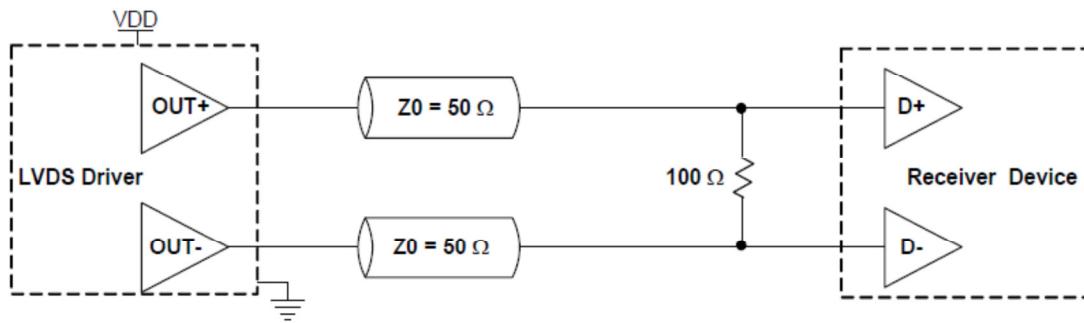
- The part family is SiT5021
- Revision A
- Industrial temperature range (-40 °C to 85°C)
- LVDS output
- 7mm x 5mm package size
- ±5.0 ppm frequency stability. The PLL will get the same stability of the reference oscillator.
- 3.3V ±10% power supply
- Pin1: Output Enable. A HIGH on this pin enables the reference oscillator output
- Frequency = 100 MHz.

This reference oscillator consumes less than 69 mA.

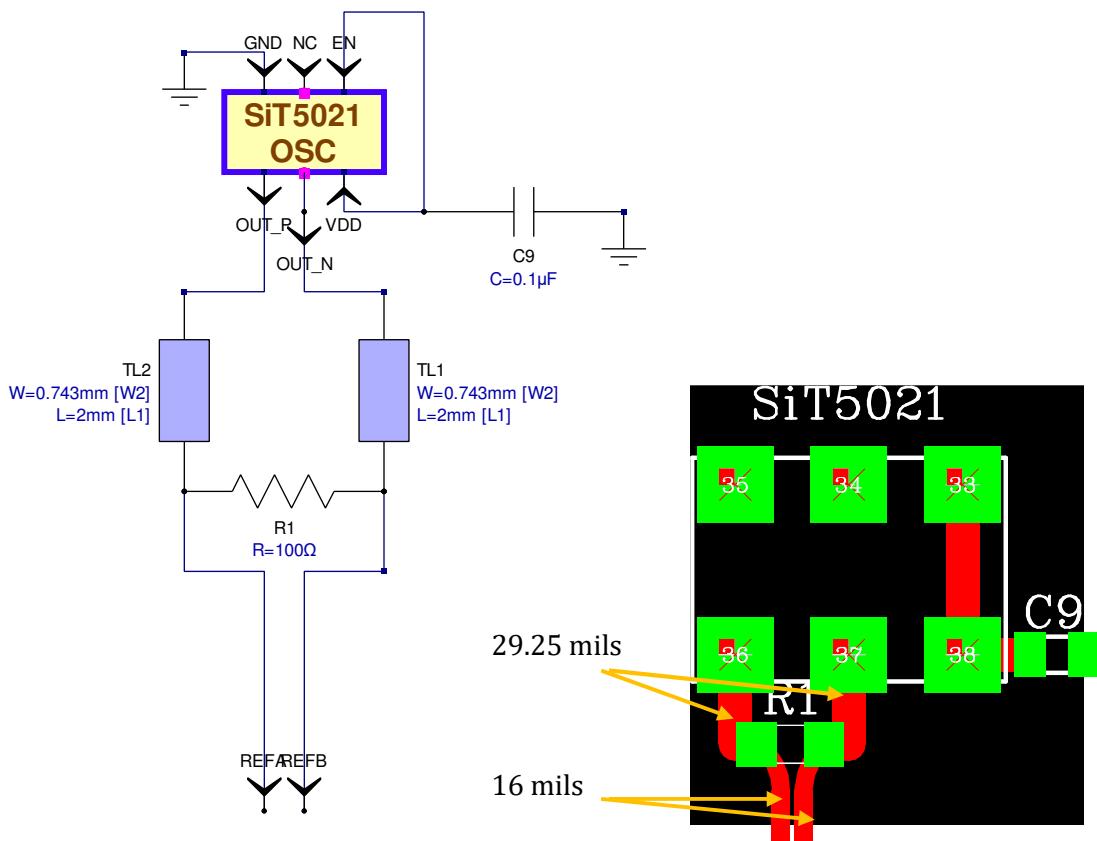


**Figure 7. The SIT5021AI-2DE-33E-100.000000X clock generator**

The LVDS differential output of the reference oscillator should be connected as shown in the following figure.



**Figure 8. Differential connection of the LVDS output**

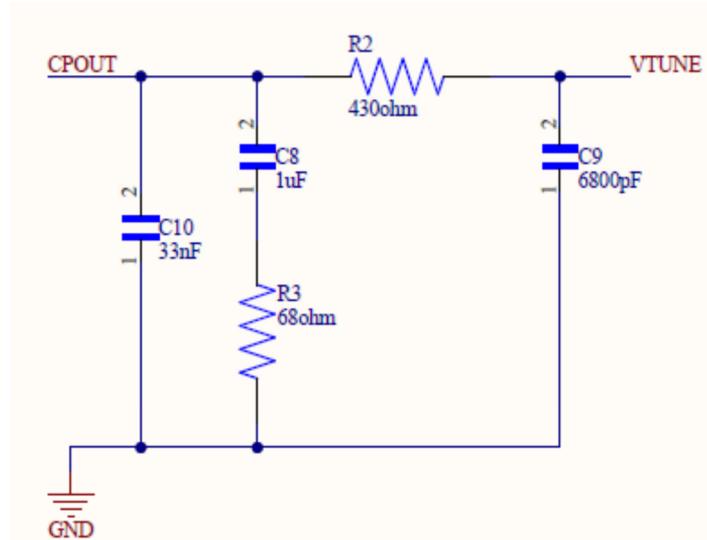


**Figure 9. SiT5021 Reference Oscillator connections**

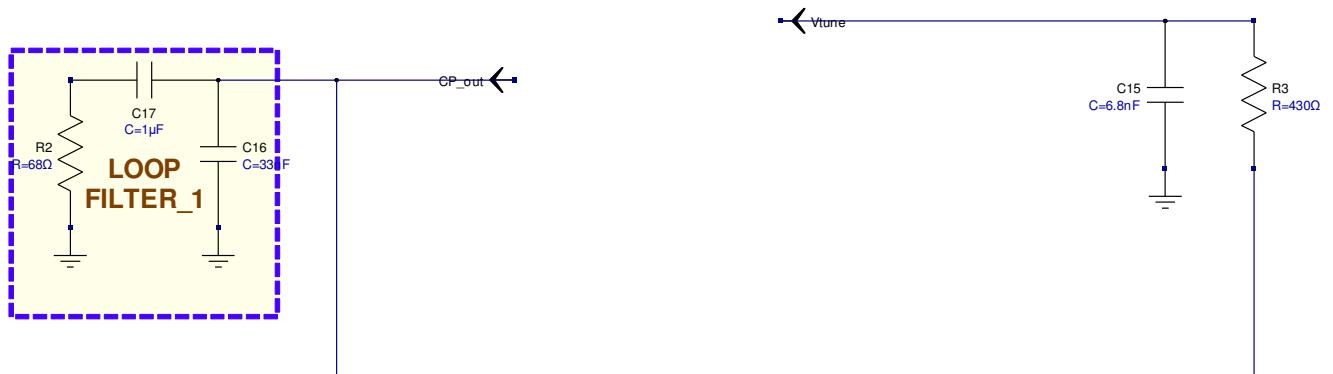
As seen in this figure, the differential output is taken via two matched microstrip transmission lines with the exact 0.743mm (29.25 mils) width for 50  $\Omega$  characteristic impedance for 2 millimeters until they are terminated by the 100  $\Omega$  resistance to forbid reflection. Then they are driven to the high impedance common emitter inputs of the reference oscillator input in the PLL via two 16 mil microstrip transmission lines.

## 2.4.The Loop Filter

The PLL loop filter has already been designed by the project owner. It is given in the following figure.



**Figure 10a.** The PLL Loop Filter as designed by the project owner



**Figure 10b.** The PLL Loop Filter in our design

## 2.5. PLL Power Supply

### 2.5.1. Power Supply Requirements

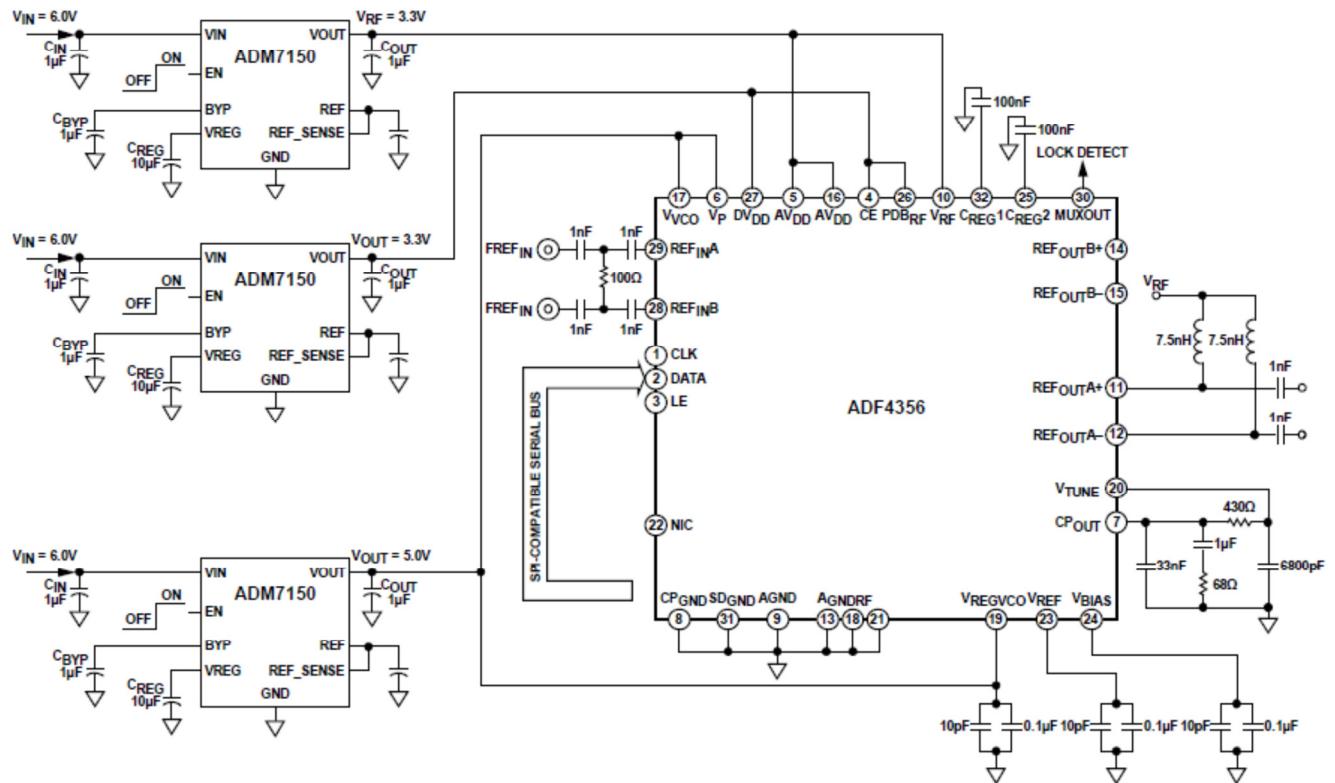
The ADF4356 needs two different supply voltages; +5V and +3.3V.

In order to design the power PLL supply we have to study the required current from each voltage.

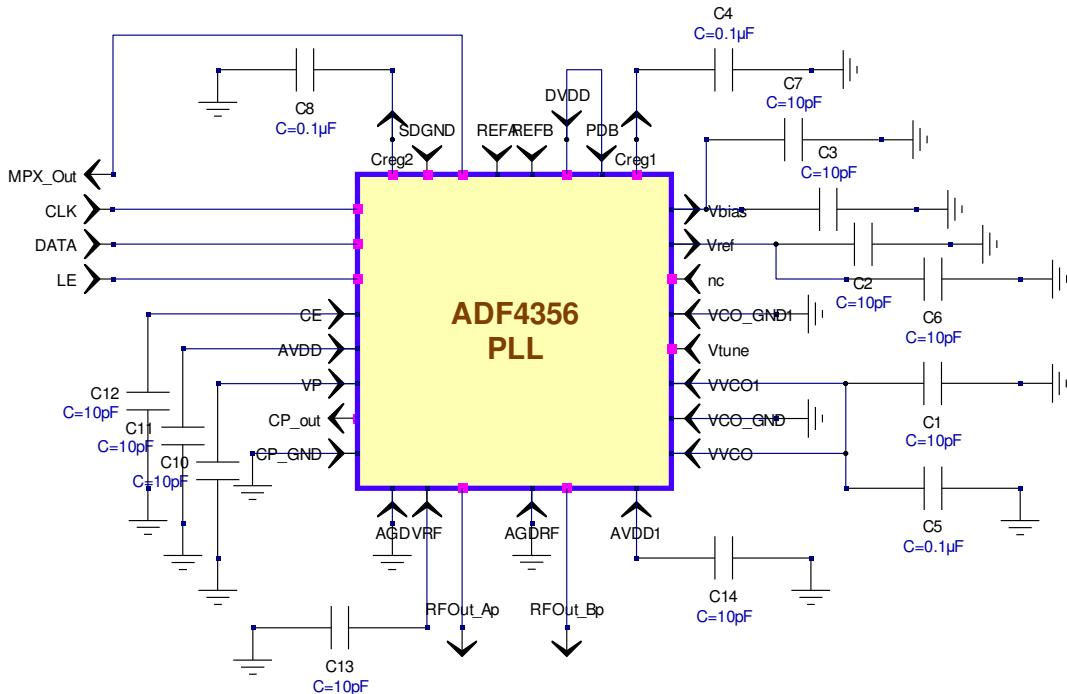
**TABLE 1. POWER SUPPLY REQUIREMENTS**

Load	Supply Voltage	Max. Supply Current	Notes
	V	mA	
<b>VCO</b>	+5	90	
<b>CP</b>	+5	9	<i>Charge pump</i>
<b>5V Total</b>	<b>+5</b>	<b>99</b>	<b>Total 5V supply current</b>
<b>AV<sub>DD</sub></b>	+3.3	92	<i>Analog circuits</i>
<b>DV<sub>DD</sub></b>	+3.3		<i>Digital circuits</i>
<b>Frq. dividers</b>	+3.3	36	
<b>RFout</b>	+3.3	108	<i>Both outputs active at +5dBm</i>
<b>3.3V total</b>	<b>+3.3</b>	<b>136</b>	<b>Total 3.3V supply current</b>

Analog Devices recommends to use the ADM7150 low-noise linear regulator. Although it is capable of supplying up to 800 mA, it is recommended to separate digital supplies from analog supplies. Therefore, it is recommended to use three ADM7150 low-noise linear regulators, one for +3.3V analog supply, another for +3.3V digital supply and a third one for +5V supply, as shown in the following figure.



**Figure 11a. Recommended PLL Power Supplies**

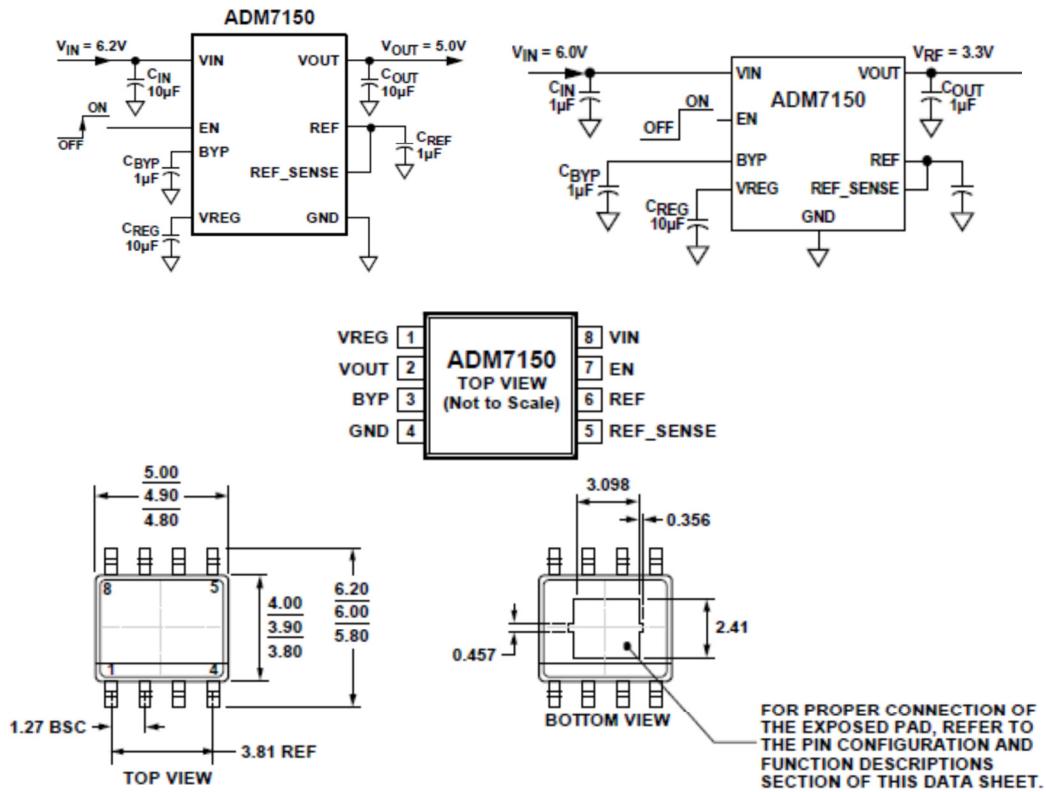


**Figure 11b. PLL Power Supplies in our design**

## 2.5.2.The ADM7150

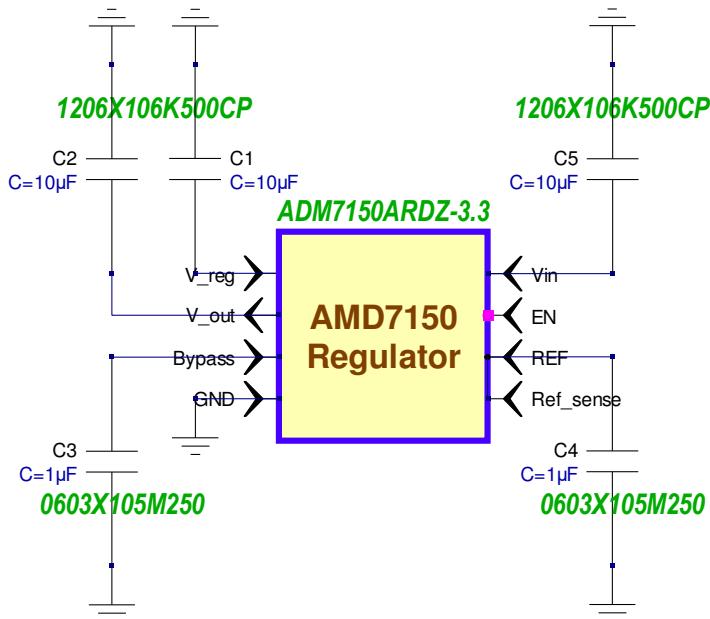
### MAIN FEATURES

- Input voltage range: 4.5 V to 16 V
- Maximum output current: 800 mA
- Low noise
  - $\mu$ V rms total integrated noise from 100 Hz to 100 kHz
  - 1.6  $\mu$ V rms total integrated noise from 10 Hz to 100 kHz
  - Noise spectral density: 1.7 nV $\sqrt{\text{Hz}}$  typical from 10 kHz to 1 MHz
- Power supply rejection ratio (PSRR) at 400 mA load
  - >90 dB from 1 kHz to 100 kHz, VOUT = 5 V
  - >60 dB at 1 MHz, VOUT = 5 V
- Dropout voltage: 0.6 V at VOUT = 5 V, 800 mA load
- Initial voltage accuracy:  $\pm 1\%$
- Voltage accuracy over line, load and temperature:  $\pm 2\%$
- Quiescent current (IGND): 4.3 mA at no load
- Low shutdown current: 0.1  $\mu$ A
- Stable with a 10  $\mu$ F ceramic output capacitor
- Fixed output voltage options: 1.8 V, 2.8 V, 3.0 V, **3.3 V**, 4.5 V, 4.8 V, and **5.0 V** (16 outputs between 1.5 V and 5.0 V are available)
- Exposed pad 8-lead LFCSP and 8-lead SOIC packages

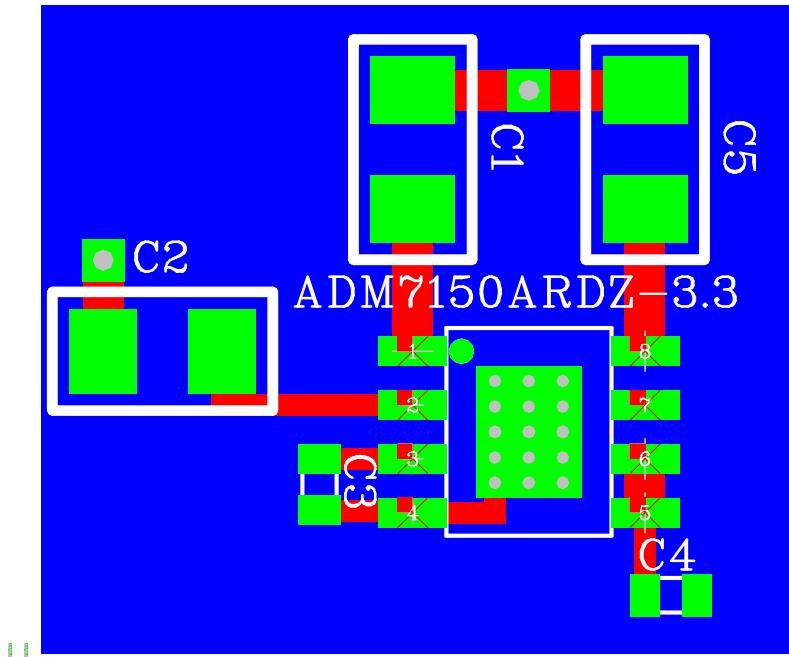


**Figure 12. The ADM7150 Voltage Regulator**

### 2.5.3.Power Supply Design



**Figure 13a. Voltage Regulator schematic in our design, complete with part numbers**



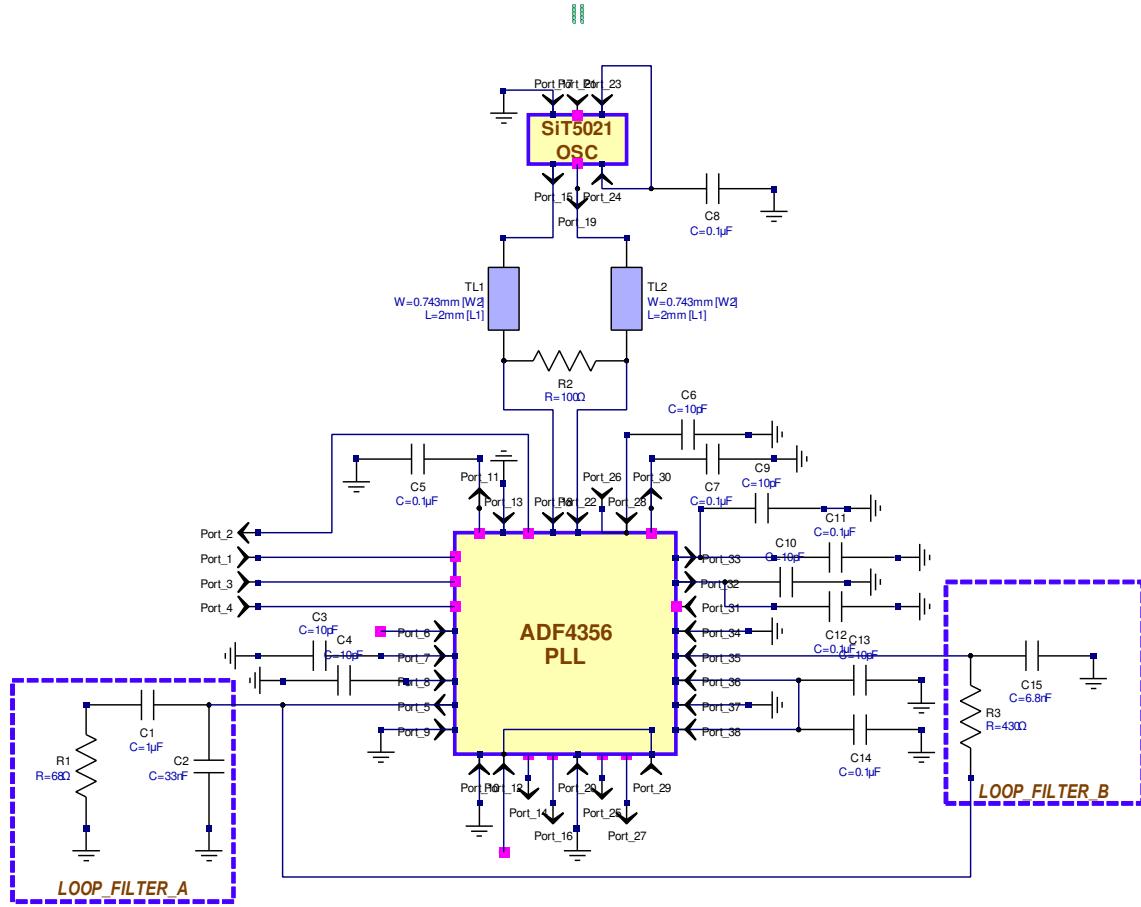
**Figure 13b. 3.3V Voltage Regulator layout in our design**

We shall use two ADM7150ARDZ-3.3 ICs for the analog and digital 3.3V supply and one ADM7150ARDZ-5.0 for 5V supply. As recommended by the manufacturer, separate power supplies are used for analog and digital circuits.

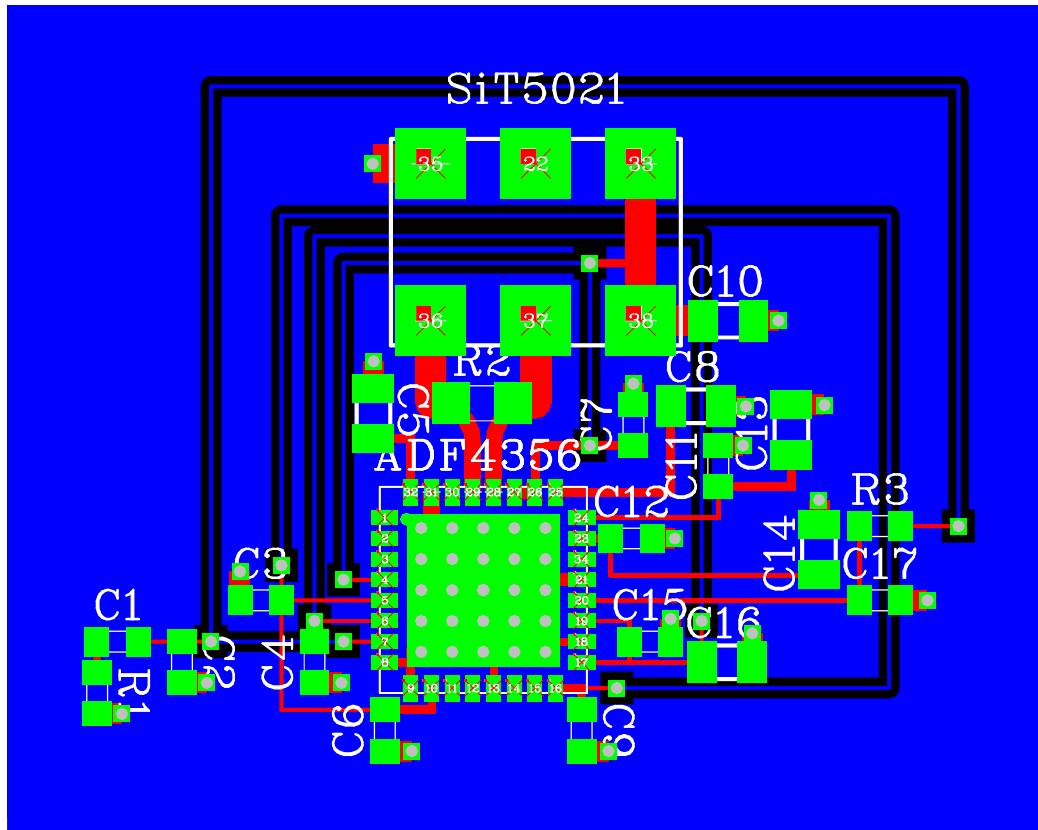
As recommended by the manufacturer, we have selected chip **ceramic capacitors**. The voltage rates of those capacitors have been selected as high as 50V for input and output capacitors, and 25V otherwise.

## 2.6.The PLL Schematic and Layout Design

The following figure shows the schematic design of the PLL frequency synthesizer.



**Figure 14a. Schematic design of the PLL Frequency Synthesizer**



**Figure 14b. Layout design of the PLL frequency synthesizer**

## 2.7. Updating the PLL Schematic and Layout Design

According to the project owner's feedback, the following updates have been done:

- All ENABLE inputs of different integrated circuits have been separated from the DC supply and connected to different pins of a special connector to be under MCU control.
- Some bypass capacitance values have been changed from the datasheet values to the project owner's specified values.

The updated PLL schematic design drawing is shown on the following figure. Some recommended part numbers are given on the schematic drawing.

The next figure shows the updated PLL layout design drawing, complete with the power supplies and the MCU interface connector.

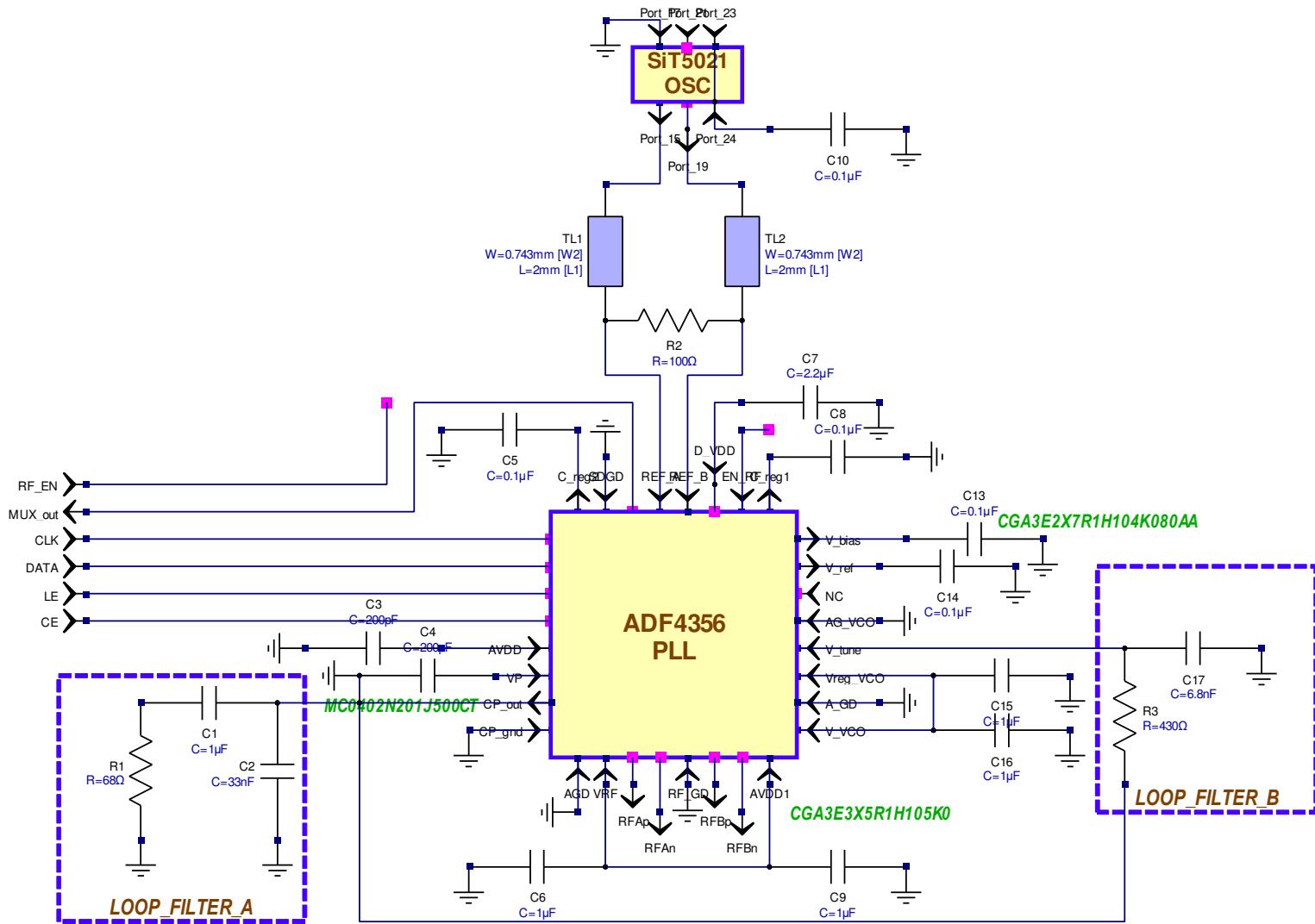
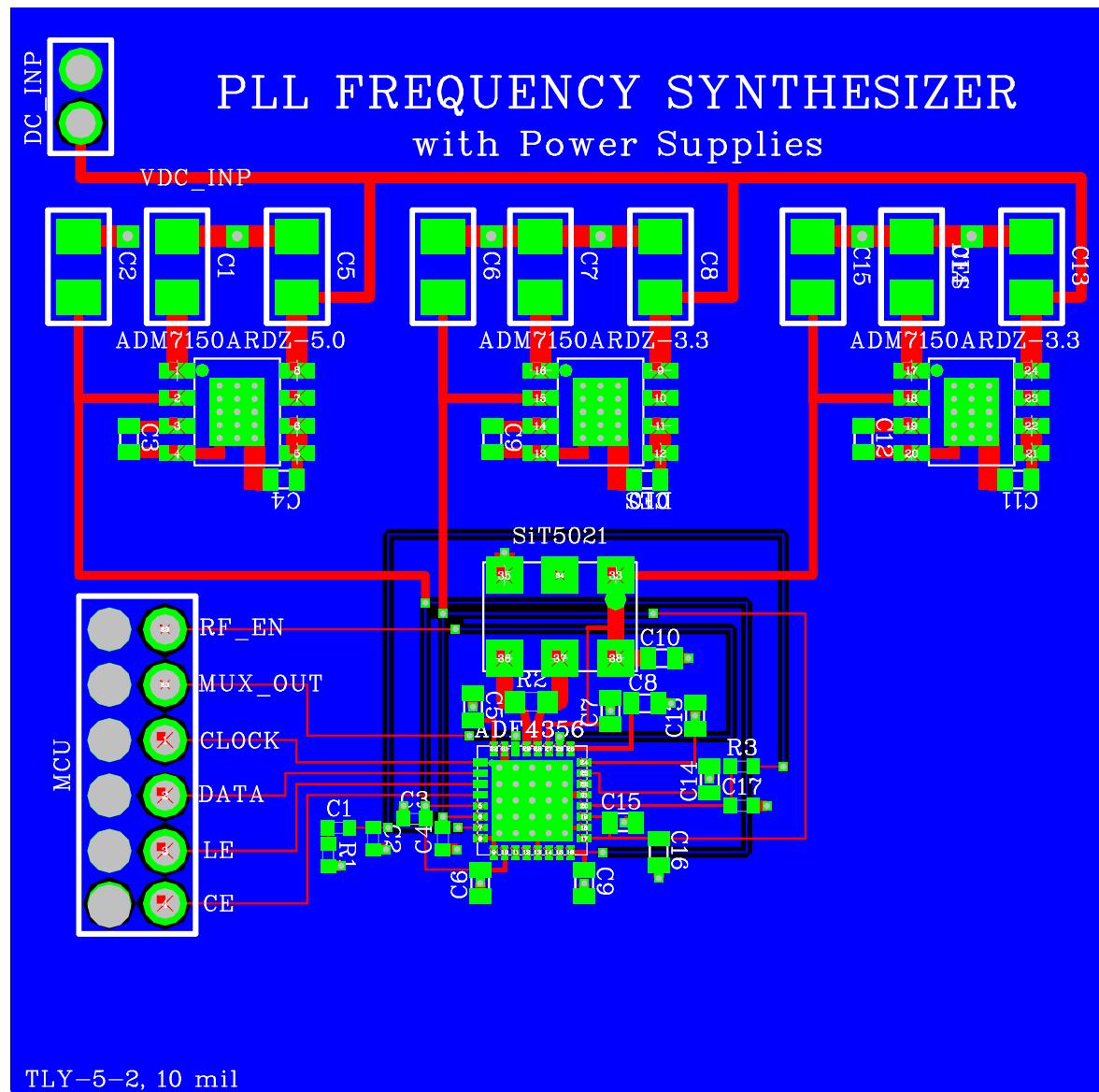


Figure 15. Updated PLL Schematic with the required MCU control inputs



**Figure 16. The PLL Synthesizer Layout with power supplies and MCU controls**

### 3. RF TRANSMITTER

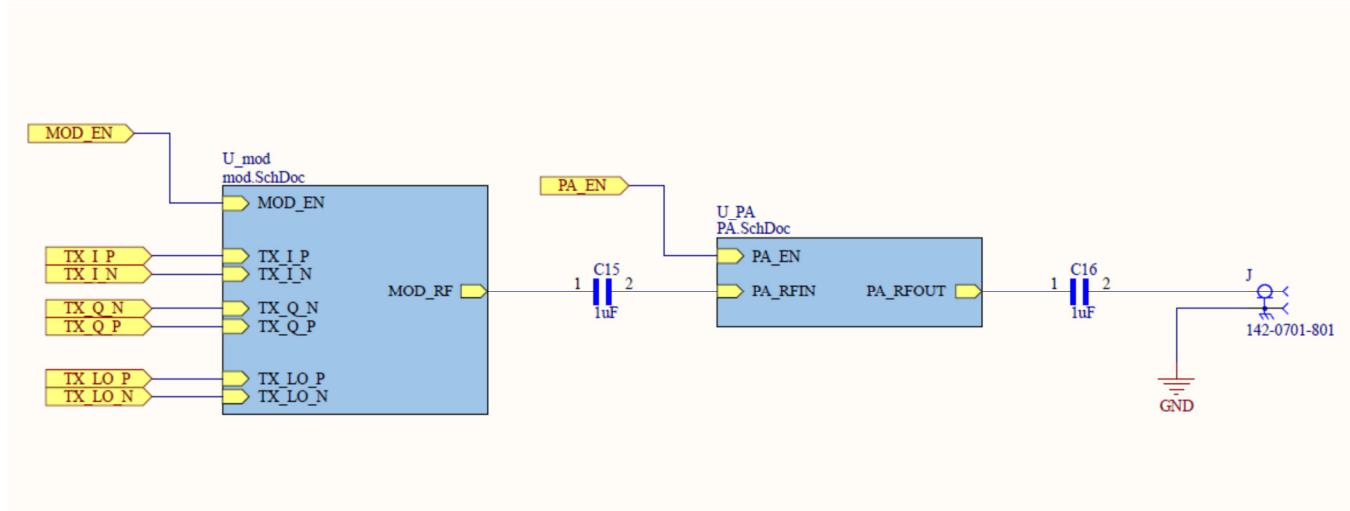


Figure 17. The RF Transmitter

The RF transmitter consists of:

1. The **ADL5375-15ACPZ-R7** Broadband Quadrature (I/Q) Modulator.
2. The **RFPA5542** three-stage power amplifier (PA) designed for 802.11a/n/ac applications.

In the following sections, design details of the two main trasnmitter stages are discussed.

#### 3.1. The I/Q MODULATOR

The project owner selected the ADL5375-15ACPZ-R7 Broadband Quadrature (I/Q) Modulator. The following figure shows some information about this modulator.

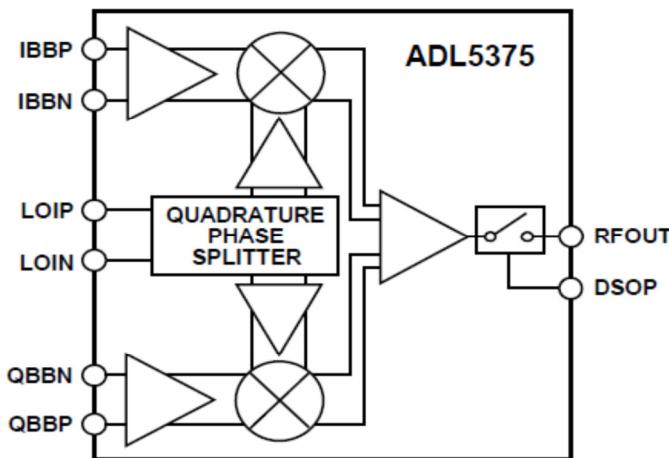


Figure 18a. Quadrature Modulator Functional Diagram

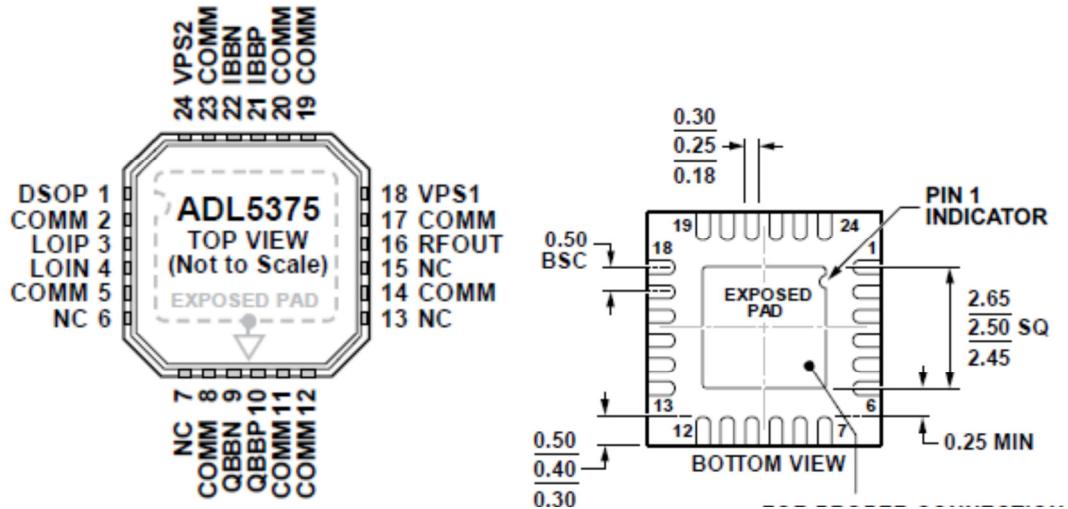


Figure 18b. The ADL5375-15ACPZ-R7 I/Q Modulator

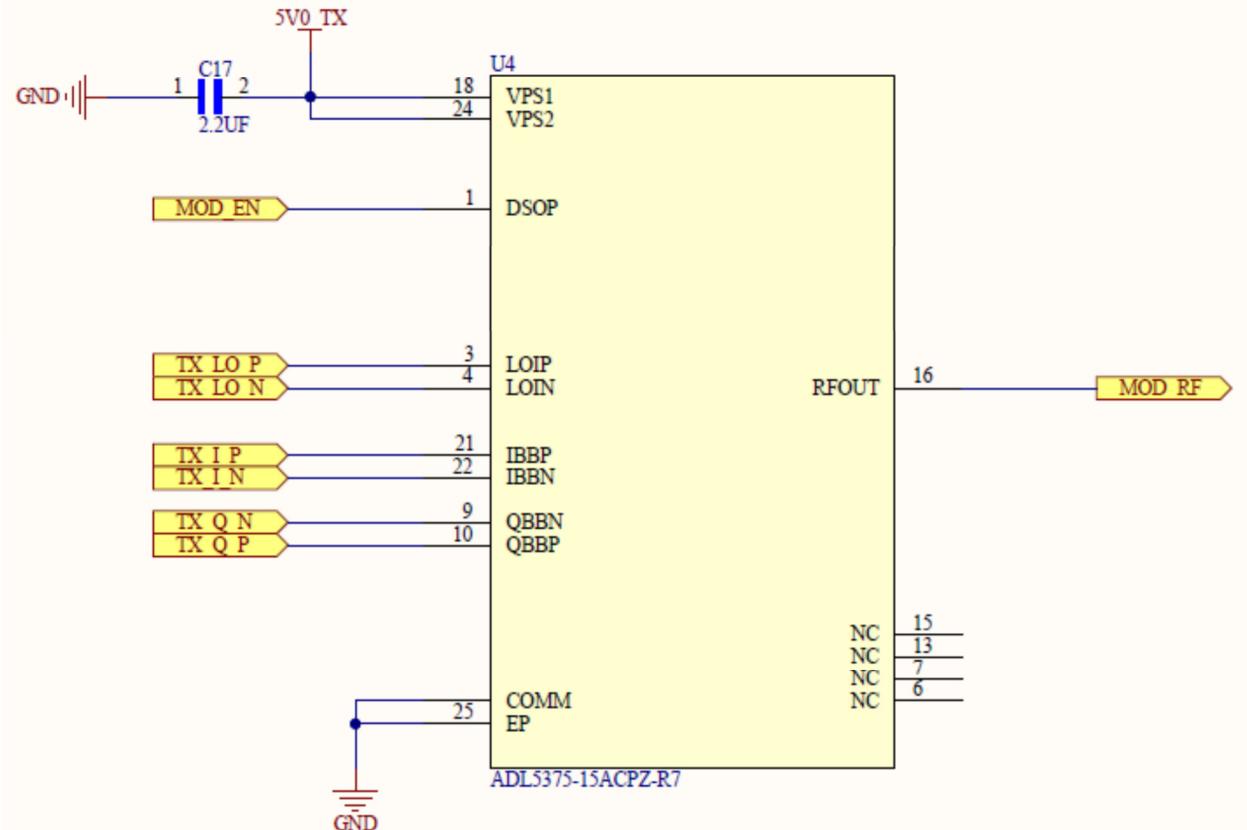
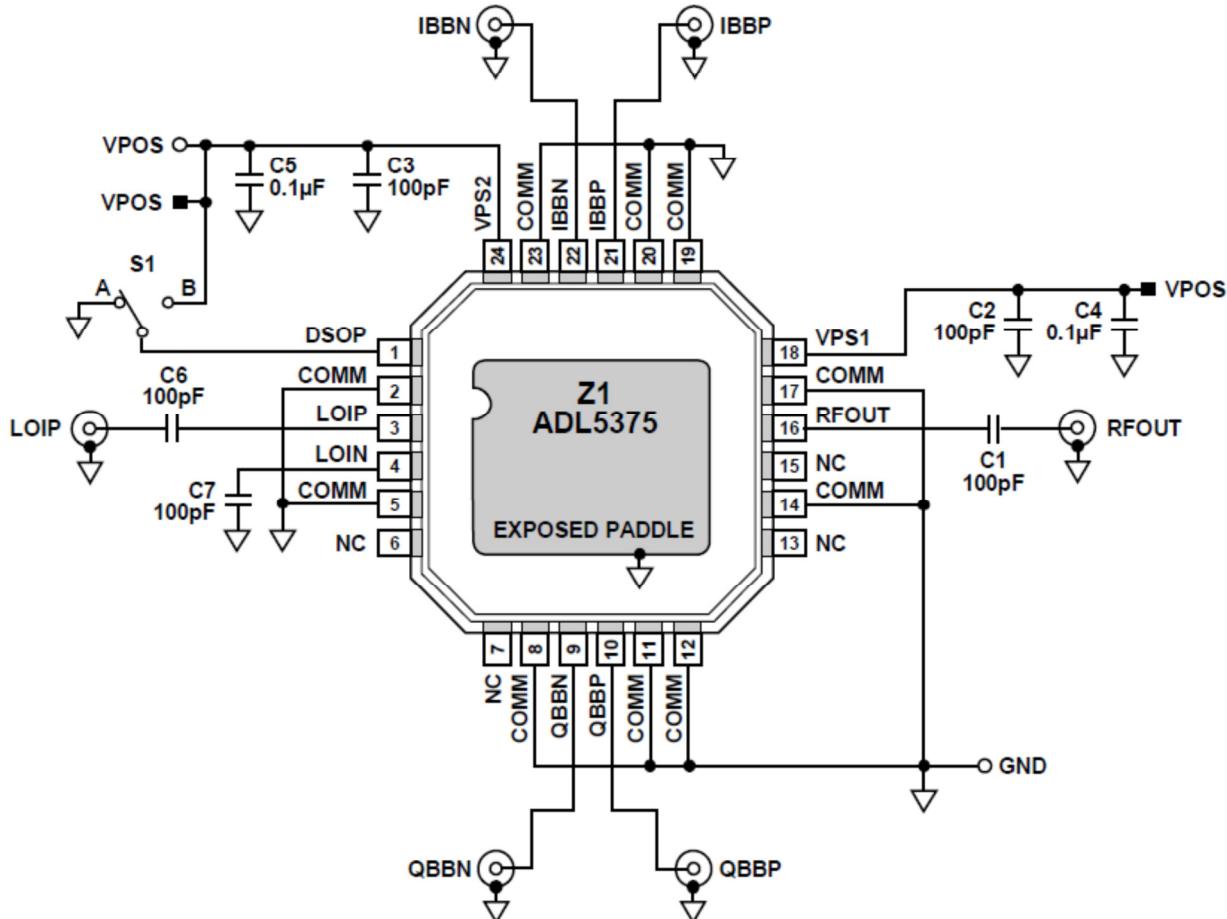


Figure 19. The schematic design drawing of the I/Q Modulator

The last figure shows the schematic design drawing of the I/Q Modulator in our project. The next figure shows the main connections as recommended by the device manufacturer.



**Figure 20. Manufacturer recommended connections of the ADL5375**

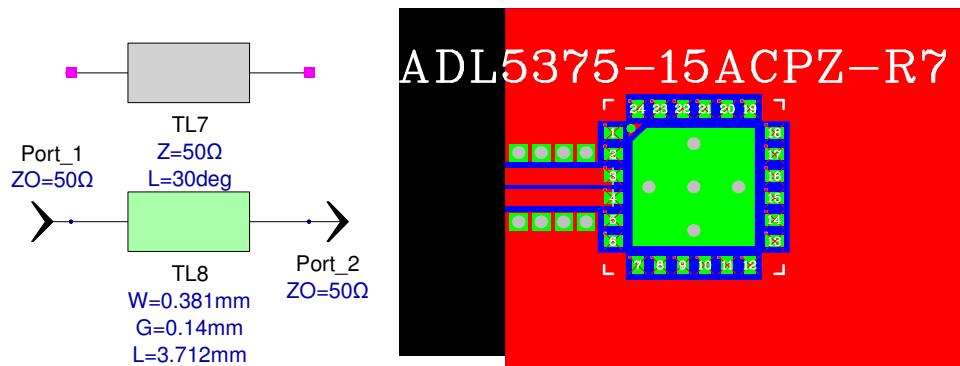
- It gets the balanced LO input from one of the two two differential outputs of the PLL Synthesizer. Two 1 [ $\mu\text{F}$ ] capacitors are used as coupling capacitors between the PLL and the modulator. We shall use the owner-recommended differential coupling scheme, not that single-ended one shown in the above manufacturer's example.
- The other differential output of the PLL Synthesizer goes to the I/Q Demodulator of the Receiver.
- The two paths must be well isolated from each other. Specila [recautions shpuld be done to guarantee that. A special CST electromagnetic simulation will be done to evaluate this isolation.
- Two baseband differentaial inputs will be connected via pin connectors to the MCU I and Q modulation signals to be transmitted.
- The single ended (unbalanced) 50 [ $\Omega$ ] output of the modulator will be given to the RF power amplifier via a shprt 50 [ $\Omega$ ] microstrip TL, as recommended by the project owner.
- The ADL5375-15ACPZ-R7 needs a +5V DC power supply. The typical current is 203 mA.
- Pin 18 (VPS1) and Pin 24 (VPS2) should be connected to the same 5 V source. Each pin should be decoupled with a 100 pF capacitor and a 0.1  $\mu\text{F}$  capacitor. These capacitors

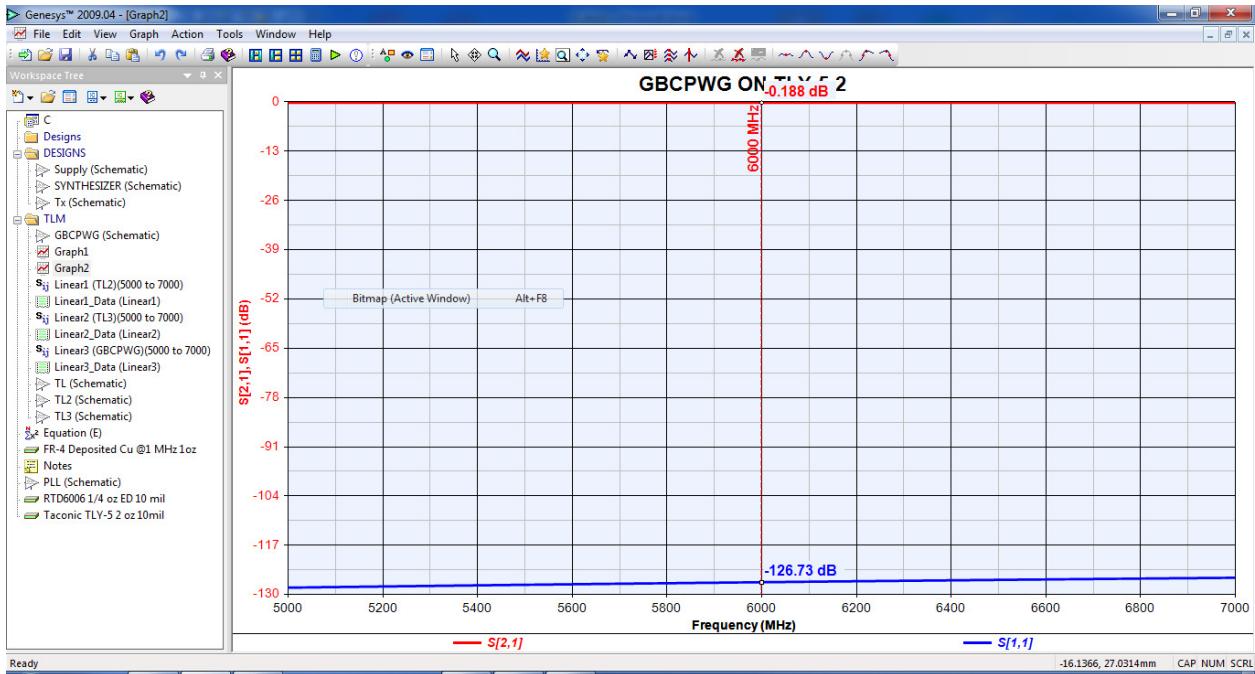
should be located as close as possible to the device. The power supply can range between 4.75 V and 5.25 V.

- The project owner uses a single 2.2 [mF] capacitor to bypass the two supply pins to ground, instead of the four capacitors recommended by the manufacturer.
- We shall adhere to the manufacturer datasheet recommendations regarding the decoupling capacitors.
- The two supply pins will be connected to the main +5V power supply. As the total 5V load was 99 mA, it will become  $99 + 203 = 302$  mA. The 5V power supply still supports up to 800 mA maximum load. The remaining supply current for the power amplifier is 498 mA.

### 3.1.1.The Input Transmissioin lines

Since the distance between the two input pins is only 0.5 mm, it is a very good solution to use two GBCPWG transmission lines with 0.14 mm gap and 0.381mm width each. Such a transmission line is very well matched as seen in the frequency response.



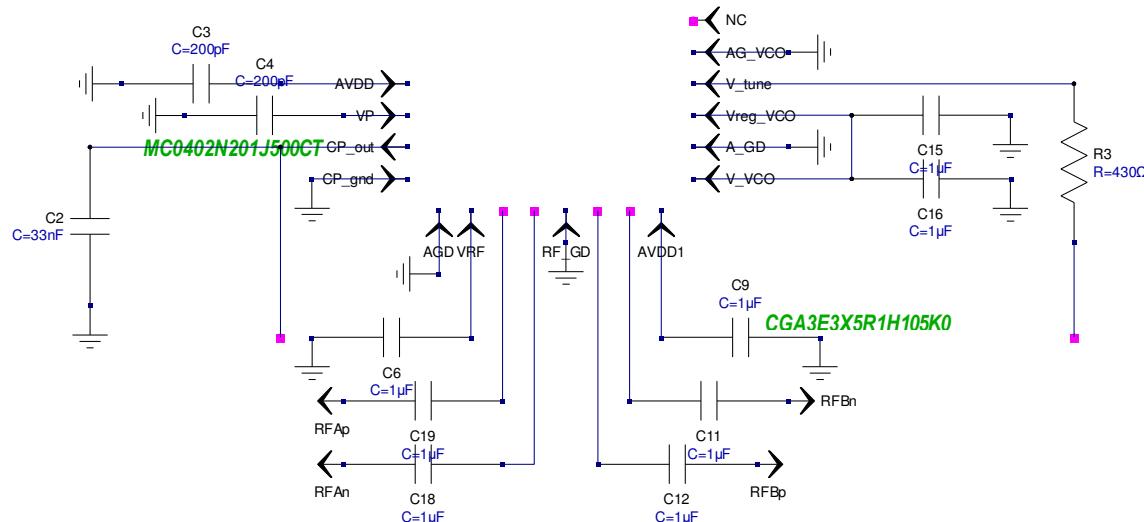


**Figure 21.** GBCPWG transmission line with 0.14mm gap on Taconic TLY-5 2 oz 10mil

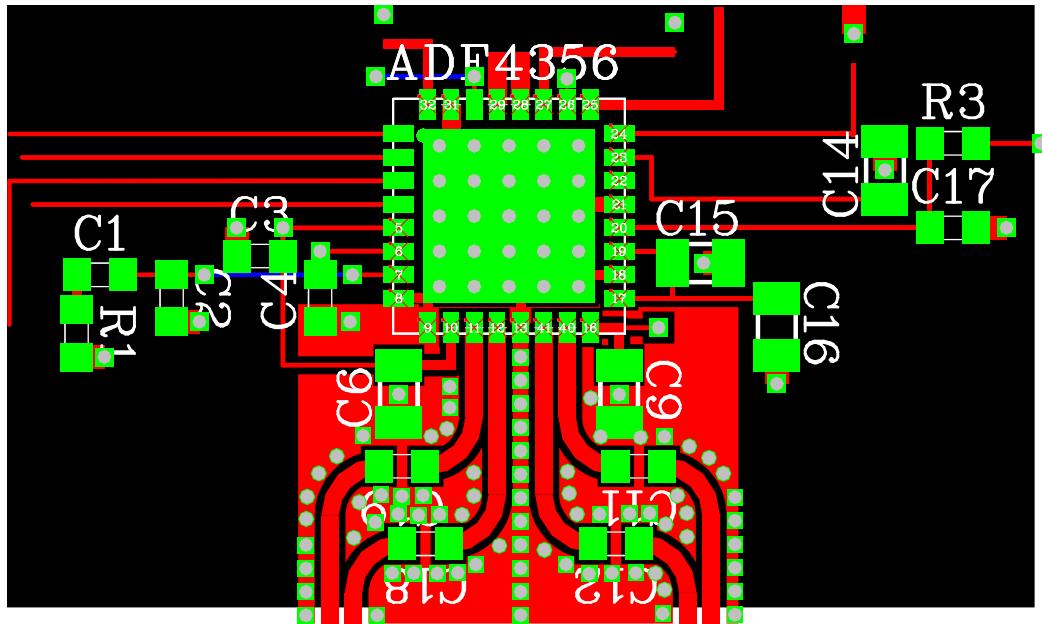
### 3.1.2.Coupling caoacitors from PLL to Modulator

Two 1 [mF] capacitors are recommended between the differential PLL output and the differential LO input of the I/Q modulator.

The following figure shows the proposed schematic drawing design of the two coupling capacitors



**Figure 22a.** Proposed schematic of PLL-Modulator coupling



**Figure 22b. Proposed layout design drawing of PLL-Modulator coupling**

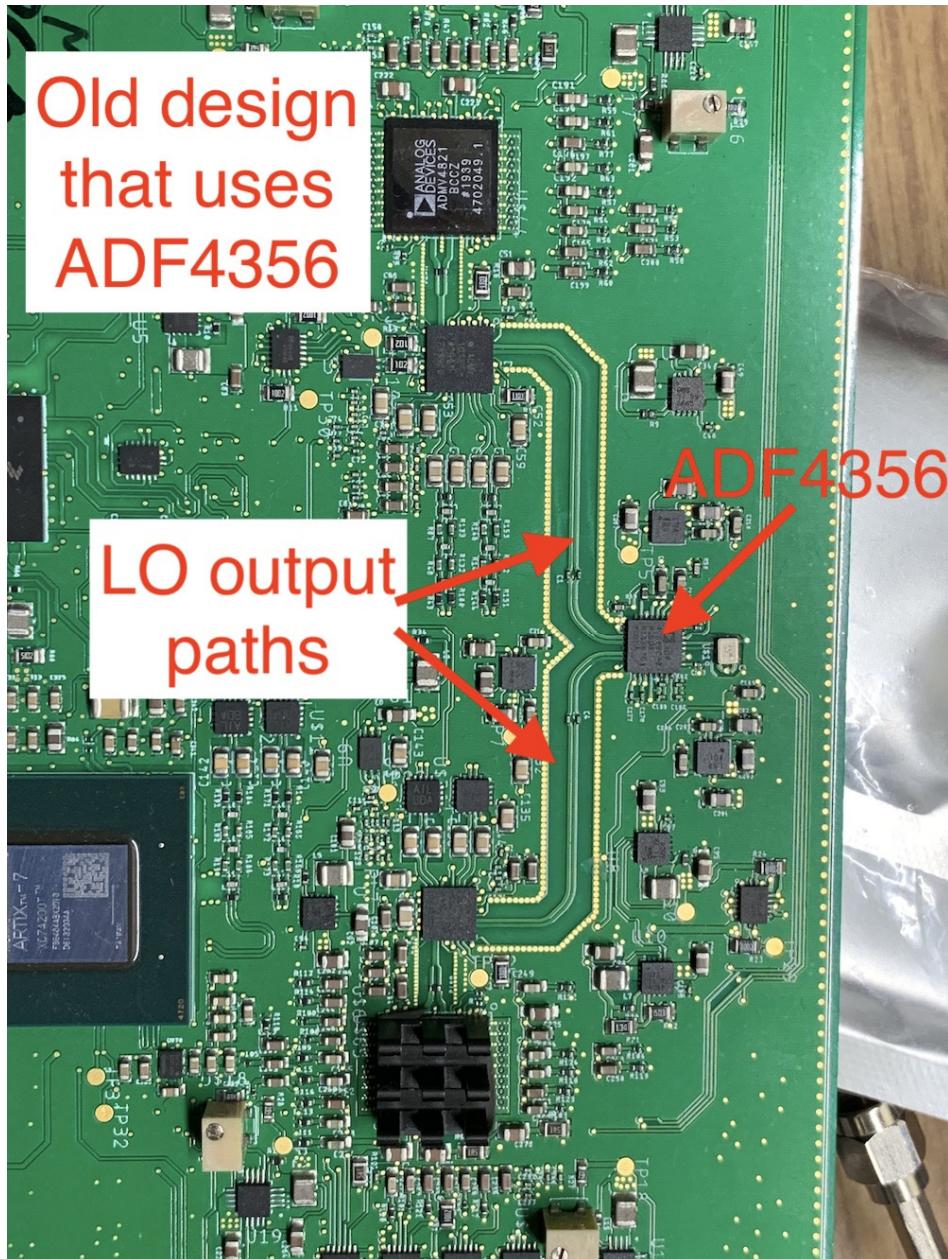
- We have used the following:
  - 0.381mm wide GBCPWG transmission lines with 0.14mm gaps
  - CGA3E3X5R1H105K080AB capacitors with 1 [ $\mu$ F] value, 10V maximum voltage and C0402 package.
  - 90° circular transitions of the GBCPWG transmission lines.
  - Viaholes with 0.3mm dril, 0.35mm circular and rectangular pads and 0.5mm maximum separation to connect the TOP and BOTTM ground planes. Please note that the guided wavelength at 6 GHz is 36.884 mm and the maximum viahole pitch is less than 0.014  $\lambda_g$ .
- The TL separation at the output of the coupling area is exactly 0.5 mm, equal to the pin separation of the modulator.
- In this way we can guarantee a perfect matched coupling between the PLL output and the Modulator LO input with the recommended 1 [ $\mu$ F] coupling capacitors.
- The same coupling mechanism has been repeated for the Receiver Demodulator LO input as seen in the above figure.
- This design lays the transmitter and the eceiver at the same ditection from the PLL.

### 3.1.3.Another Tx-Rx Layout Design

In this layout design, the Tx and the Rx are laid and fed in a line perpendicular to the PLL RF output TL.

This layout may be useful for more Tx-Rx isolation. It is similar to the old layout design of the project owner, shown in the following two figures.

In these two figures, it can be seen that the LO output was a single ended transmission line, while that of the new design is a balanced differential transmission line.



**Figure 23a. The old layout design**

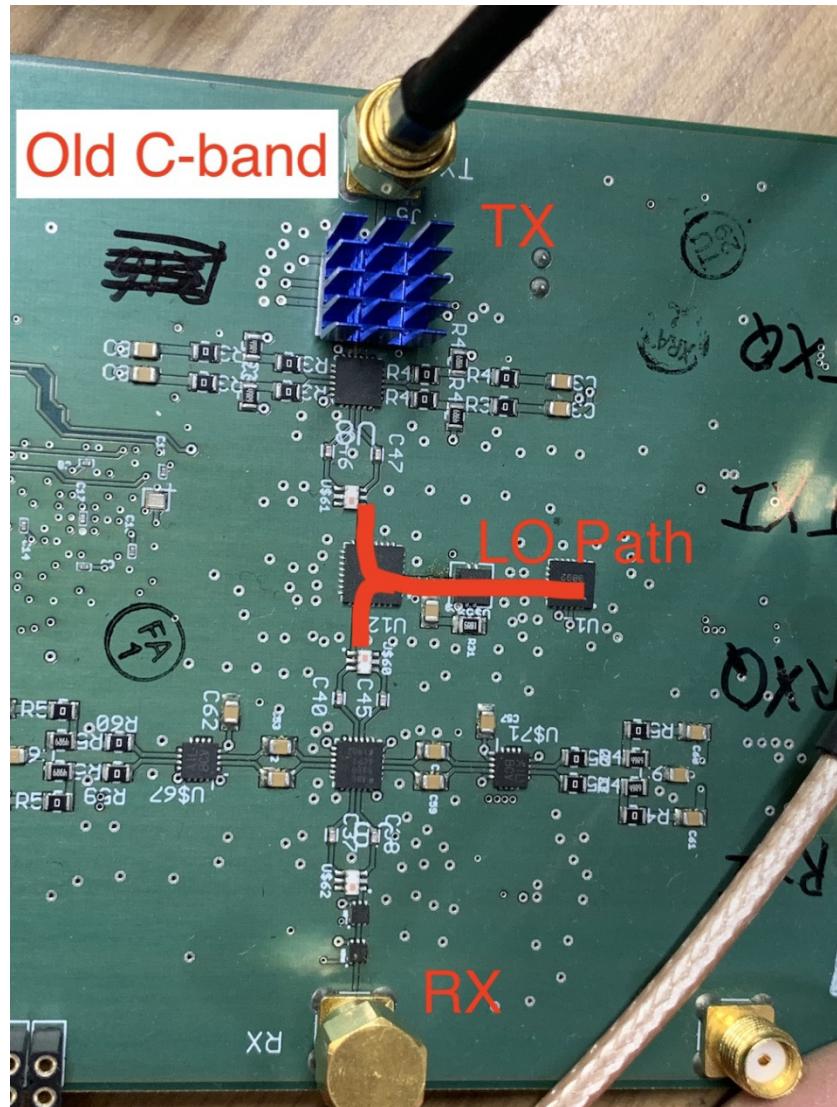


Figure 23b. The old layout design

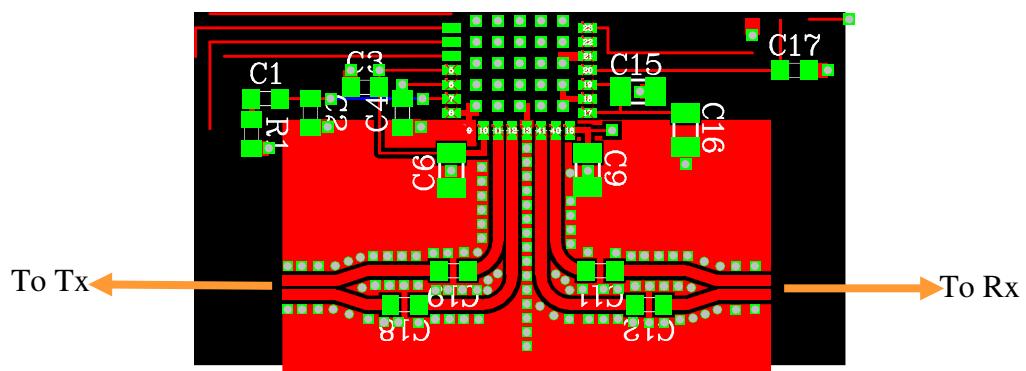


Figure 24. The second layout design drawing of PLL-Modulator coupling

### 3.1.4.Modulator Schematic and Layout Design

The following figure shows the schematic and layout design drawings.

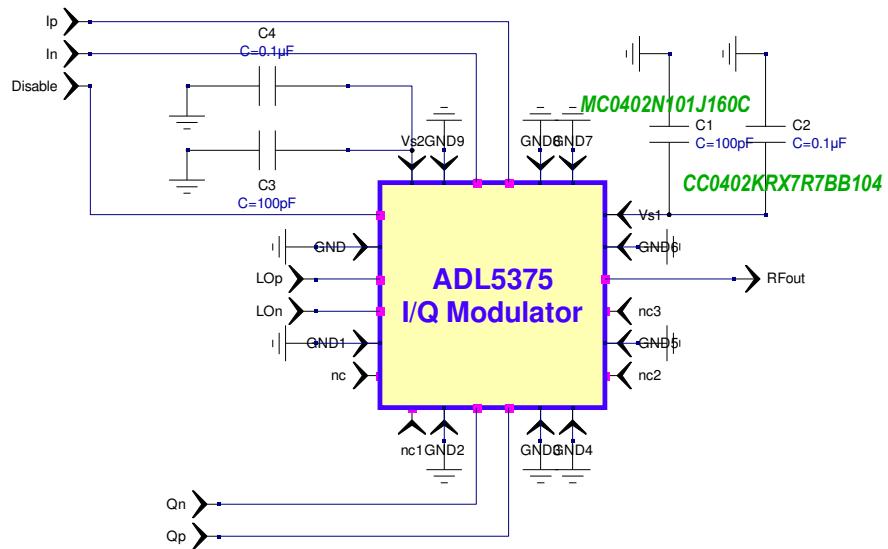


Figure 25a. Quadrature Modulator Schematic Design

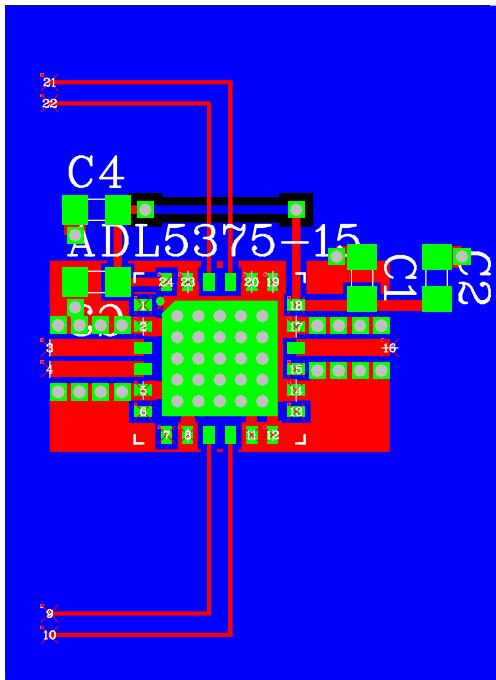


Figure 25b. Quadrature Modulator Layout Design

## 3.2.The POWER AMPLIFIER

### 3.2.1.Power Amplifier Schematic

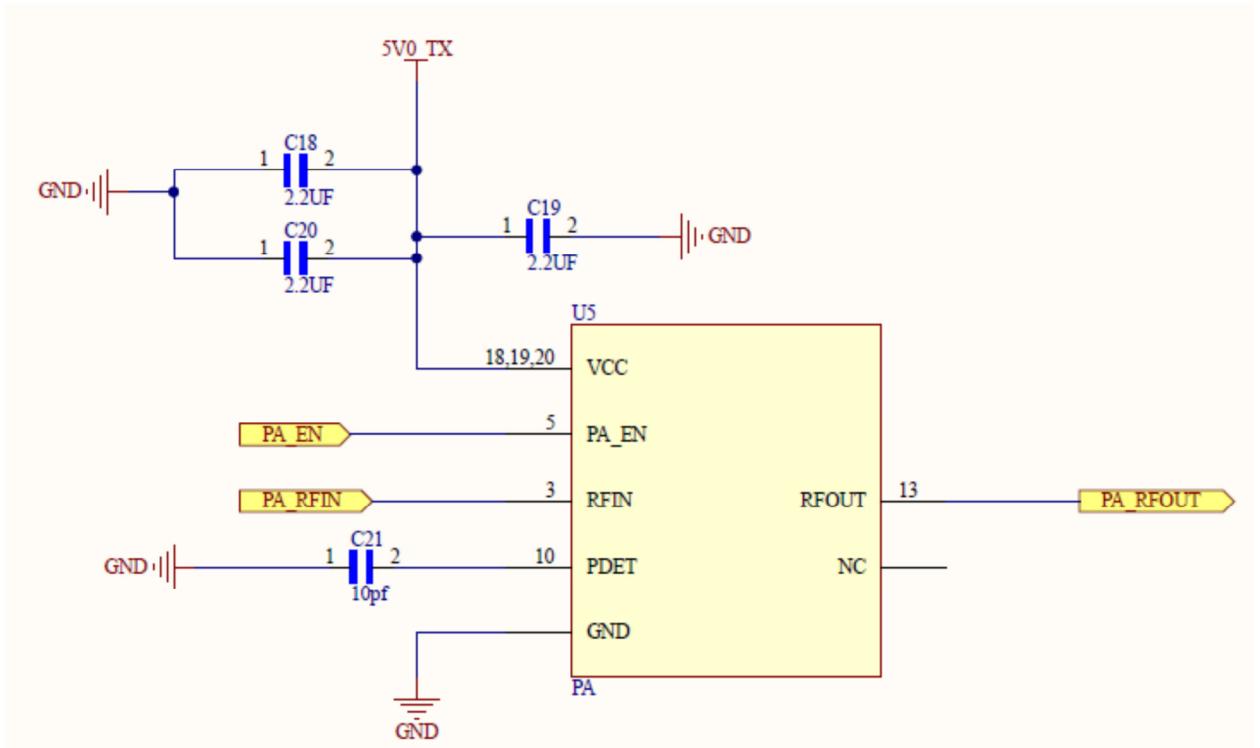
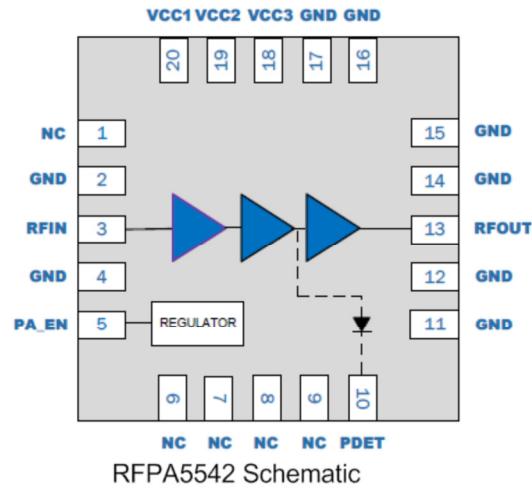


Figure 26. The given Power Amplifier Schematic

### 3.2.2.Power Amplifier IC

The project owner selected the RFPA554 three-stage power amplifier (PA) designed for 802.11a/n/ac applications. The PA is optimized to minimize the required external components to maintain linear performance.



RFPA5542 Schematic

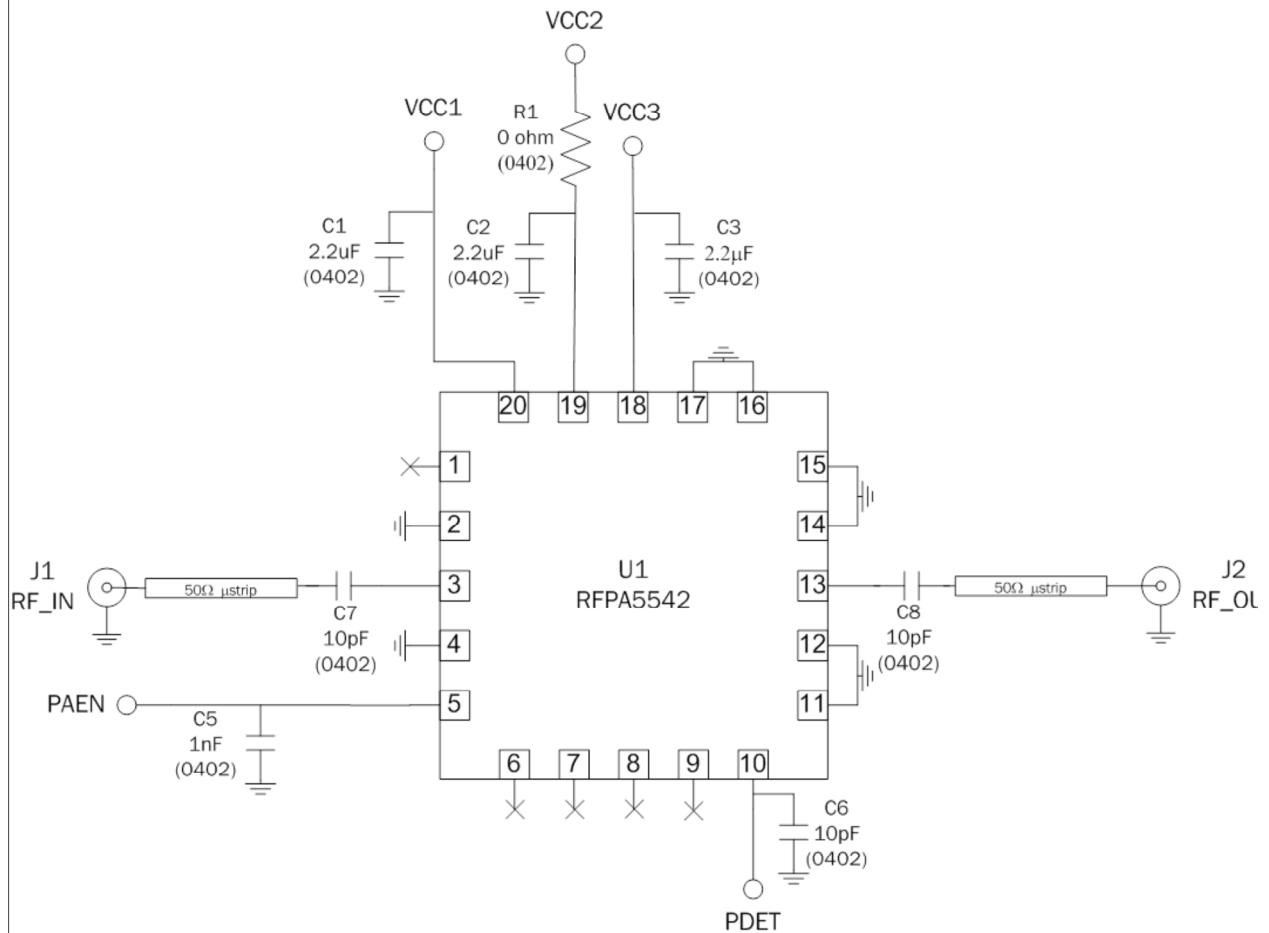
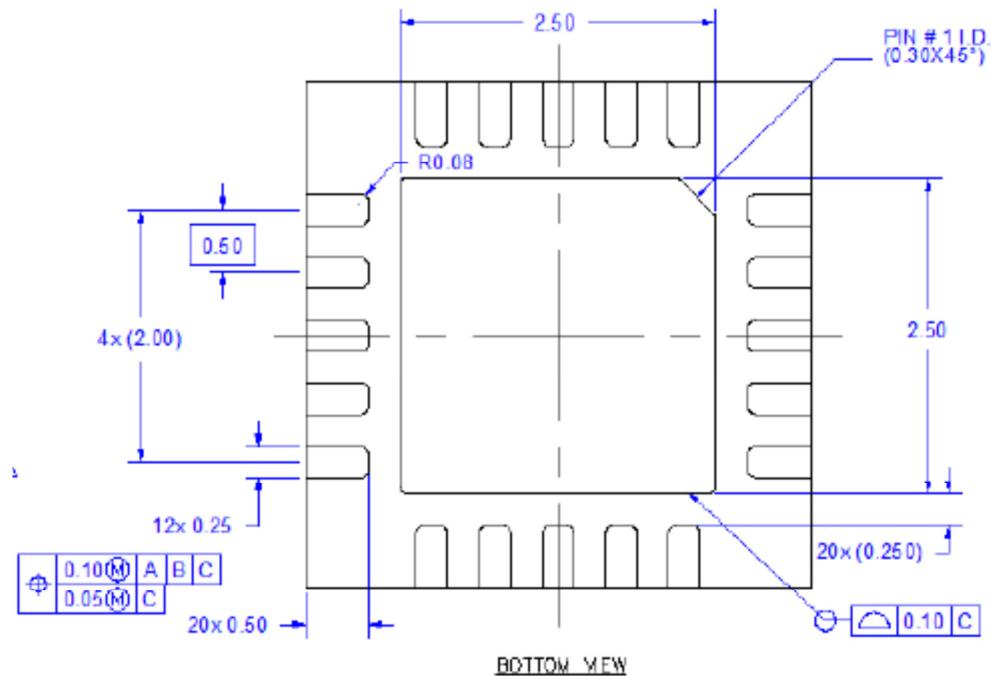
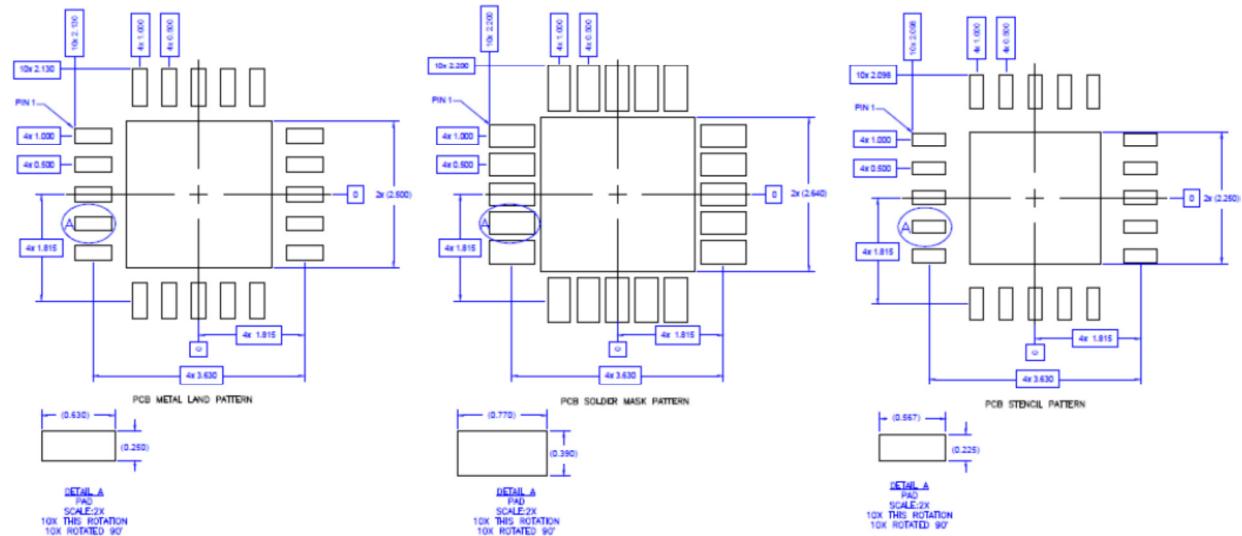


Figure 27. The RFPA554 Power Amplifier circuit



**Figure 28a. The RFPA5542 Power Amplifier**



**Figure 28b. The RFPA5542 Power Amplifier layout footprint**

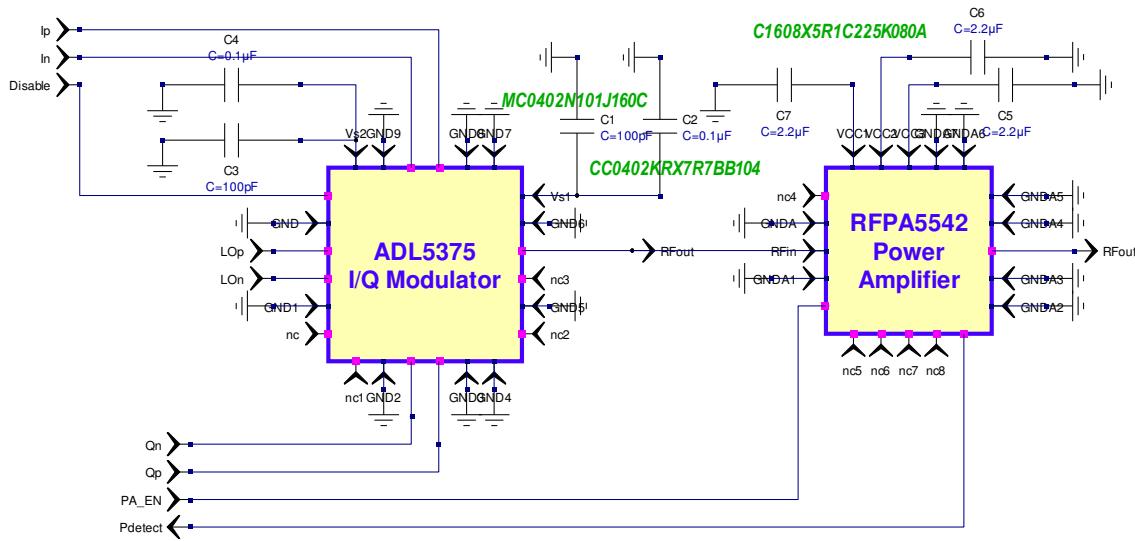
### 3.2.3.Power Supply Requirements

This power amplifier needs a +5V supply with maximum current of 430 mA (at maximum output power of +27 dBm).

The remaining power supply current (498 mA) can support that maximum current.

### 3.2.4.Power Amplifier Schematic Drawing

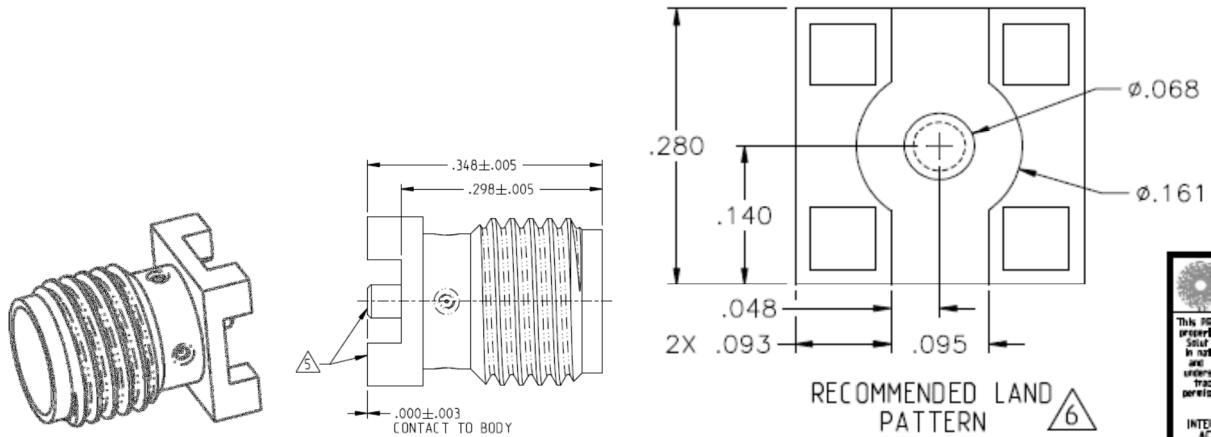
The following figure shows the schematic design drawing of the transmitter, including the power amplifier. The part numbers of some capacitors are shown on the schematic.



**Figure 29. The RF Transmitter Schematic**

### 3.2.5.The Output RF Connector

I have selected the JOHNSON - CINCH CONNECTIVITY [142-0711-201](#) surface mount sma jack connector.



**Figure 30. The [142-0711-201](#) surface mount sma jack connector.**

### 3.3.The TRANSMITTER LAYOUT DESIGN

The following figure shows the RF Transmitter layout design.

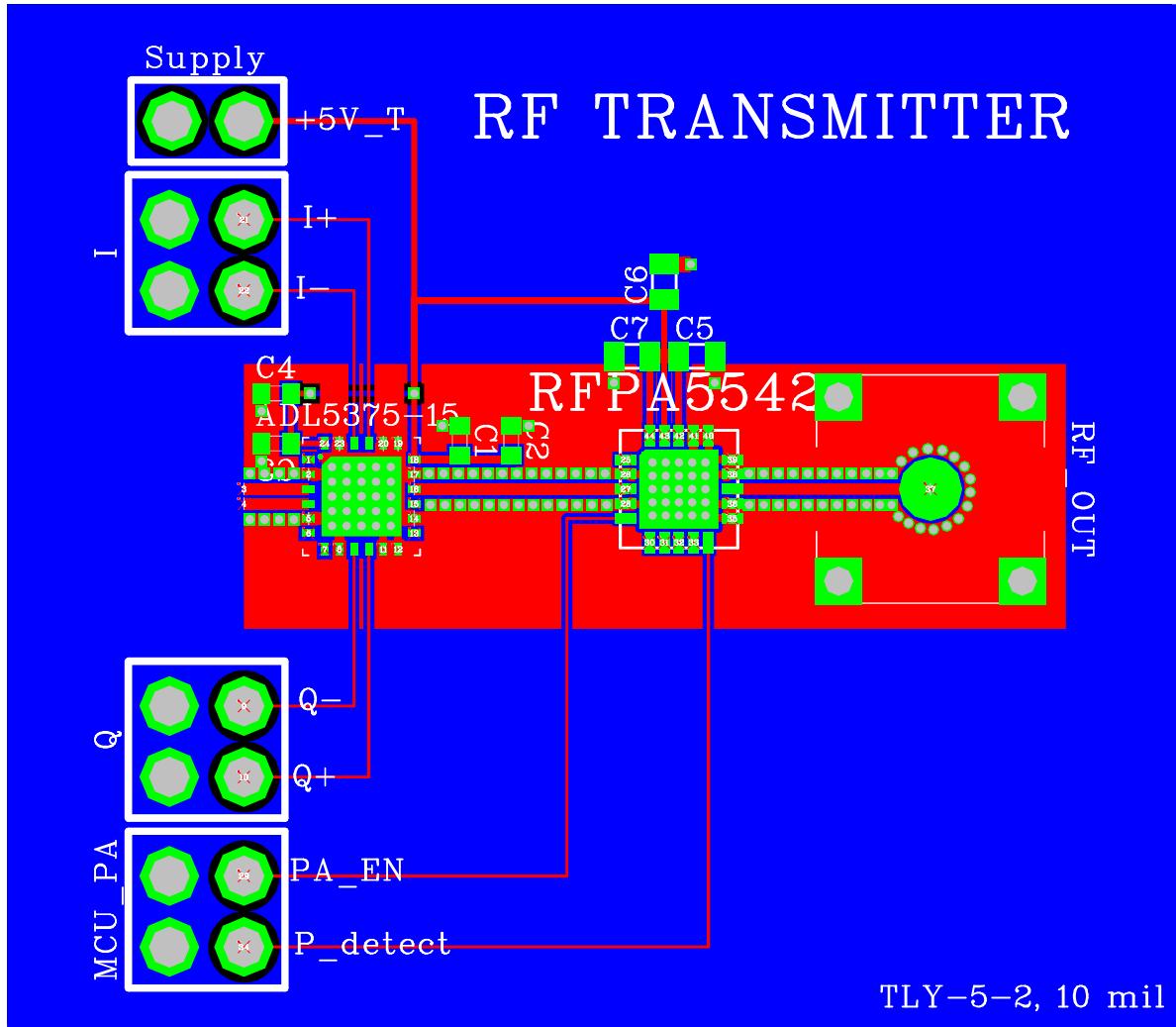
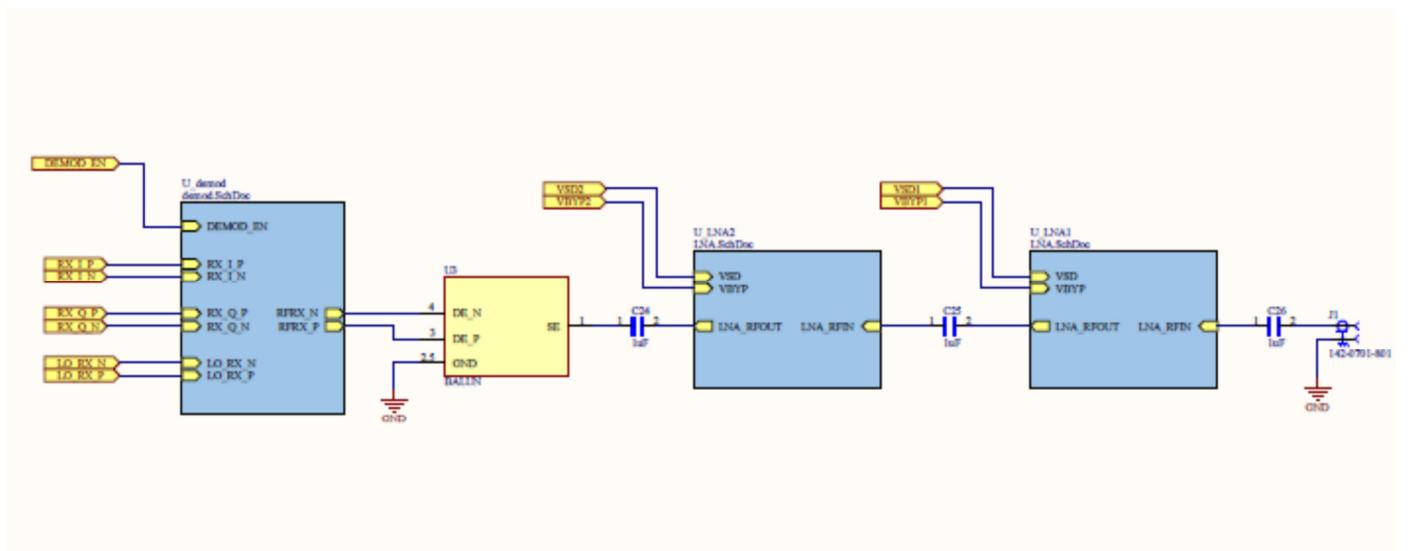


Figure 31. The Transmitter Layout Design

## 4. RF RECEIVER

### 4.1.Given Schematic Design

The given schematic design drawing for the receiver is shown in the following figure.



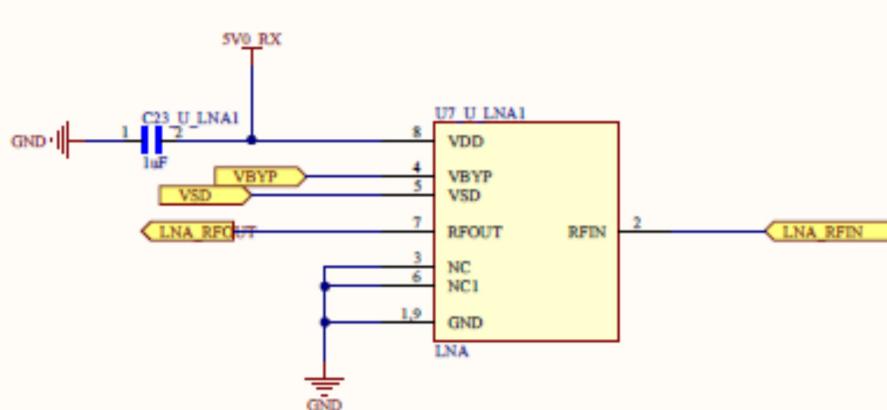
**Figure 32.** The given schematic design drawing for the receiver

The RF receiver consists of:

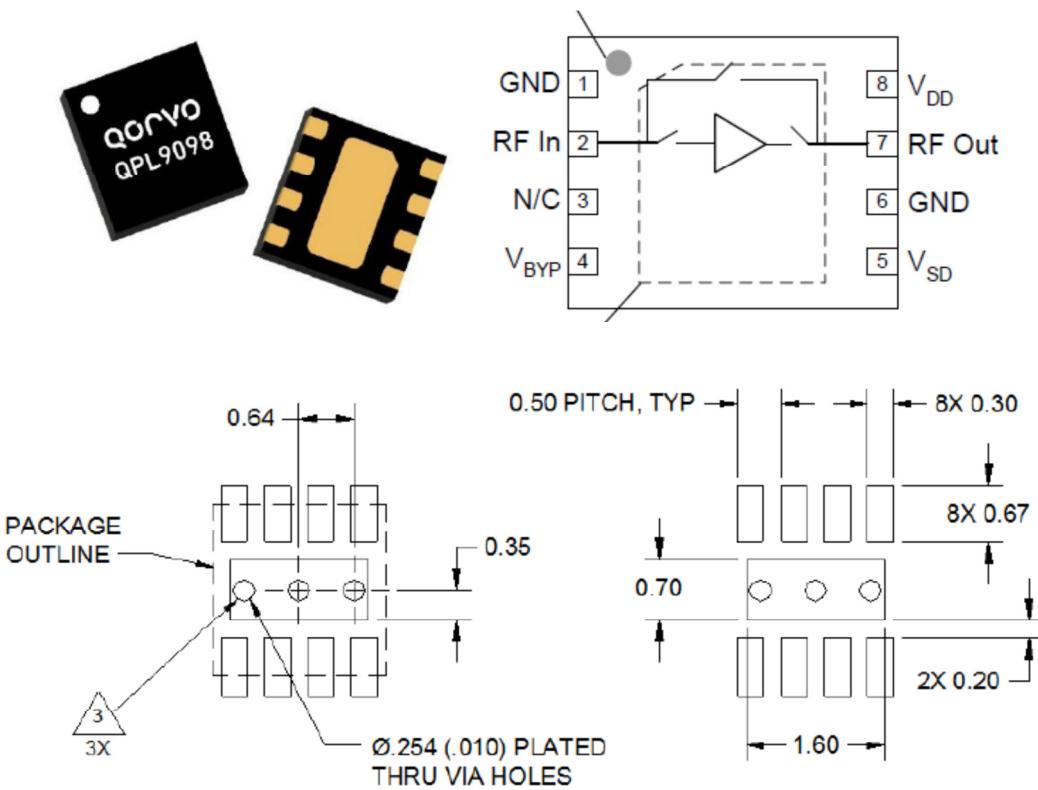
1. Two cascaded stages of the **QPL9098TR7 LNA**
2. A **2450BL15B100E BALUN Transformer**
3. The **ADL5380 Quadrature Demodulator**.

In the following sections, the different receiver stages will be discussed and described.

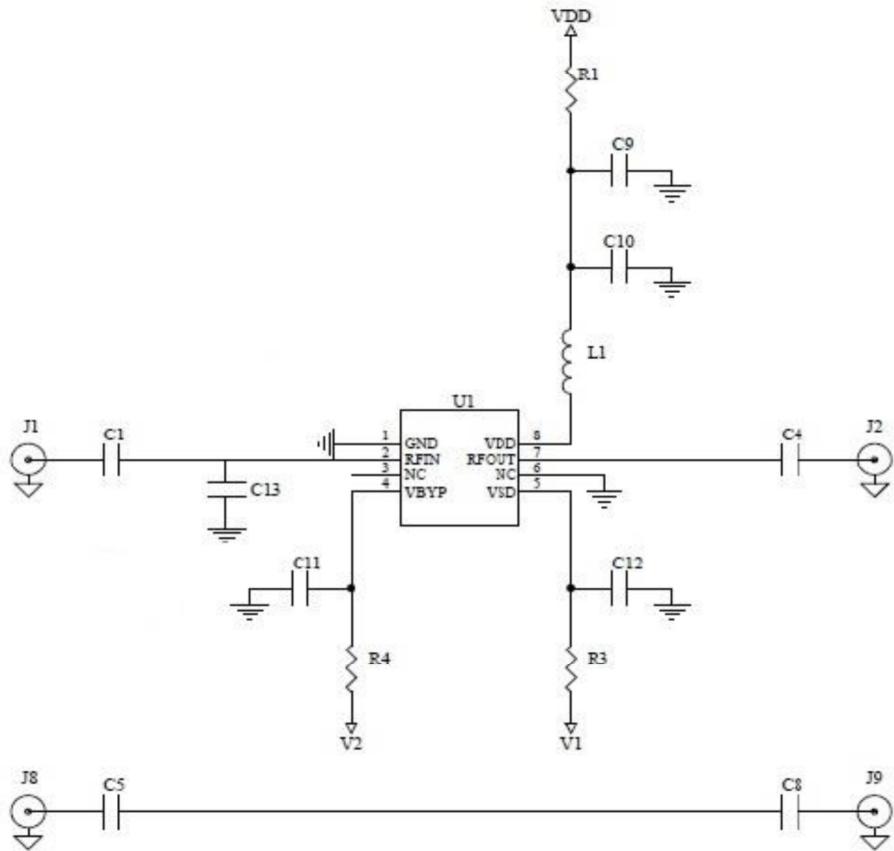
#### 4.2. The QPL9098TR7 LNA



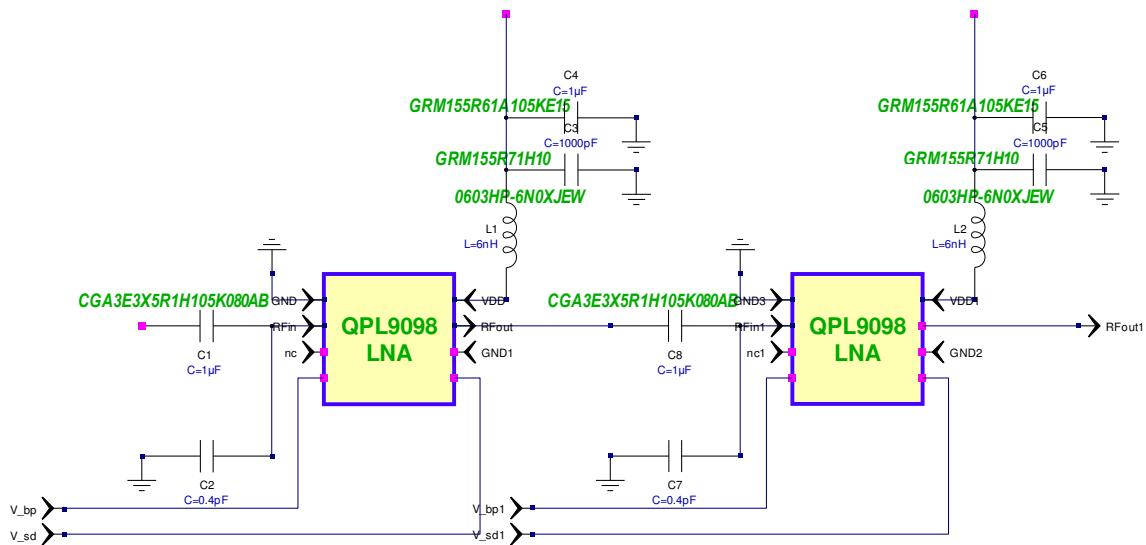
**Figure 33.** The given QPL9098TR7 LNA schematic



**Figure 34a. The QPL9098TR7 LNA**

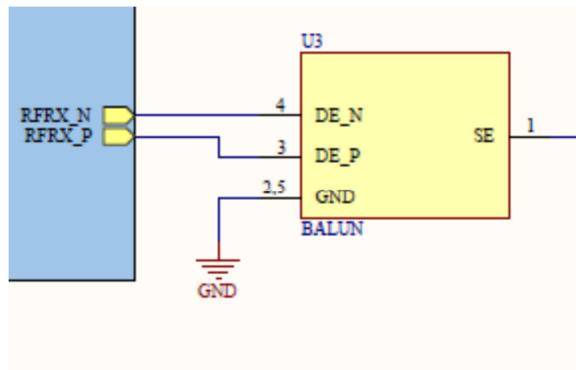


**Figure 34b. QPL9098TR7 Typical circuit**

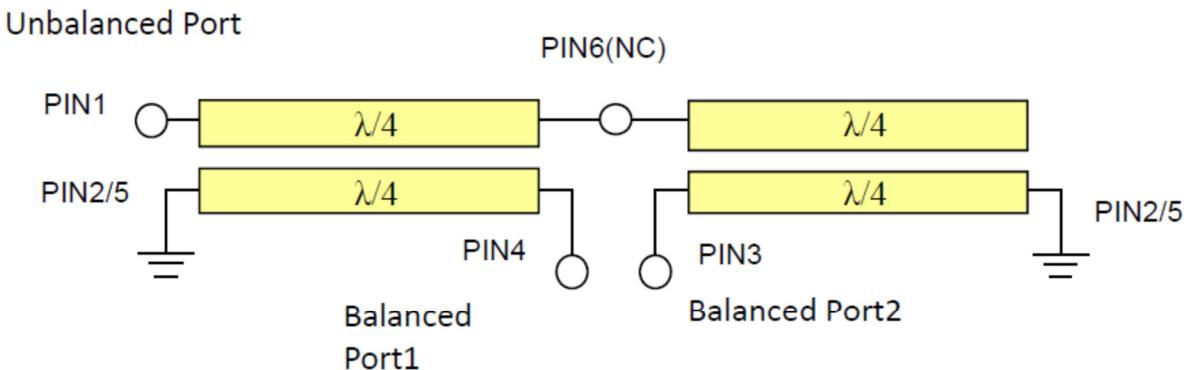


**Figure 35. Two-stage LNA Schematic Design**

#### **4.3.The 2450BL15B100E BALUN Transformer**



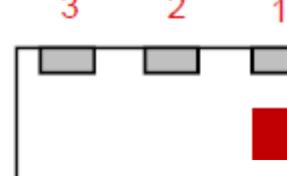
## **Figure 34. 2450BL15B100E BALUN Transformer**



**Figure 35.** BALUN Transformer Principle

Terminal Configuration			
No.	Function	No.	Function
1	Unbalanced Port	4	Balanced Port
2	GND or DC Feed	5	GND
3	Balanced Port	6	NC

3      2      1



**Figure 36a.** 2450BL15B100E pin configuration

	In	mm
L	0.079 ± 0.004	2.00 ± 0.10
W	0.049 ± 0.004	1.25 ± 0.10
T	0.033 ± 0.004	0.85 ± 0.10
a	0.012 ± 0.004	0.30 ± 0.10
b	0.008 ± 0.004	0.20 ± 0.10
c	0.012 +0.004/-0.008	0.30 +0.1/-0.2
g	0.014 ± 0.004	0.35 ± 0.10
p	0.026 ± 0.002	0.65 ± 0.05

Figure 36b. 2450BL15B100E pin configuration

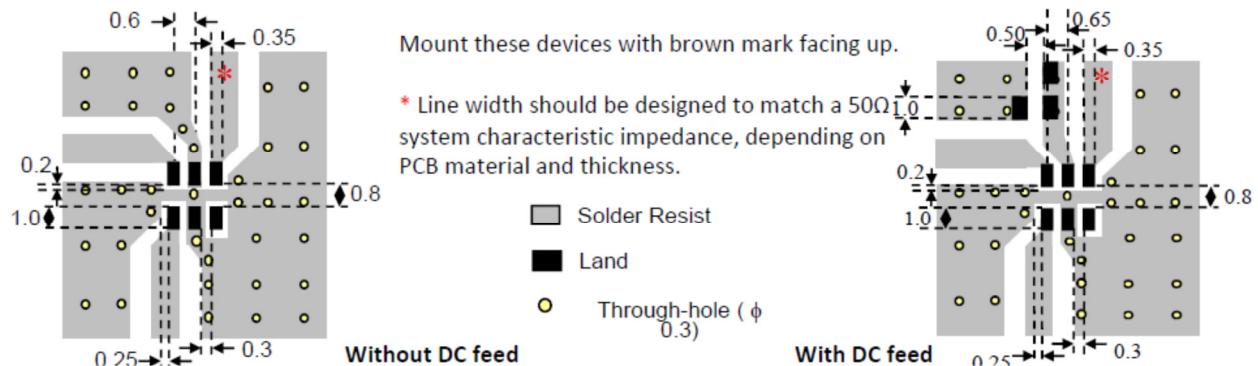


Figure 36b. 2450BL15B100E PCB mounting

Part Number	Frequency (MHz)	Impedance Unbal./Bal.	Insertion Loss (max)	Return Loss (min)	Phase Difference	Amplitude Difference (max)	Case Size (EIA)
2450BL15B100	2400 - 2500	50/100	1.0 dB	9.5 dB	$180^\circ \pm 10^\circ$	2.0 dB	0805

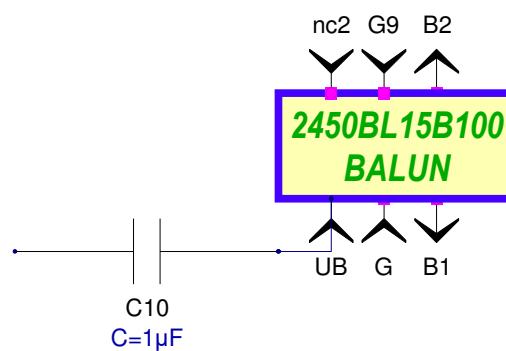


Figure 36c. 2450BL15B100E in our schematic drawing

#### 4.4. The ADL5380 Quadrature Demodulator

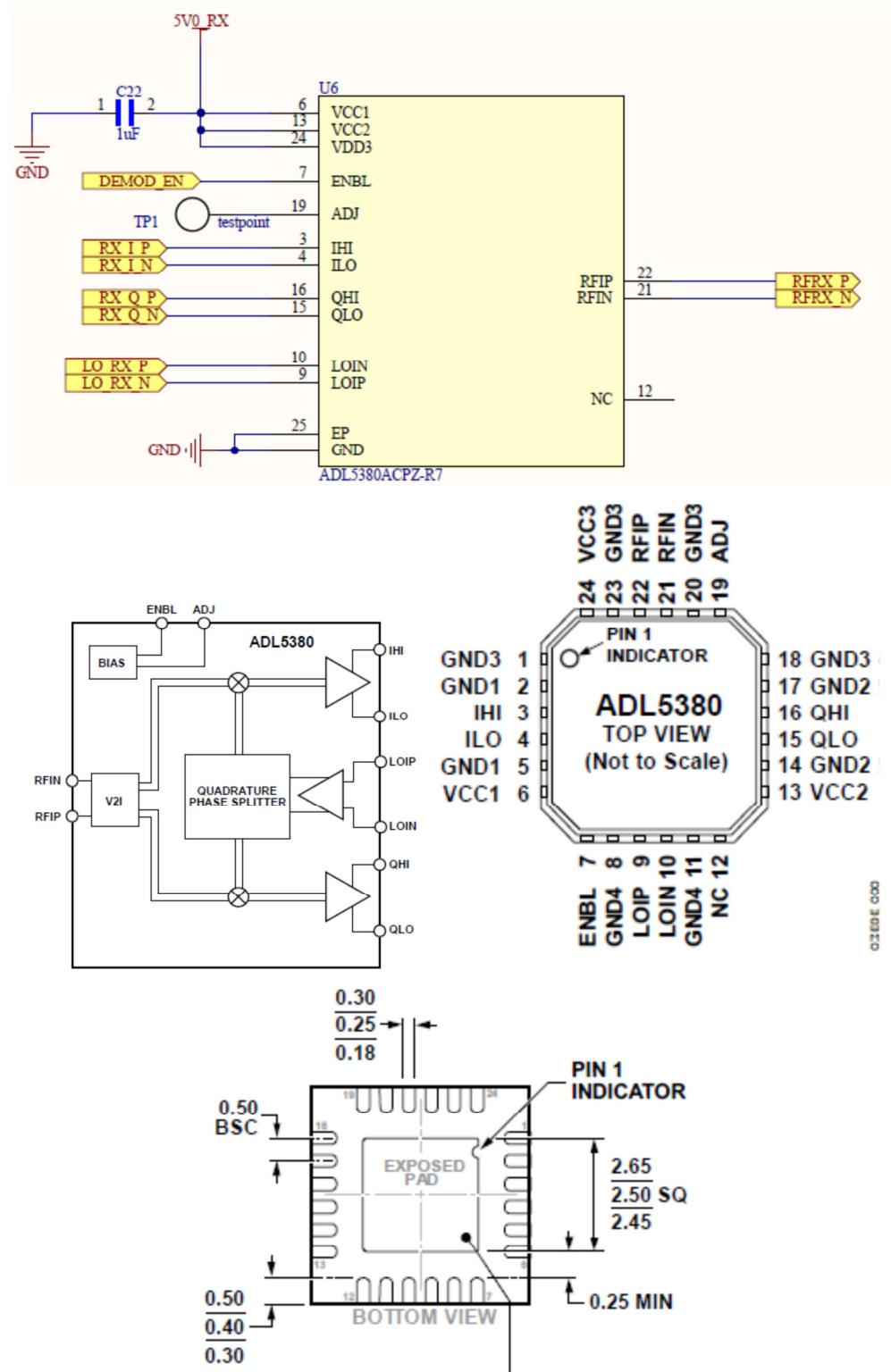
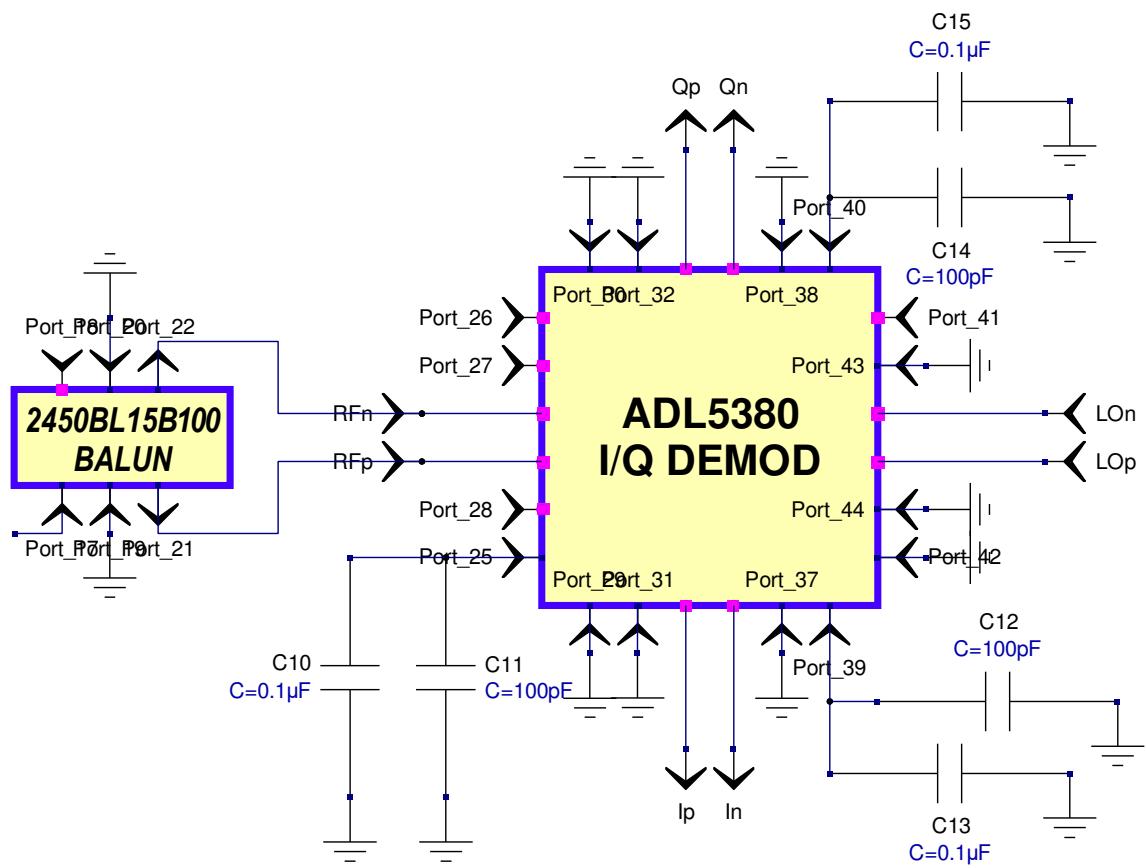


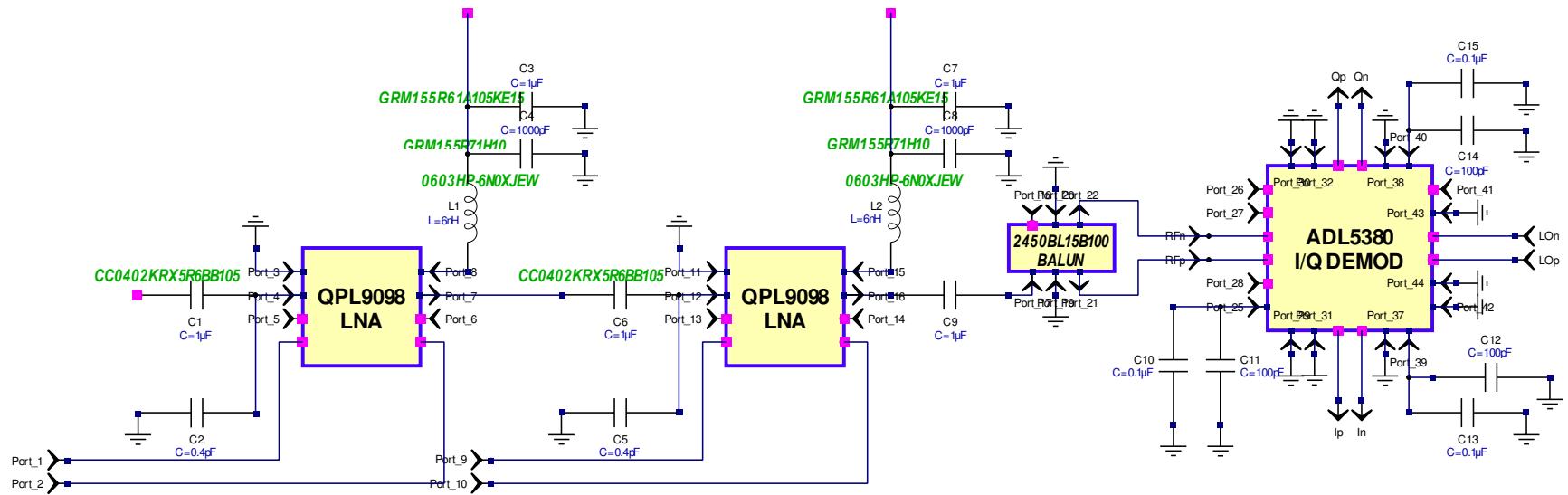
Figure 37. The ADL5380 I/Q Demodulator



**Figure 38. Modulator connections schematic design**

## 4.5. RECEIVER INTEGRATION

The integrated receiver schematic design drawing is shown in the next figure.



**Figure 39. Receiver schematic design**

The integrated receiver layout design drawing is shown in the next figure.

# RF RECEIVER

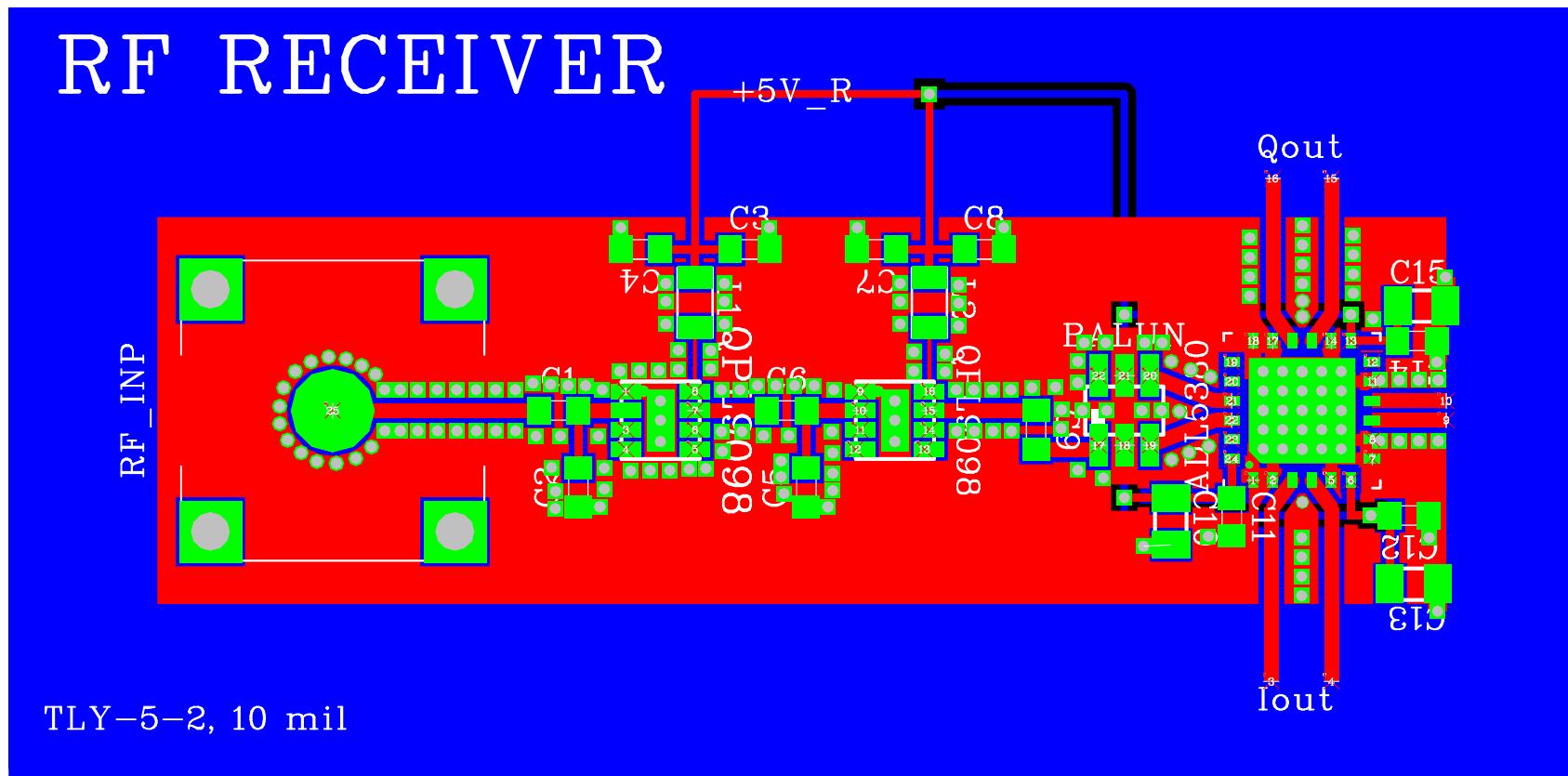


Figure 39. Receiver layout design

## 5. THE 5V POWER BUDGET

Since the two LNAs and the demodulator of the Receiver need +5V power supply, as well as the Modulator and the Power Amplifier of the transmitter and a part of the Frequency Synthesizer; it is evident that the DC current budget of the +5V power supply has to be well studied.

Let us study this current budget and decide about the +5V DC power supply.

The following table shows the +5V loads.

**TABLE 2. +5V POWER SUPPLY REQUIREMENTS**

SUB ASSEMBLY	Load	Supply Voltage	Max. Supply Current	Notes
		V	mA	
PLL	<b>VCO</b>	+5	90	
	<b>CP</b>	+5	9	<i>Charge pump</i>
Transmitter	<b>Modulator</b>	+5	203	
	<b>PAMP</b>	+5	430	
Receiver	<b>LNA</b>	+5	90	
	<b>Demodulator</b>	+5	245	
	<b>5V Total load</b>	<b>+5</b>	<b>1067</b>	<i>Total 5V supply current load</i>

It is evident from Table 2 that the total maximum load current required from the +5V supply exceeds the 800 mA of a single **ADM7150** regulator.

### 5.1. The 5V Power Supply Decision

We must use two **ADM7150** regulators; one for the Tx and another for the PLL and the Receiver.

The first **ADM7150** regulator feeds the following loads by the (+5T) feeding line:

SUB ASSEMBLY	Load	Supply Voltage	Max. Supply Current	Notes
		V	mA	
Transmitter	<b>Modulator</b>	+5	203	
	<b>PAMP</b>	+5	430	
	<b>5V Total load</b>	<b>+5</b>	<b>633</b>	<i>Total 5V supply current load</i>

The second **ADM7150** regulator feeds the following loads by the (+5R) feeding line:

:

SUB ASSEMBLY	Load	Supply Voltage	Max. Supply Current	Notes
		V	mA	
PLL	VCO	+5	90	
	CP	+5	9	<i>Charge pump</i>
Receiver	LNA	+5	90	
	Demodulator	+5	245	
	<b>5V Total load</b>	<b>+5</b>	<b>434</b>	<b>Total 5V supply current load</b>

## 6. RF PCB POWER SUPPLIES

The following figure shows the four PCB power supply schematic circuits. The recommendations of Analog Devices have been followed in this design.

Recommended component part numbers are shown on the schematic drawing. They will appear in the BOM file.

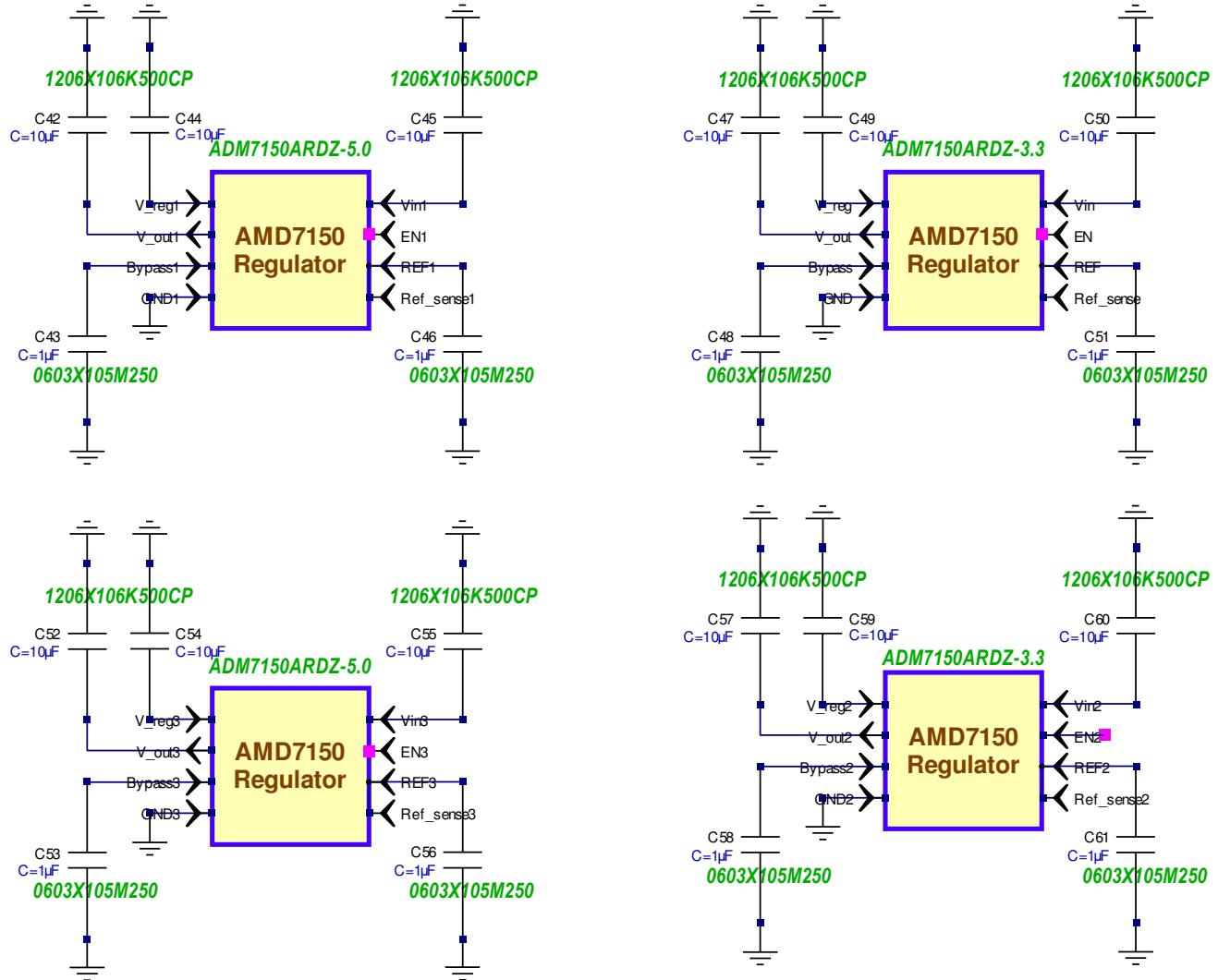
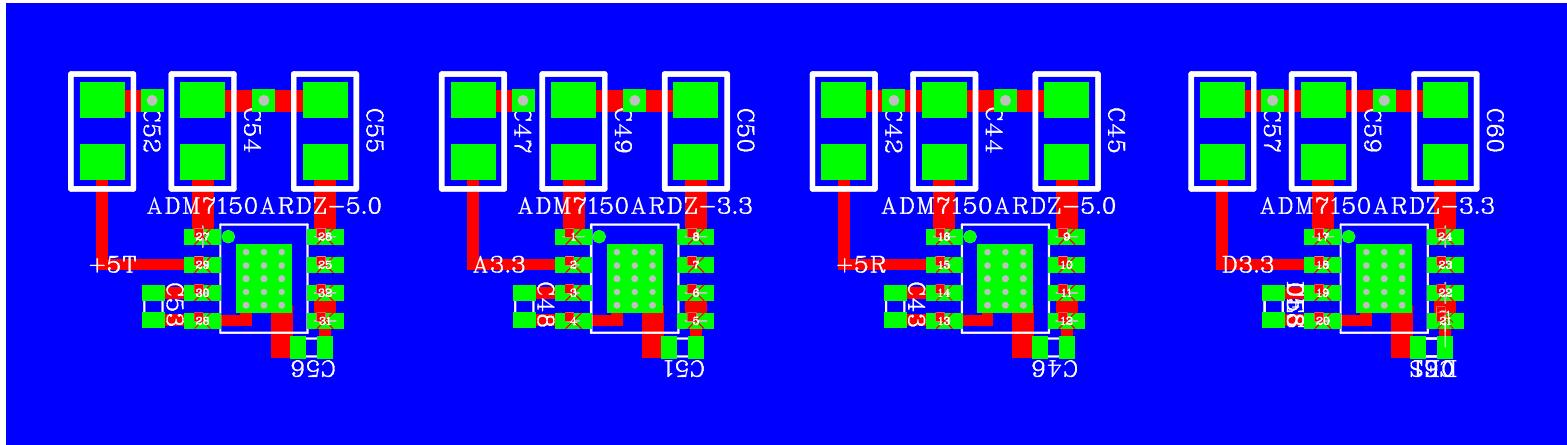


Figure 40a. Power Supply schematic design



**Figure 40b. Power Supply layout design**

## 7. RF PCB INTEGRATION

### 7.1. RF PCB SCHEMATIC DESIGN

The entire RF PCB schematic design has been integrated as shown in the following figure.

The RF design consists of three main parts; the PLL Frequency Synthesizer, The Transmitter and the Receiver. The schematic drawing of the Power Supplies is that shown in the previous figure (Figure 40b).

Some components part numbers are shown (in green) on the schematic drawing.

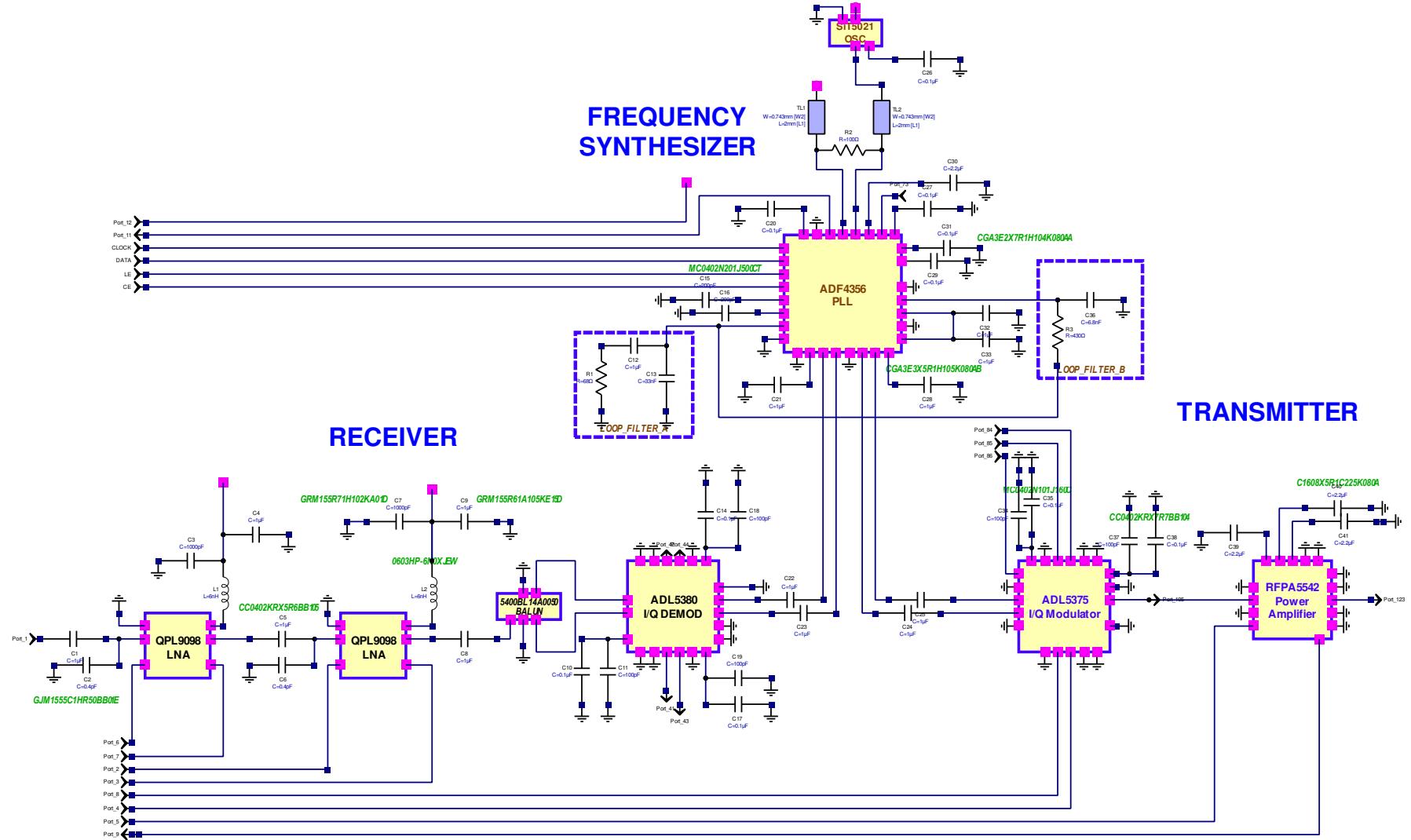


Figure 41. The integrated RF Circuit Schematic Design

## 7.2.RF PCB LAYOUT DESIGN

In the RF PCB layout design certain design rules have been followed.

### 7.2.1.RF PCB LAYOUT DESIGN

- All RF transmission lines have  $50 \text{ } [\Omega]$  characteristic impedance.
- In order to build a  $50 \text{ } [\Omega]$  microstrip transmission line on the Taconic TLY-5 2 oz 10mil substrate selected by the project owner, the  $50 \text{ } [\Omega]$  microstrip transmission line width should have been 0.712 mm, as it has been shown in detail in section 1.2. above, while the pins of the integrated circuits are separated by 0.5 mm; which would cause big problems between parallel transmission lines. Those problems would be coupling and interference and even short circuit problems.
- The project owner was notified several times with these facts. But he insisted on this substrate due to his system design decisions.
- The only solution was to use Ground\_Backed Co-Planar WaveGuide (GBCPWG) transmission lines with 0.14 mm gap and 0.381 mm line width, that gives perfect  $50 \text{ } [\Omega]$  match, as shown in the following figure.

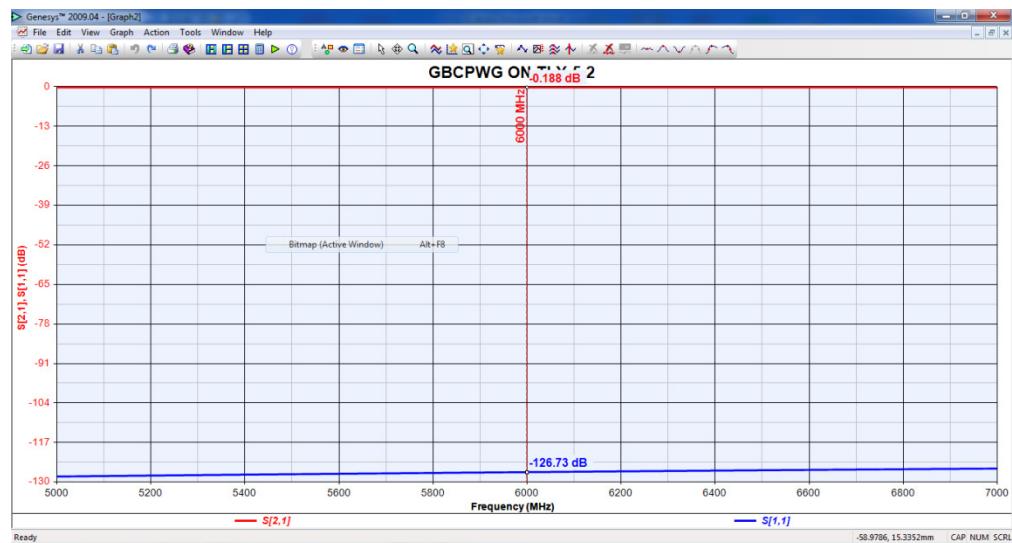
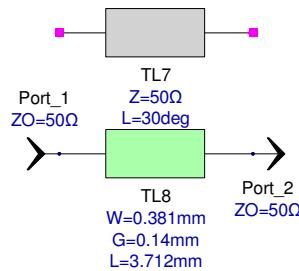
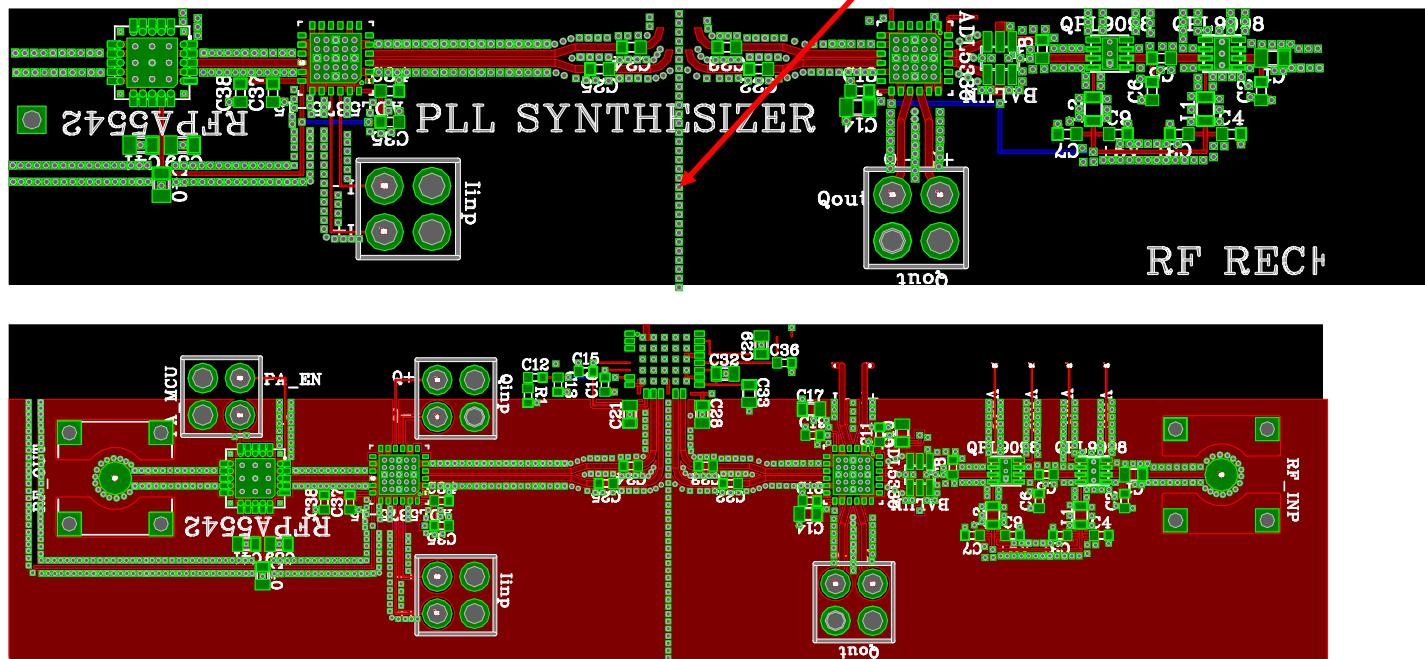


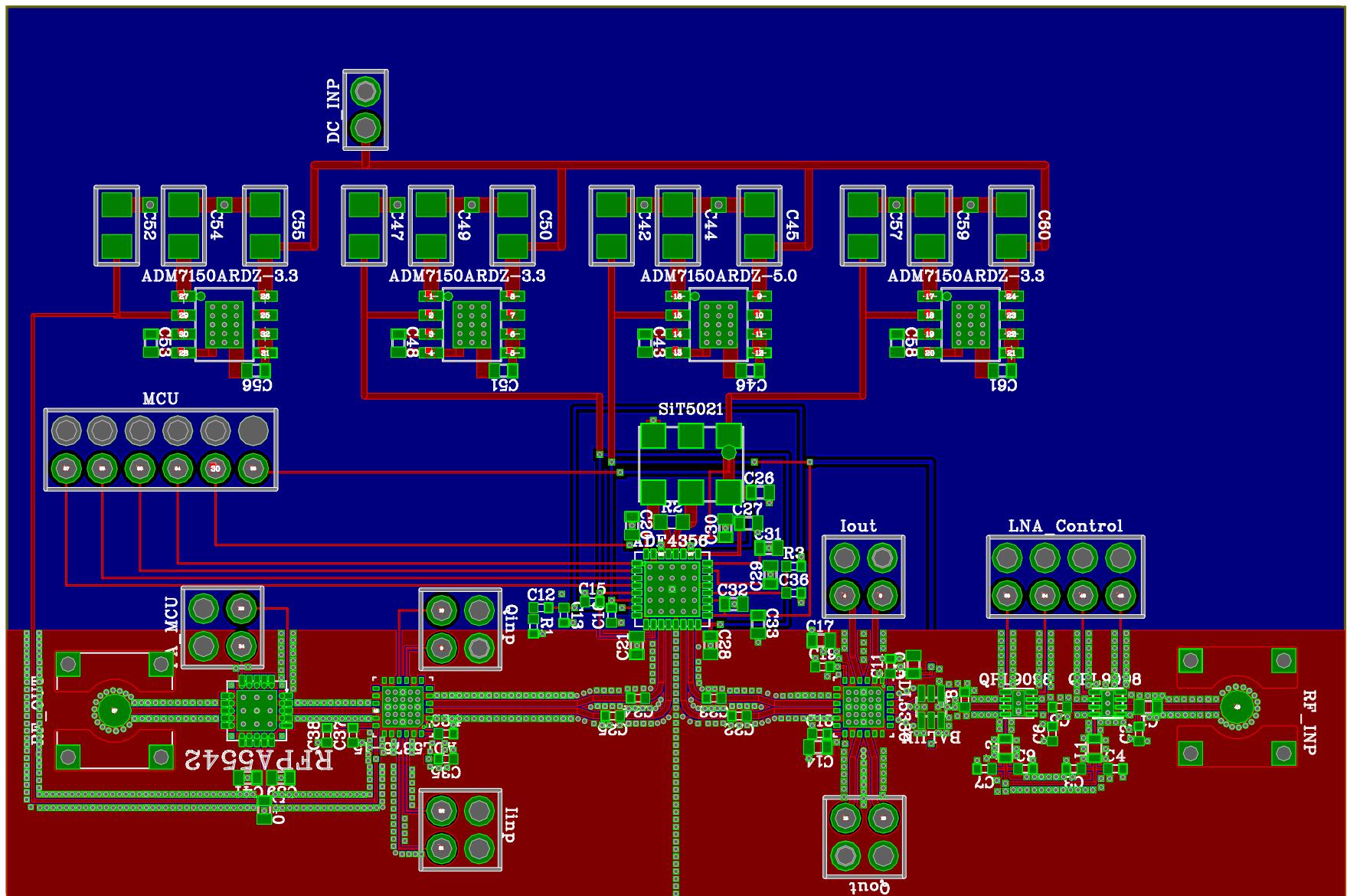
Figure 42. The  $50 \text{ } [\Omega]$  GBCPWG Transmission line

- All RF transmission lines of the Receiver, the Transmitter and the PLL Frequency Synthesizer have been designed as GNCPWG transmission lines with 0.384 mm width and 0.14 mm gap.
  - For this purpose, two ground planes have been used on the TOP and BOTTOM layers with 0.3 mm viaholes separated by 0.5 mm pitch.
  - A 0.5 mm pitch is much smaller than the guided wavelength of the used substrate at 6 GHz ( $\lambda_g = 22.896$  mm). This guarantees single mode wave propagation at 6 GHz [1].
  - As recommended by the project owner, a series of co-linear viaholes has been used to isolate the Tx and the Rx. The viaholes connect the TOP and BOTTOM ground planes of the PCB.



**Figure 43. Isolating the Tx and the Rx**

- The isolation between the Tx output and the Rx input was a main concern for the project owner. Several electromagnetic simulations have been done using the CST software. The results showed that the electromagnetic coupling between the two SMA connectors is lower than -60 dB.
  - The final layout design of the RF PCB is shown in the following figure.



**Figure 44. The RF PCB Layout Design**

### 7.3. RF PCB BILL OF MATERIALS

The BOM of the RF PCB is given ini the following table.

Bill of materials generated Fri Jun 30 14:21:58 2023

Workspace: D:\PROJECTS\1\_C\6G1.wsx

Package	Qty	Designators	Part Number	Manufacturer	Description
<hr/>					
QFN20B	01	RFPA5542	RFP A5542SB	QORVO	RF Power Amplifier
QFN24	02	ADL5380	ADL5380ACPZ-R7	AD	I/Q Demodulator
		ADL5375-15	ADL5375-15ACPZ	AD	I/Q Modulator
QFN32 VCO	01	ADF4356	ADF4356BCPZ	AD	PLL Synthesizer with
<hr/>					
SOIC-8P	04	ADM7150ARDZ-5.0	ADM7150ARDZ-5.0	AD	Voltage Regulator
		ADM7150ARDZ-5.0	ADM7150ARDZ-5.0	AD	Voltage Regulator
		ADM7150ARDZ-3.3	ADM7150ARDZ-3.3	AD	Voltage Regulator
		ADM7150ARDZ-3.3	ADM7150ARDZ-3.3	AD	Voltage Regulator
BALUN	01	BALUN	5400BL14A0050	Johanson	1:1 BALUN
DFN8	01	QPL9098	QPL9098TR7	QORVO	LNA
SIT5	01	SiT5021	SIT5021AI-2DE-33E-100.000000X	SiTime	Differential TCXO

R0603	01	R2[R=100]	CR0603-FX-1000ELF	Bourns	Chip Resistor
R0402	02	R1[R=68]	ERJ2GEJ680X	Panasonic	Chip Resistor
		R3[R=430]	ERJ2RKF4300X	Panasonic	Chip Resistor
L603	02	L1[L=6nH]	0603HP-6N0XJEW	Coilcraft	Chip Inductor
		L2[L=6nH]	0603HP-6N0XJEW	Coilcraft	Chip Inductor
CC3216[1206]	12	C42[C=10µF]	1206X106K500CP	Walsin	Chip Capacitor
		C44[C=10µF]	1206X106K500CP	Walsin	Chip Capacitor
		C45[C=10µF]	1206X106K500CP	Walsin	Chip Capacitor
		C47[C=10µF]	1206X106K500CP	Walsin	Chip Capacitor
		C49[C=10µF]	1206X106K500CP	Walsin	Chip Capacitor
		C50[C=10µF]	1206X106K500CP	Walsin	Chip Capacitor
		C52[C=10µF]	1206X106K500CP	Walsin	Chip Capacitor
		C54[C=10µF]	1206X106K500CP	Walsin	Chip Capacitor
		C55[C=10µF]	1206X106K500CP	Walsin	Chip Capacitor
		C57[C=10µF]	1206X106K500CP	Walsin	Chip Capacitor
		C59[C=10µF]	1206X106K500CP	Walsin	Chip Capacitor
		C60[C=10µF]	1206X106K500CP	Walsin	Chip Capacitor

C0402	24	C2[C=0.4pF]	GJM1555C1HR50BB01E	Murata	Chip Capacitor
		C3[C=1000pF]	GRM155R71H102KA01D	Murata	Chip Capacitor
		C4[C=1μF]	GRM155R61A105KE15D	Murata	Chip Capacitor
		C5[C=1μF]	CC0402KRX5R6BB105	YAGEO	Chip Capacitor
		C6[C=0.4pF]	GJM1555C1HR50BB01E	Murata	Chip Capacitor
		C7[C=1000pF]	GRM155R71H102KA01D	Murata	Chip Capacitor
		C8[C=1μF]	CC0402KRX5R6BB105	YAGEO	Chip Capacitor
		C9[C=1μF]	GRM155R61A105KE15D	Murata	Chip Capacitor
		C11[C=100pF]	MC0402N101J160CT	Multicomp	Chip Capacitor
		C12[C=1μF]	GRM155R61A105KE15D	Murata	Chip Capacitor
		C13[C=33nF]	MC0402B333K250CT	Multicomp	Chip Capacitor
		C15[C=200pF]	MC0402N201J500CT	Multicomp	Chip Capacitor
		C16[C=200pF]	MC0402N201J500CT	Multicomp	Chip Capacitor
		C18[C=100pF]	MC0402N101J160CT	Multicomp	Chip Capacitor
		C19[C=100pF]	MC0402N101J160CT	Multicomp	Chip Capacitor
		C22[C=1μF]	CC0402KRX5R6BB105	YAGEO	Chip Capacitor
		C23[C=1μF]	CC0402KRX5R6BB105	YAGEO	Chip Capacitor
		C24[C=1μF]	CC0402KRX5R6BB105	YAGEO	Chip Capacitor
		C25[C=1μF]	CC0402KRX5R6BB105	YAGEO	Chip Capacitor
		C34[C=100pF]	MC0402N101J160CT	Multicomp	Chip Capacitor
		C35[C=0.1μF]	CC0402KRX7R7BB104	YAGEO	Chip Capacitor

		C36[C=6.8nF]	MC0402B682K500CT	Multicomp	Chip Capacitor
		C37[C=100pF]	MC0402N101J160CT	Multicomp	Chip Capacitor
		C38[C=0.1μF]	CC0402KRX7R7BB104	YAGEO	Chip Capacitor
C603	25	C1[C=1μF]	CGA3E3X5R1H105K080AB	TDK	Chip Capacitor
		C10[C=0.1μF]	CS0603KRX7R8BB104	YAGEO	Chip Capacitor
		C14[C=0.1μF]	CS0603KRX7R8BB104	YAGEO	Chip Capacitor
		C17[C=0.1μF]	CS0603KRX7R8BB104	YAGEO	Chip Capacitor
		C20[C=0.1μF]	CS0603KRX7R8BB104	YAGEO	Chip Capacitor
		C21[C=1μF]	CGA3E3X5R1H105K080AB	TDK	Chip Capacitor
		C26[C=0.1μF]	CS0603KRX7R8BB104	YAGEO	Chip Capacitor
		C27[C=0.1μF]	CS0603KRX7R8BB104	YAGEO	Chip Capacitor
		C28[C=1μF]	CGA3E3X5R1H105K080AB	TDK	Chip Capacitor
		C29[C=0.1μF]	CS0603KRX7R8BB104	YAGEO	Chip Capacitor
		C30[C=2.2μF]	C1608X5R1C225K080A	TDK	Chip Capacitor
		C31[C=0.1μF]	CS0603KRX7R8BB104	YAGEO	Chip Capacitor
		C32[C=1μF]	CGA3E3X5R1H105K080AB	TDK	Chip Capacitor
		C33[C=1μF]	CGA3E3X5R1H105K080AB	TDK	Chip Capacitor
		C39[C=2.2μF]	C1608X5R1C225K080A	TDK	Chip Capacitor
		C40[C=2.2μF]	C1608X5R1C225K080A	TDK	Chip Capacitor
		C41[C=2.2μF]	C1608X5R1C225K080A	TDK	Chip Capacitor

		C43[C=1μF]	0603X105M250CT	Walsin	Chip Capacitor
		C46[C=1μF]	0603X105M250CT	Walsin	Chip Capacitor
		C48[C=1μF]	0603X105M250CT	Walsin	Chip Capacitor
		C51[C=1μF]	0603X105M250CT	Walsin	Chip Capacitor
		C53[C=1μF]	0603X105M250CT	Walsin	Chip Capacitor
		C56[C=1μF]	0603X105M250CT	Walsin	Chip Capacitor
		C58[C=1μF]	0603X105M250CT	Walsin	Chip Capacitor
		C61[C=1μF]	0603X105M250CT	Walsin	Chip Capacitor
POST2x2	05	Qout	67996-202HLF	Amphenol	Pin Header 2x2
		Qinp	67996-202HLF	Amphenol	Pin Header 2x2
		Iinp	67996-202HLF	Amphenol	Pin Header 2x2
		Iout	67996-202HLF	Amphenol	Pin Header 2x2
		PA MCU	67996-202HLF	Amphenol	Pin Header 2x2
POST2x4	01	LNA_Control	TLW-102-05-G-D	Samtec	Pin Header 2x4
POST1x2	02	MOD_EN	87224-2	TE Connectivity	Pin Heaser 1x2
		DEMOD_EN	87224-2	TE Connectivity	Pin Heaser 1x2
sma	02	RF_OUT	132134-10	Amphenol	sma Connector
		RF_INP	132134-10	Amphenol	sma Connector

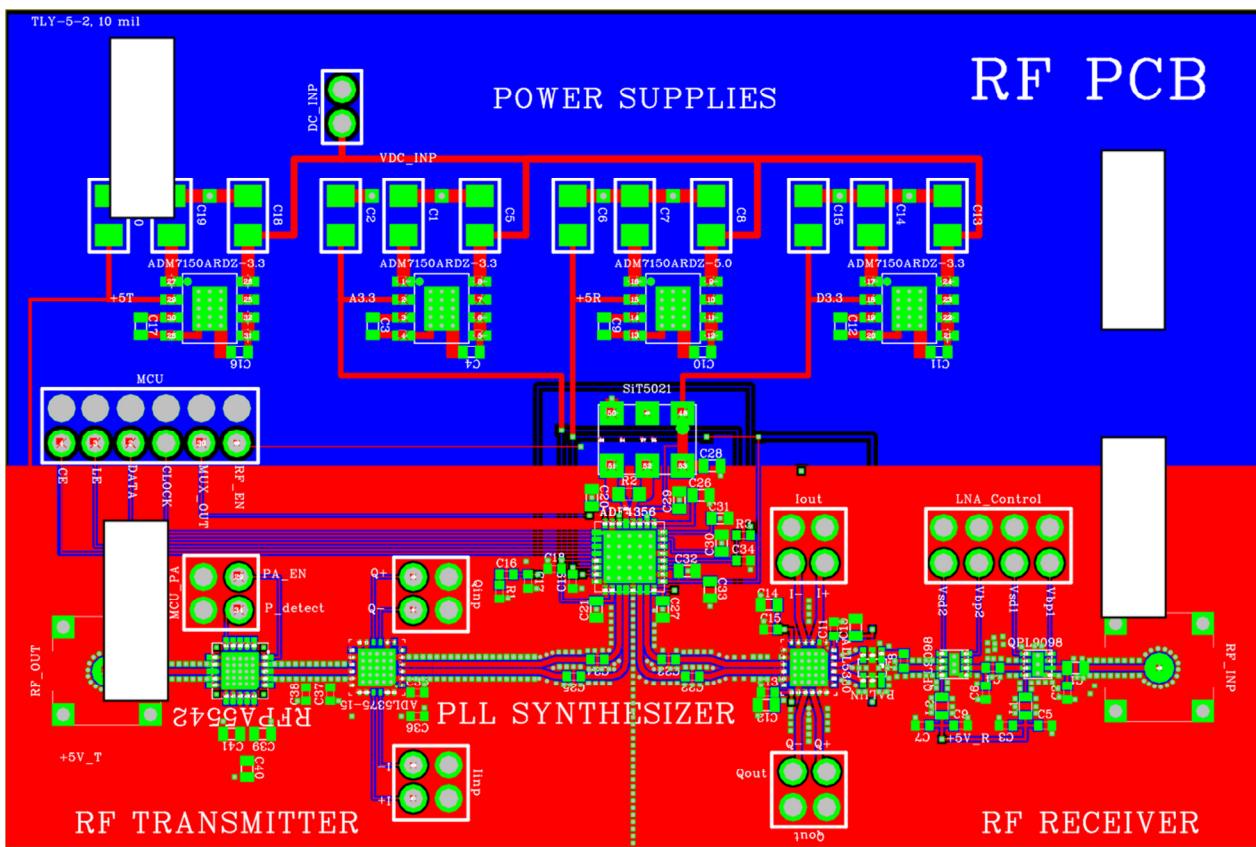
## 8. PROJECT OWNER'S FEEDBACK

This is very good,

Your labeling of the components and sub-systems is greatly appreciated!

But, I have some changes that I need:

1. I need 4 connectors for the signals and power, I would like them arranged in 4 banks of 12 pins (2x6), arranged in a square and aligned to a 5mm grid. I am attaching a rough sketch to show the approximate locations. Also, I want these connectors on the backside of the board, the opposite side of the RF SMA connectors.



RX: Downconverter -> limiting amps (MAX3747) -> limiting amps (MAX3747) -> LC filter -> connector

TX: Connector -> Lim Amp -> LC filter -> Upconverter

And this will need to be duplicated for both the I and Q channels on each. Please use 0603 devices for the LC filter. If any of this is unclear, please let me know and I am happy to clarify.

4. Power supplies: please use smaller SMT devices at the top of the power supplies. Also, if there is not enough room on the front side of the board, you can move the power supplies to the backside of the board, but then I need test-points (1mm disc) on the fronts side of the board, clearly labeled)
5. I would like to keep board around 65mm x 95mm
6. Eventually, I will also need the full design files in addition to Gerbers

## **9. IMPLEMENTATION OF THE OWNER'S MODIFICATIONS**

### **9.1. GENERAL MECHANICAL MODIFICATIONS**

- The PCB area has been increased to 95 mm x 65 mm.
- Four grounded plated mounting holes for M3 screws are drilled at 5mm x 5mm from each corner
- The four power supply circuits have been moved to the BOTTOM layer. All necessary modifications and connections have been done.
- Four labeled test points for the four power supply voltages have been added [Analog 3.3V (A3.3), Digital 3.3V (D3.3), 5V for Tx (+5T) and 5V for Rx (+5R)].
- All the RF circuits have been moved vertically to allow for the two new pin headers at the bottom of the PCB.
- Four identical 2x6 pin headers are placed at equal distances (5mm multiples) from the PCB center where all low frequency and DC input/output signals will be connected to/from the PCB.
- I/Q processing circuits for Rx and Tx have been located on the TOP layer in the available spaces after moving the power supply circuits.
- An outline sketch in the following figure shows these modifications.

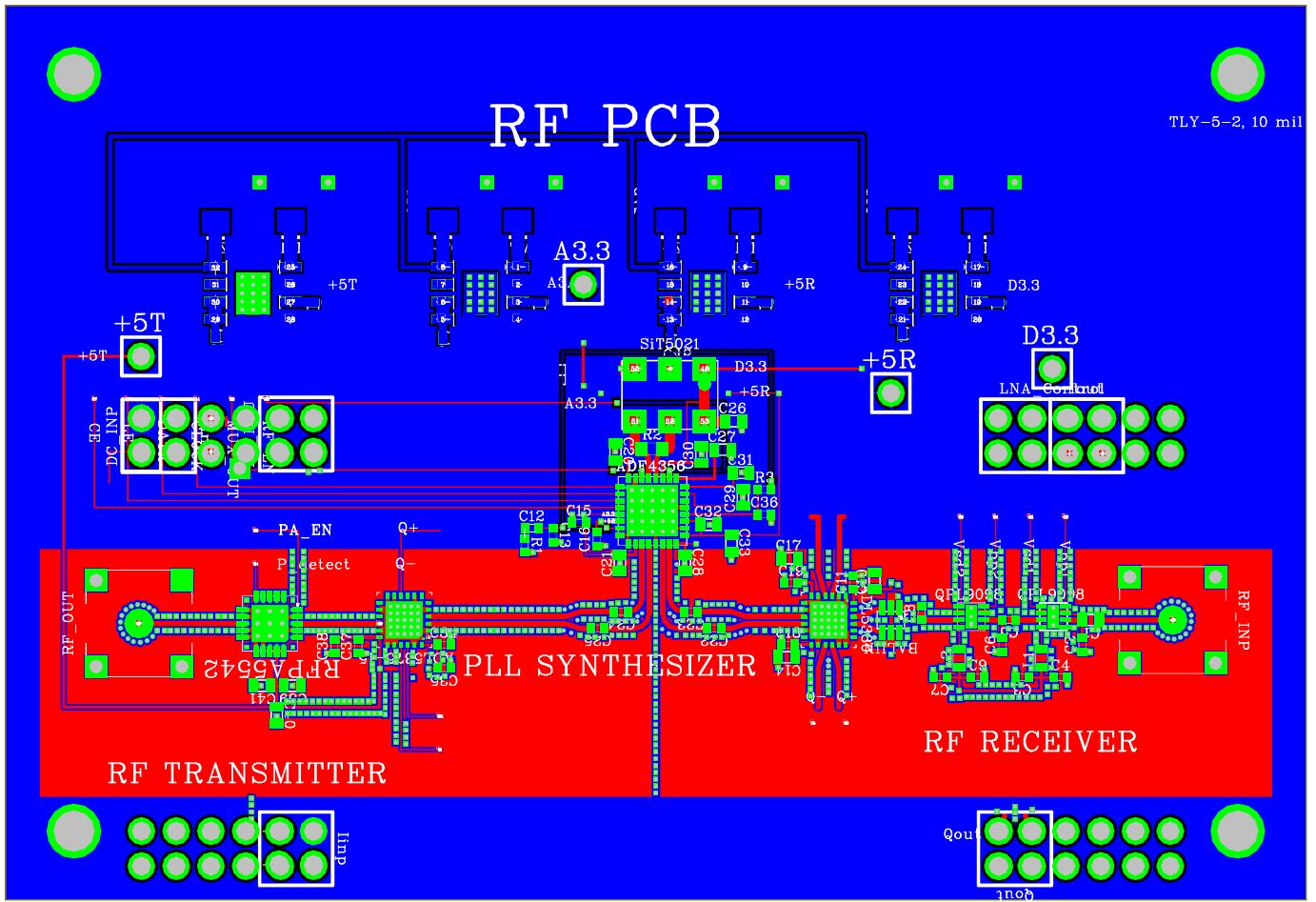


Figure 46. Proposed Layout modifications

## 9.2. I/Q PROCESSING CIRCUITS DESIGN

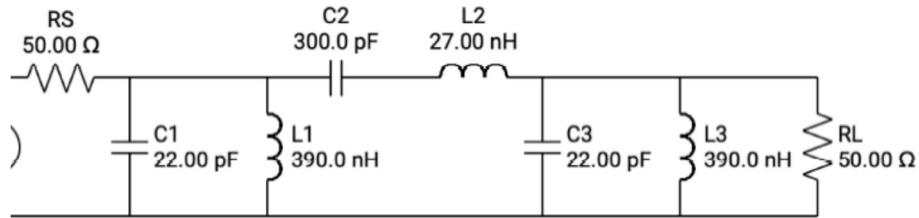
### 9.2.1. RECEIVER I/Q OUTPUT PROCESSING CIRCUITS

The project owner asked for additional circuits for I/Q output signal processing after the demodulator. He recommended to use the MAX3747A limiting amplifier and to filter its differential output signals by two identical band-pass filters with 10 to 1 in the ADL5380 Demodulator datasheet, the I/Q outputs are described as follows:

"I Channel and Q Channel Mixer Baseband Outputs. These outputs have a  $50\ \Omega$  differential output impedance ( $25\ \Omega$  per pin). Each output pair can swing 2 V p-p (differential) into a load of  $200\ \Omega$ . The output 3 dB bandwidth is ~400 MHz."

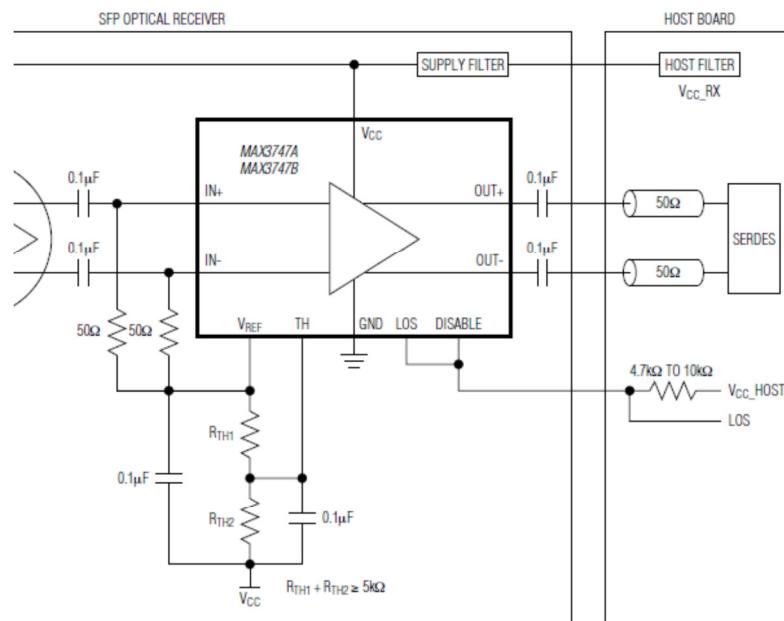
The output emitter followers inside the chip drive the differential I and Q signals off chip. The output impedance is set by on-chip  $25\ \Omega$  series resistors that yield a  $50\ \Omega$  differential output impedance for each baseband port. The fixed output impedance forms a voltage divider with the load impedance that reduces the effective gain. For example, a  $500\ \Omega$  differential load has 1 dB lower effective gain than a high ( $10\ k\Omega$ ) differential load impedance.

As we shall use a MAX3747A differential limiting amplifier with high input impedance for each output, we can match its two input impedances to  $50 \text{ } \Omega$  and use as short as possible transmission lines.



**Figure 47. The BPF**

### 9.2.2.LIMITING AMPLIFIER DESIGN



**Figure 48. The limiting amplifier circuit**

As recommended by the project owner, we shall use the MAX3747 limiting amplifier. It will be fed by the  $+3.3\text{V}$  power supply for digital circuits (D3.3).

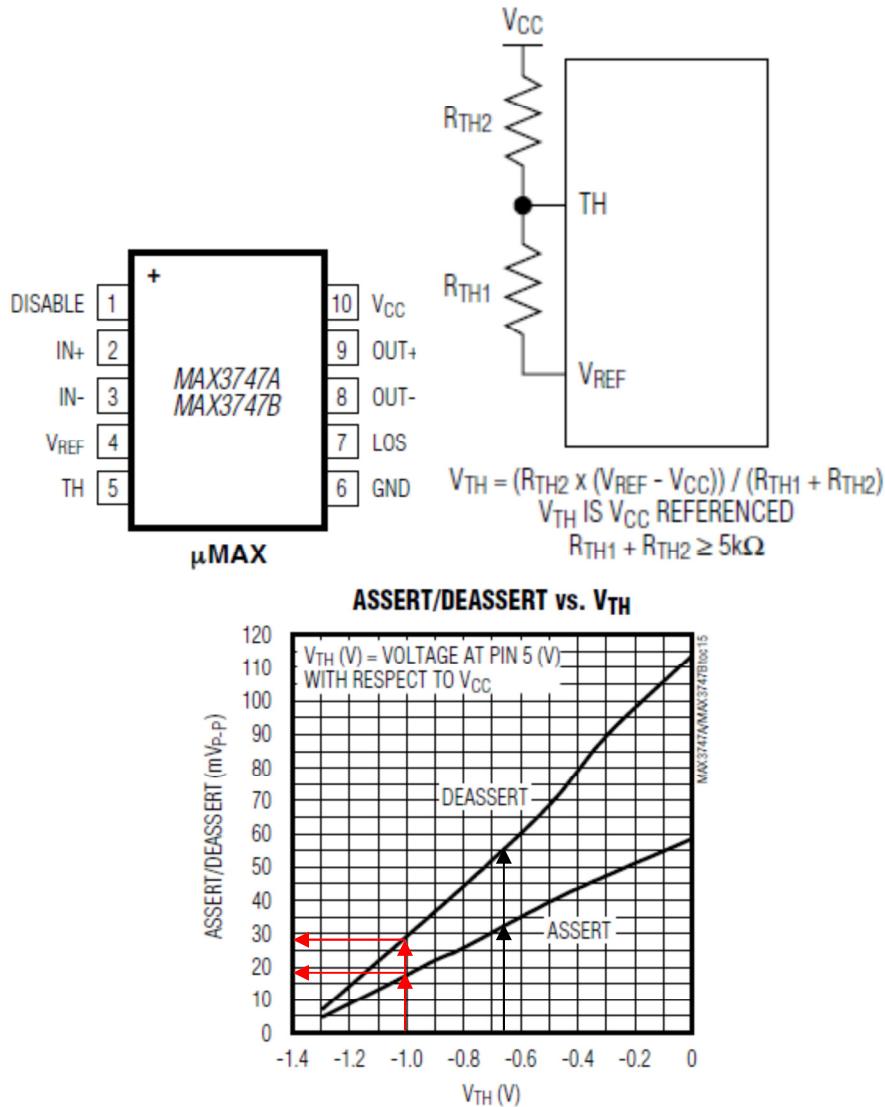
The limiting threshold is set by a resistive voltage divider as shown in the following figure.

Let us assume that we set the threshold at  $2.3 \text{ V} = \text{VCC} - 1\text{V}$ .

From Figure 49 we can get:

$$V_{\text{assert}} = 19 \text{ [mV]}$$

$$V_{\text{deassert}} = 28 \text{ [mV].}$$



**Figure 48. The MAX3747**

Then we apply the following equations to calculate the two resistances:

$$R_{th1} + R_{th2} > 5 \text{ [kΩ].} \quad (1)$$

$$\text{Let us take } R_{th1} + R_{th2} = 10 \text{ [kΩ]. Then } R_{th2} = 10 - R_{th1} \quad (2)$$

$$V_{ref} = V_{CC} - 1.3 = 3.3 - 1.3 = 2 \text{ [V].} \quad (3)$$

$$V_{th} = \frac{R_{th2}(V_{ref} - V_{CC})}{R_{th1} + R_{th2}} \quad (4)$$

Substituting in (4) we get:

$$V_{th} = -1 = \frac{R_{th2}(V_{ref}-V_{CC})}{R_{th1}+R_{th2}} = \frac{R_{th2}(2-3.3)}{10}$$

$$-1 = \frac{R_{th2}(2-3.3)}{10}$$

$$-1 = \frac{R_{th2}(-1.3)}{10}$$

$$R_{th2} = 10/1.3 = 7.6923 \text{ [k}\Omega\text{]} \text{ and } R_{th1} = 10 - 7.6923 = 2.3 \text{ [k}\Omega\text{].}$$

We shall use the [CRCW04027K68FKED](#) 7.68 kΩ resistor and the [ERJ2RKF2321X](#) 2.32 kΩ resistor.

Substituting with these practical values we get:

$$V_{th} = 3.3 + \frac{7.68(2-3.3)}{2.32+7.68} = 3.3 - 0.9984 = 2.3016 \approx 2.3 \text{ [V].}$$

### 9.2.3. Project Owner's Requests regarding the Rx Limiting Amplifier

- “This is for the assert/deassert of the LoS line, it does not affect the operation of the amp directly. But, we need to handle it properly. Please make the Rth1/2 resistors both 10kOhm.”

“Also, please

- Connect the LoS output pin via a 10kOhm resistor to Gnd.

THEY HAVE BEEN PULLED-UP TO VCC ACCORDING TO THE DATASHEET.

- And connect the DISABLE pin to GND via 1kOhm resistor”.

DONE, THEY HAVE BEEN CONNECTED DIRECTLY TO GROUND ACCORDING TO THE MANUFACTURER'E RECOMMENDATION.

Applying the same equations with two 10kW resistors we get:

$$V_{th} = \frac{R_{th2}(V_{ref}-V_{CC})}{R_{th1}+R_{th2}}$$

$$= \frac{10(2-3.3)}{20}$$

$$= -(1.3/2)$$

$$= -0.65 \text{ [V].}$$

From Figure 48 above, the Assert level will be 32 mV and the Deassert level will be 55 mV.

## 9.3. INPUT/OUTPUT & CONTROL SIGNALS

We have 27 Input / Output and Control signals in this RF Assembly.

They can be classified as follows:

1. Two RF signals, one input signal to the Receiver and one output signal from the Transmitter. These two signals have been labeled 1 and 2.
2. Eight LF information signals. They are the following:
  - 2.1. The balanced Trnamitter input I signal, Itx\_p and Itx\_n.
  - 2.2. The balanced Trnamitter input Q signal, Qtx\_p and Qtx\_n.
  - 2.3. The balanced Receiver output I signal, Irx\_p and Irx\_n.
  - 2.4. The balanced Receiver output Q signal, Qtx\_p and Qtx\_n.

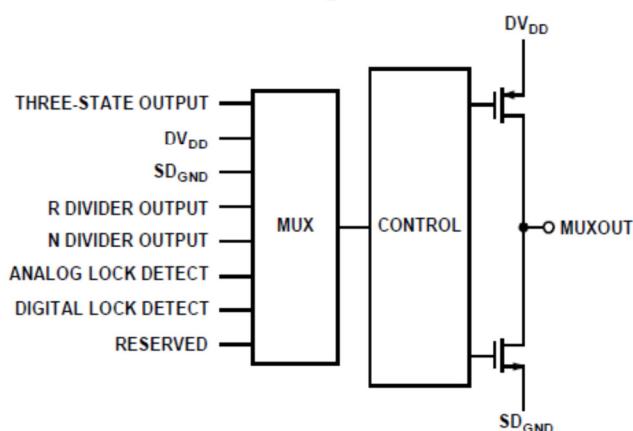
These eight LF signal ports have been labeled 3 to 10.

3. Three Tx control signals:
  - 3.1. Tx\_disable, active HIGH, to disable the Modulator
  - 3.2. Pdetect, an output voltage proportional to the RF output power level.
  - 3.3. PA\_EN, active HIGH to enable the Power Amplifier. It should never be disabled before disabling the PLL RF output.

They have been labeled 11, 12 and 13 respectively.

***The seven Transmitter control signals (including the I/Q input signals) are grouped in a single 2x6 pin-header connector, called (Tx\_Signals)***

4. Six PLL control signals:
  - 4.1. RF\_EN, active HIGH, to enable the RF output of the PLL. It should never be enabled before enabling the RF Amplifier, labeled 14.
  - 4.2. MUX\_OUT, an output signal from the PLL that can monitor any PLL internal signal, to be user selected from those shown in the following figure. It is labeled 15.



**Figure 49. Multiplexed PLL output signals**

- 4.3. CLOCK signal from the MCU to synchronize digital communication with the PLL. It is labeled 16.
- 4.4. DATA exchanged between the MCU and the PLL, labeled 17.
- 4.5. LE, Load Enable, to enable loading data on the PLL DATA port, labeled 18.
- 4.6. CE, Chip Enable. A logic low on this pin powers down the PLL and puts the charge pump into three-state mode. A logic high on this pin powers up the PLL, depending on the status of the power-down bits. It has been labeled 19.

***The six PLL control signals are grouped in a 2x6 pin header connector called “PLL\_Signals”.***

- 5. Four Receiver control signals:
  - 5.1. Vbp1
  - 5.2. Vsd1
  - 5.3. Vbp2
  - 5.4. Vsd2.

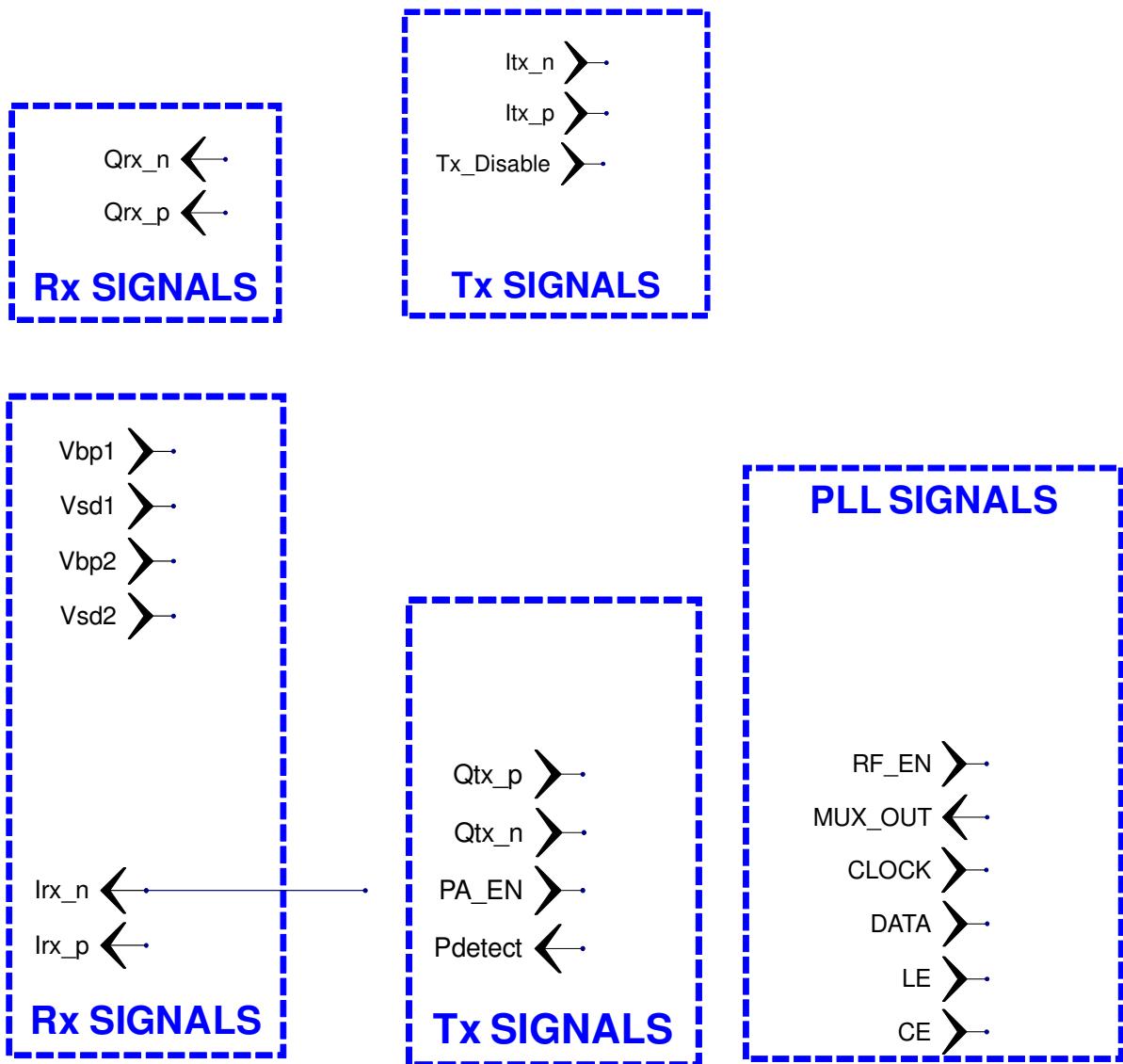
They are labeled 20, 21, 22 and 23 respectively.

***The eight Receiver control signals (including the I/Q output signals) are grouped in a single 2x6 pin-header connector, called (Rx\_Signals)***

- 6. One DC\_INP port, labeled 24.
- 7. Four power supply enable input signals, active HIGH. They are grouped together in one input control port (Power\_EN) labeled 25.
- 8. Four DC Power Supply voltages, called D3.3, +5R, A3.3 and +5T, labeled 26, 27, 28 and 29, respectively.

***The six DC Power Supply signals (including the EN control signal) are grouped in a single 2x6 pin-header connector, called (Power\_Supply)***

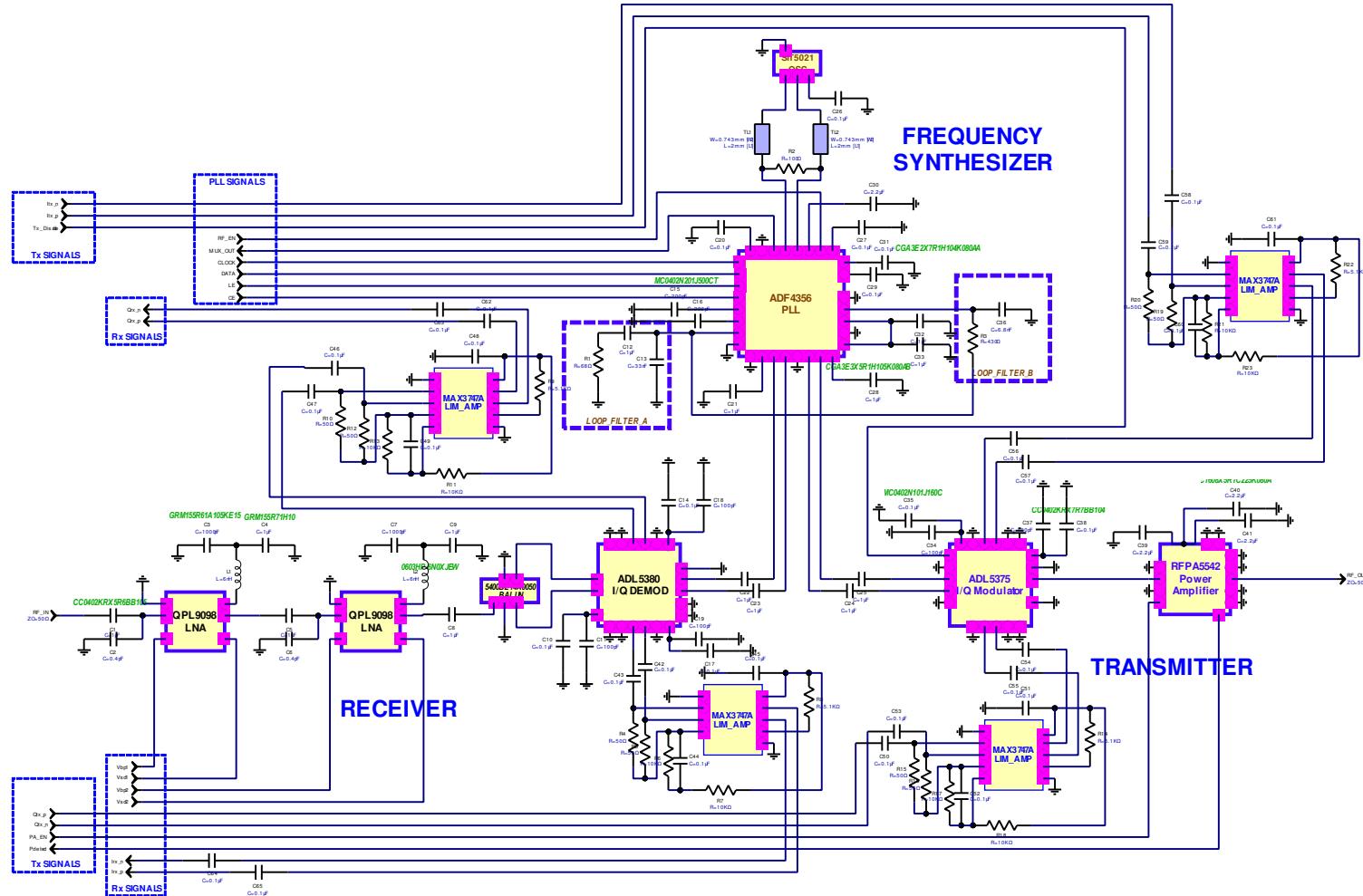
***As recommended by the project owner, the four 2x6 pin header connectors are symmetrical located at the four sides of the RF Assembly.***

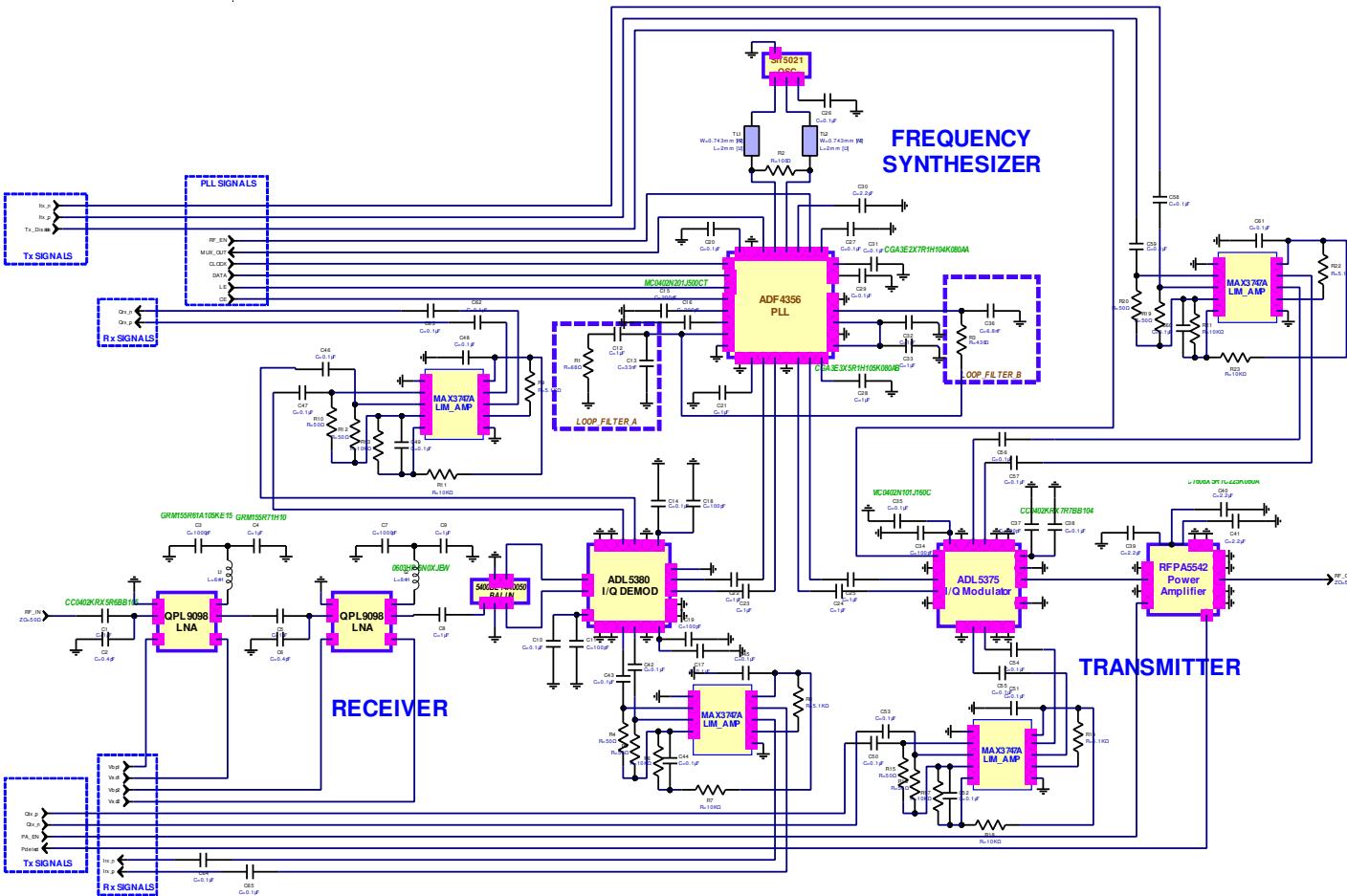


**Figure 50. Tx, Rx and PLL Control Signals**

#### **9.4. SCHEMATIC DESIGN DRAWING OF THE RF ASSEMBLY**

The schematic design drawing of the RF Assembly after the owner's modifications is shown in the following figure





**Figure 51. Schematic Design Drawing of the RF Assembly**

## 9.5. LAYOUT DESIGN DRAWING OF THE RF ASSEMBLY

The following figure shows the layout design drawing of the RF Assembly after the modifications asked by the project owner.

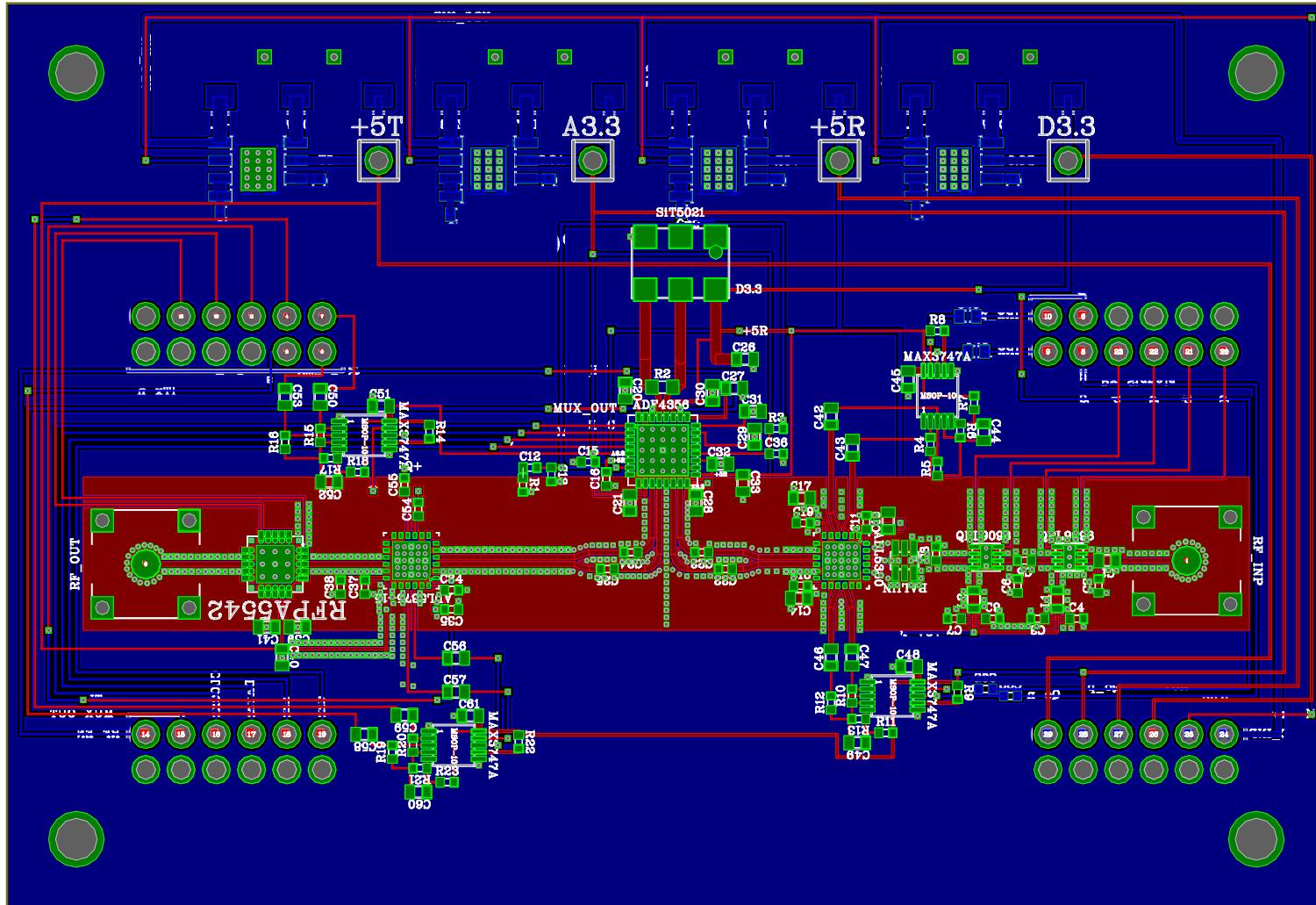


Figure 52. The Layout Design Drawing of the RF Assembly

## 10. NEW REQUIREMENTS OF THE PROJECT OWNER

On 25 July 2023, the project owner added the following new requirements:

### RF\_Sch additions (25 July 2023)

#### A. RX DOWN-CONVERTER OUTPUT ADL5380 •

Need Differential LC output filter • Between ADL5380 and Lim. Amps

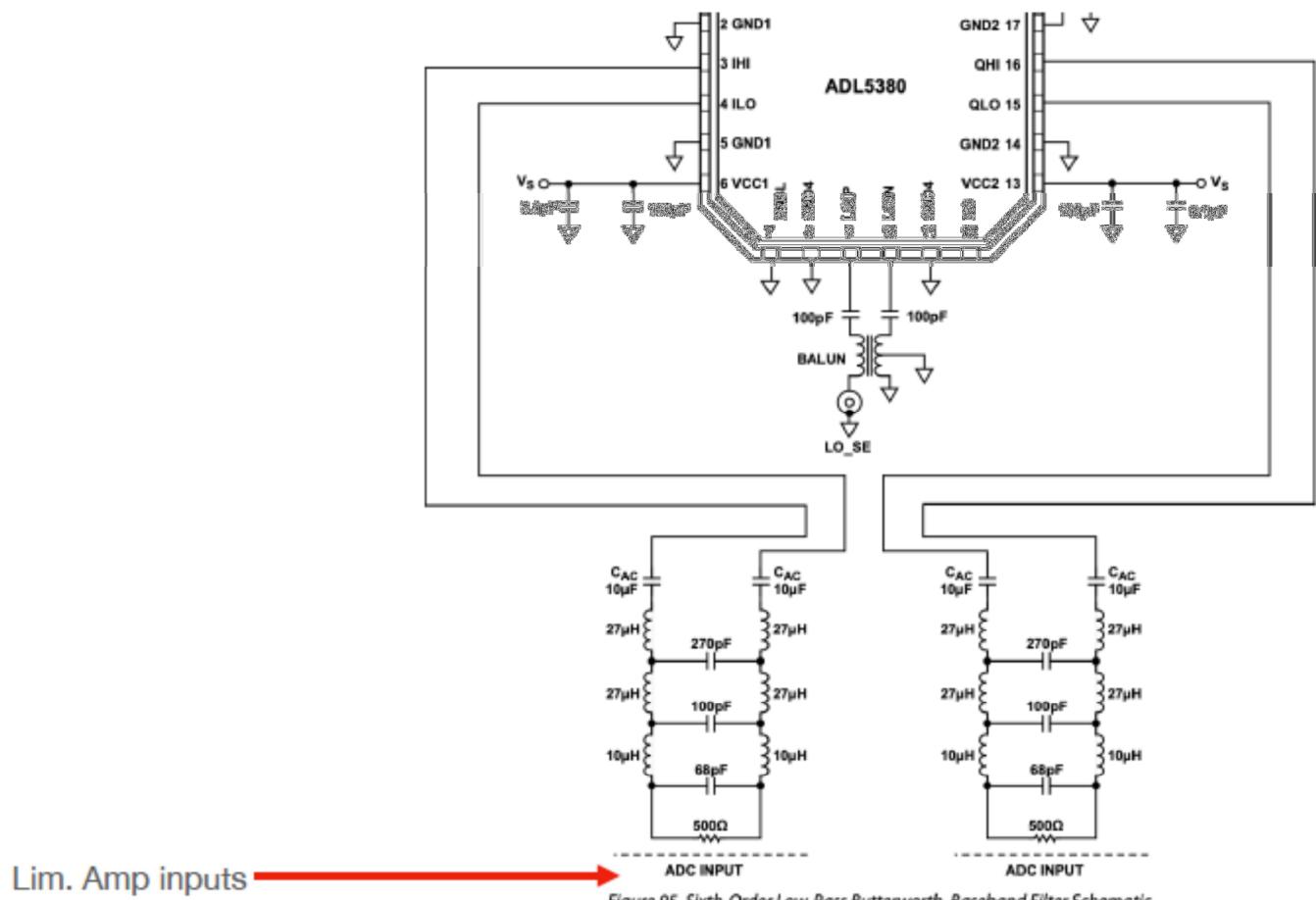


Figure 95. Sixth-Order Low-Pass Butterworth, Baseband Filter Schematic

figure 53. the required i/q output filter

#### B. TX UP-CONVERTER LO INPUT ADL5375 •

Need Differential LC filter on LO input • More discussion in data sheet • Do NOT put Zbias devices, they are not needed for ADF4356 Our PLL: ADF4356

Our PLL: ADF4356

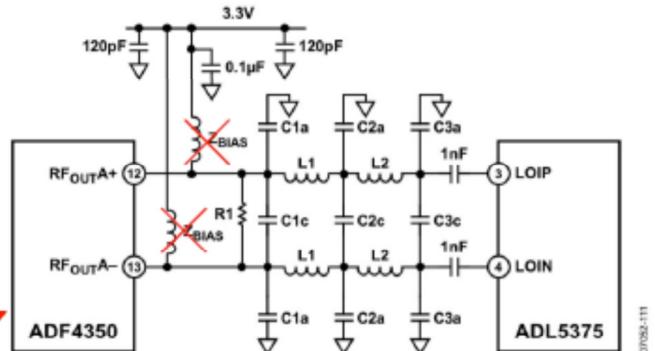


Figure 57. PLL-Modulator Interface Schematic

**Figure 54. The required RF LPF between the PLL and the Modulator**

### C. TX UP-CONVERTER DATA INPUT ADL5375 •

Need Differential LC filter on Data inputs

- More discussion in data sheet
- Input resistors need to go to bias voltage of 500mV. I have not decided how to generate that yet.

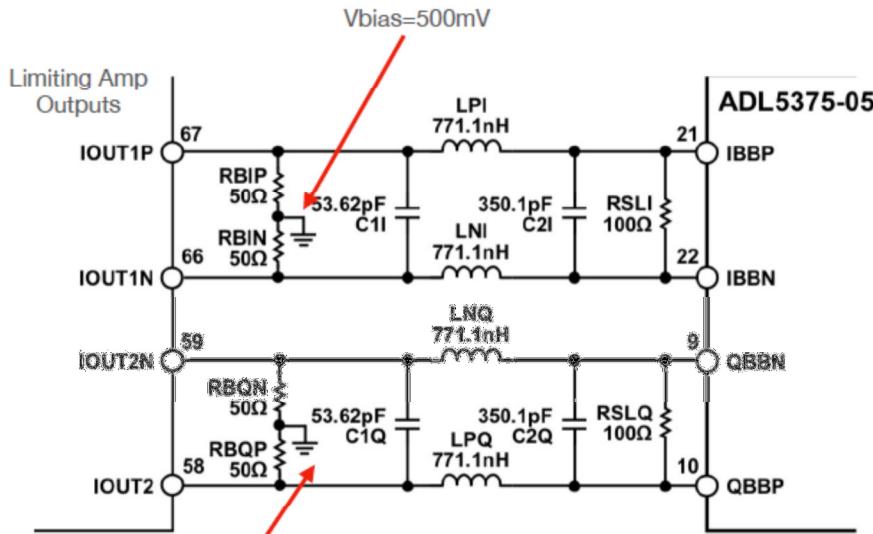


Figure 61. DAC Modulator Interface with  
10 MHz Third-Order, Bessel Filter

Vbias=500mV

**Figure 55. The required I/Q differential LPF at the modulator input**

## **D. ANOTHER SPEC THAT I FORGOT TO POINT OUT AS WELL:**

Our baseband (data) bandwidth: It should be no higher than 300MHz. So, the data input and output LC filters should have a cutoff of 500MHz. This is perhaps a bit high, but I want to keep fast transitions on the data edges. Also, they should be Bessel filters to preserve step response.

## **11. DESIGN AND IMPLEMENTATION OF THE REQUIRED FILTERS**

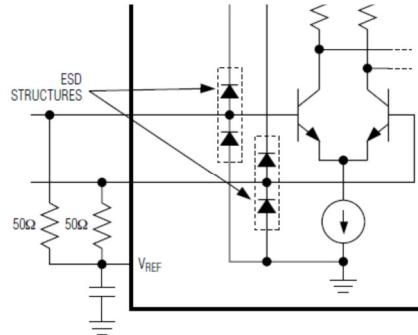
### **11.1. RX downconverter Output Filters**

It is required to design two identical differential elliptic LPF between the demodulator and the limiting amplifier. The cut-off frequency of both filters is 500 MHz.

### **11.2. Baseband LPF Design**

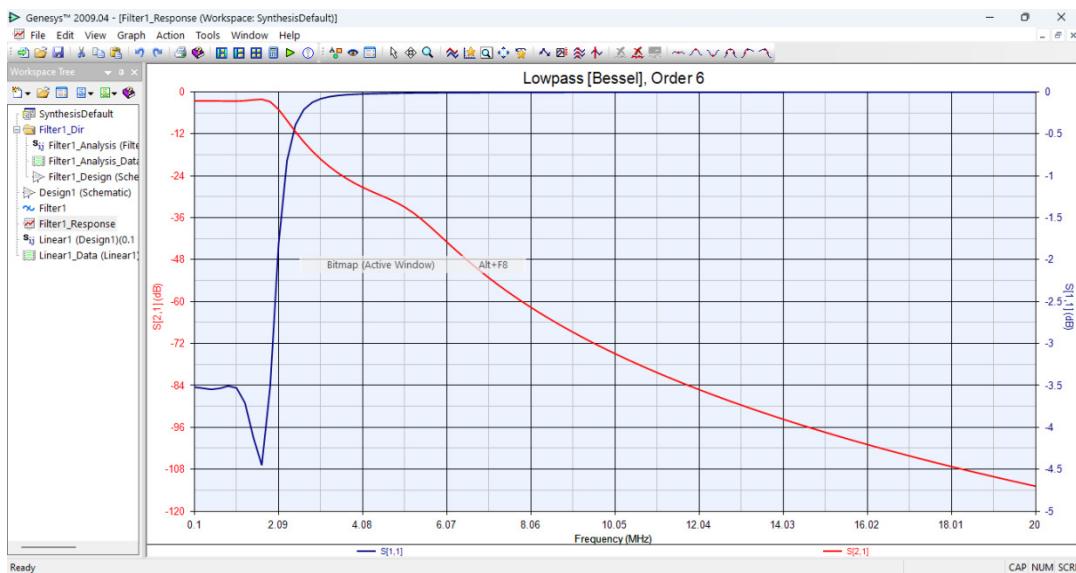
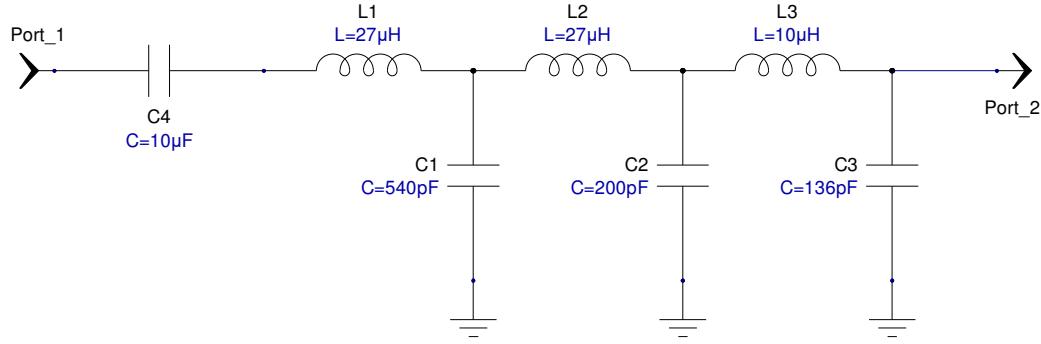
The differential output resistance of the demodulator is 50 [W]. This means a single ended 25 Ohm resistance. [50  $\Omega$  differential output impedance (25  $\Omega$  per pin) as stated in the datasheet].

The limiting amplifir has a high input resistance. A shunt resistance should be placed at each of its two differential input ports.

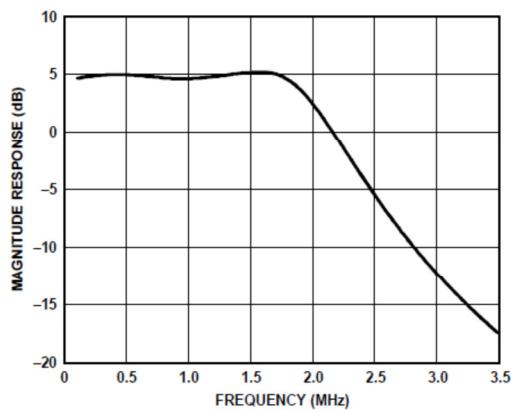


**Figure 56. The MAX3747A input circuit**

The filter reported in Figure 53 above has been simulated with the results shown below.

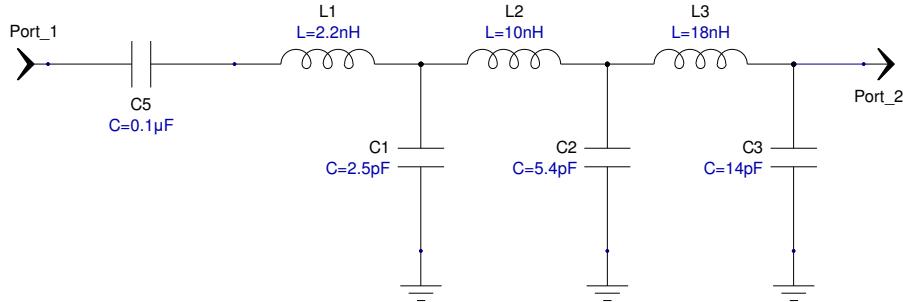


**Figure 57a. Simulation of the single-ended equivalent LPF**

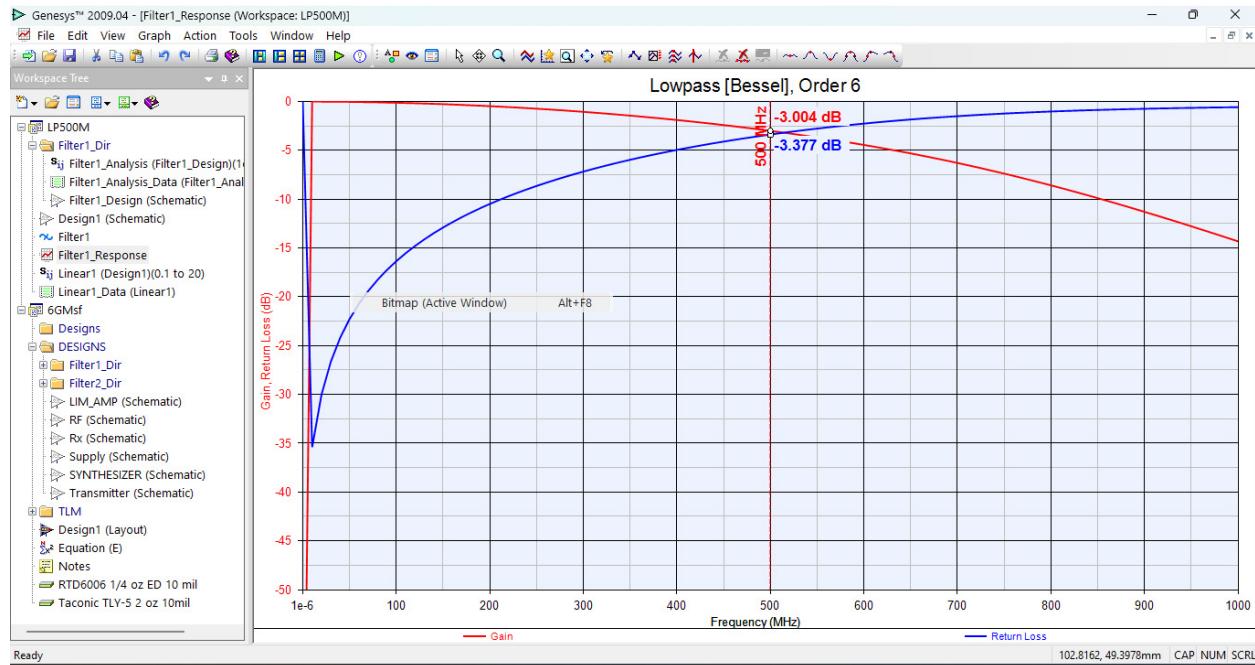


**Figure 57b. Simulation of the same LPF by AD**

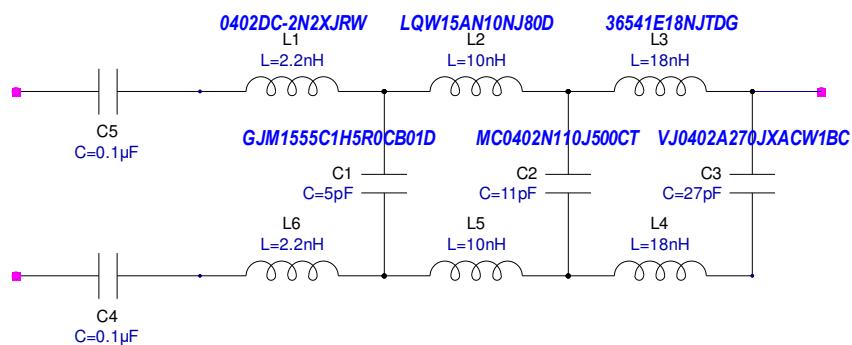
Let us design a single ended elliptic LPF with  $25 \text{ } [\Omega]$  input impedance,  $50 \text{ } [\Omega]$  output impedance and 500 MHz cut-off frequency. At the LPF input the  $0.1[\mu\text{F}]$  coupling capacitor has been inserted as required.



**Figure 58a. The elliptic 500MHz LPF**

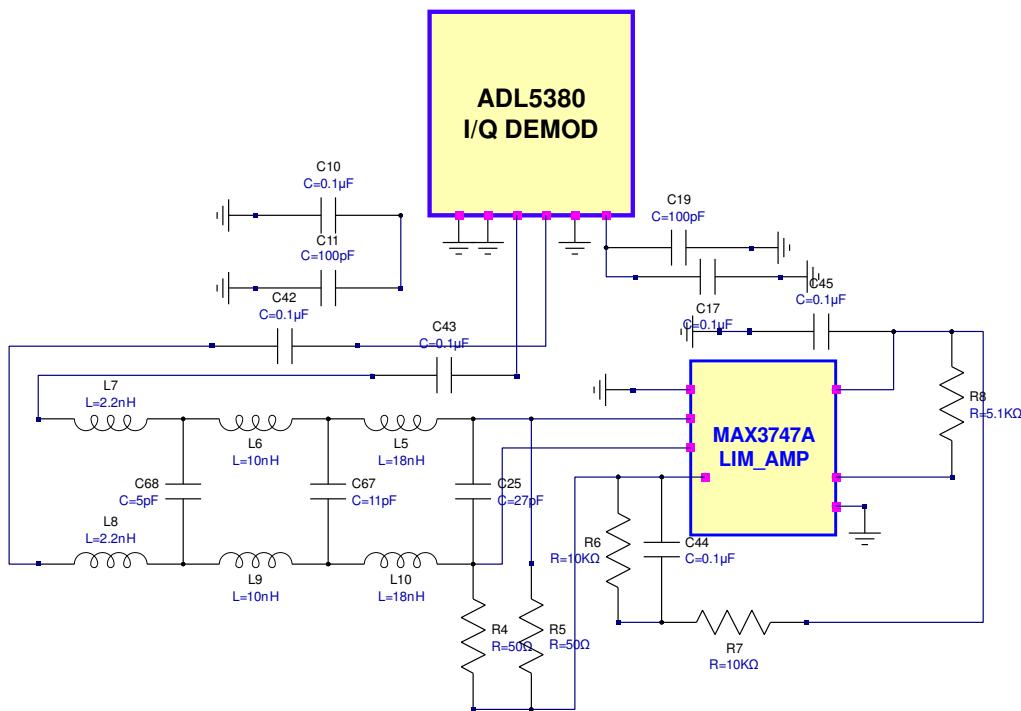


**Figure 58b. The elliptic 500MHz LPF frequency response**

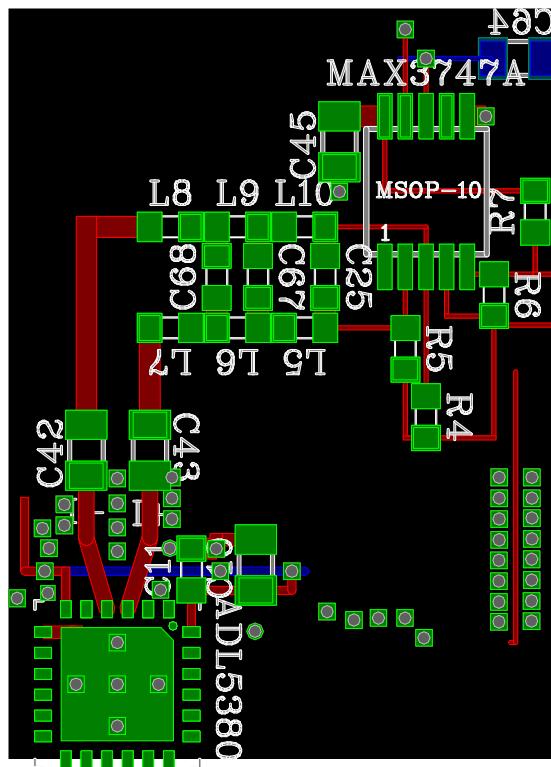


**Figure 59. The equivalent balanced LPF**

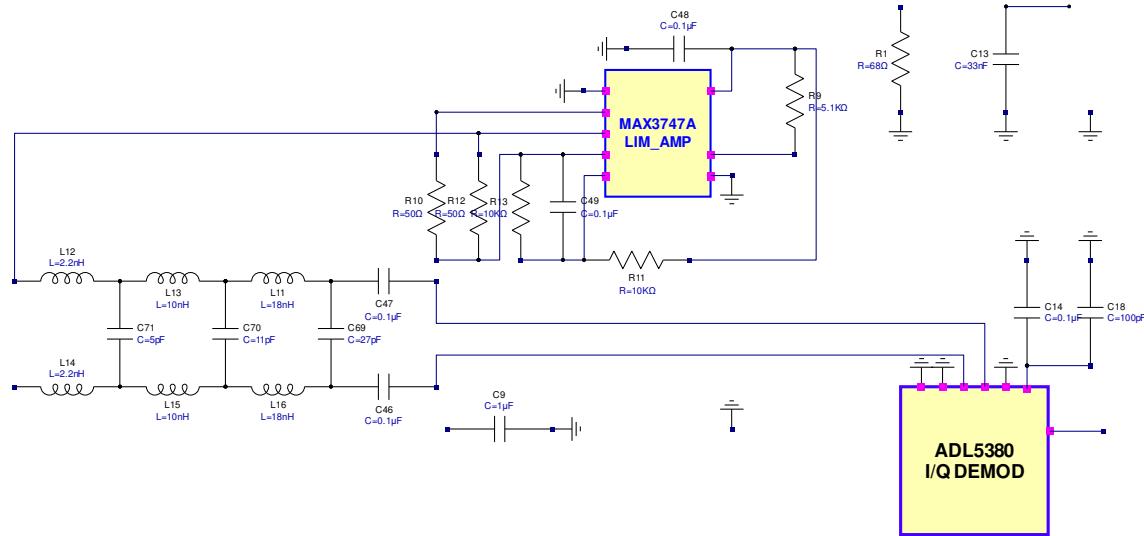
The following figure shows the connection of the new balanced LPF between the demodulator output and the limiting amplifier input.



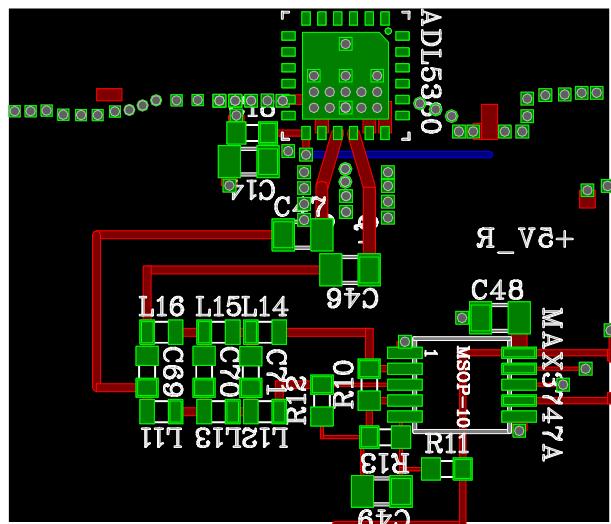
**Figure 60a. Connecting the differential LPF to the I limiting amplifier schematic**



**Figure 60b.** Connecting the differential LPF to the I limiting amplifier layout



**Figure 61a.** Connecting the differential LPF to the Q limiting amplifier schematic



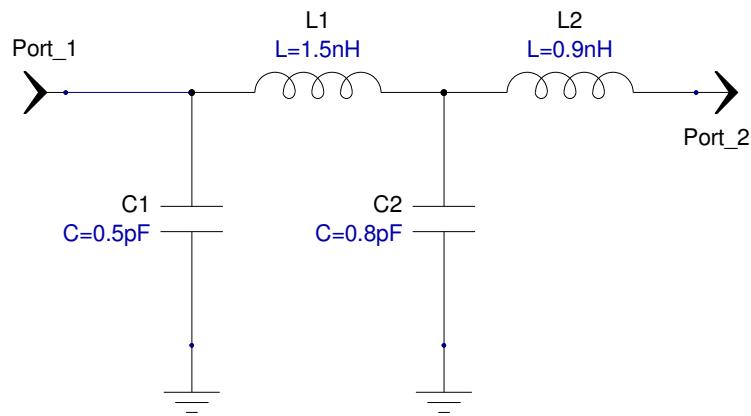
**Figure 61b.** Connecting the differential LPF to the Q limiting amplifier layout

### 11.3. RF LPF between the PLL and the Modulator

It is required to design a differential LPF between the PLL output and the modulator LO port. It should suppress the third harmonic at least by 20 dB in addition to the 10 dB already done by the VCO itself.

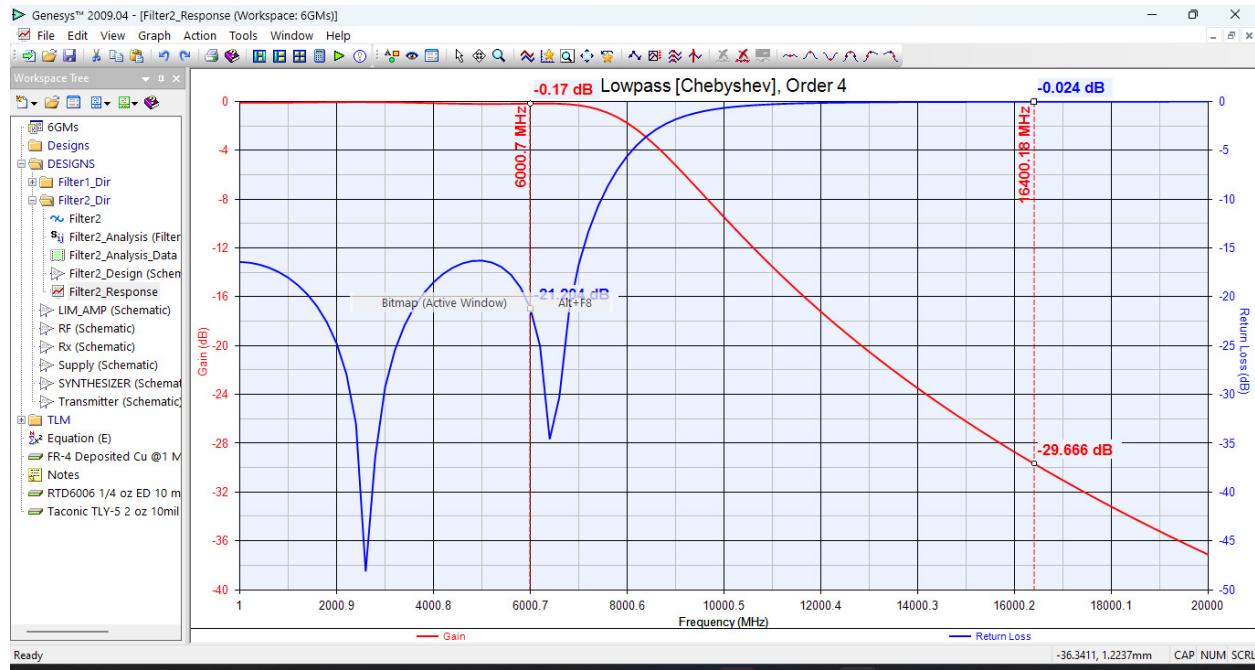
### 11.3.1. RF LPF Design

The following filter shows the 4<sup>th</sup> order minimum inductor Chebyshev LPF that has been designed.



**Figure 56.** The 4<sup>th</sup> order Chebyshev LPF

The optimized frequency response of this LPF is shown in the following figure.

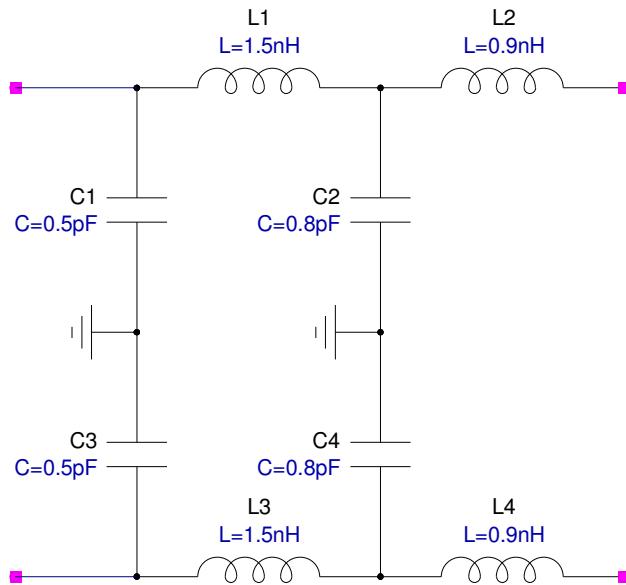


**Figure 57. The 4<sup>th</sup> order Chebyshev LPF response**

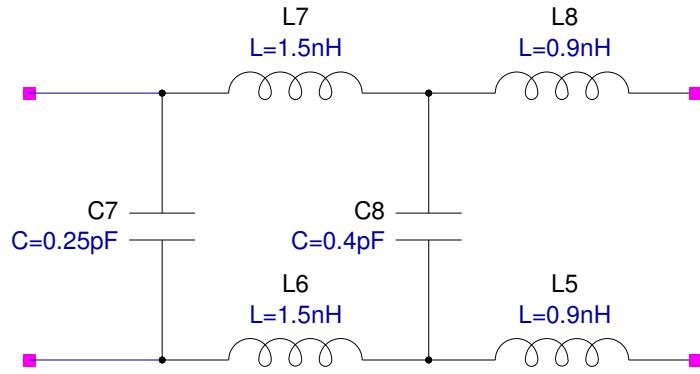
It can be clearly seen that the third harmonic of a 5.5 GHz signal is suppressed by more than 29 dB.

### 11.3.2. Differential LPF induction

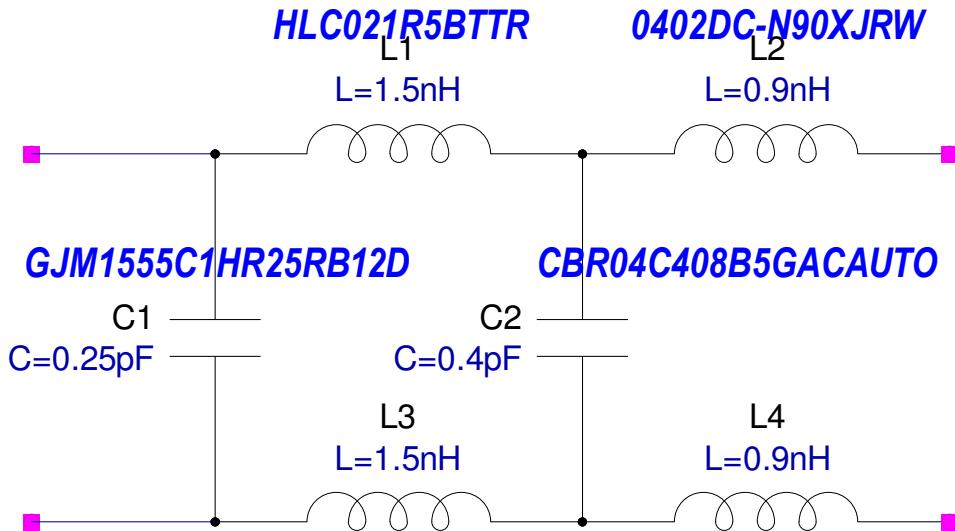
A differential LPF can be induced from the LPF design as shown in the following figure.



**Figure 58a. First step of differential LPF induction**



**Figure 58b. Second step of differential LPF induction**

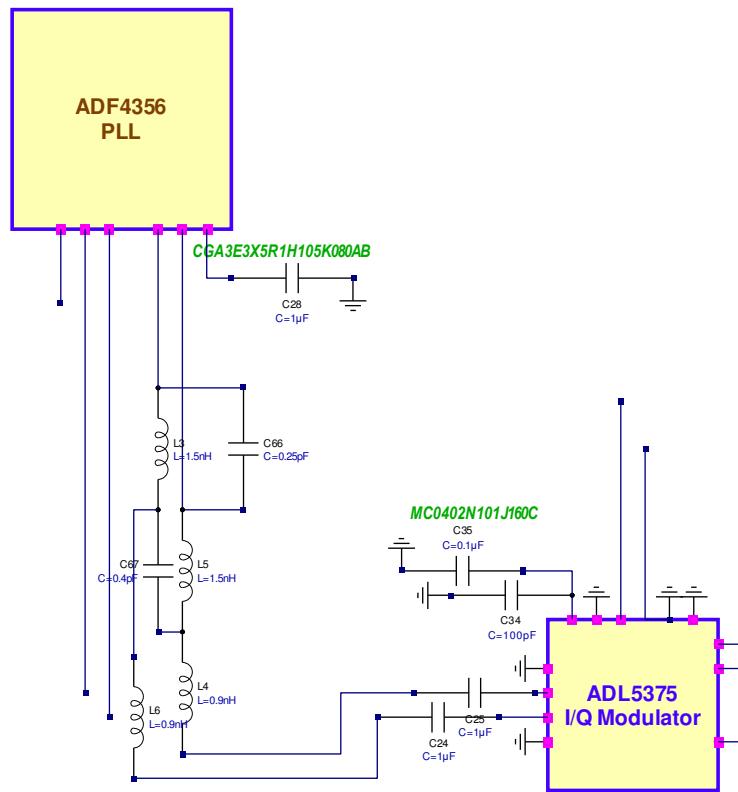


**Figure 58c. The differential LPF Schematic**

The part number of each component is written on the schematic drawing.

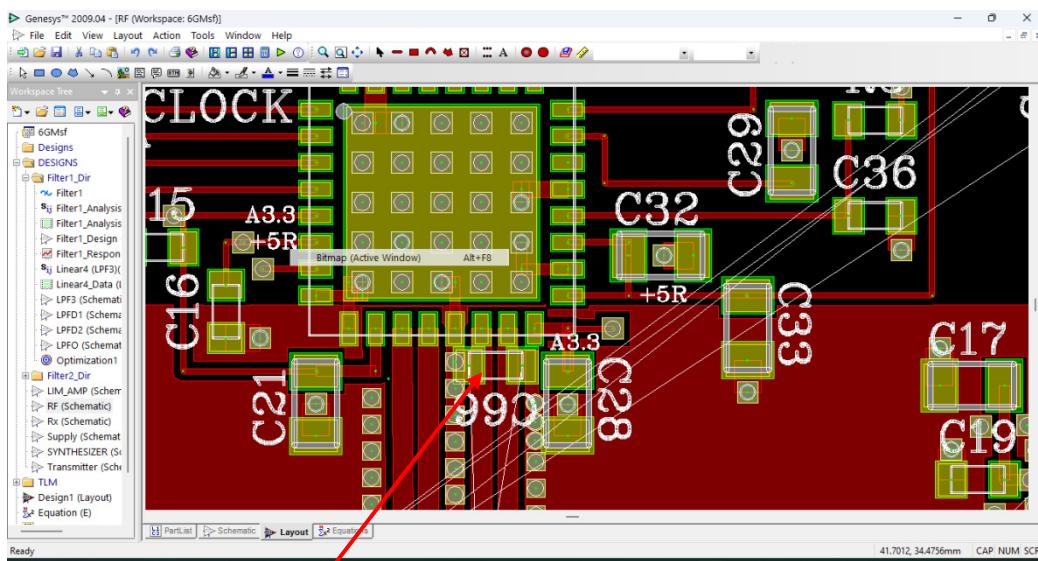
### 11.3.3. Inserting the differential LPF in the RF Assembly schematic

This is shown in the following figure.



**Figure 59. Inserting the differential LPF in the RF Assembly schematic**

#### 11.3.4. Inserting the differential LPF in the RF Assembly layout



**Figure 60. Inserting the C0402 shunt filter capacitor between the two transmission lines**

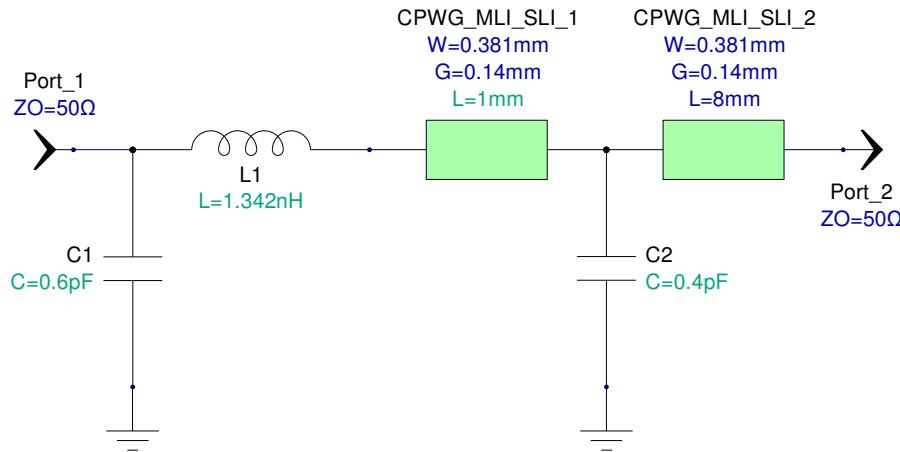
Trying to insert the 0.25pF shunt capacitor between the two GBCPWG transmission lines at the ADF4356 PLL synthesizer, it is clear that it would short circuit with the ground pin at its left and with the supply pin at its right.

Therefore, a C0402 capacitor cannot be inserted in this place.

There is no 0.25pF with the C0201 package.

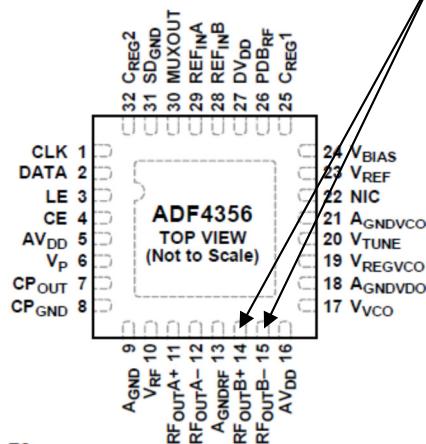
It was not possible to optimize the LPF with existing values of C0201 capacitors.

I have followed another approach. I have simulated the entire circuit including the GBCPWG transmission lines and the LPF elements. The simulation model is shown in the following figure.



**Figure 61. A modified LPF for the 5.5 GHz LO signal**

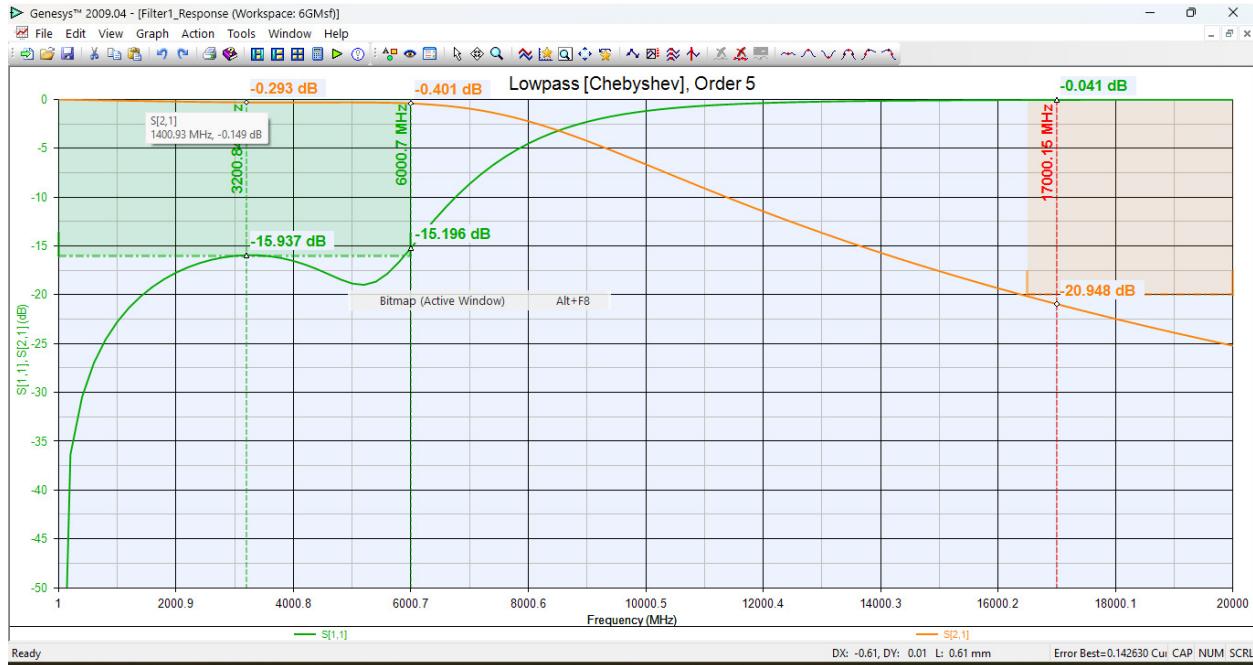
A shunt C0201 capacitor is inserted between the two RF output pins of the ADF4356.



**Figure 62. The ADF4356**

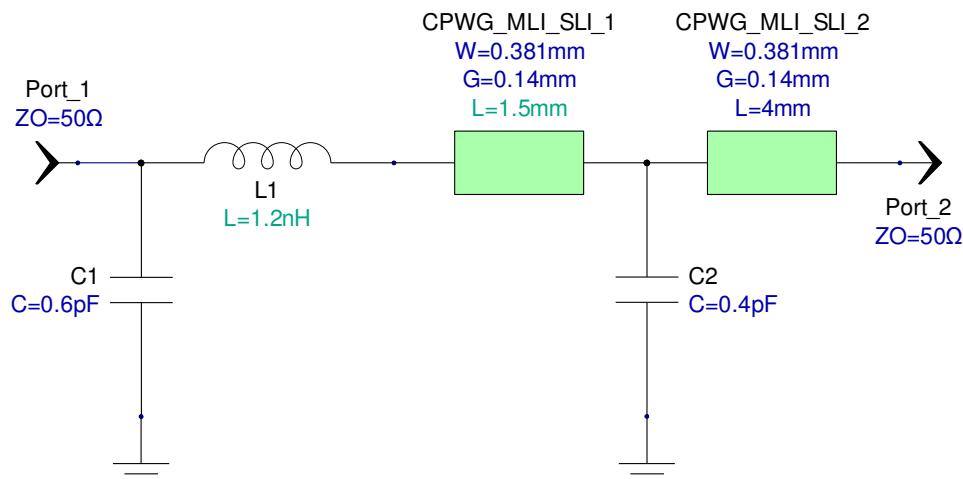
The length of a C0201 capacitor is 0.6mm, while the pin separation is 0.5mm.

While forcing the first shunt capacitor value to 0.3pF, a value existing with the C0201 package, the other circuit parameters have been changed by the optimizer to get the desired filter performance. The optimization results are shown in the following figure.

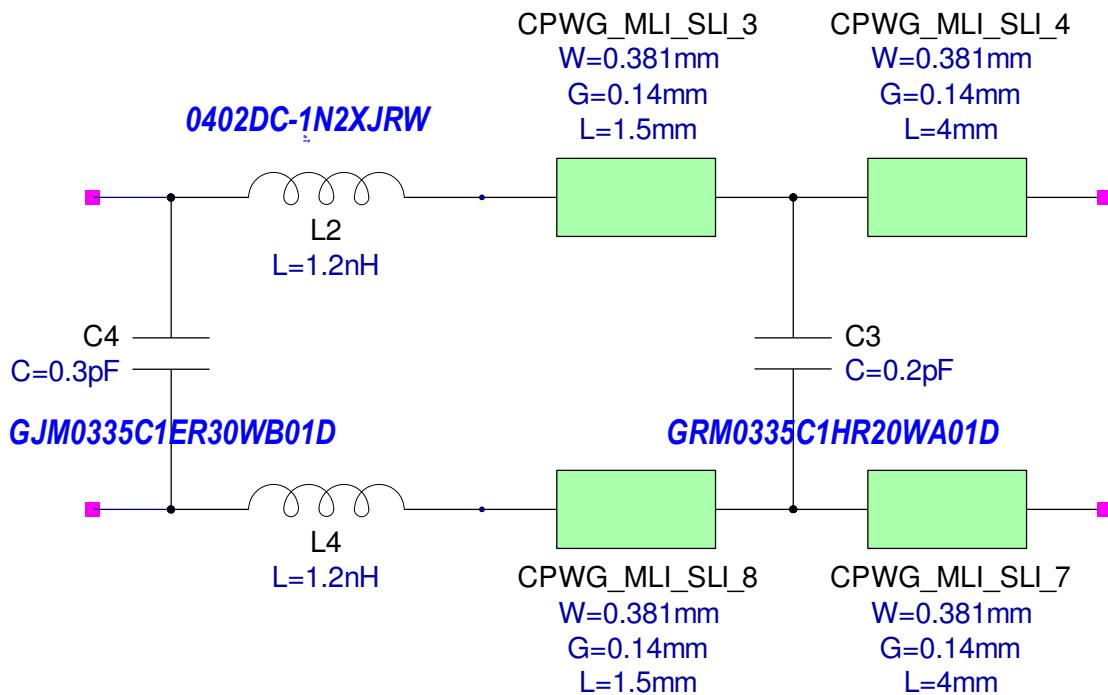


**Figure 63. Optimized frequency response of the LPF shown in the last figure**

It was found that a 1.5mm of the transmission line after the first section of the filter gives the best possible performance, while the TL length after the filter does not affect the frequency response. The optimized LPF and the corresponding differential LPF are shown in the following figure.



**Figure 64a. The optimized LPF**



**Figure 64. The differential LPF tp be inserted between the PLL and the modulator**

We shall use the [0402DC-1N2XJRW](#) inductor that has a 25 GHz self resonance frequency and  $Q > 27$  at 900 MHz.

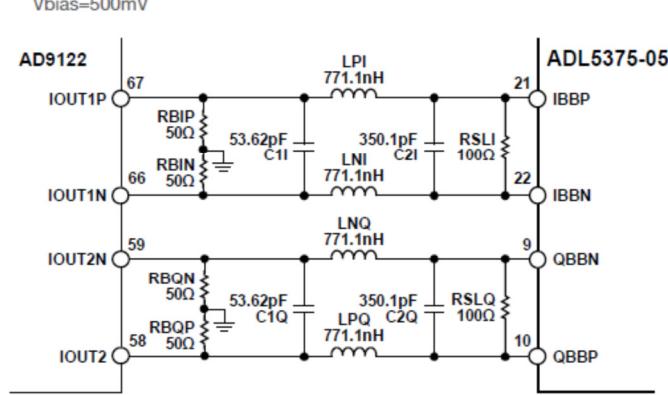
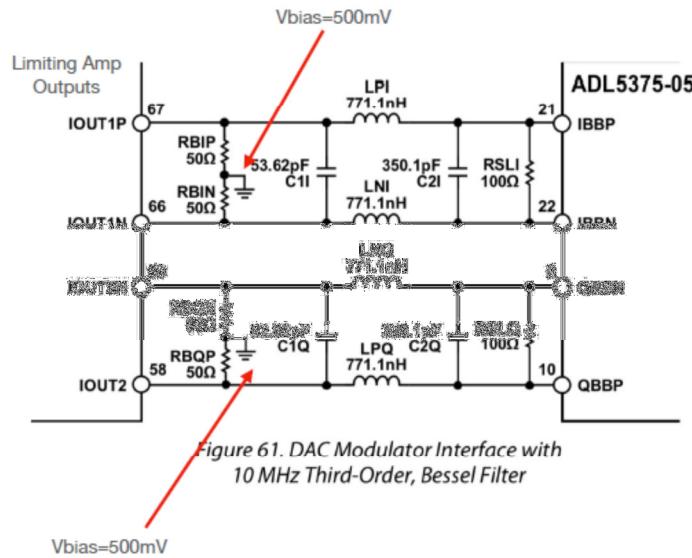
For the two capacitors we have selected the [GRM0335C1HR20WA01D](#) and the [GJM0335C1ER30WB01D](#).

## 11.4. Tx Up-converter Data Input Filters

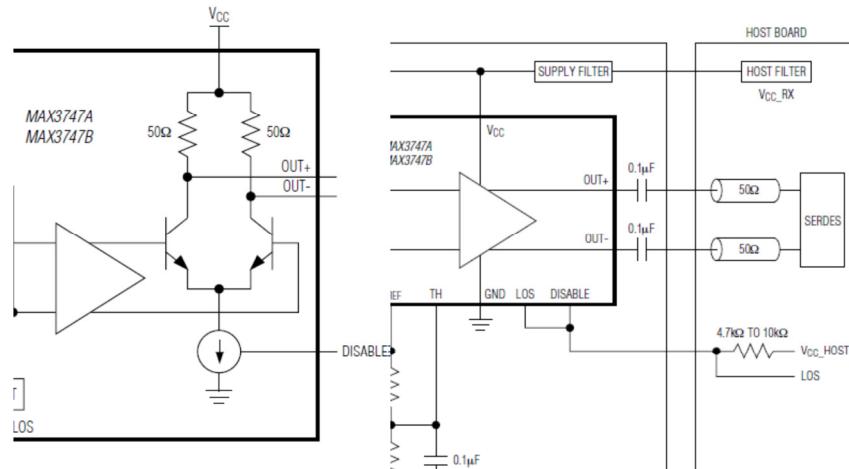
The following figure shows the balanced filter proposed by the manufacturer and by the project owner.

In this figure, 50 [ $\Omega$ ] resistors are inserted between each output port of the DAC; since the AD9122 DAC has a large output resistance.

Using the MAX3747A limiting amplifier with 50 [ $\Omega$ ] output resistance, those two resistors are not required.



**Figure 65.** The proposed balanced filter for modulator input data signal



**Figure 66.** The MAX3747A output

## 11.5. Simulating the Single Ended LPF

A single-ended version of the proposed LPF is shown in the following figure.

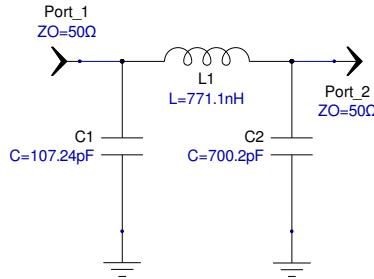


Figure 67. Single-ended LPF

Simulating this LPF we have got the frequency response shown in the following figure.

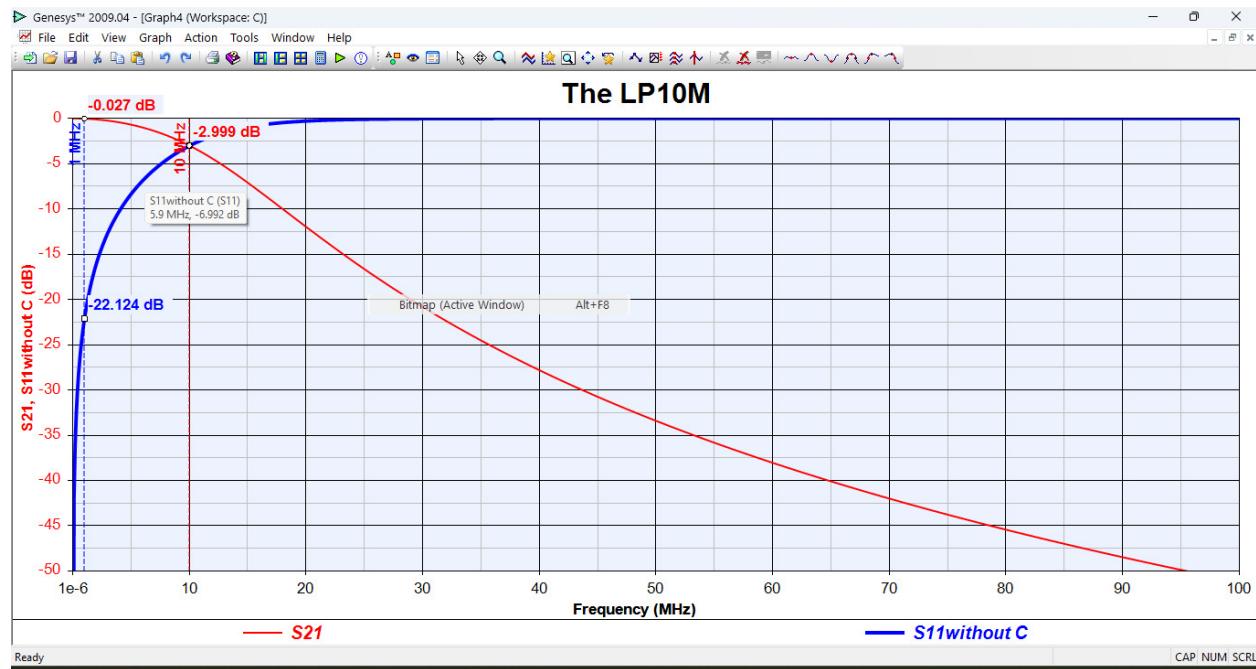
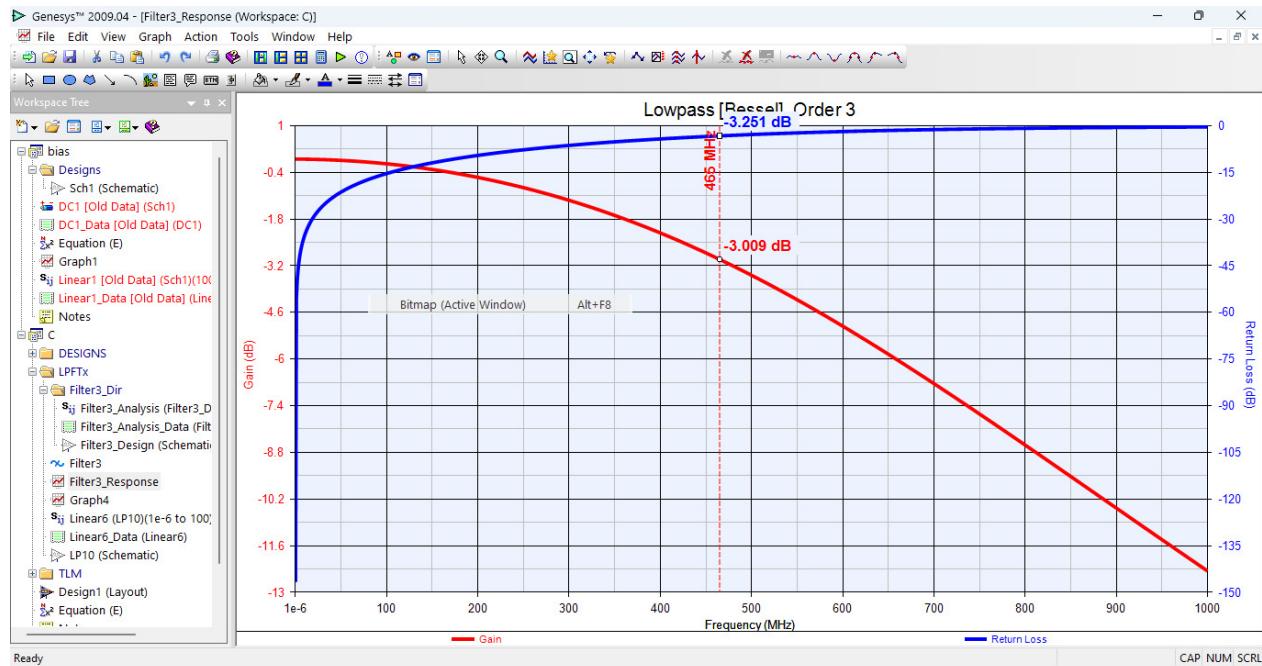
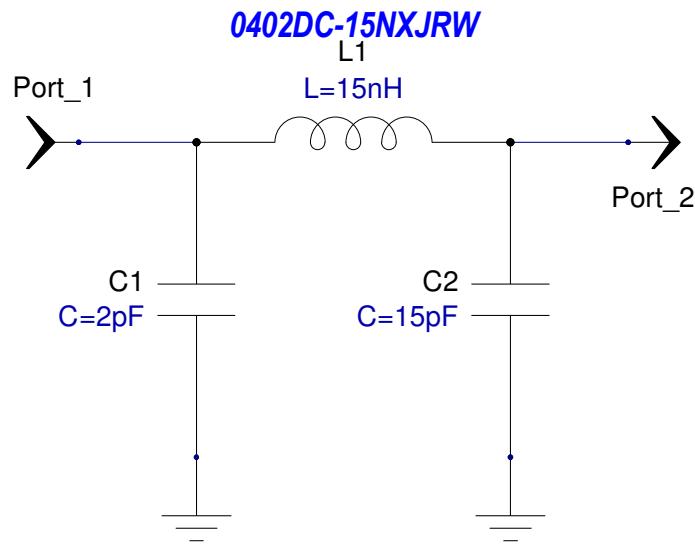


Figure 68. The LPF frequency response

It is a 10 MHz LPF.

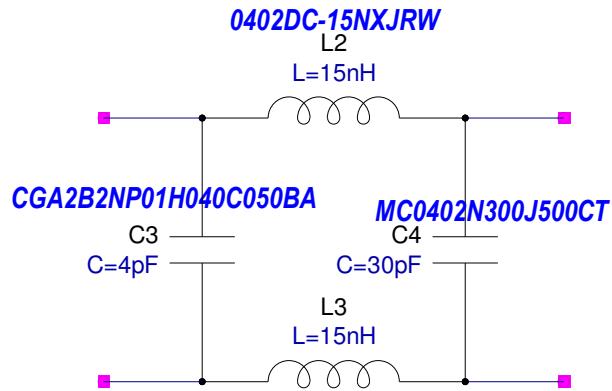
Given that the project owner uses a very high data rate and uses 500 MHz LPF in the receiver, I shall change this LPF to pass the same 500 MHz passband of the receiver.

A 500 MHz third order Bessel LPF design is shown in the following figure with its frequency response.



**Figure 69.** A 500MHz LPF design

The balanced version of this LPF is shown in the following figure.

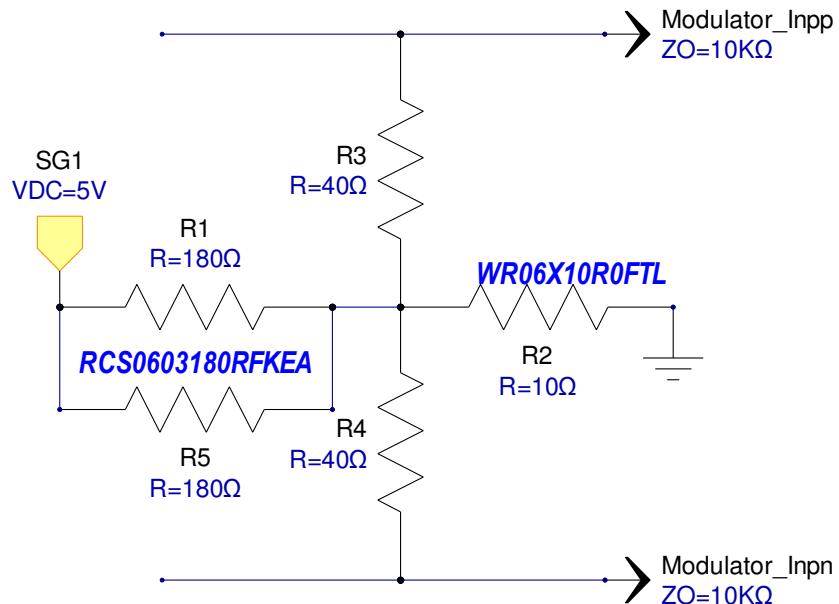


**Figure 70. The balanced 500MHz LPF for Tx data**

### 11.6. Biasing the ADLS375-05 Modulator data inputs

The [ADL5375-05](#) modulator needs an input bias level of 500 mV. Such a bias can be achieved by using a resistive voltage divider from the 5V power supply.

The voltage divider consumes 50 mA to give the required 500 mV bias at the central point of the circuit.



**Figure 65. Proposed bias circuit for the modulator data input ports**

We have used two 30 [ $\Omega$ ] resistors in parallel and two 69.8 [ $\Omega$ ] resistors in parallel to support the power consumption of the voltage divider.

The power consumption of the 90 [ $\Omega$ ] resistor can be estimated as follows:

$$\begin{aligned}
 P &= I^2 R \\
 &= (0.05)^2 \times 90 \\
 &= 0.225 \text{ [w].}
 \end{aligned}$$

We shall use two resistors in parallel, each with 180 [ $\Omega$ ] value and 0.25 [w] power rating.

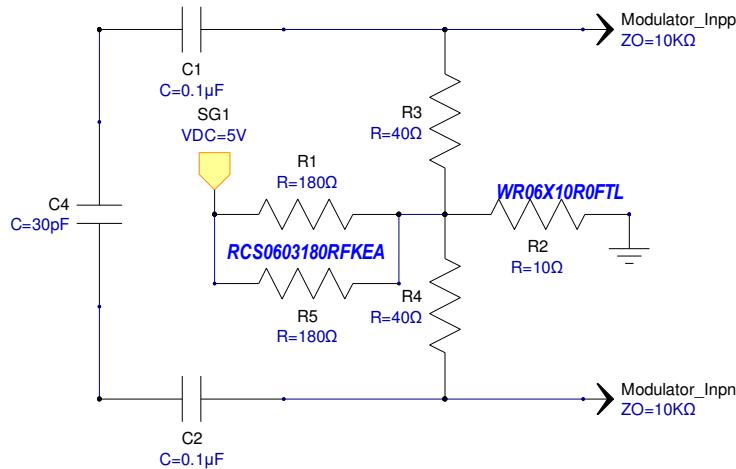
The power consumption of the 10 [ $\Omega$ ] resistor can be estimated as follows:

$$\begin{aligned}
 P &= I^2 R \\
 &= (0.05)^2 \times 10 \\
 &= 0.025 \text{ [w].}
 \end{aligned}$$

The two ports of the circuit are the differential I/Q input of the ADLS375-5 modulator. These two input ports of the modulator have high input resistance.

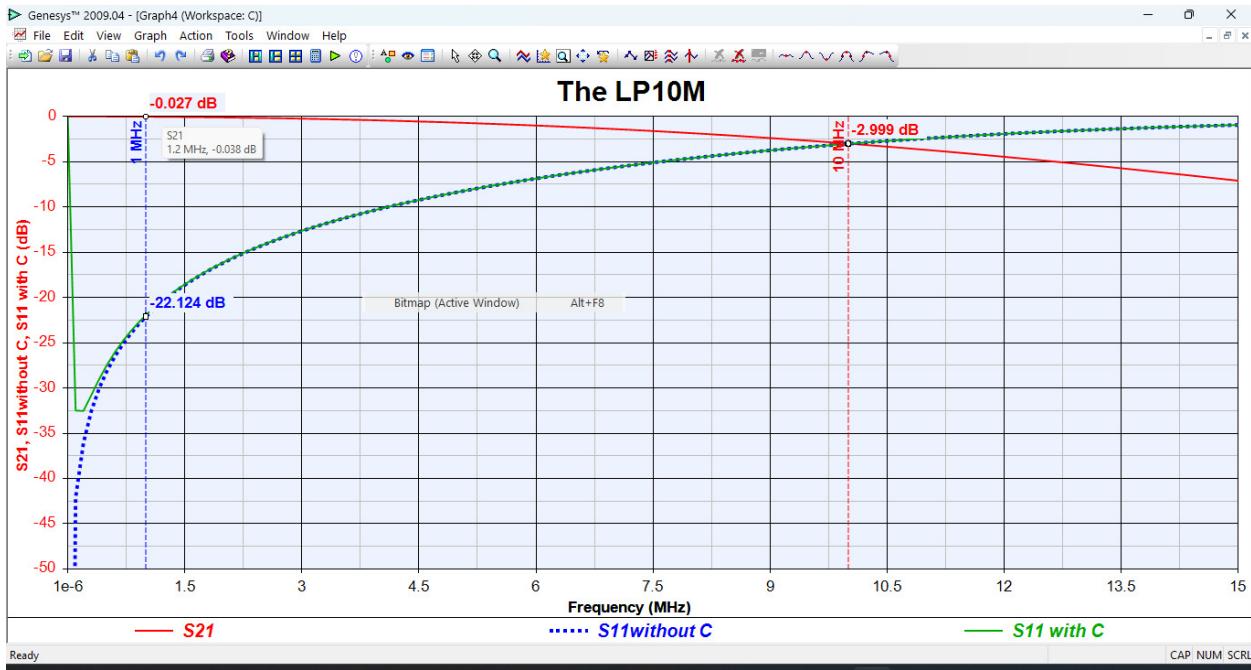
Looking from each of these two ports, the modulator will see 50 Ohms.

The bias circuit will be isolated from the differential data input ports (the differential LPF output) by two large capacitors as shown in the following figure.



**Figure 66. Isolating the modulator bias from the differential input data port**

Such a large capacitor will not affect the frequency response of the LPF. The LPF frequency response without and with the large capacitor are shown in the following figure.

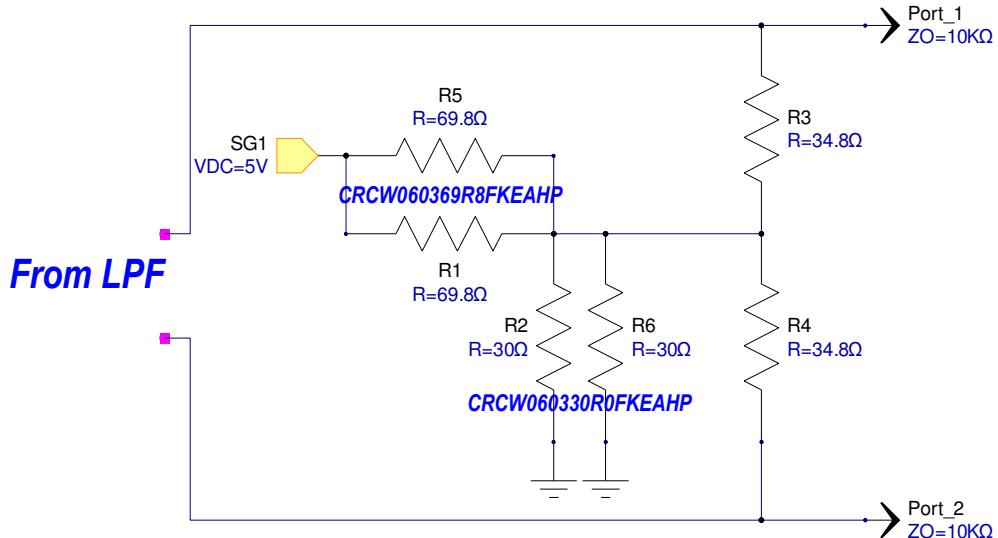


**Figure 67. Effect of large series capacitance on the LPF**

### 11.7. Biasing the ADLS375-15 Modulator data inputs

The **ADL5375-15** modulator needs an input bias level of 1.5 V. Such a bias can be achieved by using a resistive voltage divider from the 5V power supply.

The voltage divider should consume 100 mA to give the required 1500 mV bias at the central point of the circuit.



**Figure 68. Proposed bias circuit for the modulator data input ports**

We have used two  $30\ [\Omega]$  resistors in parallel and two  $69.8\ [\Omega]$  resistors in parallel to support the power consumption of the voltage divider.

This power consumption can be estimated as follows:

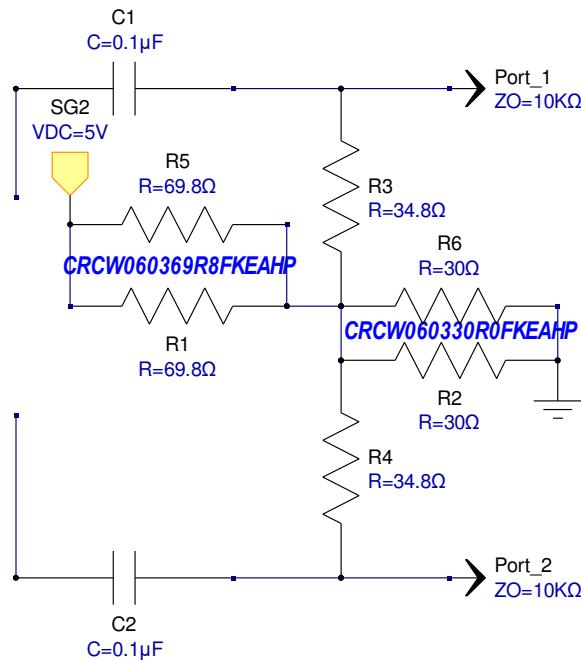
$$\begin{aligned} P &= I^2 R \\ &= (0.1)^2 \times 35 \\ &= 0.35 \text{ [w].} \end{aligned}$$

That is why we use two parallel resistors, each consuming  $170\ [\text{mw}]$ . All these resistors are 0603 size resistors.

The two ports of the circuit are the differential I/Q input of the ADLS375-15 modulator. These two input ports of the modulator have high input resistance.

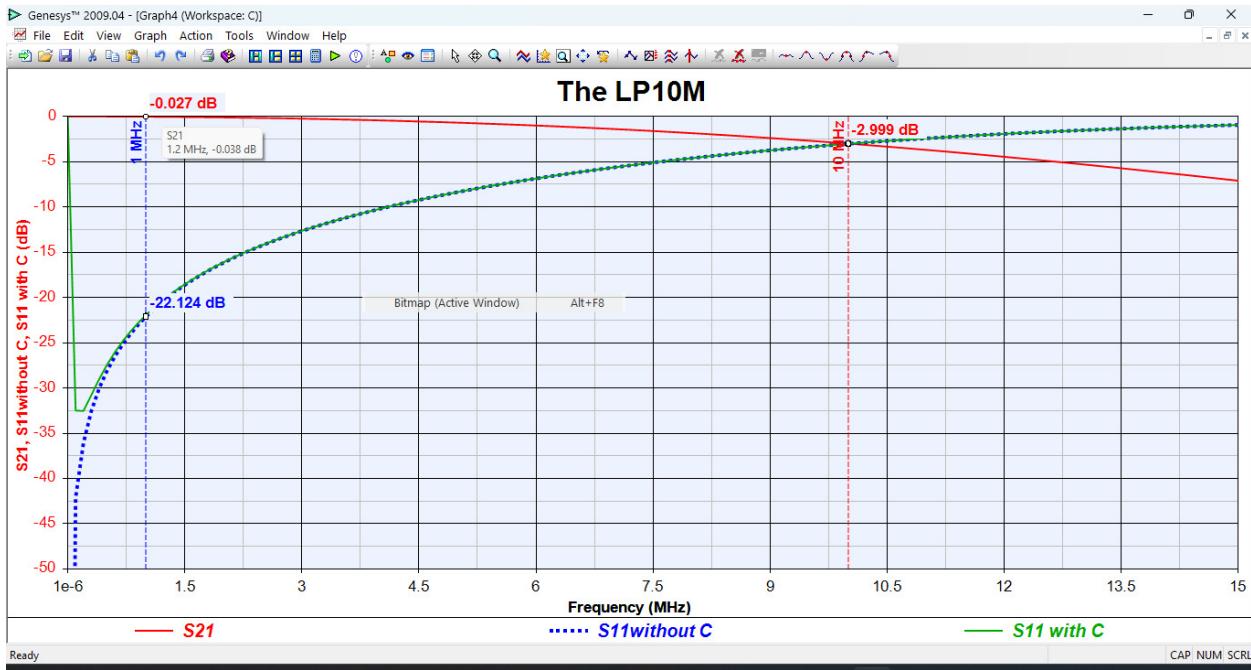
Looking from each of these two ports, the modulator should see  $50\ \Omega$ .

The bias circuit will be isolated from the differential data input ports (the differential LPF output) by two large capacitors as shown in the following figure.



**Figure 69. Isolating the modulator bias from the differential input data port**

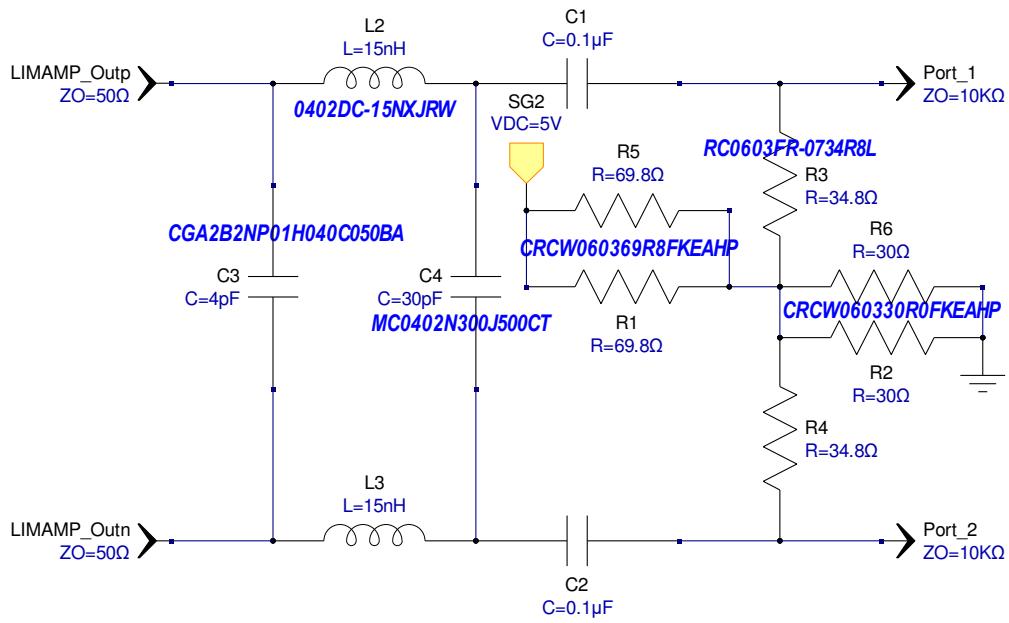
Such a large capacitor will not affect the frequency response of the LPF. The LPF frequency response without and with the large capacitor are shown in the following figure.



**Figure 70. Effect of large series capacitance on the LPF**

### 11.8. Inserting the LPF and bias at the modulator inputs

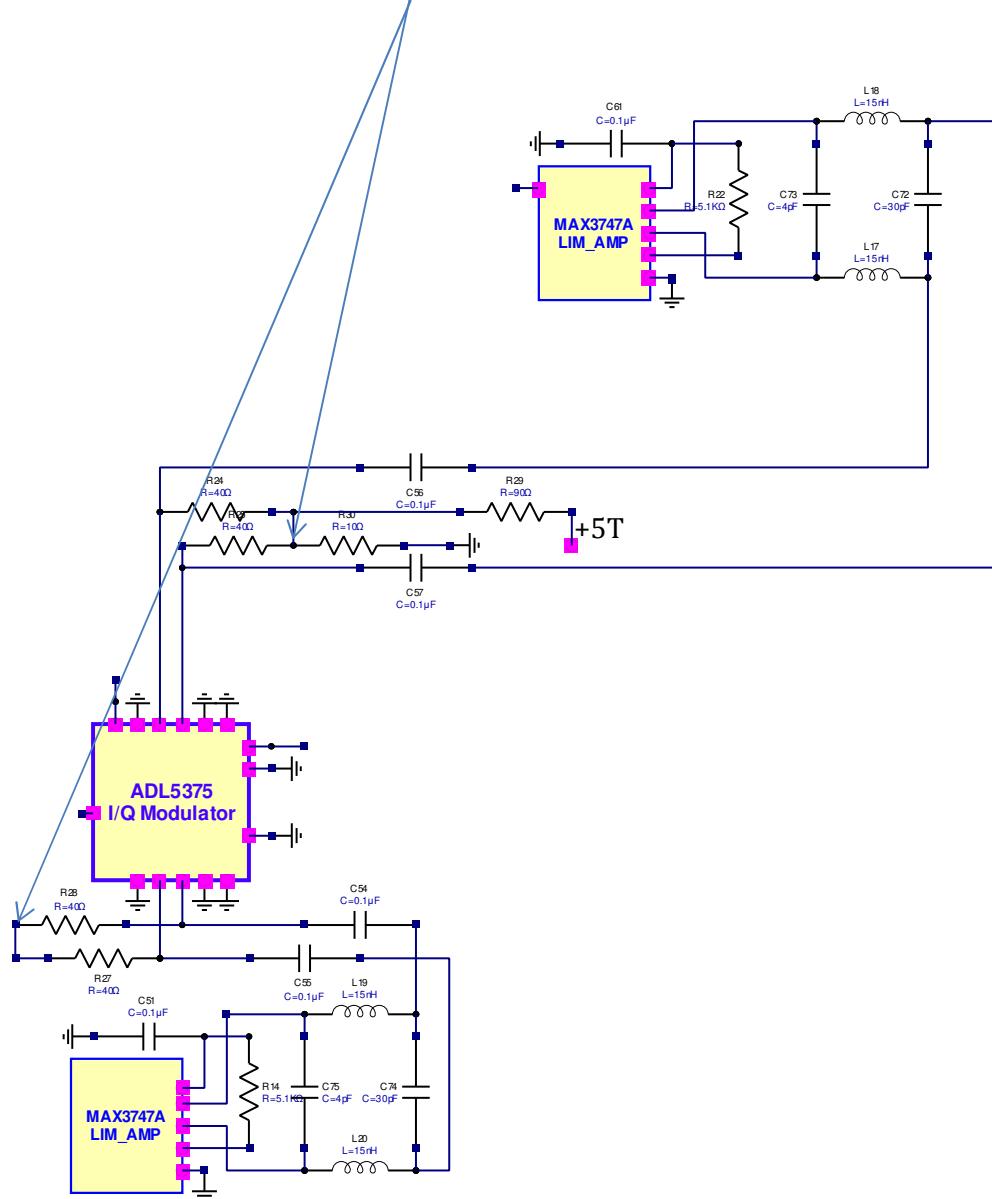
As recommended by the project owner, a differential LPF will be connected between the limiting amplifier and each modulator I/Q input. The 1500 mV bias will be inserted at the same input port. The 0.1  $\mu$ F DC blocking capacitors are inserted between the bias circuit and the I/Q input ports. The differential LPF-bias circuit combination will be as shown in the following figure.



**Figure 71. Differential LPF-Bias circuit combination**

The LPF will be duplicated, once for the I input and the other for the Q input, while only one bias circuit is needed. The 1500mV bias for the I and Q input ports will be taken from the same point.

The following figure shows the schematic design drawing for the I and Q interface circuits, including the differential LPFs and the Bias network.



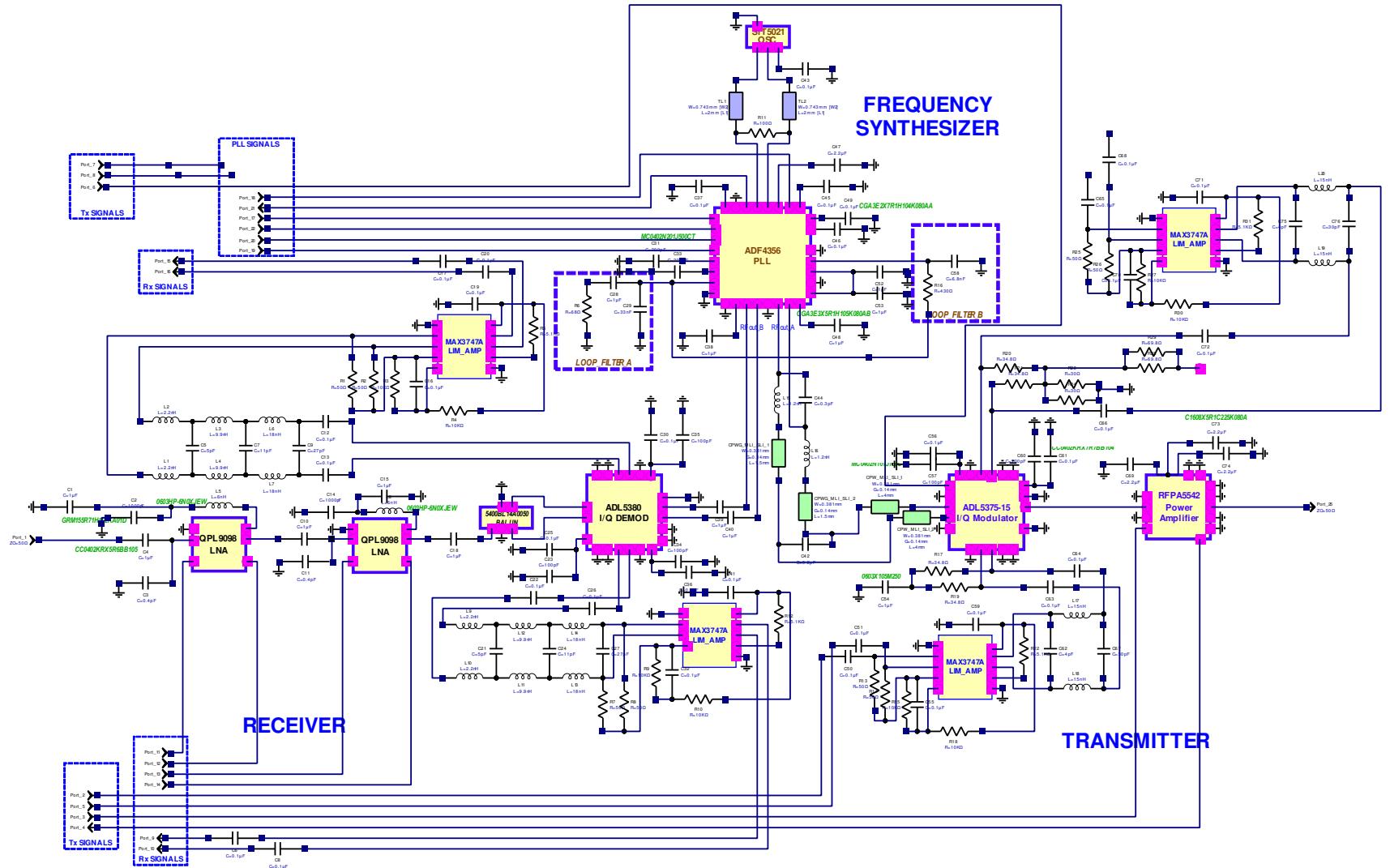


Figure 73a. Updated Schematic Design with ADL5375-15 Modulator

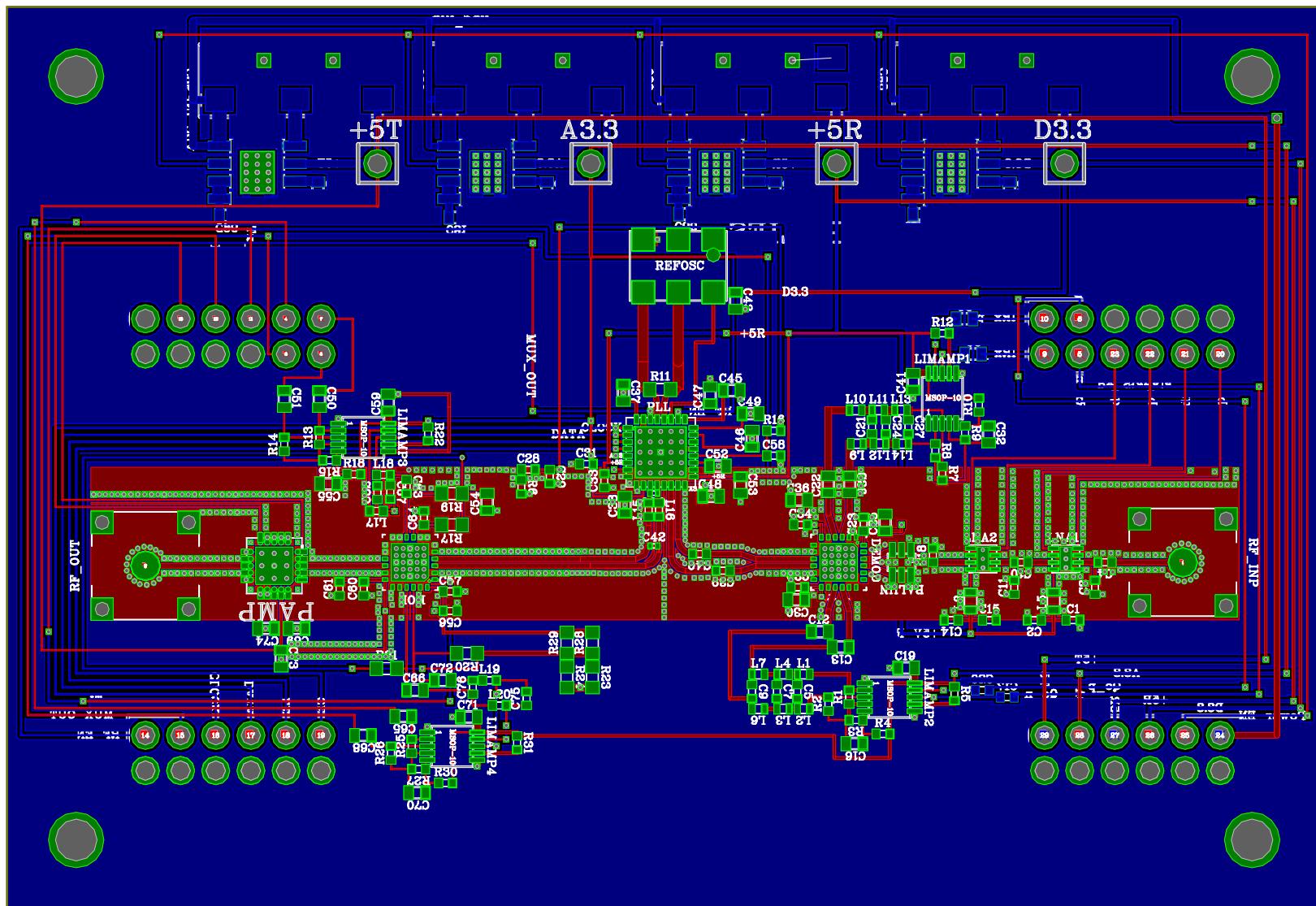


Figure 73b. Updated Layout Design with ADL5375-15 Modulator

## 12.2. BOM with ADL5375-15 Modulator

The following table shows the BOM for this design

**Bill of materials generated Sun Aug 13 15:36:08 2023**  
**Workspace: D:\1\_PROJECTS\1\_C\DESIGN\6GM15.wsx**

Package	Qty	Designators	Part Number	Manufacturer	Description
<hr/>					
DFN8	02	LNA1	QPL9098	Qorvo	Low noise amplifier
		LNA2	QPL9098	Qorvo	Low noise amplifier
<hr/>					
QFN32	01	PLL	ADF4356BCPZ	AD	PLL frequency synthesizer with VCO
<hr/>					
SOIC-8P	04	REG1	ADM7150ARDZ-3.3	AD	Voltage regulator
		REG2	ADM7150ARDZ-5.0	AD	Voltage regulator
		REG3	ADM7150ARDZ-3.3	AD	Voltage regulator
		REG4	ADM7150ARDZ-5.0	AD	Voltage regulator
<hr/>					
QFN24	02	DEMOD	ADL5380ACPZ-R7	AD	I/Q demodulator
		MOD	ADL5375-15ACPZ	AD	I/Q modulator

MSOP10	04	LIMAMP1	MAX3747A	AD (Maxim)	Limiting amplifier
		LIMAMP2	MAX3747A	AD (Maxim)	Limiting amplifier
		LIMAMP3	MAX3747A	AD (Maxim)	Limiting amplifier
		LIMAMP4	MAX3747A	AD (Maxim)	Limiting amplifier
SIT5	01	REFOSC	SIT5021AI-2DE-33E-100.000000X	SiTime	Reference Oscillator
BALUN	01	BALUN	5400BL14A0050	JOHANSON Tech.	1:1 BALUN Transformer
QFN20B	01	PAMP	RFPA5542SB	QORVO (RFMD)	RF Power Amplifier
R0603	09	R11[R=100]	CR0603-FX-1000ELF	Bourns	Chip Resistor
		R17[R=34.8]	RC0603FR-0734R8L	Yageo	Chip resistor
		R19[R=34.8]	RC0603FR-0734R8L	Yageo	Chip resistor
		R20[R=34.8]	RC0603FR-0734R8L	Yageo	Chip resistor
		R21[R=34.8]	RC0603FR-0734R8L	Yageo	Chip resistor
		R23[R=30]	CRCW060330R0FKEAHP	Vishay Dale	Chip resistor
		R24[R=30]	CRCW060330R0FKEAHP	Vishay Dale	Chip resistor
		R28[R=69.8]	CRCW060369R8FKEAHP	Vishay Dale	Chip resistor
		R29[R=69.8]	CRCW060369R8FKEAHP	Vishay Dale	Chip resistor

R0402	22	R1[R=50]	AC0402JR-0750RL	Yageo	Chip resistor
		R2[R=50]	AC0402JR-0750RL	Yageo	Chip resistor
		R3[R=10K]	RC0402JR-7W10KL	Yageo	Chip resistor
		R4[R=10K]	RC0402JR-7W10KL	Yageo	Chip resistor
		R5[R=5.1K]	CRCW04025K10FKEDHP	Vishay Dale	Chip Resistor
		R6[R=68]	ERJ2GEJ680X	Panasonic	Chip Resistor
		R7[R=50]	AC0402JR-0750RL	Yageo	Chip resistor
		R8[R=50]	AC0402JR-0750RL	Yageo	Chip resistor
		R9[R=10K]	RC0402JR-7W10KL	Yageo	Chip resistor
		R10[R=10K]	RC0402JR-7W10KL	Yageo	Chip resistor
		R12[R=5.1K]	CRCW04025K10FKEDHP	Vishay Dale	Chip Resistor
		R13[R=50]	AC0402JR-0750RL	Yageo	Chip resistor
		R14[R=50]	AC0402JR-0750RL	Yageo	Chip resistor
		R15[R=10K]	RC0402JR-7W10KL	Yageo	Chip resistor
		R16[R=430]	ERJ2RKF4300X	Panasonic	Chip Resistor
		R18[R=10K]	RC0402JR-7W10KL	Yageo	Chip resistor
		R22[R=5.1K]	CRCW04025K10FKEDHP	Vishay Dale	Chip Resistor
		R25[R=50]	AC0402JR-0750RL	Yageo	Chip resistor
		R26[R=50]	AC0402JR-0750RL	Yageo	Chip resistor
		R27[R=10K]	RC0402JR-7W10KL	Yageo	Chip resistor
		R30[R=10K]	RC0402JR-7W10KL	Yageo	Chip resistor

		R31[R=5.1K]	CRCW04025K10FKEDHP	Vishay Dale	Chip Resistor
L603	02	L5[L=6nH]	0603HP-6N0XJEW	Coilcraft	Chip Inductor
		L8[L=6nH]	0603HP-6N0XJEW	Coilcraft	Chip Inductor
L0402DC	18	L1[L=2.2nH]	0402DC-2N2XJRW	Coilcraft	Chip Inductor
		L2[L=2.2nH]	0402DC-2N2XJRW	Coilcraft	Chip Inductor
		L3[L=9.9nH]	0402DC-9N9XGRW	Coilcraft	Chip Inductor
		L4[L=9.9nH]	0402DC-9N9XGRW	Coilcraft	Chip Inductor
		L6[L=18nH]	0402DC-18NXJRW	Coilcraft	Chip Inductor
		L7[L=18nH]	0402DC-18NXJRW	Coilcraft	Chip Inductor
		L9[L=2.2nH]	0402DC-2N2XJRW	Coilcraft	Chip Inductor
		L10[L=2.2nH]	0402DC-2N2XJRW	Coilcraft	Chip Inductor
		L11[L=9.9nH]	0402DC-9N9XGRW	Coilcraft	Chip Inductor
		L12[L=9.9nH]	0402DC-9N9XGRW	Coilcraft	Chip Inductor
		L13[L=18nH]	0402DC-18NXJRW	Coilcraft	Chip Inductor
		L14[L=18nH]	0402DC-18NXJRW	Coilcraft	Chip Inductor
		L15[L=1.2nH]	0402DC-1N2XJRW	Coilcraft	Chip Inductor
		L16[L=1.2nH]	0402DC-1N2XJRW	Coilcraft	Chip Inductor
		L17[L=15nH]	0402DC-15NXJRW	Coilcraft	Chip Inductor
		L18[L=15nH]	0402DC-15NXJRW	Coilcraft	Chip Inductor

	L19[L=15nH]	0402DC-15NXJRW	Coilcraft	Chip Inductor
	L20[L=15nH]	0402DC-15NXJRW	Coilcraft	Chip Inductor
CC3216 [1206] 12	C77[C=10 uF]	1206X106K500CP	Walsin	Chip Capacitor
	C79[C=10 uF]	1206X106K500CP	Walsin	Chip Capacitor
	C80[C=10 uF]	1206X106K500CP	Walsin	Chip Capacitor
	C82[C=10 uF]	1206X106K500CP	Walsin	Chip Capacitor
	C84[C=10 uF]	1206X106K500CP	Walsin	Chip Capacitor
	C85[C=10 uF]	1206X106K500CP	Walsin	Chip Capacitor
	C87[C=10 uF]	1206X106K500CP	Walsin	Chip Capacitor
	C89[C=10 uF]	1206X106K500CP	Walsin	Chip Capacitor
	C90[C=10 uF]	1206X106K500CP	Walsin	Chip Capacitor
	C92[C=10 uF]	1206X106K500CP	Walsin	Chip Capacitor
	C94[C=10 uF]	1206X106K500CP	Walsin	Chip Capacitor
	C95[C=10 uF]	1206X106K500CP	Walsin	Chip Capacitor
C603 45	C6[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
	C8[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
	C12[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
	C13[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor

C16[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C19[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C22[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C25[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C26[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C30[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C32[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C36[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C37[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C38[C=1 uF]	CGA3E3X5R1H105K080AB	TDK	Chip Capacitor
C41[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C43[C=0.1F]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C45[C=0.1F]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C46[C=0.1F]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C47[C=2.2uF]	C1608X5R1C225K080A	TDK	Chip Capacitor
C48[C=1uF]	CGA3E3X5R1H105K080AB	TDK	Chip Capacitor
C49[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C50[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C51[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C52[C=1uF]	CGA3E3X5R1H105K080AB	TDK	Chip Capacitor
C53[C=1uF]	CGA3E3X5R1H105K080AB	TDK	Chip Capacitor

C54[C=1uF]	CGA3E3X5R1H105K080AB	TDK	Chip Capacitor
C55[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C59[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C65[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C66[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C68[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C69[C=2.2uF]	C1608X5R1C225K080A	TDK	Chip Capacitor
C70[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C71[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C72[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C73[C=2.2uF]	C1608X5R1C225K080A	TDK	Chip Capacitor
C74[C=2.2uF]	C1608X5R1C225K080A	TDK	Chip Capacitor
C78[C=1uF]	CGA3E3X5R1H105K080AB	TDK	Chip Capacitor
C81[C=1uF]	CGA3E3X5R1H105K080AB	TDK	Chip Capacitor
C83[C=1uF]	CGA3E3X5R1H105K080AB	TDK	Chip Capacitor
C86[C=1uF]	CGA3E3X5R1H105K080AB	TDK	Chip Capacitor
C88[C=1uF]	CGA3E3X5R1H105K080AB	TDK	Chip Capacitor
C91[C=1uF]	CGA3E3X5R1H105K080AB	TDK	Chip Capacitor
C93[C=1uF]	CGA3E3X5R1H105K080AB	TDK	Chip Capacitor
C96[C=1uF]	CGA3E3X5R1H105K080AB	TDK	Chip Capacitor

C0402	37	C1[C=1uF]	CC0402KRX5R6BB105	YAGEO	Chip Capacitor
		C2[C=1000pF]	GRM155R71H102KA01D	Murata	Chip Capacitor
		C3[C=0.4pF]	GJM1555C1HR50BB01E	Murata	Chip Capacitor
		C4[C=1 uF]	CC0402KRX5R6BB105	Yageo	Chip Capacitor
		C5[C=5pF]	CGA2B2C0G1H050C050BA	TDK	Chip Capacitor
		C7[C=11pF]	0402N110J500CT	Walsin	Chip Capacitor
		C9[C=27pF]	0402N270F500CT	Walsin	Chip Capacitor
		C10[C=1uF]	CC0402KRX5R6BB105	YAGEO	Chip Capacitor
		C11[C=0.4pF]	GJM1555C1HR50BB01E	Murata	Chip Capacitor
		C14[C=1000pF]	GRM155R71H102KA01D	Murata	Chip Capacitor
		C15[C=1uF]	CC0402KRX5R6BB105	YAGEO	Chip Capacitor
		C17[C=0.1uF]	CC0402KRX7R7BB104	YAGEO	Chip Capacitor
		C18[C=1uF]	CC0402KRX5R6BB105	YAGEO	Chip Capacitor
		C20[C=0.1uF]	CC0402KRX7R7BB104	YAGEO	Chip Capacitor
		C21[C=5pF]	CGA2B2C0G1H050C050BA	TDK	Chip Capacitor
		C23[C=100pF]	MC0402N101J160CT	Multicomp Pro	Chip Capacitor
		C24[C=11pF]	0402N110J500CT	Walsin	Chip Capacitor
		C27[C=27pF]	0402N270F500CT	Walsin	Chip Capacitor
		C28[C=1uF]	CC0402KRX5R6BB105	YAGEO	Chip Capacitor
		C29[C=33nF]	MC0402B333K250CT	Multicomp	Chip Capacitor
		C31[C=200pF]	C0402C201J5GAC7867	Kemet	Chip Capacitor

		C33[C=200pF]	C0402C201J5GAC7867	Kemet	Chip Capacitor
		C34[C=100pF]	MC0402N101J160CT	Multicomp Pro	Chip Capacitor
		C35[C=100pF]	MC0402N101J160CT	Multicomp Pro	Chip Capacitor
		C39[C=1uF]	CC0402KRX5R6BB105	YAGEO	Chip Capacitor
		C40[C=1uF]	CC0402KRX5R6BB105	YAGEO	Chip Capacitor
		C56[C=0.1uF]	CC0402KRX7R7BB104	YAGEO	Chip Capacitor
		C57[C=100pF]	MC0402N101J160CT	Multicomp Pro	Chip Capacitor
		C58[C=6.8nF]	MC0402B682K500CT	Multicomp	Chip Capacitor
		C60[C=100pF]	MC0402N101J160CT	Multicomp Pro	Chip Capacitor
		C61[C=0.1uF]	CC0402KRX7R7BB104	YAGEO	Chip Capacitor
		C62[C=4pF]	GCM1555C1H4R0BA16D	Murata	Chip Capacitor
		C63[C=0.1uF]	CC0402KRX7R7BB104	YAGEO	Chip Capacitor
		C64[C=0.1uF]	CC0402KRX7R7BB104	YAGEO	Chip Capacitor
		C67[C=30pF]	0402N300J500CT	Walsin	Chip Capacitor
		C75[C=4pF]	GCM1555C1H4R0BA16D	Murata	Chip Capacitor
		C76[C=30pF]	0402N300J500CT	Walsin	Chip Capacitor
C0201	02	C42[C=0.2pF]	GRM0335C1HR20BA01D	Murata	Chip Capacitor
		C44[C=0.3pF]	GRM0335C1HR30BA01D	Murata	Chip Capacitor
sma	03	RF_INP	132134-10	Amphenol	sma Connector

		RF_OUT	132134-10	Amphenol	sma Connector
POST2x6	04	Rx_Signals	612006235121	Wurth Electronik	Pin Header
		PLL_SIGNALS	612006235121	Wurth Electronik	Pin Header
		Tx_Signals	612006235121	Wurth Electronik	Pin Header
		POWER_SUPP.	612006235121	Wurth Electronik	Pin Header
POST1x1	04	A3.3	TS-104-T-AA	Samtec	Pin Header
		+5T	TS-104-T-AA	Samtec	Pin Header
		+5R	TS-104-T-AA	Samtec	Pin Header
		D3.3	TS-104-T-AA	Samtec	Pin Header

### 12.3. Design with ADL5375-05 Modulator

The following figure shows the updated schematic and layout design with ADL5375-05 modulator. The bias is adjusted at 0.5 V.

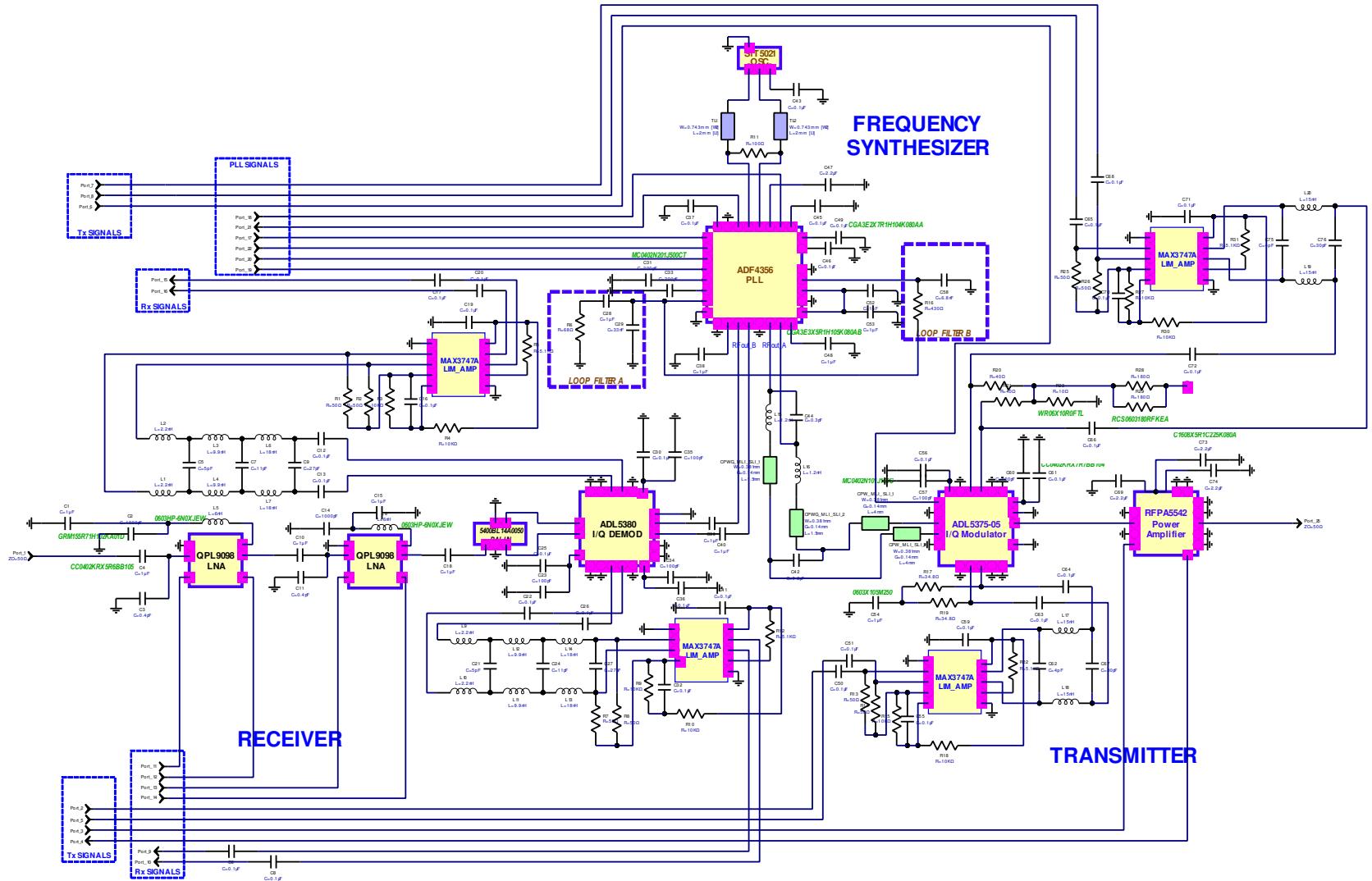
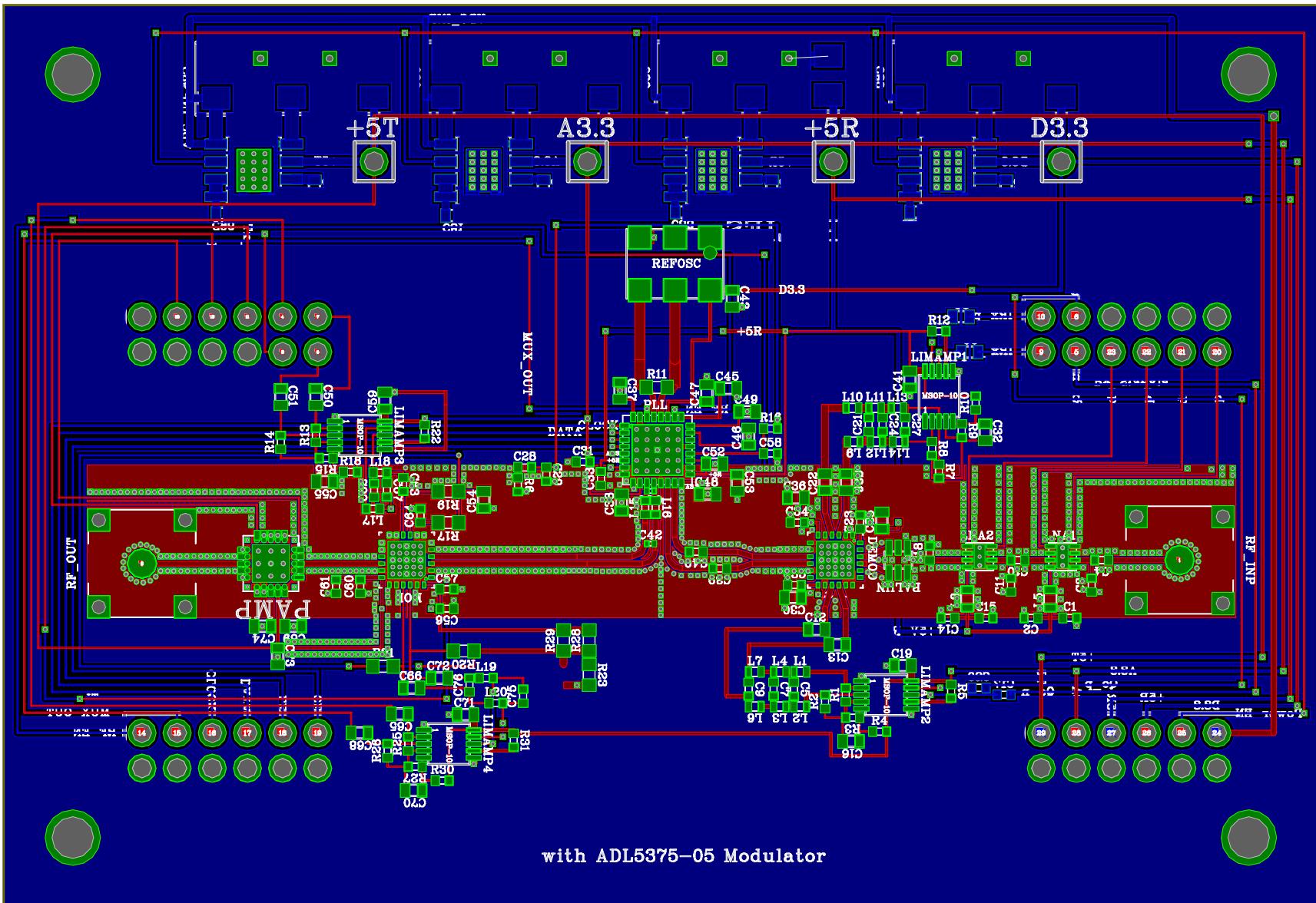


Figure 74a. Updated Schematic Design with ADL5375-05 Modulator



**Figure 74b. Updated Layout Design with ADL5375-05 Modulator**

## 12.4. BOM with ADL5375-05 Modulator

The following table shows the BOM for this design

**Bill of materials generated Sun Aug 13 15:36:08 2023**

**Workspace: D:\1\_PROJECTS\1\_C\DESIGN\6GM15.wsx**

Package	Qty	Designators	Part Number	Manufacturer	Description
<hr/>					
DFN8	02	LNA1	QPL9098	Qorvo	Low noise amplifier
		LNA2	QPL9098	Qorvo	Low noise amplifier
<hr/>					
QFN32	01	PLL	ADF4356BCPZ	AD	PLL frequency synthesizer with VCO
<hr/>					
SOIC-8P	04	REG1	ADM7150ARDZ-3.3	AD	Voltage regulator
		REG2	ADM7150ARDZ-5.0	AD	Voltage regulator
		REG3	ADM7150ARDZ-3.3	AD	Voltage regulator
		REG4	ADM7150ARDZ-5.0	AD	Voltage regulator
<hr/>					
QFN24	02	DEMOD	ADL5380ACPZ-R7	AD	I/Q demodulator
		MOD	ADL5375-15ACPZ	AD	I/Q modulator

MSOP10	04	LIMAMP1	MAX3747A	AD (Maxim)	Limiting amplifier
		LIMAMP2	MAX3747A	AD (Maxim)	Limiting amplifier
		LIMAMP3	MAX3747A	AD (Maxim)	Limiting amplifier
		LIMAMP4	MAX3747A	AD (Maxim)	Limiting amplifier
SIT5	01	REFOSC	SIT5021AI-2DE-33E-100.000000X	SiTime	Reference Oscillator
BALUN	01	BALUN	5400BL14A0050	JOHANSON Technology	1:1 BALUN Transformer
QFN20B	01	PAMP	RFPA5542SB	QORVO (RFMD)	RF Power Amplifier
R0603	08	R11[R=100]	CR0603-FX-1000ELF	Bourns	Chip Resistor
		R17[R=34.8]	RC0603FR-0734R8L	Yageo	Chip resistor
		R19[R=34.8]	RC0603FR-0734R8L	Yageo	Chip resistor
		R20[R=34.8]	RC0603FR-0734R8L	Yageo	Chip resistor
		R21[R=34.8]	RC0603FR-0734R8L	Yageo	Chip resistor
		R23[R=10]	WR06X10R0FTL	Walsin	Chip resistor
		R28[R=180]	RCS0603180RFKEA	Vishay Dale	Chip resistor
		R29[R=180]	RCS0603180RFKEA	Vishay Dale	Chip resistor

R0402	22	R1[R=50]	AC0402JR-0750RL	Yageo	Chip resistor
		R2[R=50]	AC0402JR-0750RL	Yageo	Chip resistor
		R3[R=10K]	RC0402JR-7W10KL	Yageo	Chip resistor
		R4[R=10K]	RC0402JR-7W10KL	Yageo	Chip resistor
		R5[R=5.1K]	CRCW04025K10FKEDHP	Vishay Dale	Chip Resistor
		R6[R=68]	ERJ2GEJ680X	Panasonic	Chip Resistor
		R7[R=50]	AC0402JR-0750RL	Yageo	Chip resistor
		R8[R=50]	AC0402JR-0750RL	Yageo	Chip resistor
		R9[R=10K]	RC0402JR-7W10KL	Yageo	Chip resistor
		R10[R=10K]	RC0402JR-7W10KL	Yageo	Chip resistor
		R12[R=5.1K]	CRCW04025K10FKEDHP	Vishay Dale	Chip Resistor
		R13[R=50]	AC0402JR-0750RL	Yageo	Chip resistor
		R14[R=50]	AC0402JR-0750RL	Yageo	Chip resistor
		R15[R=10K]	RC0402JR-7W10KL	Yageo	Chip resistor
		R16[R=430]	ERJ2RKF4300X	Panasonic	Chip Resistor
		R18[R=10K]	RC0402JR-7W10KL	Yageo	Chip resistor
		R22[R=5.1K]	CRCW04025K10FKEDHP	Vishay Dale	Chip Resistor
		R25[R=50]	AC0402JR-0750RL	Yageo	Chip resistor
		R26[R=50]	AC0402JR-0750RL	Yageo	Chip resistor
		R27[R=10K]	RC0402JR-7W10KL	Yageo	Chip resistor
		R30[R=10K]	RC0402JR-7W10KL	Yageo	Chip resistor

		R31[R=5.1K]	CRCW04025K10FKEDHP	Vishay Dale	Chip Resistor
L603	02	L5[L=6nH]	0603HP-6N0XJEW	Coilcraft	Chip Inductor
		L8[L=6nH]	0603HP-6N0XJEW	Coilcraft	Chip Inductor
L0402DC	18	L1[L=2.2nH]	0402DC-2N2XJRW	Coilcraft	Chip Inductor
		L2[L=2.2nH]	0402DC-2N2XJRW	Coilcraft	Chip Inductor
		L3[L=9.9nH]	0402DC-9N9XGRW	Coilcraft	Chip Inductor
		L4[L=9.9nH]	0402DC-9N9XGRW	Coilcraft	Chip Inductor
		L6[L=18nH]	0402DC-18NXJRW	Coilcraft	Chip Inductor
		L7[L=18nH]	0402DC-18NXJRW	Coilcraft	Chip Inductor
		L9[L=2.2nH]	0402DC-2N2XJRW	Coilcraft	Chip Inductor
		L10[L=2.2nH]	0402DC-2N2XJRW	Coilcraft	Chip Inductor
		L11[L=9.9nH]	0402DC-9N9XGRW	Coilcraft	Chip Inductor
		L12[L=9.9nH]	0402DC-9N9XGRW	Coilcraft	Chip Inductor
		L13[L=18nH]	0402DC-18NXJRW	Coilcraft	Chip Inductor
		L14[L=18nH]	0402DC-18NXJRW	Coilcraft	Chip Inductor
		L15[L=1.2nH]	0402DC-1N2XJRW	Coilcraft	Chip Inductor
		L16[L=1.2nH]	0402DC-1N2XJRW	Coilcraft	Chip Inductor
		L17[L=15nH]	0402DC-15NXJRW	Coilcraft	Chip Inductor
		L18[L=15nH]	0402DC-15NXJRW	Coilcraft	Chip Inductor

	L19[L=15nH]	0402DC-15NXJRW	Coilcraft	Chip Inductor
	L20[L=15nH]	0402DC-15NXJRW	Coilcraft	Chip Inductor
CC3216 [1206] 12	C77[C=10 uF]	1206X106K500CP	Walsin	Chip Capacitor
	C79[C=10 uF]	1206X106K500CP	Walsin	Chip Capacitor
	C80[C=10 uF]	1206X106K500CP	Walsin	Chip Capacitor
	C82[C=10 uF]	1206X106K500CP	Walsin	Chip Capacitor
	C84[C=10 uF]	1206X106K500CP	Walsin	Chip Capacitor
	C85[C=10 uF]	1206X106K500CP	Walsin	Chip Capacitor
	C87[C=10 uF]	1206X106K500CP	Walsin	Chip Capacitor
	C89[C=10 uF]	1206X106K500CP	Walsin	Chip Capacitor
	C90[C=10 uF]	1206X106K500CP	Walsin	Chip Capacitor
	C92[C=10 uF]	1206X106K500CP	Walsin	Chip Capacitor
	C94[C=10 uF]	1206X106K500CP	Walsin	Chip Capacitor
	C95[C=10 uF]	1206X106K500CP	Walsin	Chip Capacitor
C603 45	C6[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
	C8[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
	C12[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
	C13[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor

C16[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C19[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C22[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C25[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C26[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C30[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C32[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C36[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C37[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C38[C=1 uF]	CGA3E3X5R1H105K080AB	TDK	Chip Capacitor
C41[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	
C43[C=0.1F]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C45[C=0.1F]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C46[C=0.1F]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C47[C=2.2uF]	C1608X5R1C225K080A	TDK	Chip Capacitor
C48[C=1uF]	CGA3E3X5R1H105K080AB	TDK	Chip Capacitor
C49[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C50[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C51[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C52[C=1uF]	CGA3E3X5R1H105K080AB	TDK	Chip Capacitor
C53[C=1uF]	CGA3E3X5R1H105K080AB	TDK	Chip Capacitor

C54[C=1uF]	CGA3E3X5R1H105K080AB	TDK	Chip Capacitor
C55[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C59[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C65[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C66[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C68[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C69[C=2.2uF]	C1608X5R1C225K080A	TDK	Chip Capacitor
C70[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C71[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C72[C=0.1uF]	CGA3E2X7R1H104K080AA	TDK	Chip Capacitor
C73[C=2.2uF]	C1608X5R1C225K080A	TDK	Chip Capacitor
C74[C=2.2uF]	C1608X5R1C225K080A	TDK	Chip Capacitor
C78[C=1uF]	CGA3E3X5R1H105K080AB	TDK	Chip Capacitor
C81[C=1uF]	CGA3E3X5R1H105K080AB	TDK	Chip Capacitor
C83[C=1uF]	CGA3E3X5R1H105K080AB	TDK	Chip Capacitor
C86[C=1uF]	CGA3E3X5R1H105K080AB	TDK	Chip Capacitor
C88[C=1uF]	CGA3E3X5R1H105K080AB	TDK	Chip Capacitor
C91[C=1uF]	CGA3E3X5R1H105K080AB	TDK	Chip Capacitor
C93[C=1uF]	CGA3E3X5R1H105K080AB	TDK	Chip Capacitor
C96[C=1uF]	CGA3E3X5R1H105K080AB	TDK	Chip Capacitor

C0402	37	C1[C=1uF]	CC0402KRX5R6BB105	YAGEO	Chip Capacitor
		C2[C=1000pF]	GRM155R71H102KA01D	Murata	Chip Capacitor
		C3[C=0.4pF]	GJM1555C1HR50BB01E	Murata	Chip Capacitor
		C4[C=1 uF]	CC0402KRX5R6BB105	Yageo	Chip Capacitor
		C5[C=5pF]	CGA2B2C0G1H050C050BA	TDK	Chip Capacitor
		C7[C=11pF]	0402N110J500CT	Walsin	Chip Capacitor
		C9[C=27pF]	0402N270F500CT	Walsin	Chip Capacitor
		C10[C=1uF]	CC0402KRX5R6BB105	YAGEO	Chip Capacitor
		C11[C=0.4pF]	GJM1555C1HR50BB01E	Murata	Chip Capacitor
		C14[C=1000pF]	GRM155R71H102KA01D	Murata	Chip Capacitor
		C15[C=1uF]	CC0402KRX5R6BB105	YAGEO	Chip Capacitor
		C17[C=0.1uF]	CC0402KRX7R7BB104	YAGEO	Chip Capacitor
		C18[C=1uF]	CC0402KRX5R6BB105	YAGEO	Chip Capacitor
		C20[C=0.1uF]	CC0402KRX7R7BB104	YAGEO	Chip Capacitor
		C21[C=5pF]	CGA2B2C0G1H050C050BA	TDK	
		C23[C=100pF]	MC0402N101J160CT	Multicomp Pro	Chip Capacitor
		C24[C=11pF]	0402N110J500CT	Walsin	Chip Capacitor
		C27[C=27pF]	0402N270F500CT	Walsin	Chip Capacitor
		C28[C=1uF]	CC0402KRX5R6BB105	YAGEO	Chip Capacitor
		C29[C=33nF]	MC0402B333K250CT	Multicomp	Chip Capacitor
		C31[C=200pF]	C0402C201J5GAC7867	Kemet	Chip Capacitor

		C33[C=200pF]	C0402C201J5GAC7867	Kemet	Chip Capacitor
		C34[C=100pF]	MC0402N101J160CT	Multicomp Pro	Chip Capacitor
		C35[C=100pF]	MC0402N101J160CT	Multicomp Pro	Chip Capacitor
		C39[C=1uF]	CC0402KRX5R6BB105	YAGEO	Chip Capacitor
		C40[C=1uF]	CC0402KRX5R6BB105	YAGEO	Chip Capacitor
		C56[C=0.1uF]	CC0402KRX7R7BB104	YAGEO	Chip Capacitor
		C57[C=100pF]	MC0402N101J160CT	Multicomp Pro	Chip Capacitor
		C58[C=6.8nF]	MC0402B682K500CT	Multicomp	Chip Capacitor
		C60[C=100pF]	MC0402N101J160CT	Multicomp Pro	Chip Capacitor
		C61[C=0.1uF]	CC0402KRX7R7BB104	YAGEO	
		C62[C=4pF]	GCM1555C1H4R0BA16D	Murata	Chip Capacitor
		C63[C=0.1uF]	CC0402KRX7R7BB104	YAGEO	Chip Capacitor
		C64[C=0.1uF]	CC0402KRX7R7BB104	YAGEO	Chip Capacitor
		C67[C=30pF]	0402N300J500CT	Walsin	Chip Capacitor
		C75[C=4pF]	GCM1555C1H4R0BA16D	Murata	Chip Capacitor
		C76[C=30pF]	0402N300J500CT	Walsin	Chip Capacitor
C0201	02	C42[C=0.2pF]	GRM0335C1HR20BA01D	Murata	Chip Capacitor
		C44[C=0.3pF]	GRM0335C1HR30BA01D	Murata	Chip Capacitor
sma	03	RF_INP	132134-10	Amphenol	sma Connector
		RF_OUT	132134-10	Amphenol	sma Connector

POST2x6	04	Rx_Signals	612006235121	Wurth Electronik Pin Header
		PLL_SIGNALS	612006235121	Wurth Electronik Pin Header
		Tx_Signals	612006235121	Wurth Electronik Pin Header
		POWER_SUP.	612006235121	Wurth Electronik Pin Header
POST1x1	04	A3.3	TS-104-T-AA	Samtec Pin Header
		+5T	TS-104-T-AA	Samtec Pin Header
		+5R	TS-104-T-AA	Samtec Pin Header
		D3.3	TS-104-T-AA	Samtec Pin Header

## 13. RECOMMENDED DESIGN

### 13.1. An Important Note regarding substrate thickness

The project owner decided to use a TLY5 laminates with 2.2 dielectric constant and 10mm thickness.

A  $50 \Omega$  microstrip transmission line for this substrate has a 0.715 mm width.

Due to the 0.5mm separation between adjacent IC pins, it is impossible to use 0.715mm  $50 \Omega$  microstrip transmission lines to connect the RF circuits of the this PCB.

He proposed a 16 mil (0.406mm) microstrip transmission line width.

The following figure shows the frequency response of a 16mil-wide microstrip transmission line on that substrate.

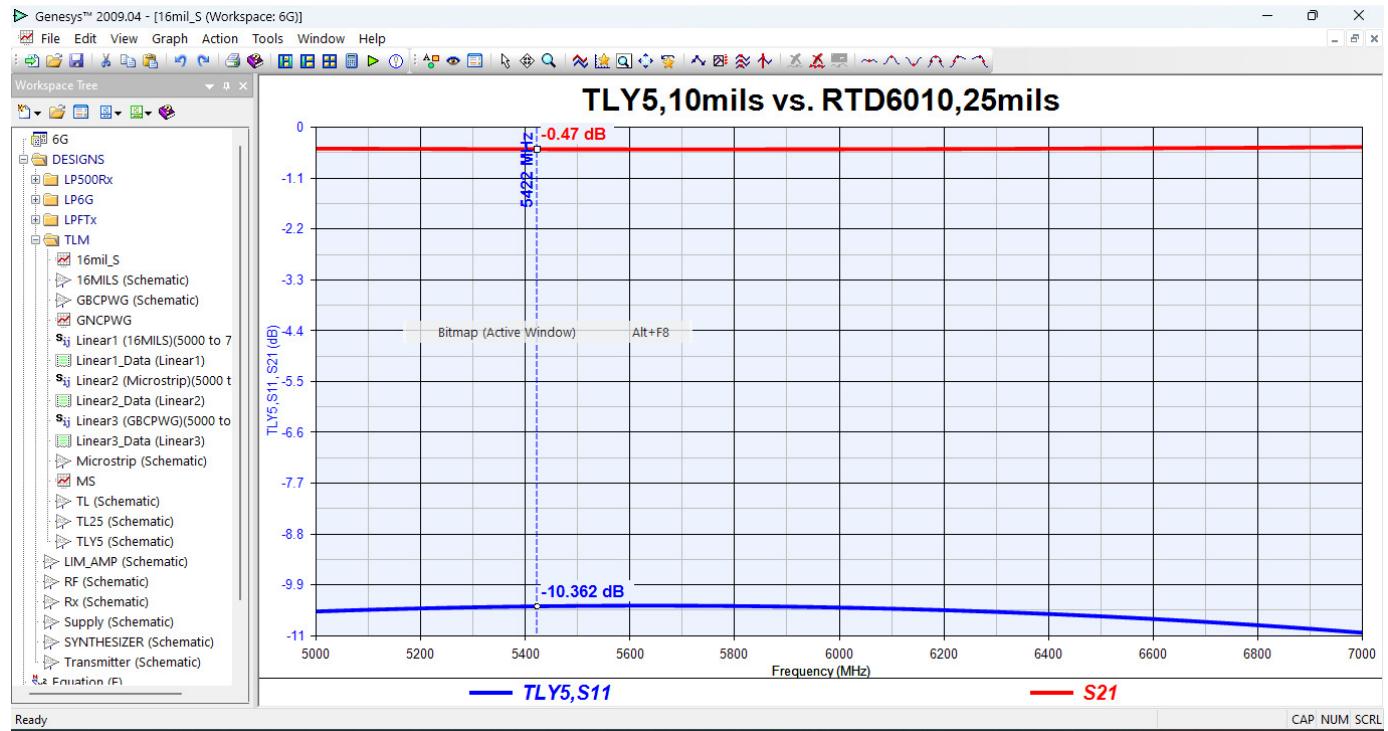
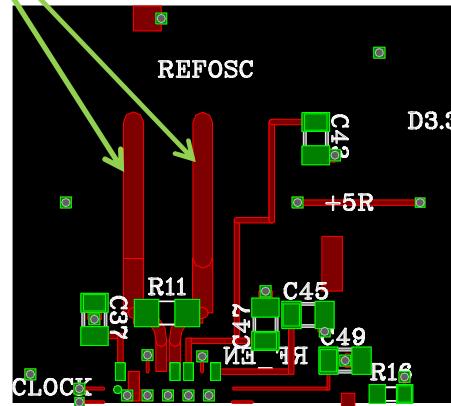


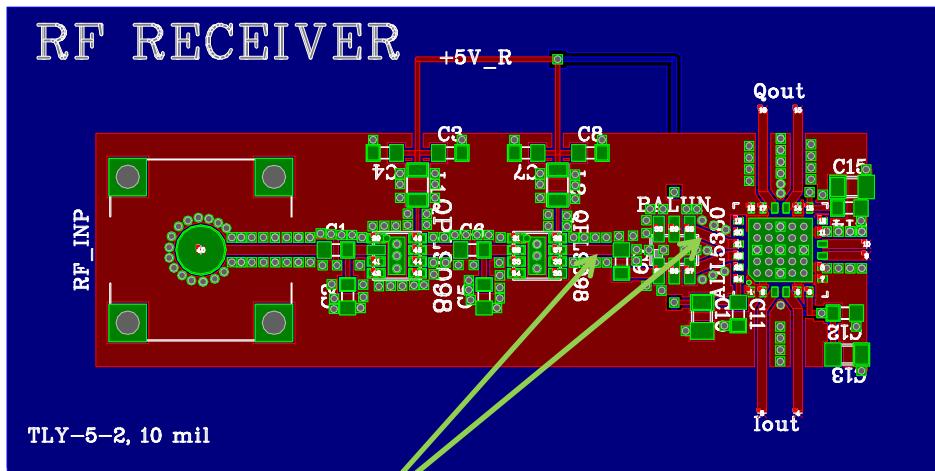
Figure 75. Frequency response of a 16mil-wide microstrip on the proposed substrate

I have used 0.715 wide microstrip transmission lines for some microstrip transmission lines that are away from the integrated circuits with 0.5mm pitch, such as that shown in the following figure.



**Figure 76.** some 50 [W] microstrip transmission lines in the design

Between integrated circuits I have applied the GBCPWG technology, where a 0.381mm width and 0.14mm gap guarantee a 50 [W] characteristic impedance, such as those shown in the following figure.



**Figure 77.** An example of 0.381mm GBCPWG application in the design

The project owner asked me to put the following components on the BOTTOM layer of the PCB:

- Four pin headers (2 x 6)
  - Four complete power supply circuits
  - At the TOP layer, there are already the following:
    - The complete PLL circuit
    - The complete Transmitter circuit, including the modulator and the power amplifier

- The complete Receiver circuit, including the demodulator and two cascaded low noise amplifiers.

He asked me to add the following circuits on the TOP layer:

- Four complete limiting amplifier circuits
- Nine complete low-pass filter circuits, one for the LO RF signal to the modulator, and four LPFs for the I and Q input and output data.

From my previous practical experience with 10 mil substrates I can confirm that a 10mil substrate cannot mechanically support the components of all the above mentioned circuits. It will bend out.

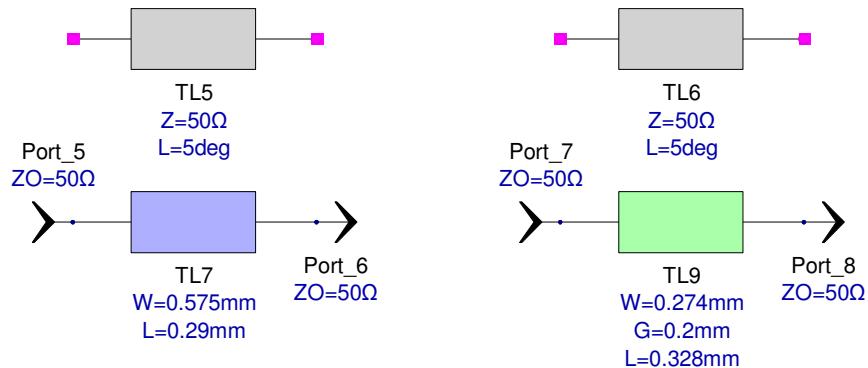
### 13.2. Recommended Substrate Parameters

For the above mentioned reasons, I recommend to use substrate laminates with the following characteristics:

- Dielectric thickness  $\geq 25$  mils (0.635mm) to suppot all the components and connectors that should be loaded on the PCB.
- Dielectric constant  $> 6$  to get as narrow as possible tranmission line widths for  $50 \text{ } [\Omega]$  characteristic impedance; in order to cope with the short separations between adjacent pins pf the integrated circuits.

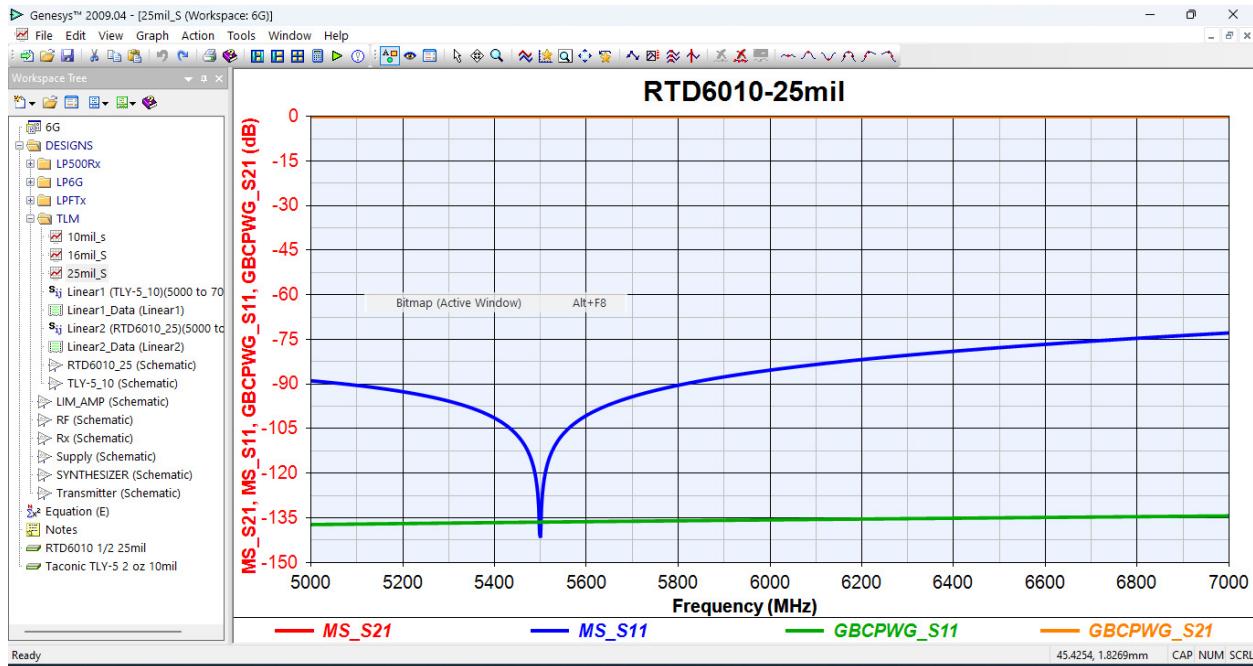
I recommend to use the 25mil RTD6010 substrate that satisfies all these characteristics.

Two samples of this recommended substrate  $50 \text{ } [\Omega]$  transmission lines (microstrip and GBCPWG) have been simulated with the following results.



**RTD6010  
25 mils**

**Figure 78. Correct TL widths for the RTD6010\_25mil substrate**



**Figure 79. S Parameters for the RTD6010\_25mil 50 Ohm transmission lines**

### 13.3. RECOMMENDED LAYOUT DESIGN

Using these correct widths for the 50 [ $\Omega$ ] microstrip and GBCPWG transmission lines, a new layout design for the same PCB has been done, both for 500mV bias and for 1500mV bias. They are shown in the following two figures.

No variations are required in schematic design. The schematic design drawings of figures 73a and 74a are still valid. The two schematic drawings are repeated here in Figures 80a and 81a for reference.

No variations are required in BOM. The BOM mentioned in sections 12.2 and 12.4 above are still valid. No need to repeat these two long tables. They can be implemented as they were reported in sections 12.2 and 12.4.

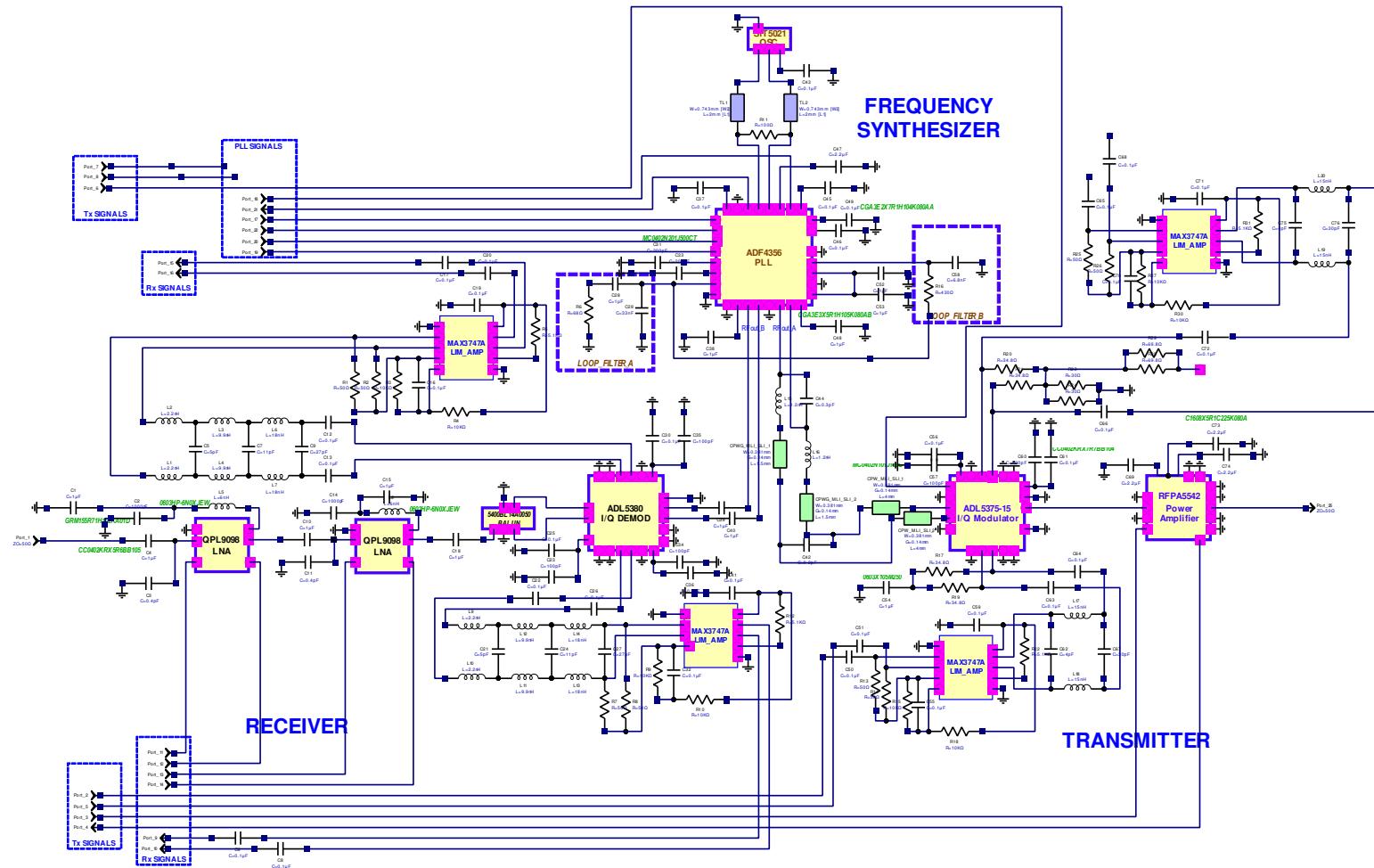
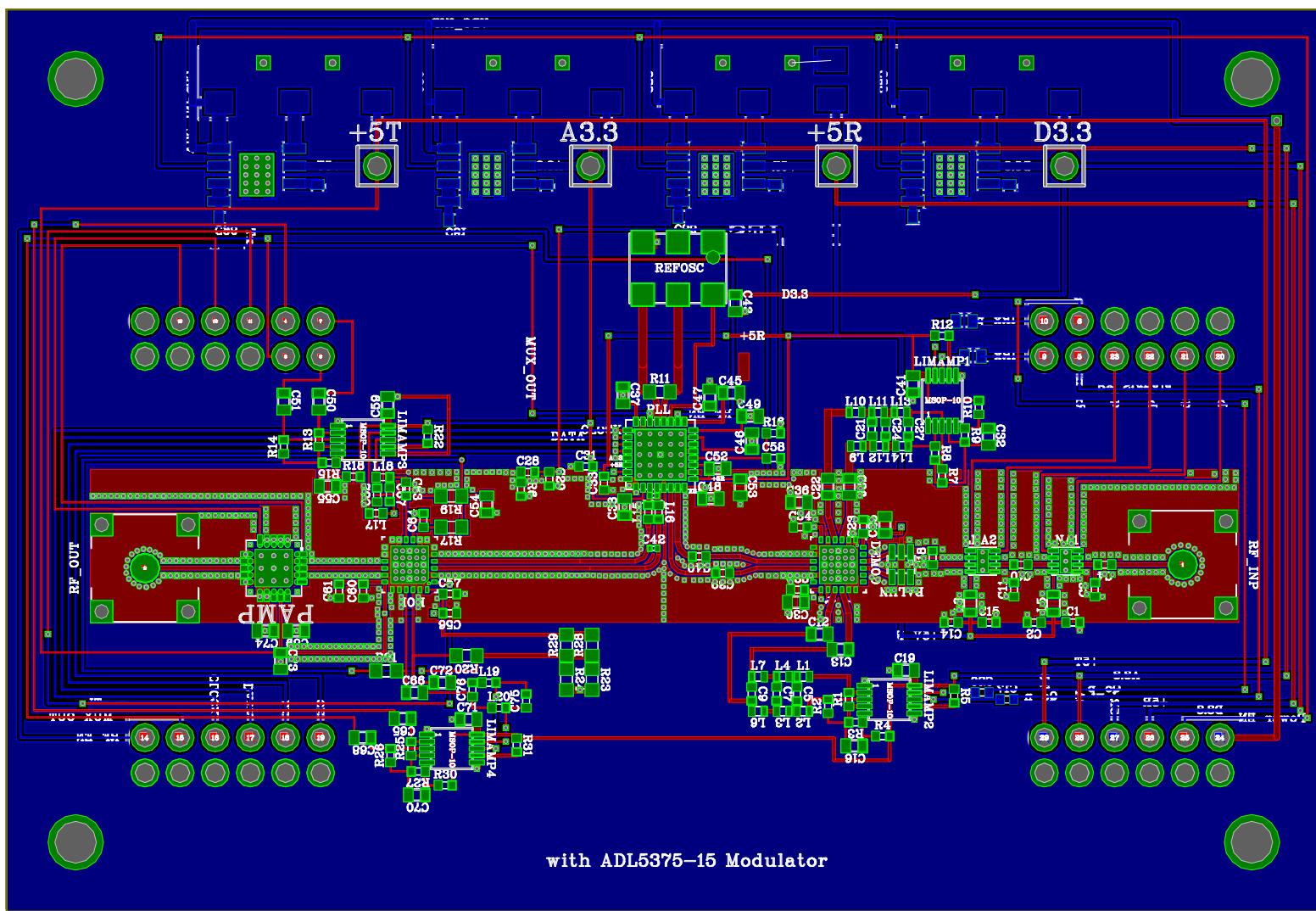


Figure 80a. Schematic Design with ADL5375-15 Modulator with 1500mV bias



**Figure 80b. Layout design with 1500mV bias on 25mil RTD6010**

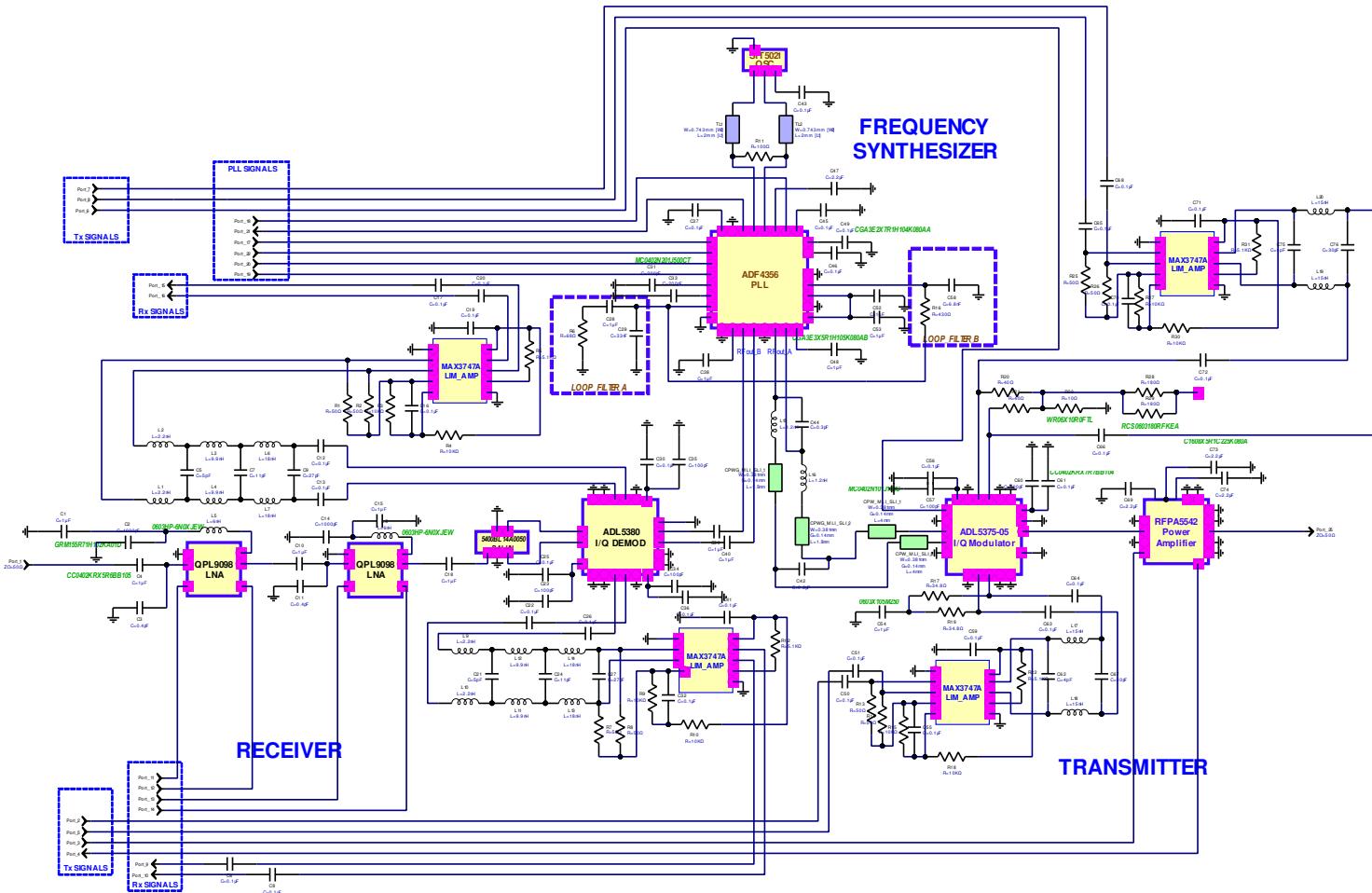
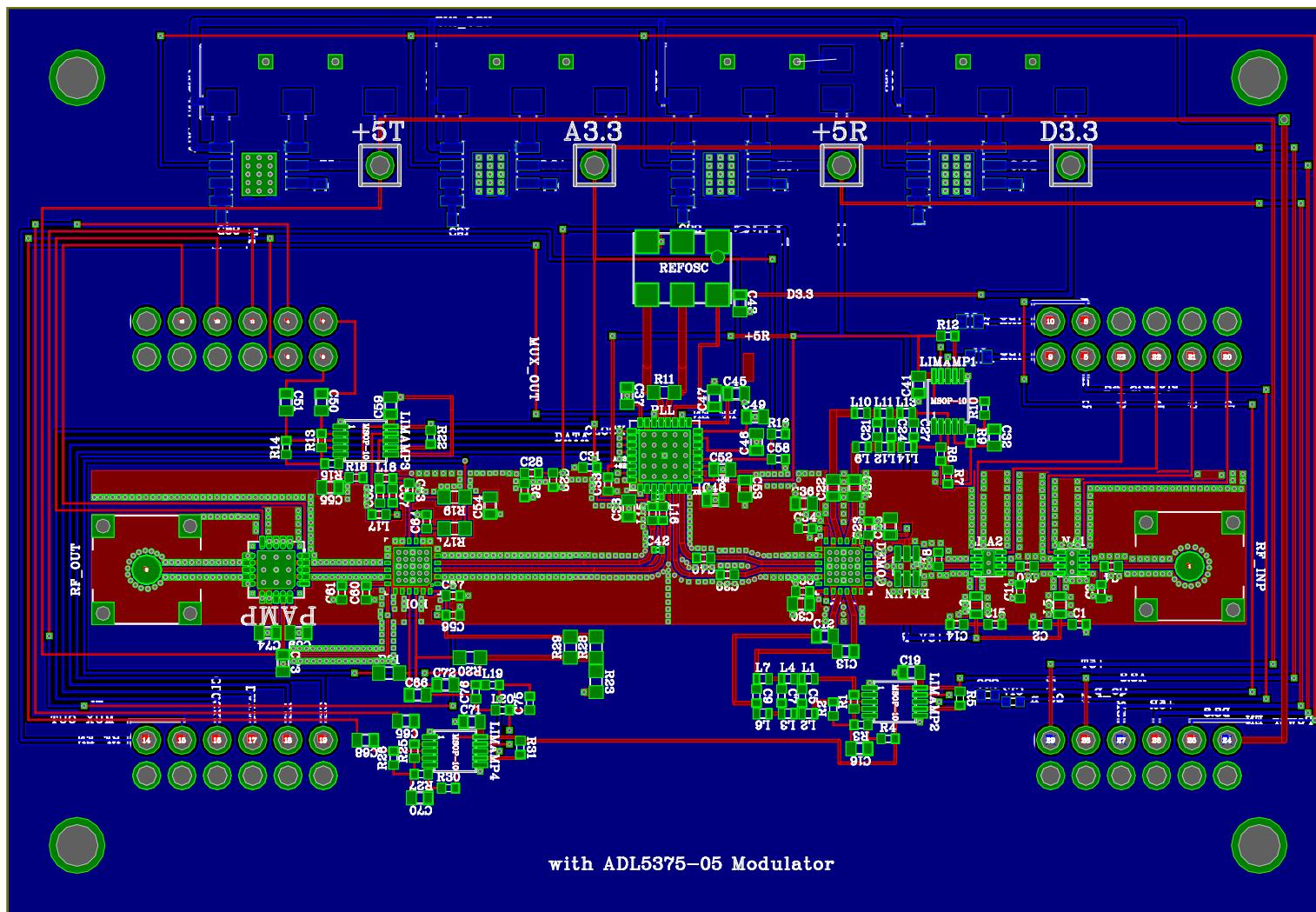


Figure 81a. Schematic design with 500mV bias



**Figure 81b.** Layout design with 500mV bias on 25mil RTD6010

## REFERENCES

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