



ROCK 5A

schematic

V1.1



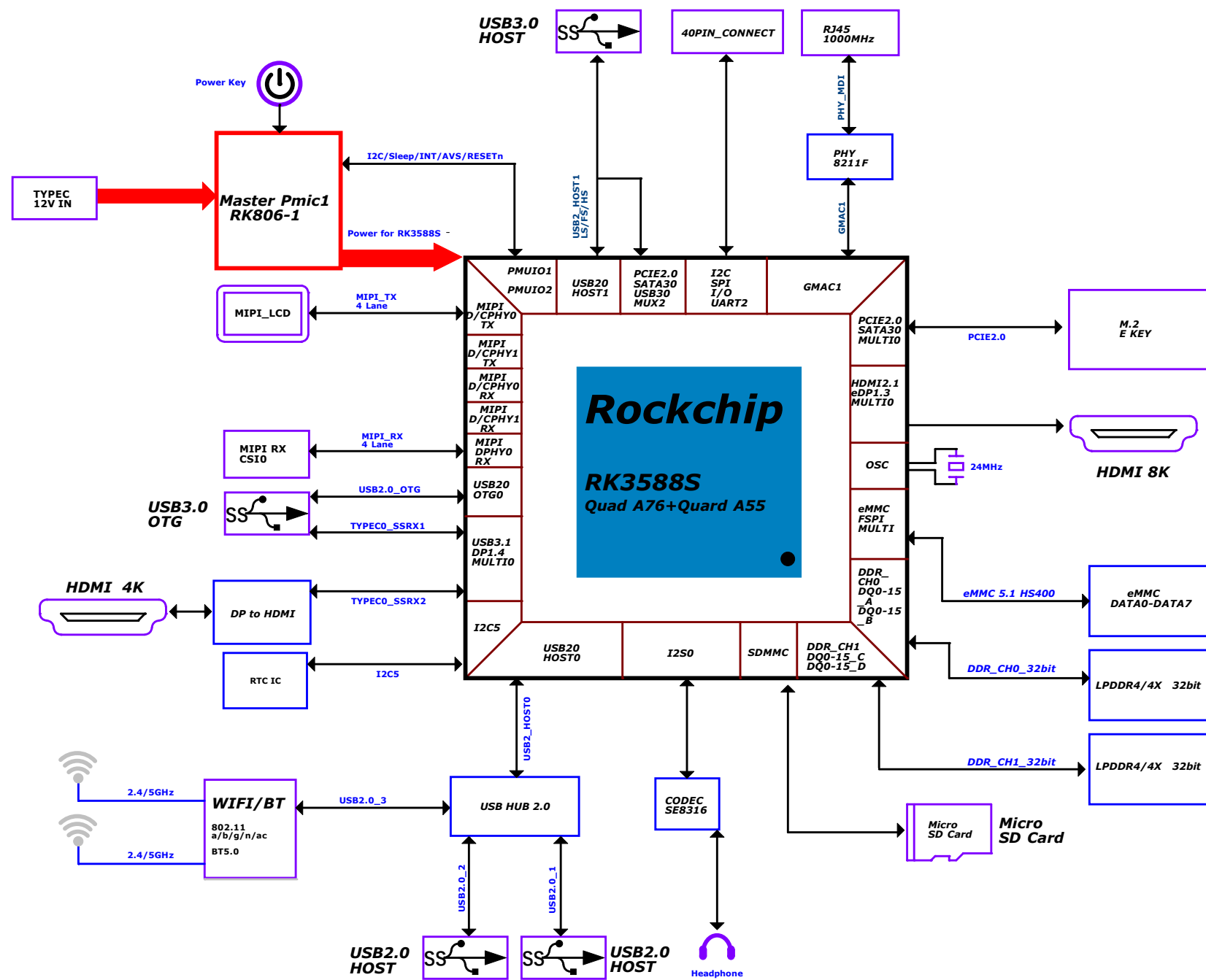
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5A Block Diagram



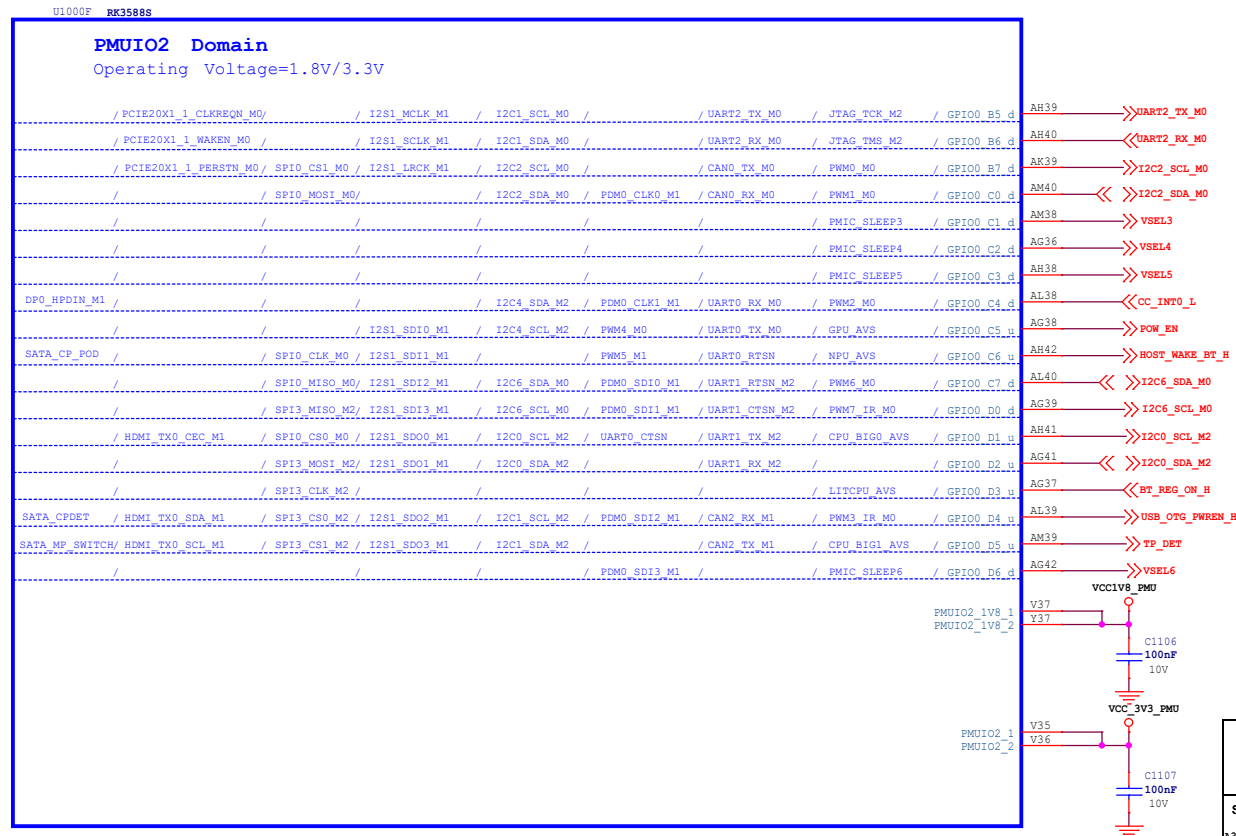
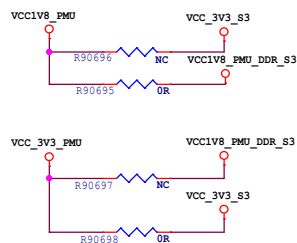
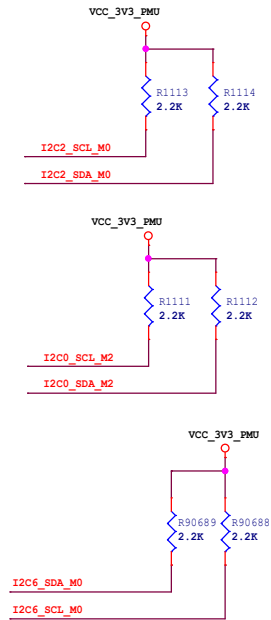
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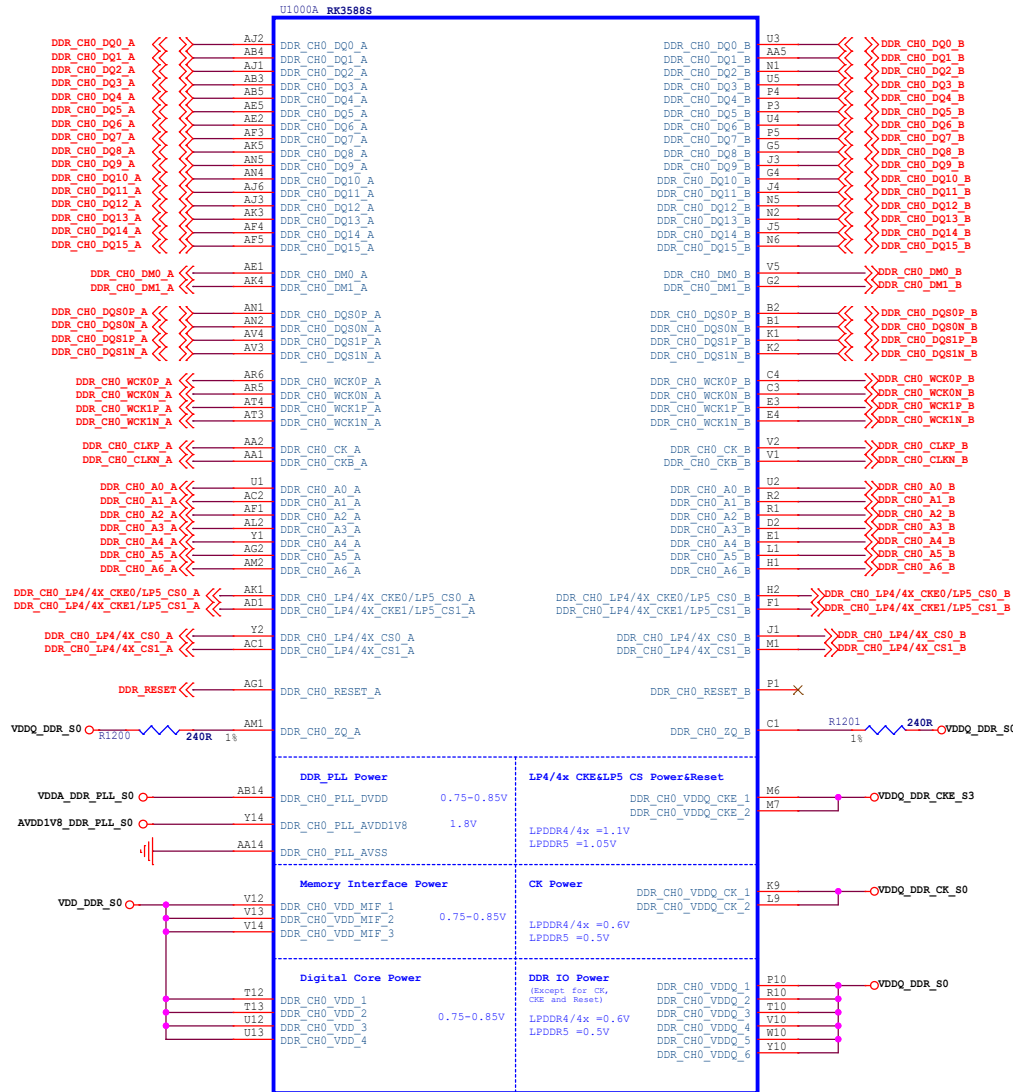


RK3588S (PMUIO2)



Size	Title: ROCK 5A	REV 1.1
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A3		
Date: Monday, April 24, 2023	Sheet	05 of 26

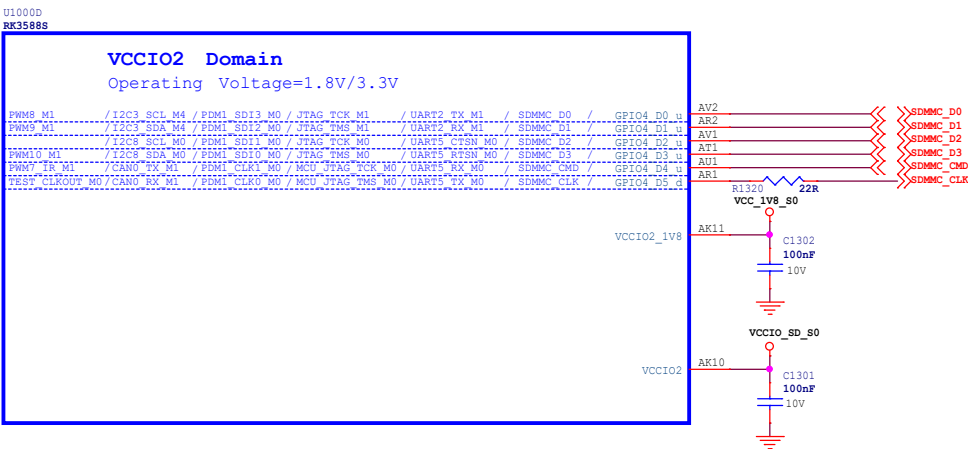
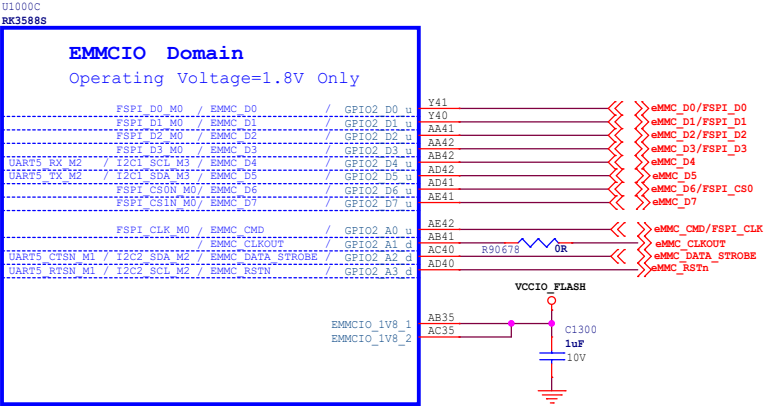
RK3588S (DDR PHY)



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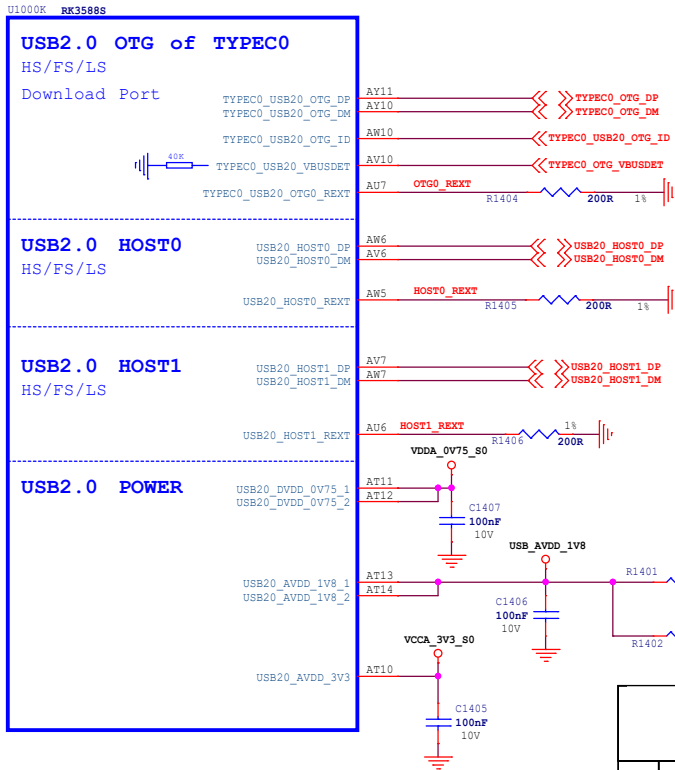
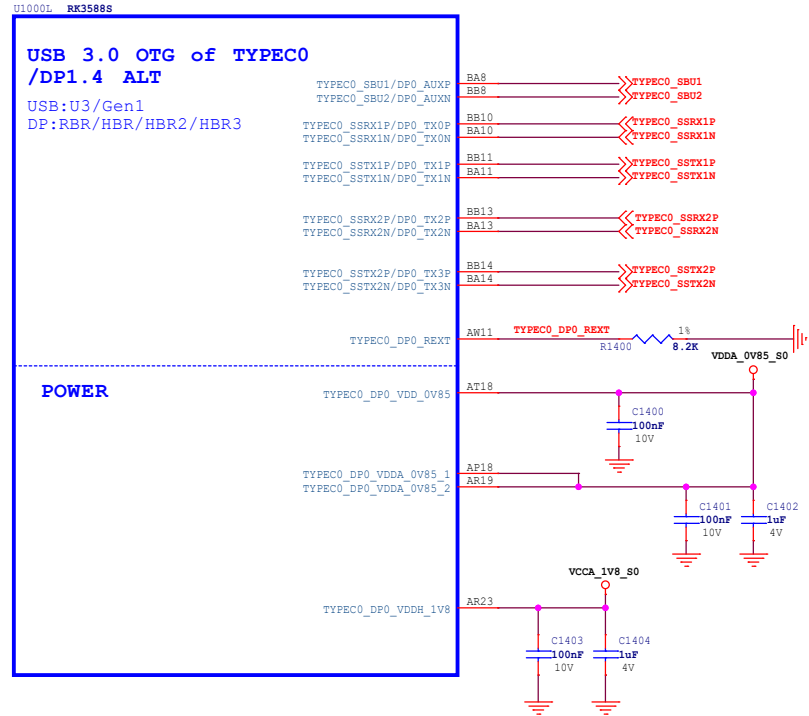
RK3588S (EMMCIO Domain)

RK3588S (VCCIO2 Domain)



RK3588S (USB3.0/DP1.4)

RK3588S (USB2.0)



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----- SARADC_VIN1_KEY/RECOVERY
----- SARADC_VIN2
----- SARADC_VIN3_HP_HOOK
----- SARADC_VIN4
----- SARADC_VIN0_BOOT

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RK3588S (MIPI_D/C PHY0)

U10000 RK3588S

MIPI D/C-PHY DSI_TX Port0

D-PHY:V2.0
4.5Gbps/Lane
C-PHY:V1.1
5.7Gbps/Trio

MIPI_DPHY0_TX_CLKP/MIPI_CPHY0_TX_TRIO1_C
MIPI_DPHY0_TX_CLKN/MIPI_CPHY0_TX_TRIO1_B
MIPI_DPHY0_TX_D0P/MIPI_CPHY0_TX_TRIO0_B
MIPI_DPHY0_TX_D0N/MIPI_CPHY0_TX_TRIO0_A
MIPI_DPHY0_TX_D1P/MIPI_CPHY0_TX_TRIO1_A
MIPI_DPHY0_TX_D1N/MIPI_CPHY0_TX_TRIO0_C
MIPI_DPHY0_TX_D2P/MIPI_CPHY0_TX_TRIO2_B
MIPI_DPHY0_TX_D2N/MIPI_CPHY0_TX_TRIO2_A
MIPI_DPHY0_TX_D3P/NO_USE
MIPI_DPHY0_TX_D3N/MIPI_CPHY0_TX_TRIO2_C

BB34 MIPI_DPHY0_TX_CLKP/MIPI_CPHY0_TX_TRIO1_C
BA34 MIPI_DPHY0_TX_CLKN/MIPI_CPHY0_TX_TRIO1_B
BB31 MIPI_DPHY0_TX_D0P/MIPI_CPHY0_TX_TRIO0_B
BA31 MIPI_DPHY0_TX_D0N/MIPI_CPHY0_TX_TRIO0_A
BA32 MIPI_DPHY0_TX_D1P/MIPI_CPHY0_TX_TRIO1_A
BB32 MIPI_DPHY0_TX_D1N/MIPI_CPHY0_TX_TRIO0_C
BA35 MIPI_DPHY0_TX_D2P/MIPI_CPHY0_TX_TRIO2_B
BB35 MIPI_DPHY0_TX_D2N/MIPI_CPHY0_TX_TRIO2_A
BB37 MIPI_DPHY0_TX_D3P
BA37 MIPI_DPHY0_TX_D3N/MIPI_CPHY0_TX_TRIO2_C

MIPI D/C-PHY CSI_RX Port0

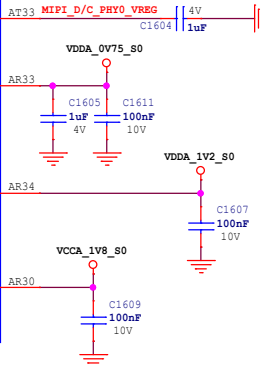
D-PHY:V2.0
4.5Gbps/Lane
C-PHY:V1.1
5.7Gbps/Trio

MIPI_DPHY0_RX_CLKP/MIPI_CPHY0_RX_TRIO1_C
MIPI_DPHY0_RX_CLKN/MIPI_CPHY0_RX_TRIO1_B
MIPI_DPHY0_RX_D0P/MIPI_CPHY0_RX_TRIO0_B
MIPI_DPHY0_RX_D0N/MIPI_CPHY0_RX_TRIO0_A
MIPI_DPHY0_RX_D1P/MIPI_CPHY0_RX_TRIO1_A
MIPI_DPHY0_RX_D1N/MIPI_CPHY0_RX_TRIO0_C
MIPI_DPHY0_RX_D2P/MIPI_CPHY0_RX_TRIO2_B
MIPI_DPHY0_RX_D2N/MIPI_CPHY0_RX_TRIO2_A
MIPI_DPHY0_RX_D3P/NO_USE
MIPI_DPHY0_RX_D3N/MIPI_CPHY0_RX_TRIO2_C

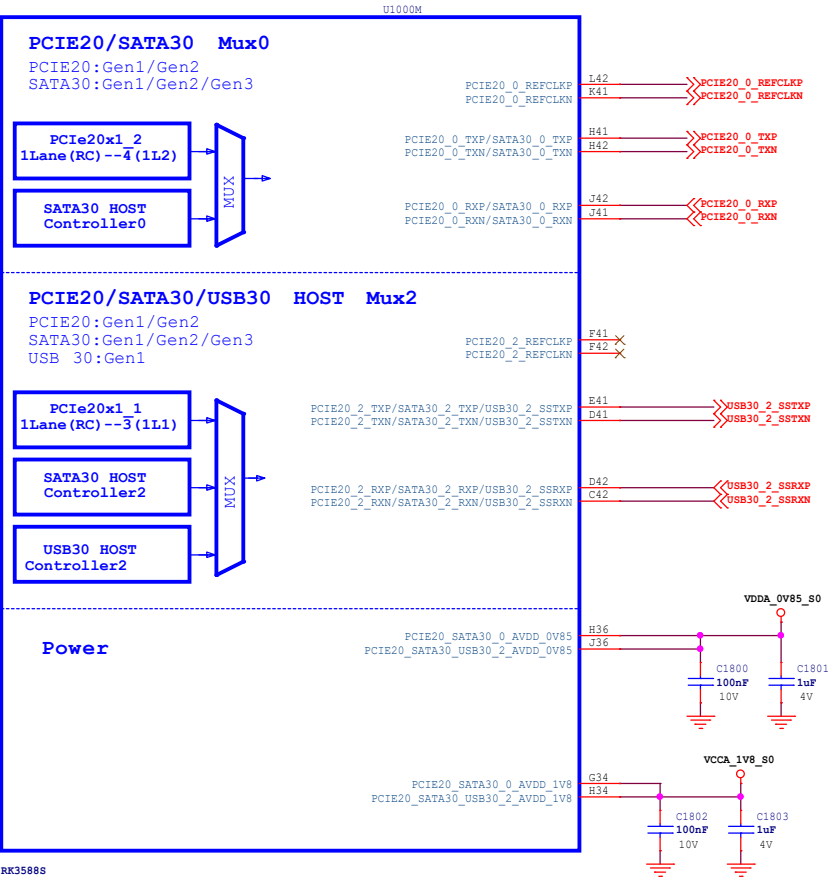
BB41
BA41
BA38
BB38
BA40
AY40
AY42
BA42
AW41
AW42

Power

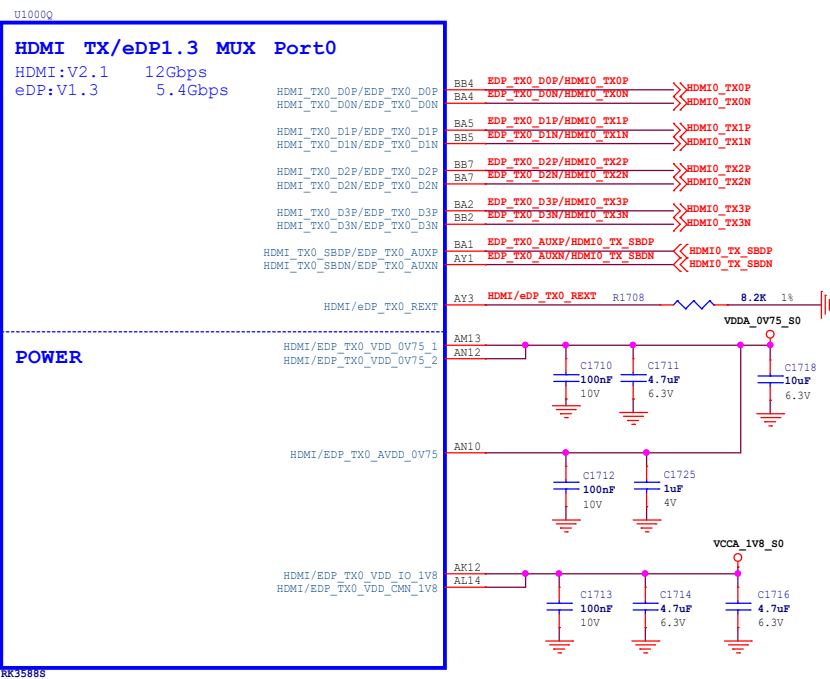
MIPI_D/C_PHY0_VREG
MIPI_D/C_PHY0_VDD
MIPI_D/C_PHY_VDD_1V2_1
MIPI_D/C_PHY_VDD_1V8_1



RK3588S (PCIE20/SATA30/USB30)



RK3588S (HDMI2.1 TX/eDP1.3 TX)



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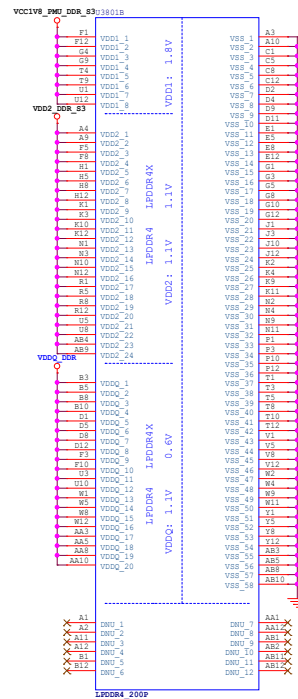
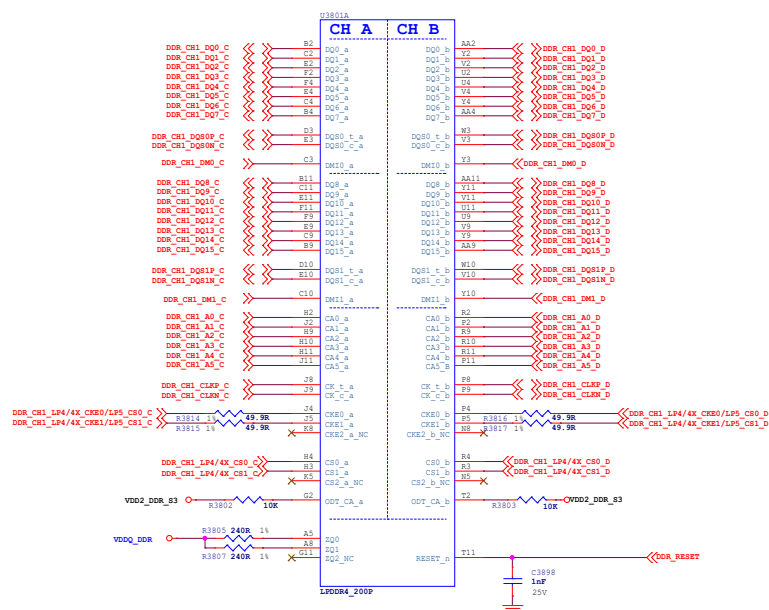
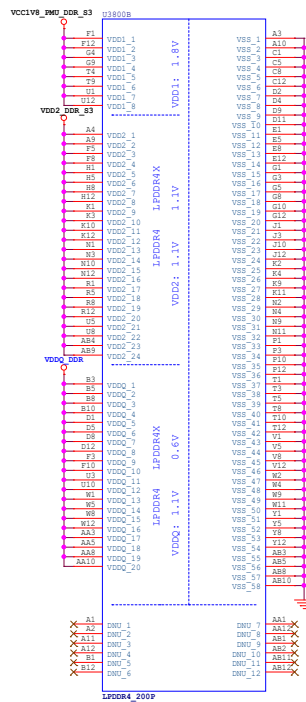
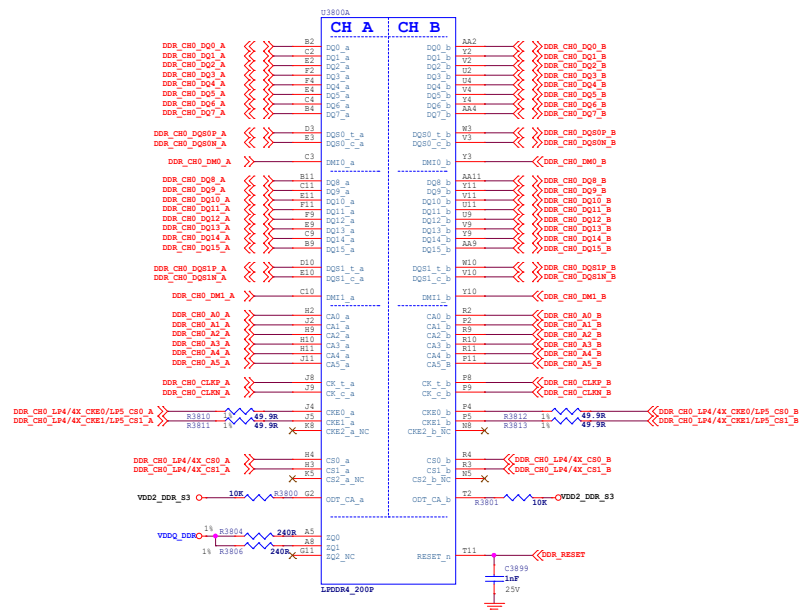
VCCIO6 Domain
Operating Voltage=1.8V/3.3V

BT1120_D0	/ CIP_D0	/	/ I201_MCLK_M0	/ UART0_RXEN_M0	/ SPI0_MISO_M0	/	/ PCIE120X1_1_CLKREQ_M0	/ GPIO4_A0_0	AV19	>>> I201_MCLK_M0	
BT1120_D1 <td>/ CIP_D1</td> <td>/</td> <td>/ I201_SCLK_M0</td> <td>/ UART0_CTS_M0</td> <td>/ SPI0_MOSI_M0</td> <td>/</td> <td>/ PCIE120X1_1_WAKEN_M0</td> <td>/ GPIO4_A1_0</td> <td>AM18 <td>>>> I201_CTS_M0</td> </td>	/ CIP_D1	/	/ I201_SCLK_M0	/ UART0_CTS_M0	/ SPI0_MOSI_M0	/	/ PCIE120X1_1_WAKEN_M0	/ GPIO4_A1_0	AM18 <td>>>> I201_CTS_M0</td>	>>> I201_CTS_M0	
BT1120_D2 <td>/ CIP_D2</td> <td>/</td> <td>/ I201_LACK_M0</td> <td>/</td> <td>/ SPI0_CS_M0</td> <td>/</td> <td>/ PCIE120X1_1_FERSTN_M0</td> <td>/ GPIO4_A2_0</td> <td>AV26 <td>>>> I201_LACK_M0</td> </td>	/ CIP_D2	/	/ I201_LACK_M0	/	/ SPI0_CS_M0	/	/ PCIE120X1_1_FERSTN_M0	/ GPIO4_A2_0	AV26 <td>>>> I201_LACK_M0</td>	>>> I201_LACK_M0	
BT1120_D3 <td>/ CIP_D3</td> <td>/</td> <td>/ UART0_TX_M0</td> <td>/</td> <td>/</td> <td>/</td> <td>/</td> <td>/ GPIO4_A3_0</td> <td>AV19 <td>>>> VCC_SVO_FUSEM0_B</td> </td>	/ CIP_D3	/	/ UART0_TX_M0	/	/	/	/	/ GPIO4_A3_0	AV19 <td>>>> VCC_SVO_FUSEM0_B</td>	>>> VCC_SVO_FUSEM0_B	
BT1120_D4 <td>/ CIP_D4</td> <td>/</td> <td>/ UART0_RX_M0</td> <td>/</td> <td>/ SPI2_MISO_M0</td> <td>/ I203_SCL_M0</td> <td>/</td> <td>/ GPIO4_A4_0</td> <td>AM19 <td>>>> LDO_FUSEM0_B</td> </td>	/ CIP_D4	/	/ UART0_RX_M0	/	/ SPI2_MISO_M0	/ I203_SCL_M0	/	/ GPIO4_A4_0	AM19 <td>>>> LDO_FUSEM0_B</td>	>>> LDO_FUSEM0_B	
BT1120_D5 <td>/ CIP_D5</td> <td>/</td> <td>/ I201_S0D0_M0</td> <td>/ UART0_TX_M0</td> <td>/ SPI2_MOSI_M0</td> <td>/ I203_SDA_M0</td> <td>/</td> <td>/ GPIO4_A5_0</td> <td>AM15 <td>>>> I201_S0D0_M0</td> </td>	/ CIP_D5	/	/ I201_S0D0_M0	/ UART0_TX_M0	/ SPI2_MOSI_M0	/ I203_SDA_M0	/	/ GPIO4_A5_0	AM15 <td>>>> I201_S0D0_M0</td>	>>> I201_S0D0_M0	
BT1120_D6 <td>/ CIP_D6</td> <td>/</td> <td>/ I201_S0D1_M0</td> <td>/ UART0_RX_M0</td> <td>/ SPI2_CS_M0</td> <td>/ I203_SCL_M0</td> <td>/</td> <td>/ GPIO4_A6_0</td> <td>AM18 <td>>>> I203_SCL_M0</td> </td>	/ CIP_D6	/	/ I201_S0D1_M0	/ UART0_RX_M0	/ SPI2_CS_M0	/ I203_SCL_M0	/	/ GPIO4_A6_0	AM18 <td>>>> I203_SCL_M0</td>	>>> I203_SCL_M0	
BT1120_D7 <td>/ CIP_D7</td> <td>/</td> <td>/ I201_S0D2_M0</td> <td>/</td> <td>/ SPI2_CSD0_M0</td> <td>/ I203_SDA_M0</td> <td>/</td> <td>/ GPIO4_A7_0</td> <td>AM24 <td><<< I203_SDA_M0</td> </td>	/ CIP_D7	/	/ I201_S0D2_M0	/	/ SPI2_CSD0_M0	/ I203_SDA_M0	/	/ GPIO4_A7_0	AM24 <td><<< I203_SDA_M0</td>	<<< I203_SDA_M0	
BT1120_CLKOUT0 <td>/ CIP_CLKOUT</td> <td>/</td> <td>/ I201_S0D1_M0</td> <td>/ UART0_TX_M0</td> <td>/ SPI2_CSI_M0</td> <td>/ I203_SDA_M0</td> <td>/</td> <td>/ GPIO4_A8_0</td> <td>AM27 <td>>>> GPIO4_A0</td> </td>	/ CIP_CLKOUT	/	/ I201_S0D1_M0	/ UART0_TX_M0	/ SPI2_CSI_M0	/ I203_SDA_M0	/	/ GPIO4_A8_0	AM27 <td>>>> GPIO4_A0</td>	>>> GPIO4_A0	
SDIOIF1_TX_M0	/ MIPI_CAMERA0G_CLK_M0	/ SATA02_ACT_LED_M0	/ I201_S0D0_M0	/ UART0_RX_M0	/ SPI0_CSI_M0	/ I203_SCL_M0	/	/ GPIO4_A9_0	AM22 <td>>>> I201_S0D0_M0</td>	>>> I201_S0D0_M0	
CAN1_RX_M0	/ BT1120_D8	/ CIP_WRRF	/ PFM04_M0	/ I201_S0D1_M0	/ UART0_RXEN_M0	/ I203_SCL_M0	/ PCIE120X1_1_BUTTON_RSTW	/ GPIO4_B0_0	AV15 <td>>>> PFM04_M0</td>	>>> PFM04_M0	
CAN1_TX_M0	/ BT1120_D9	/ CIP_VRRM0	/ PFM03_TX_M0	/ I201_S0D0_M0	/ UART0_CTS_M0	/	/ I203_SDA_M0	/ PCIE120X1_2_BUTTON_RSTW	GPIO4_A3_0	>>> PFM03_TX_M0	
BT1120_D10	/ CIP_CLKOUT	/ PFM01_TX_M0	/ I201_S0D3_M0	/ UART0_TX_M0	/	/ DPO_HPDIN_M0	/ SDIOIF0_TX_M0	/	GPIO4_B4_0	>>> SDIOIF0_TX_M0	
BT1120_D11	/	/ PFM02_M0	/	/ UART0_RX_M0	/	/ SPI3_MISO_M0	/	/	GPIO4_B5_0	>>> DSB_BOOT_FUSEM0_B	
BT1120_D12	/	/ PFM03_M0	/	/	/ SPI3_MOSI_M0	/ I203_SCL_M0	/ SATA02_ACT_LED_M0	/	GPIO4_B6_0	>>> HEMI0_TX_ON_B	
BT1120_D13	/	/	/ HEMI_TX0_RX0_M0	/	/ SPI3_CS_M0	/ I203_SDA_M0	/ PCIE120X1_2_CLKREQ_M0	/	GPIO4_M1_0	>>> HEMI_TX0_SCL_M0	
BT1120_D14	/	/	/ HEMI_TX0_SDA_M0	/	/ I203_SCL_M0	/	/ PCIE120X1_2_WAKEN_M0	/	GPIO4_M2_0	<<< HEMI_TX0_SDA_M0	
BT1120_D15	/ SDIOIF1_TX_M0	/	/ PFM06_M0	/ HEMI_TX0_CEC_M0	/	/ SPI3_CSI_M0	/ I203_SDA_M0	/ PCIE120X1_2_FERSTN_M0	/	GPIO4_C1_0	<<< HEMI_TX0_CEC_M0

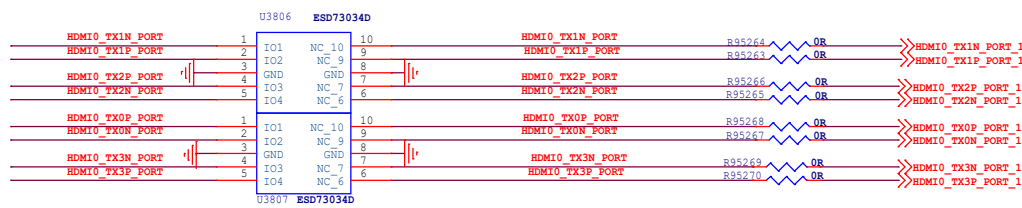
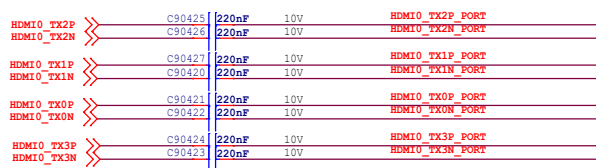
Note:
BT1120 Only Support Output

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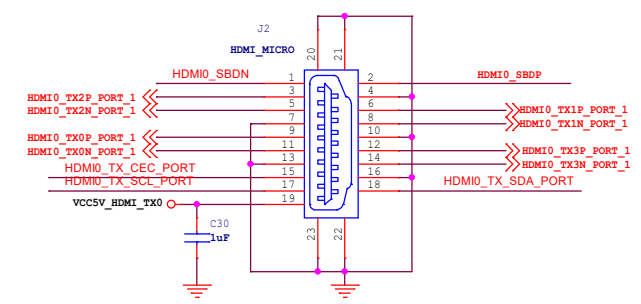
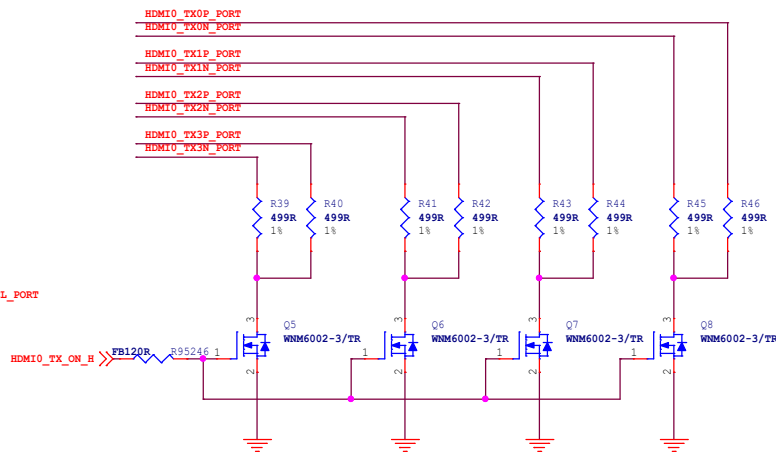
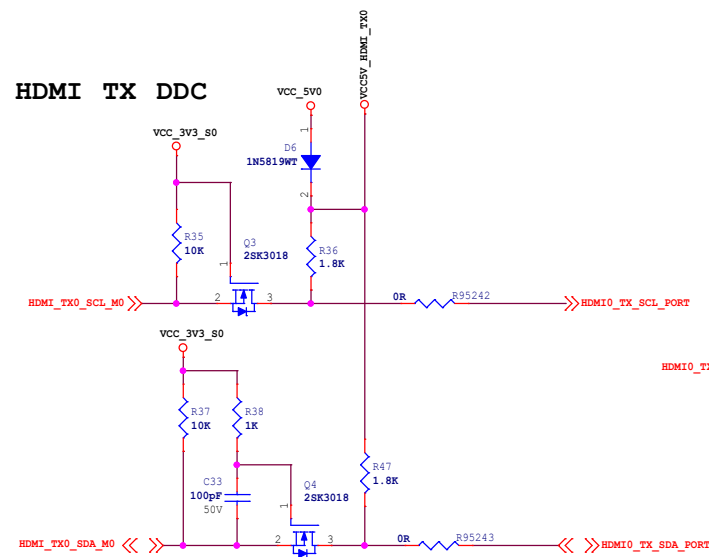
DRAM-LPDDR4/4x_2X32bit



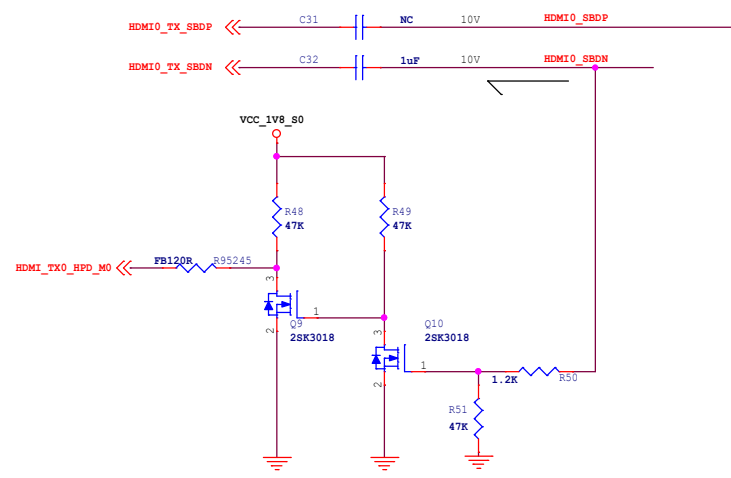
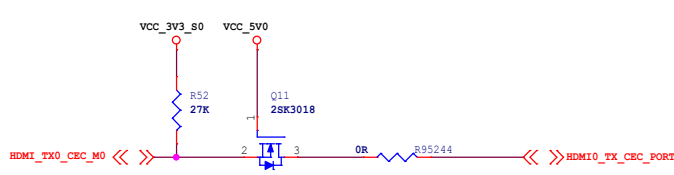
HDMI2.1 TX0

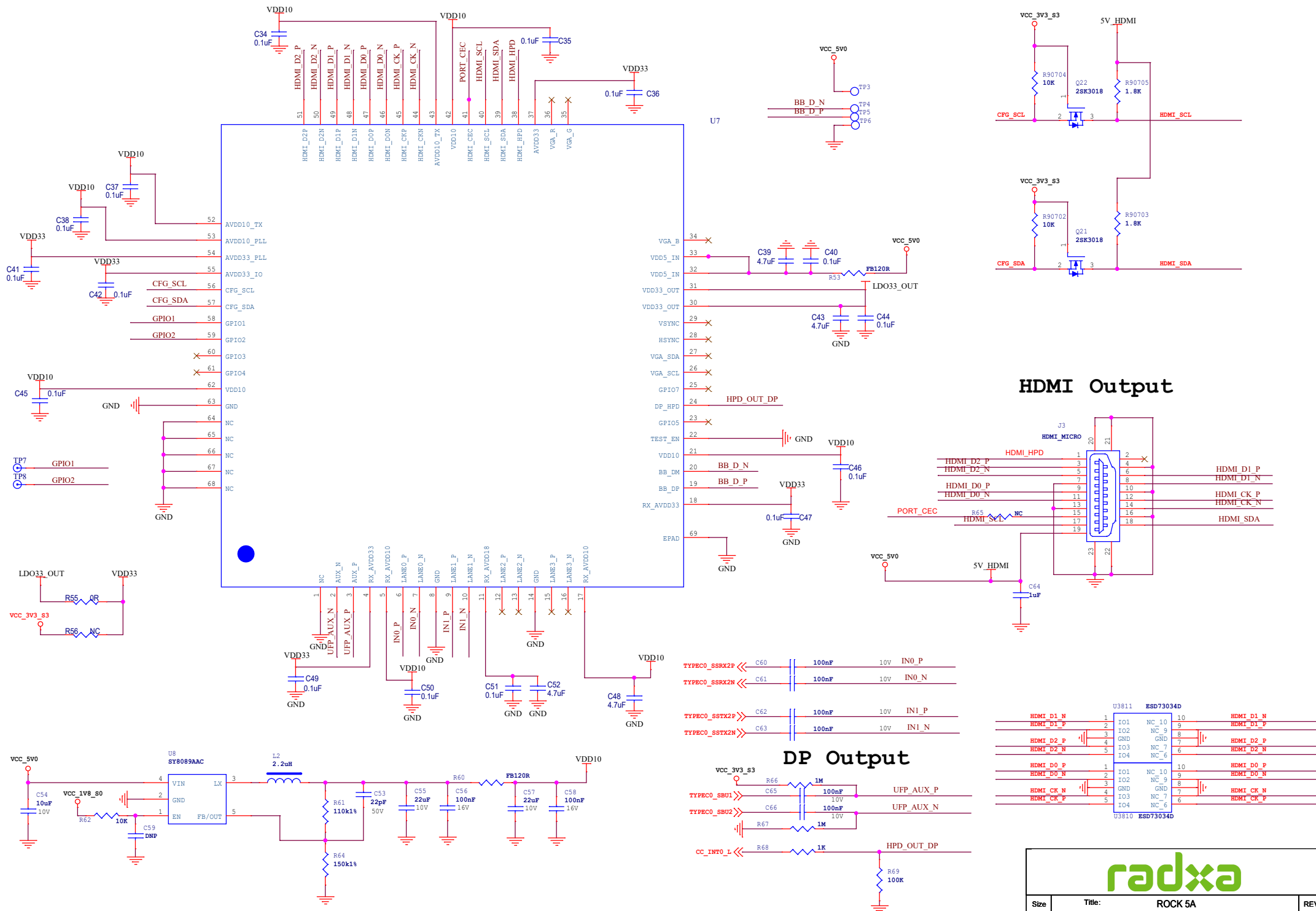


HDMI TX DDC

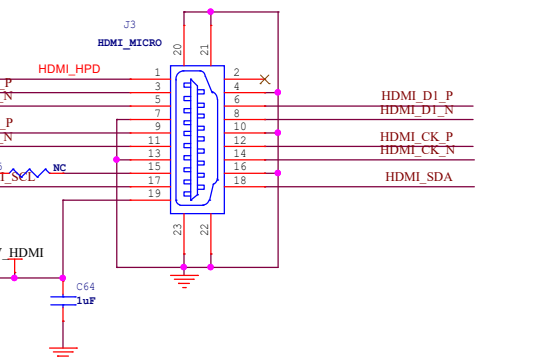


HDMI TX CEC

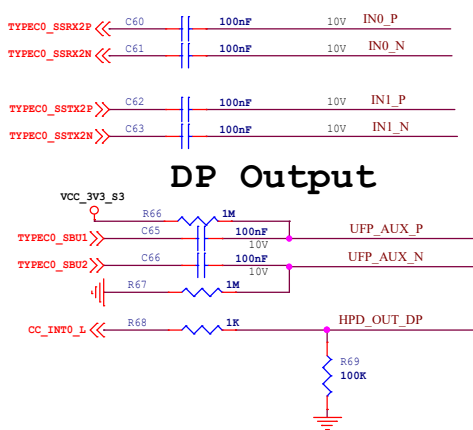




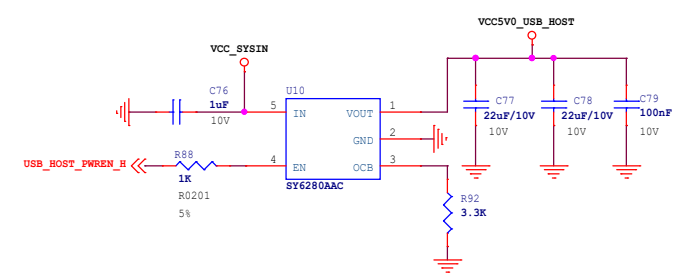
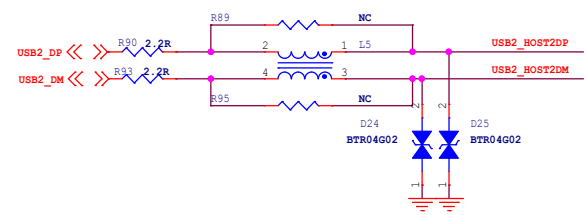
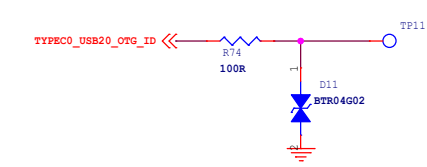
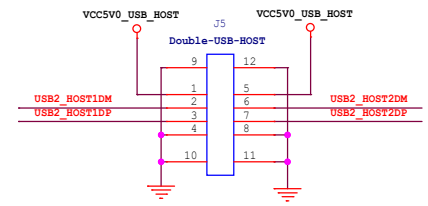
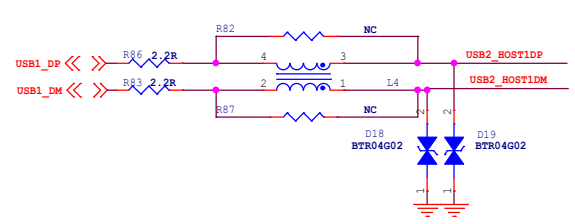
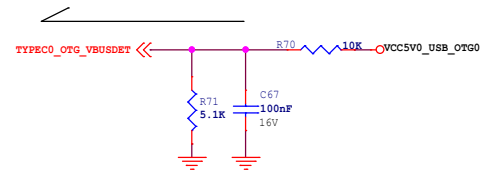
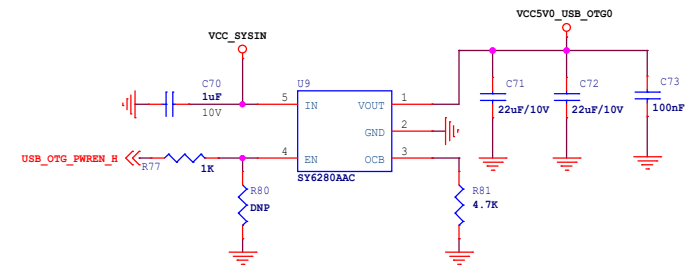
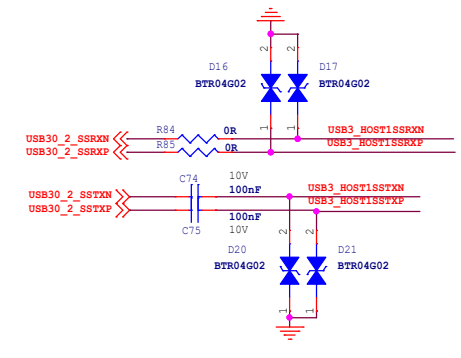
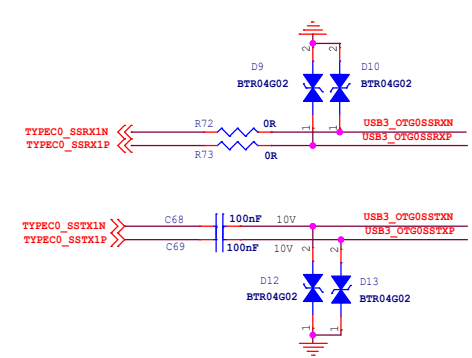
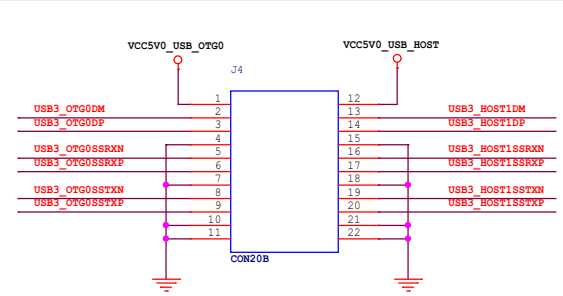
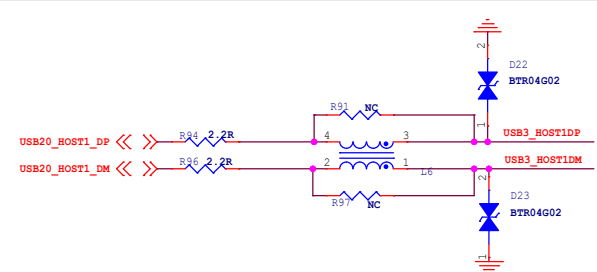
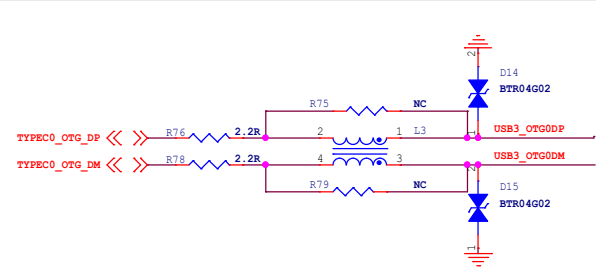
HDMI Output



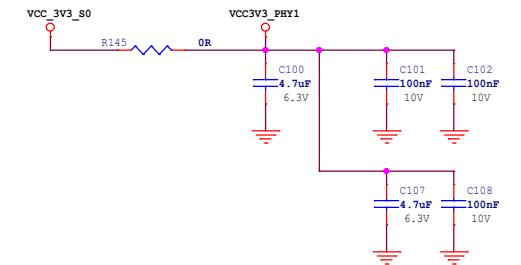
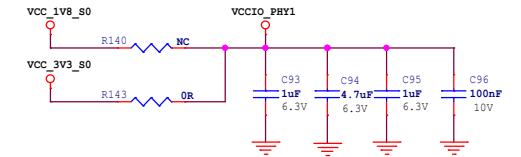
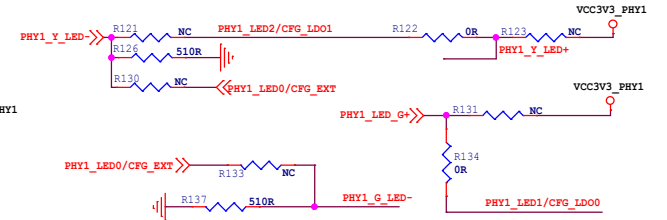
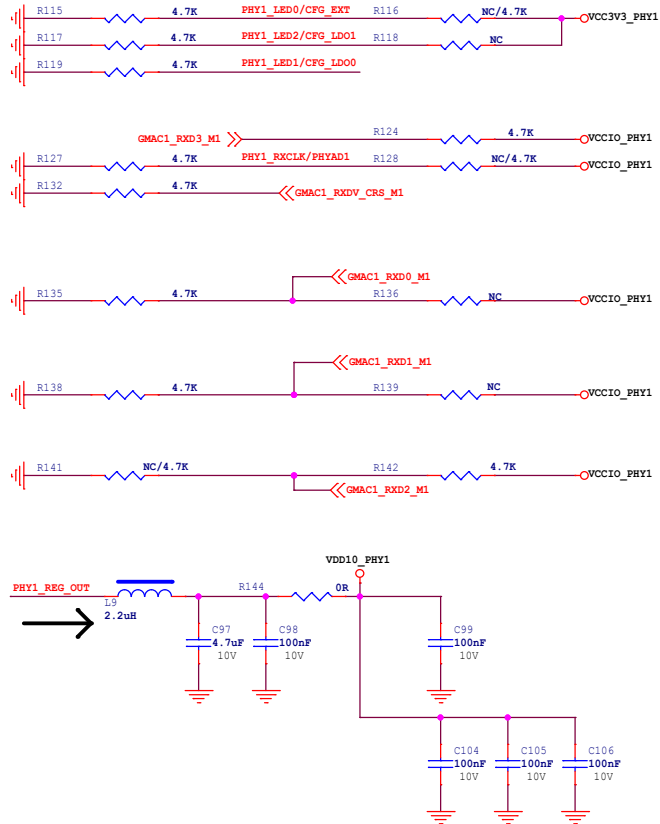
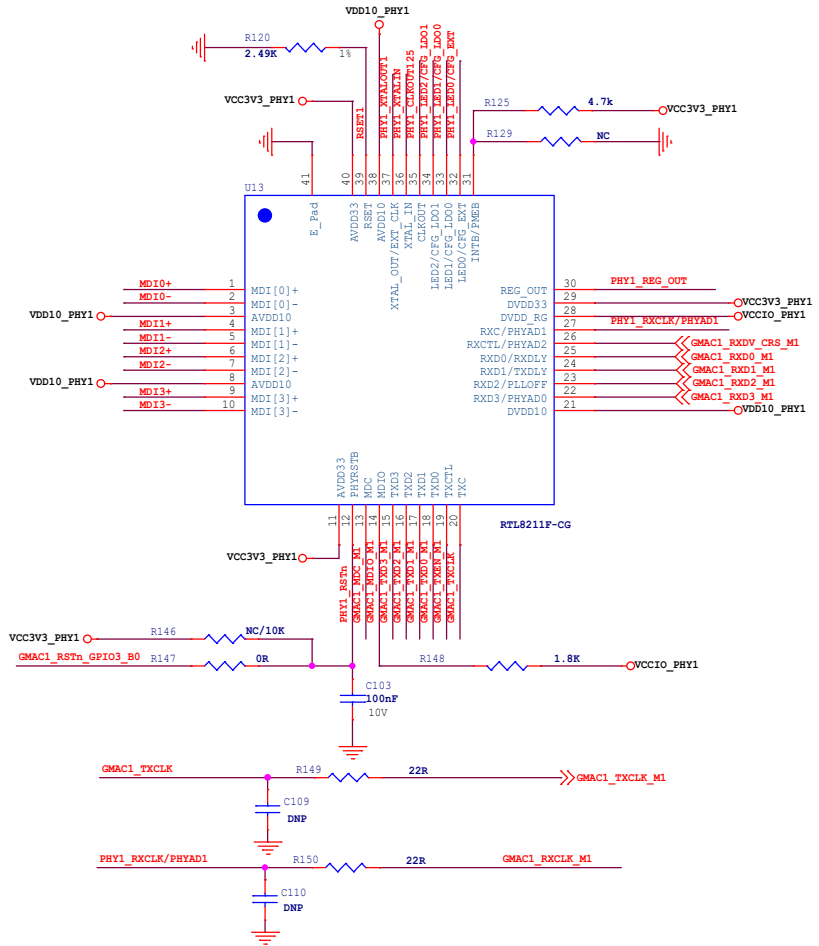
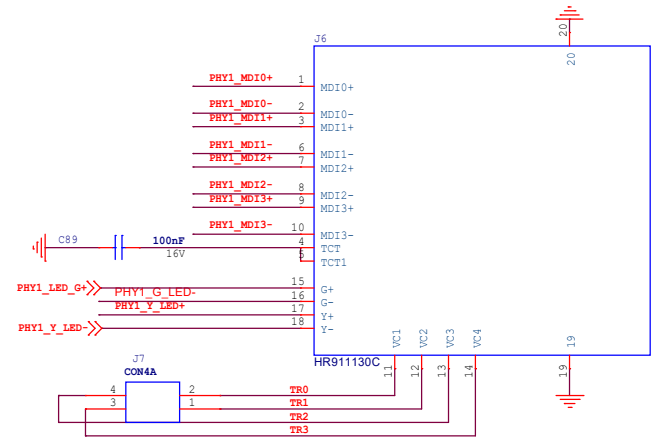
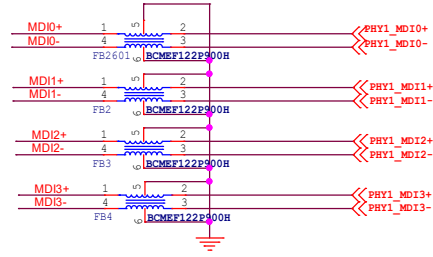
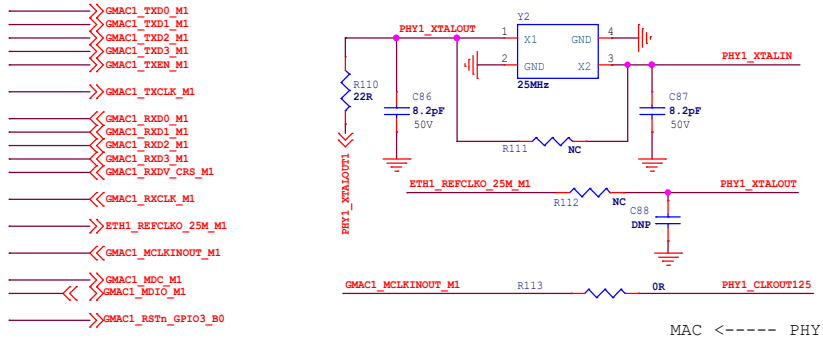
DP Output



U3811 ESD73034D		U3811 ESD73034D	
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HDMI_D1_P	2	IO2	NC 9
HDMI_D2_P	3	GND	NC 8
HDMI_D2_N	4	IO3	NC 7
HDMI_D0_P	5	IO4	NC 6
HDMI_D0_N	1	IO1	NC 10
HDMI_D0_P	2	IO2	NC 9
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HDMI_D2_N	5	IO4	NC 6

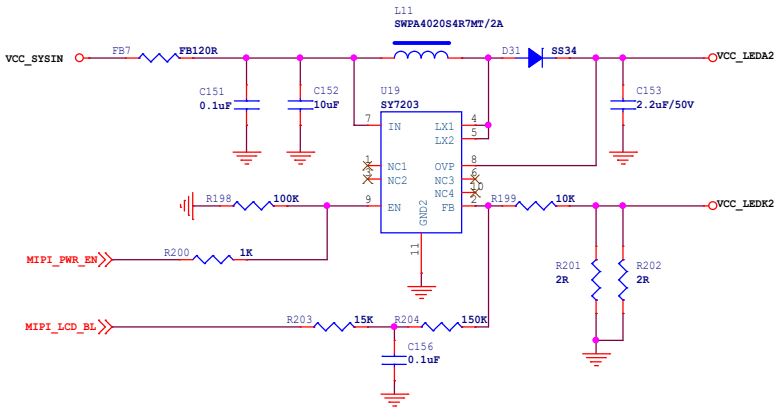


Giga PHY1

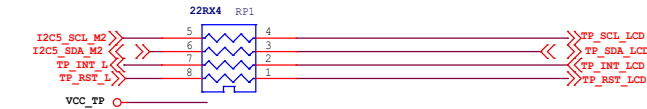


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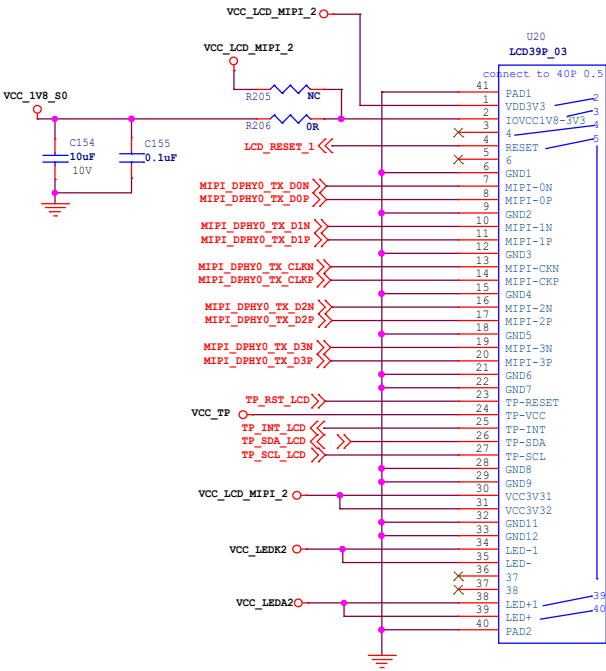
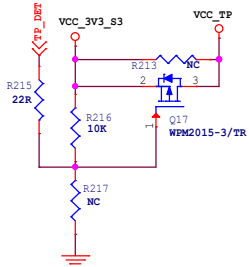
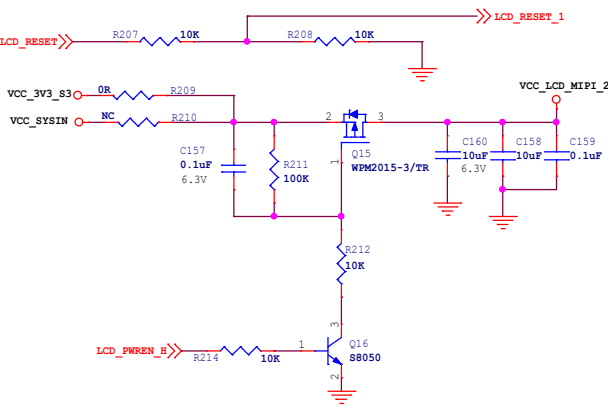
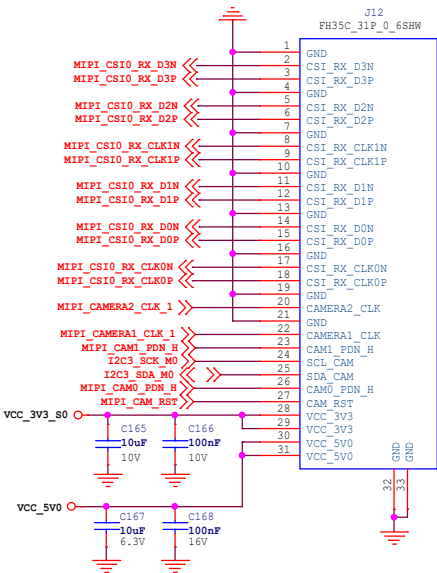
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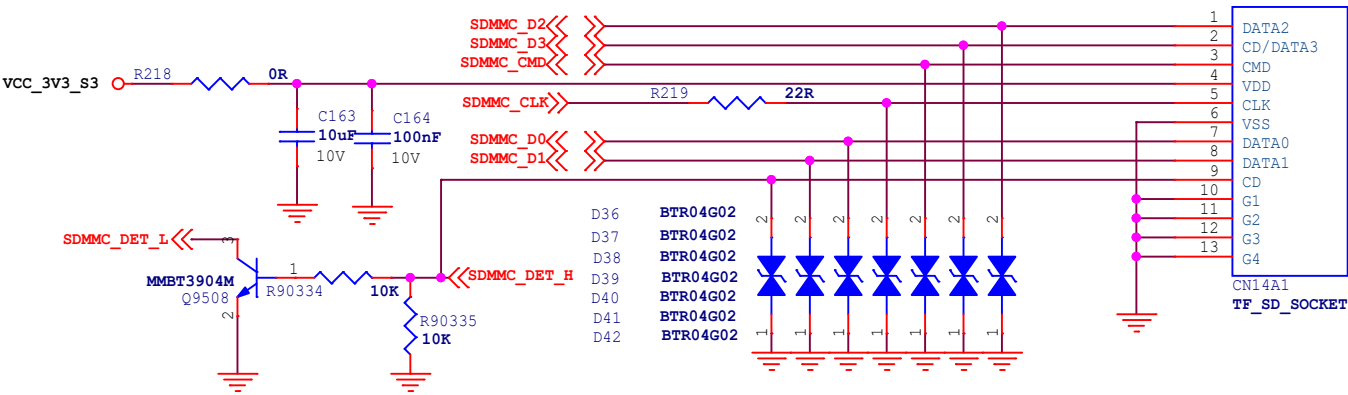
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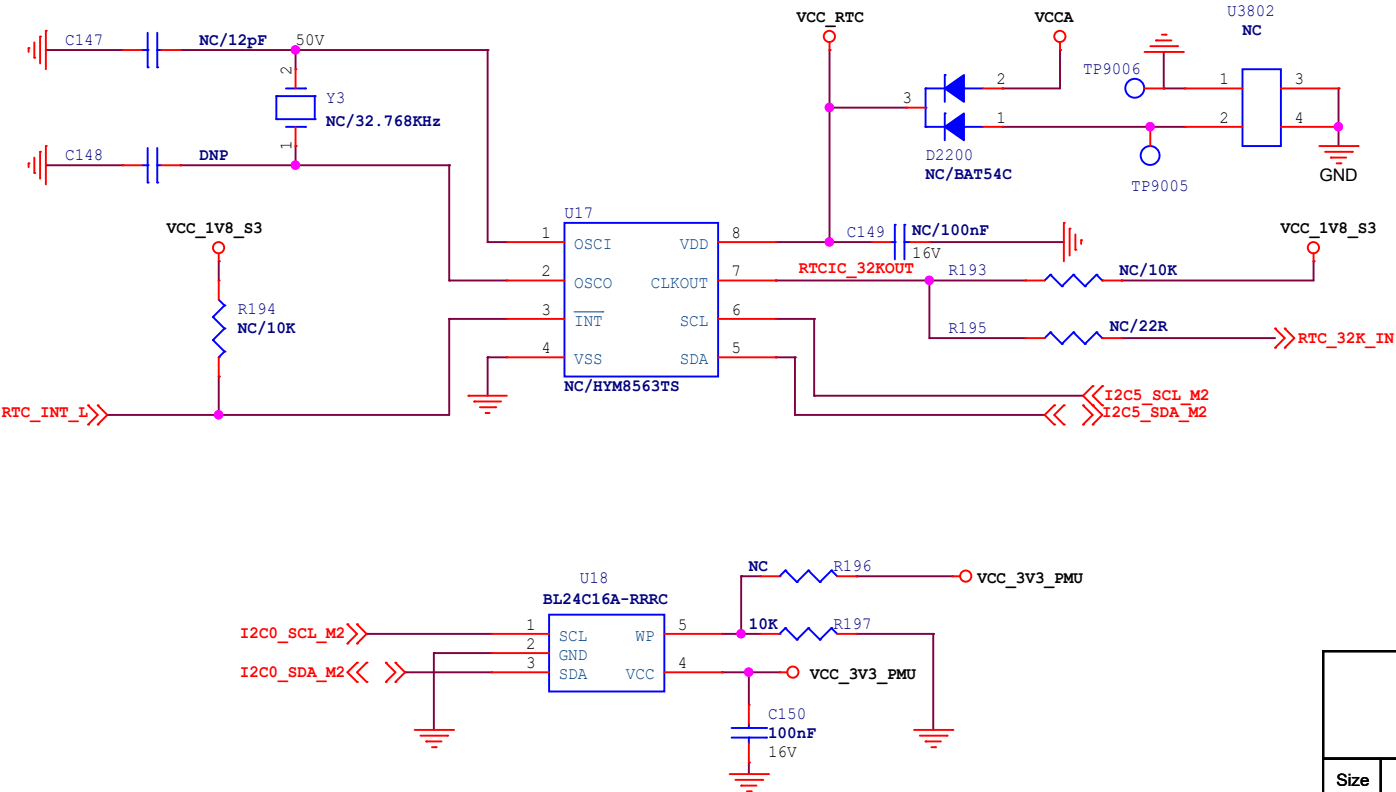
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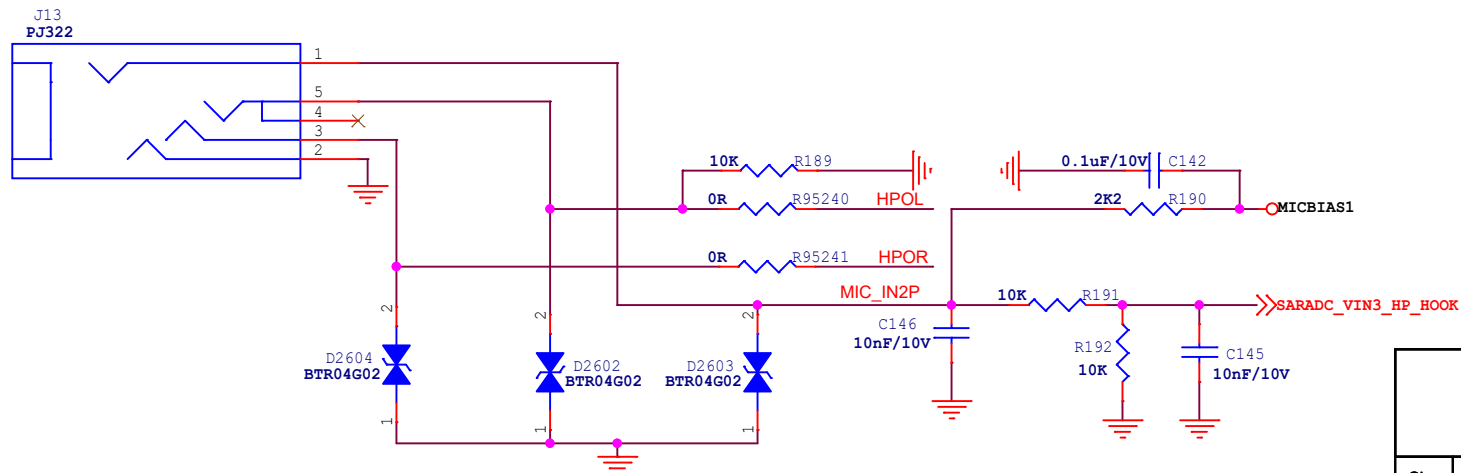
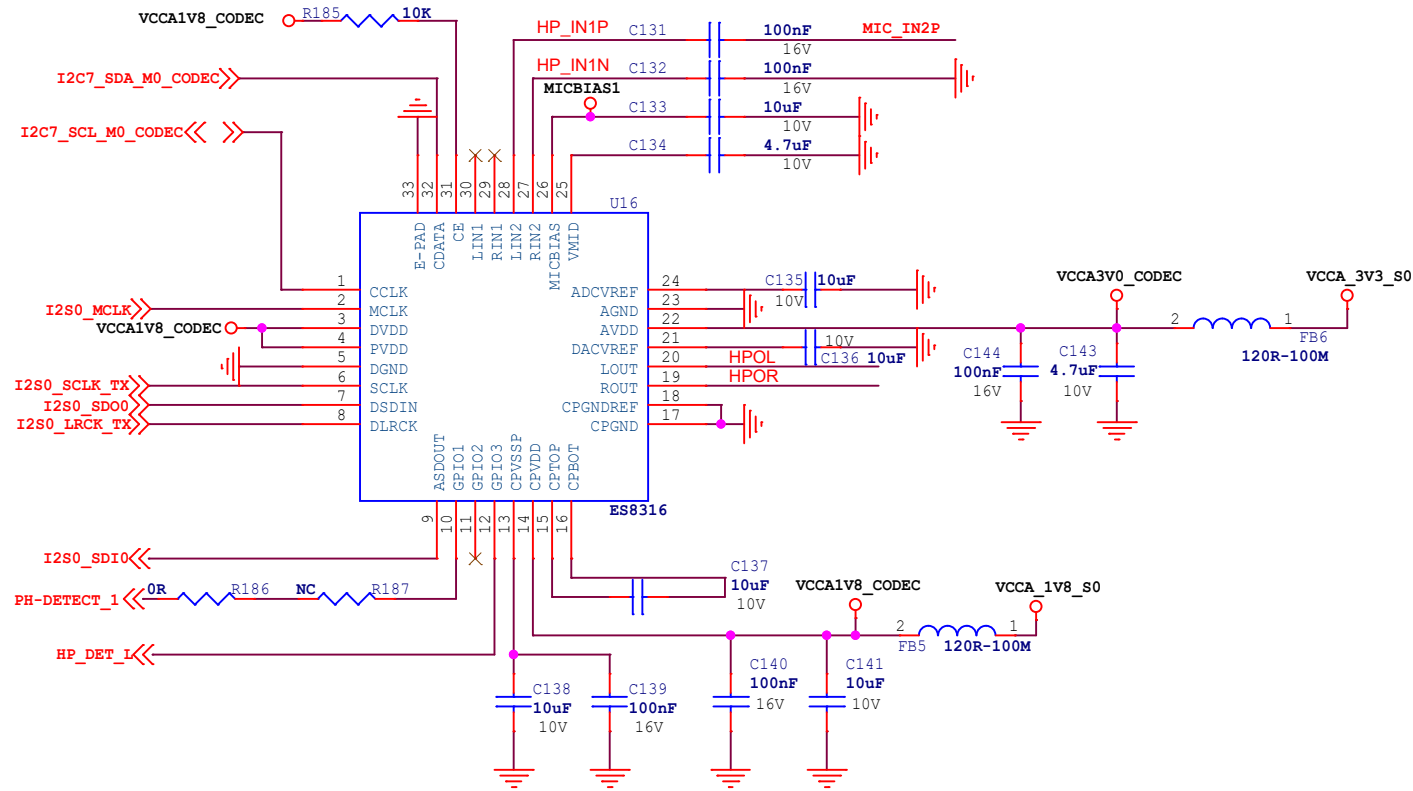
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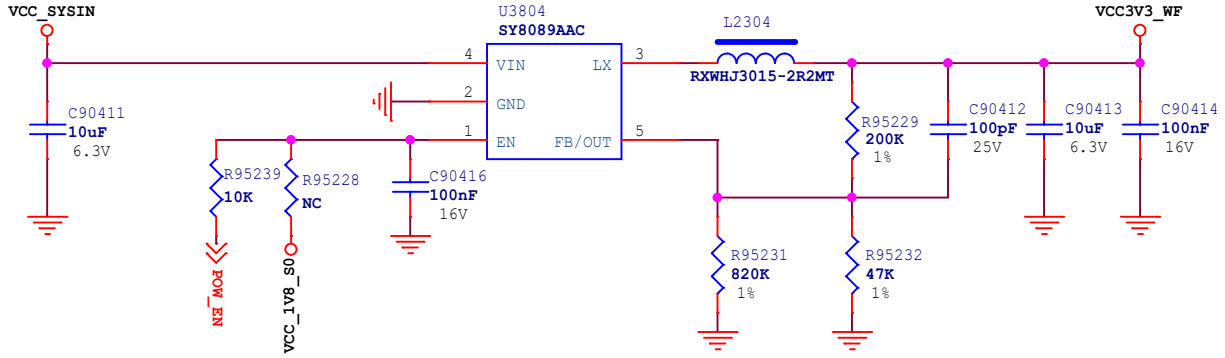
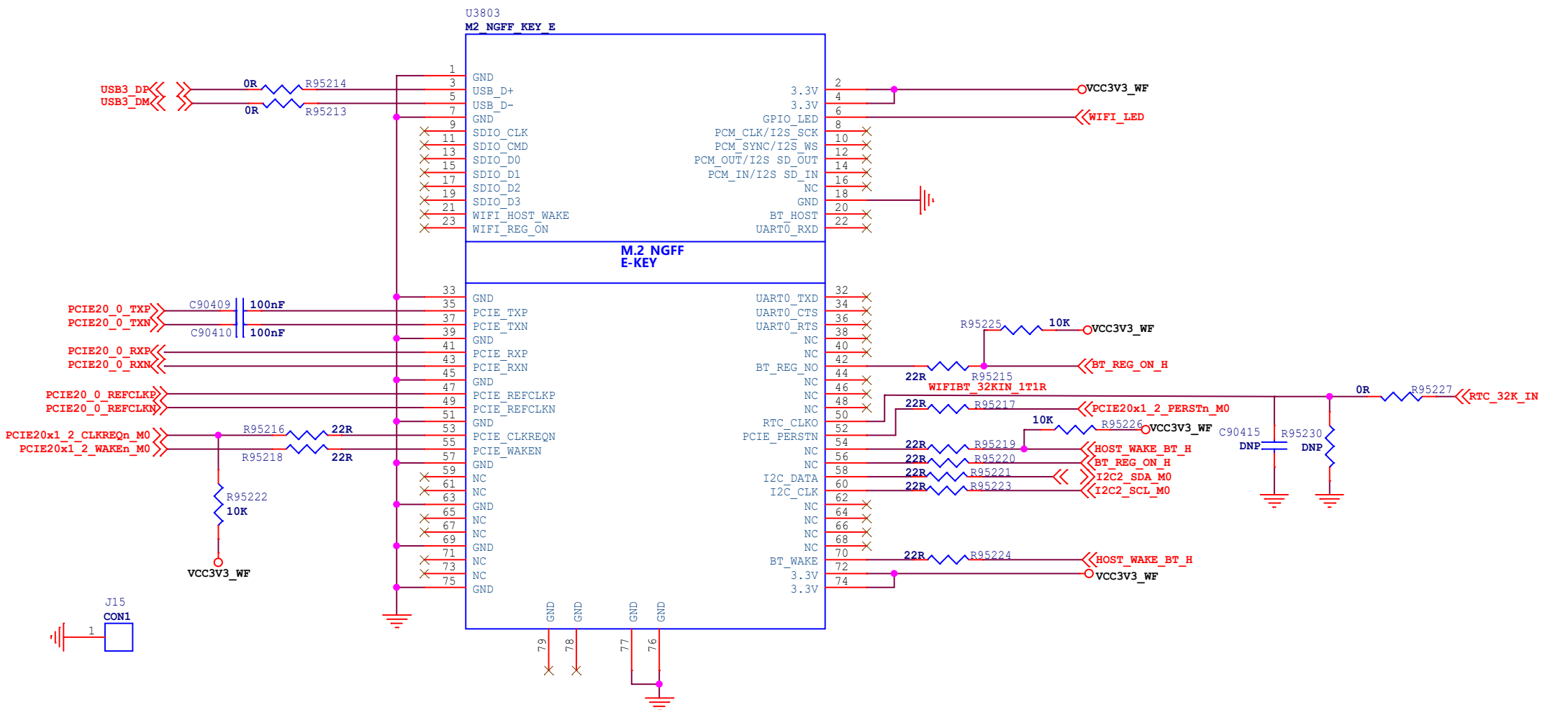
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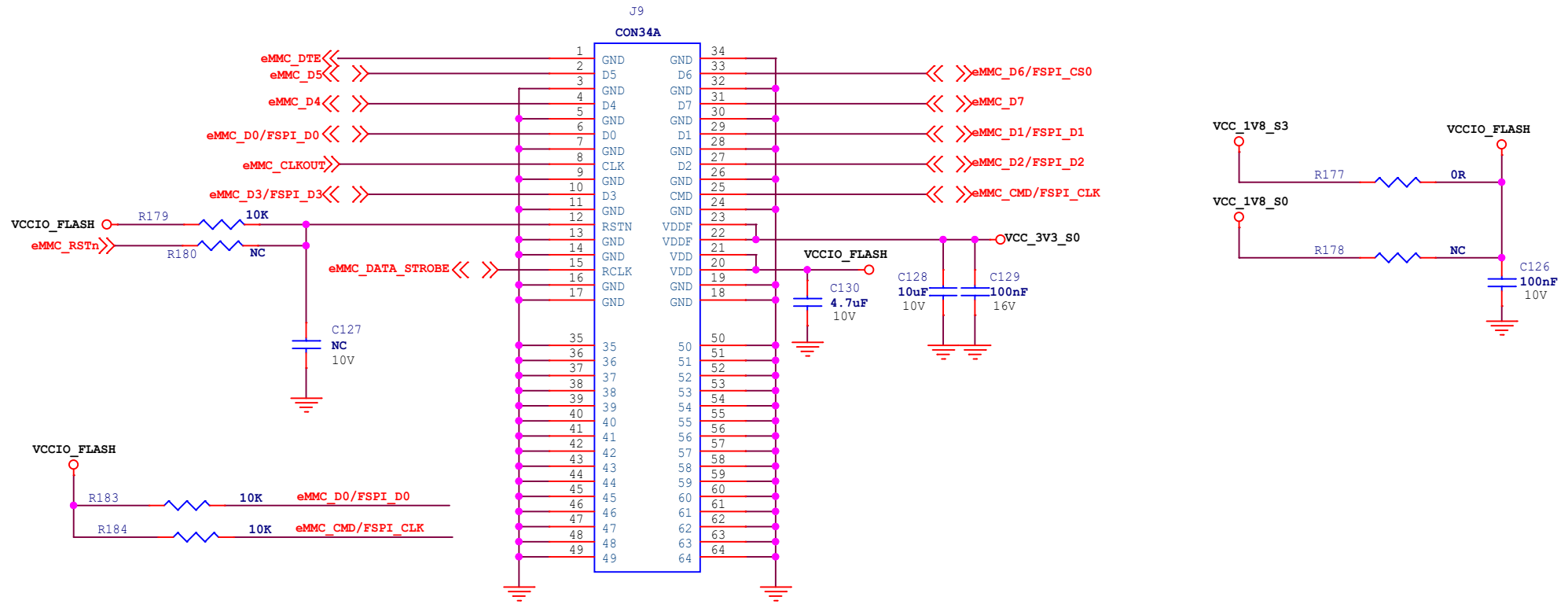
CODEC ES8316



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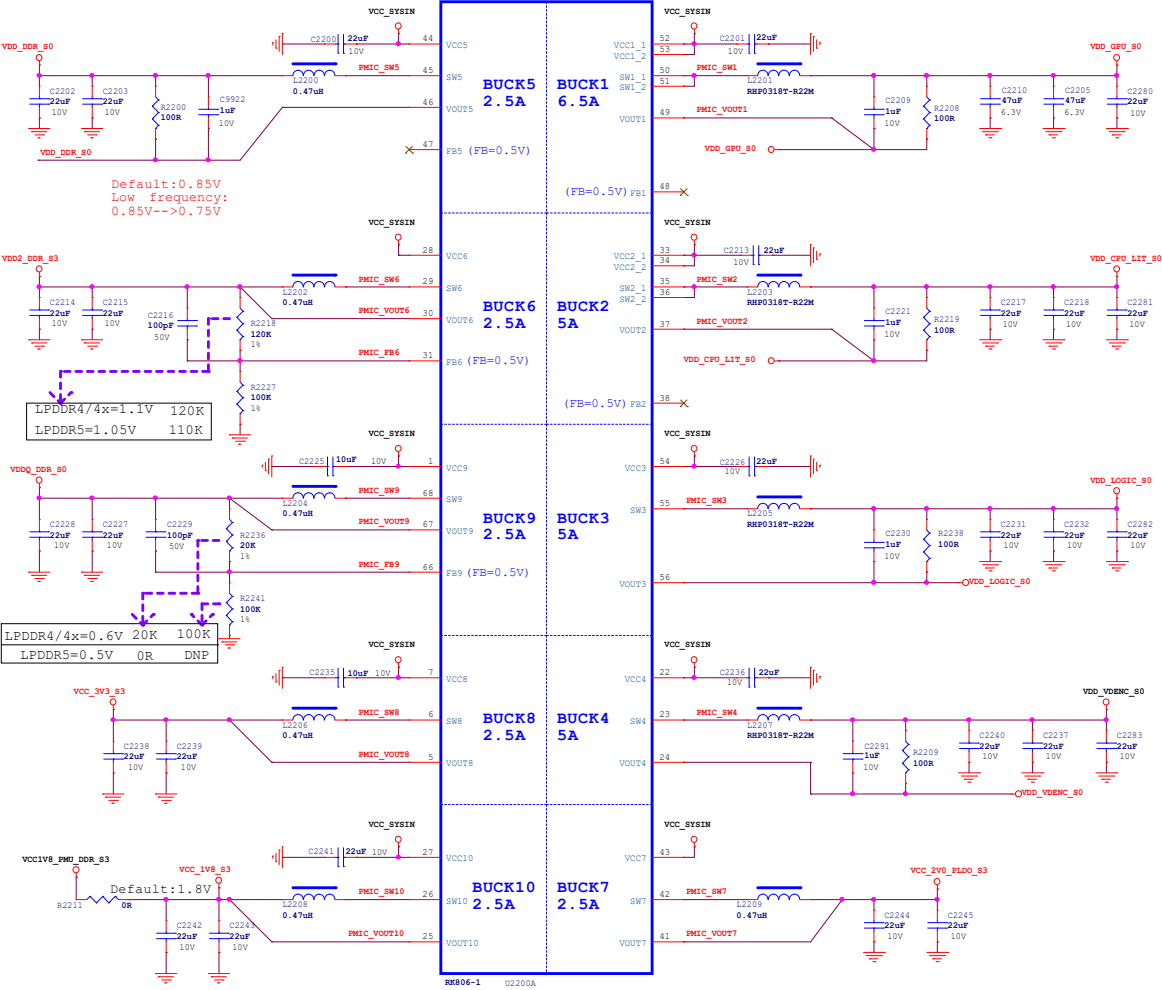
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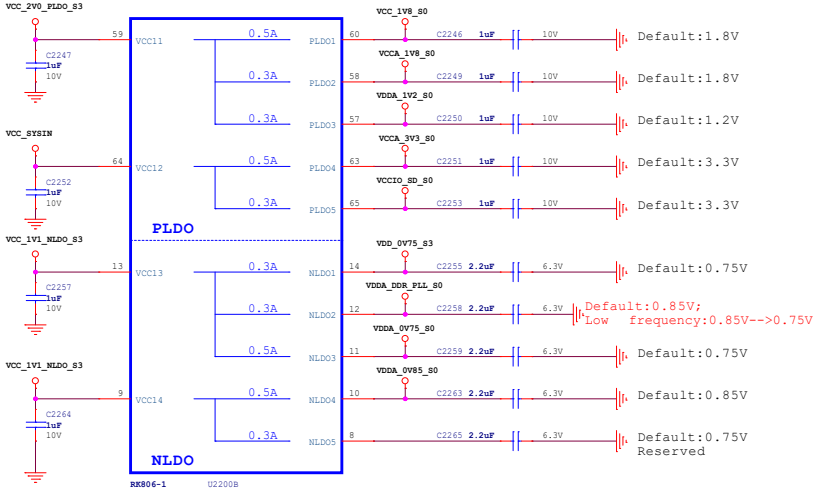
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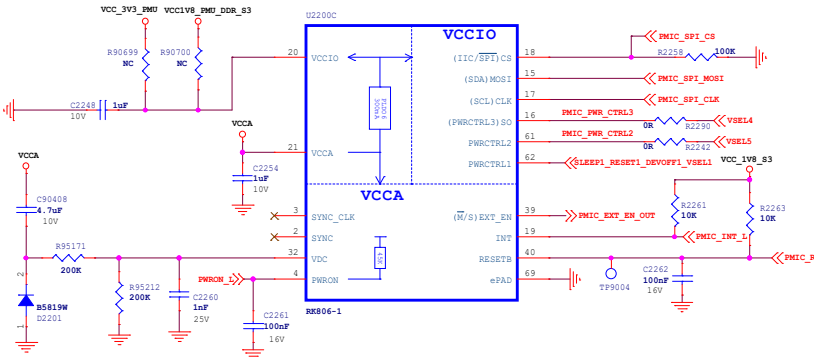
PMIC RK806-1 BUCK



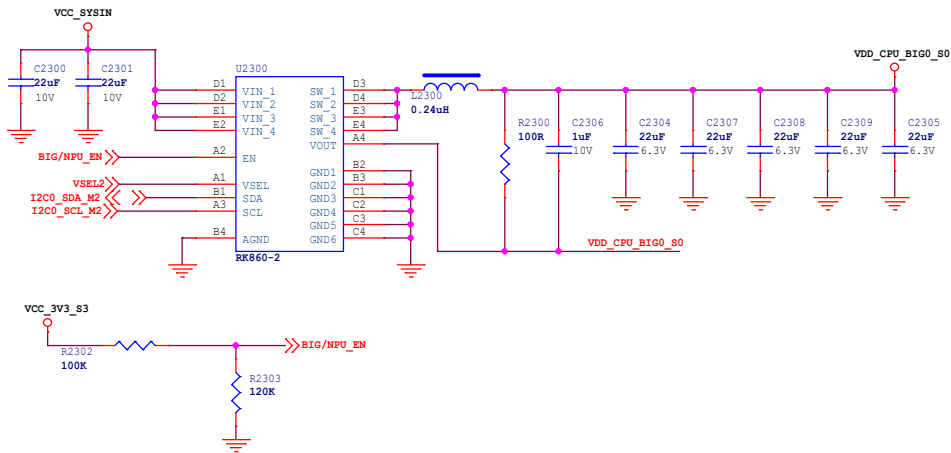
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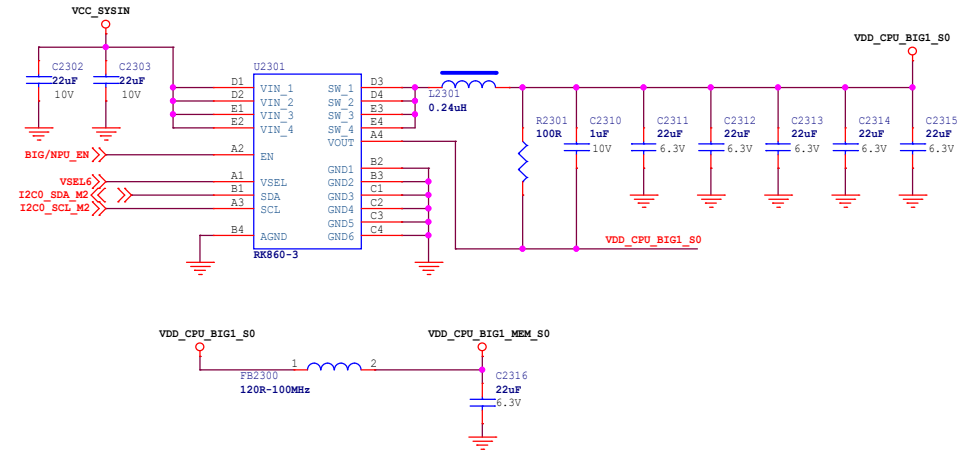
PMIC RK806-1 Managerment



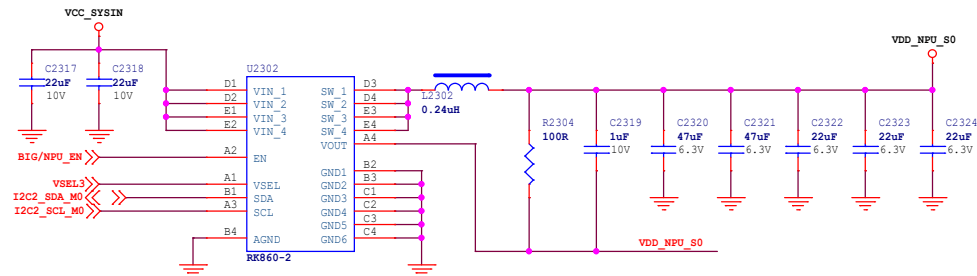
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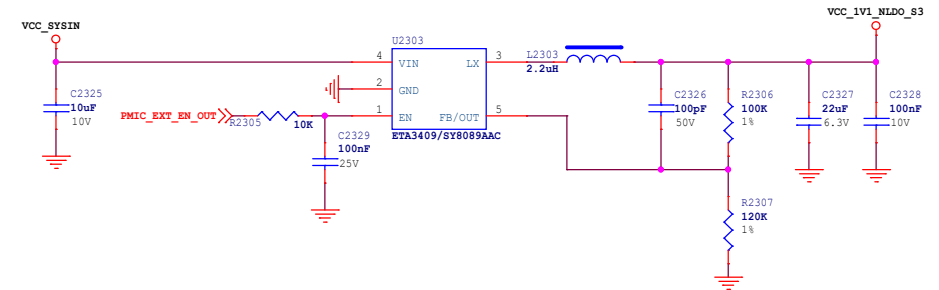
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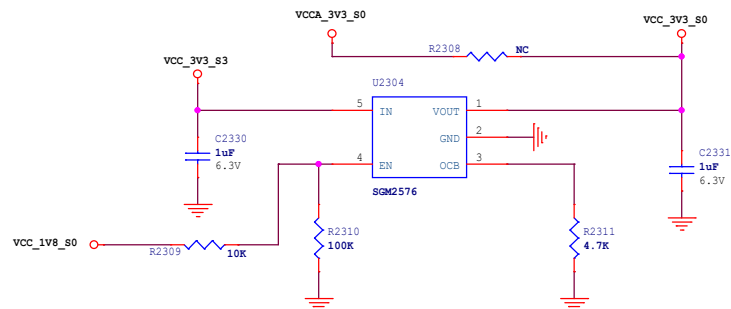
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VCC_1V1_NLDO



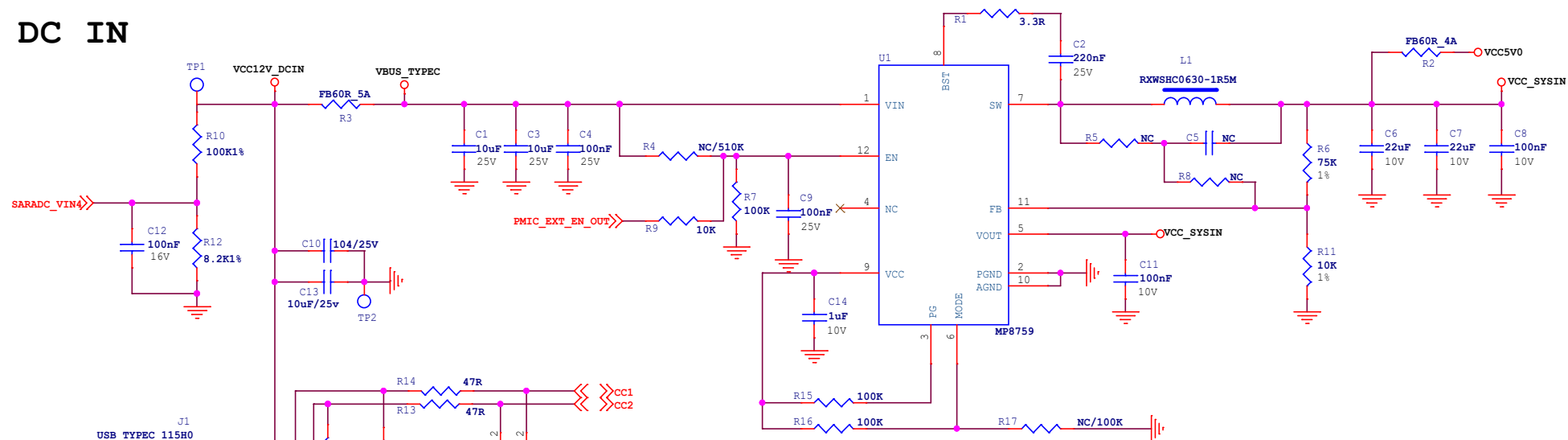
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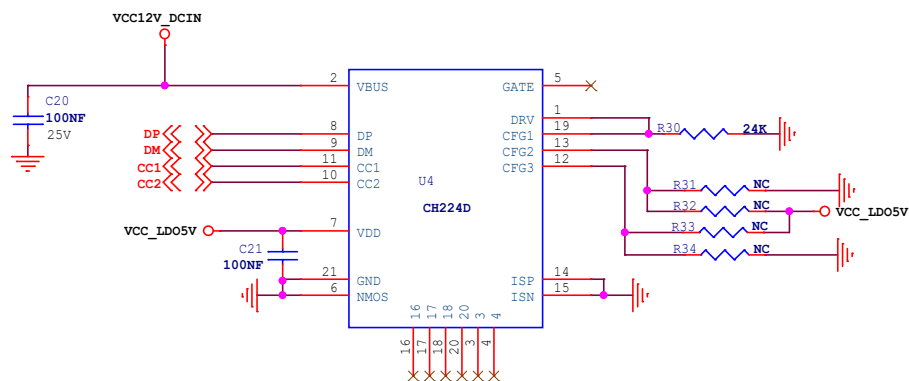
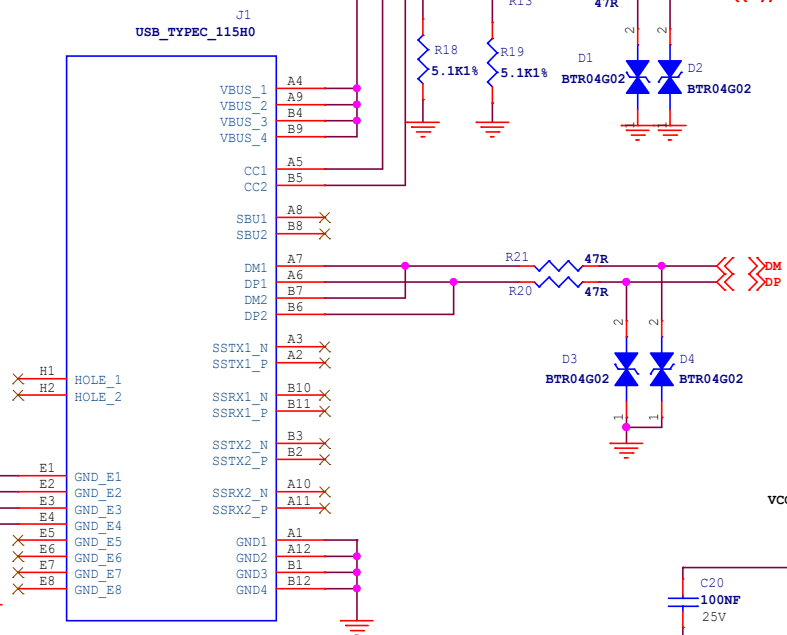
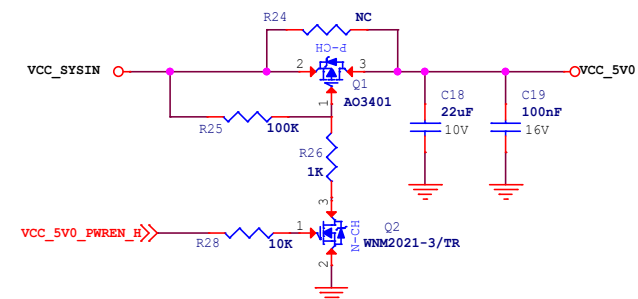
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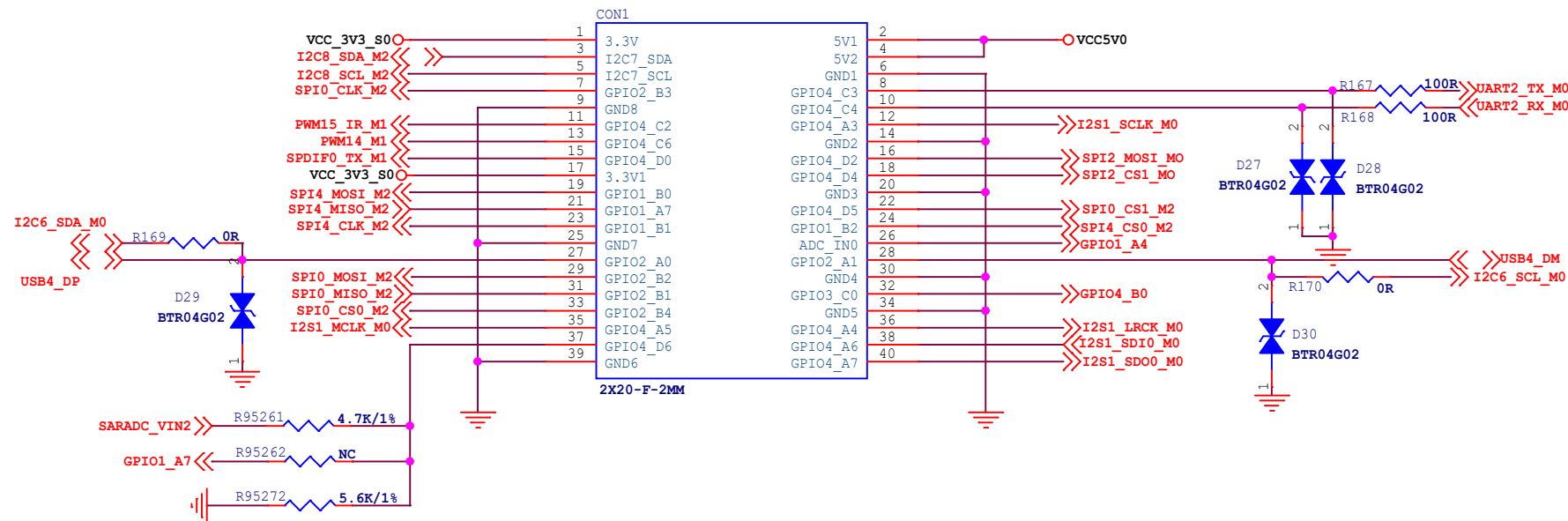
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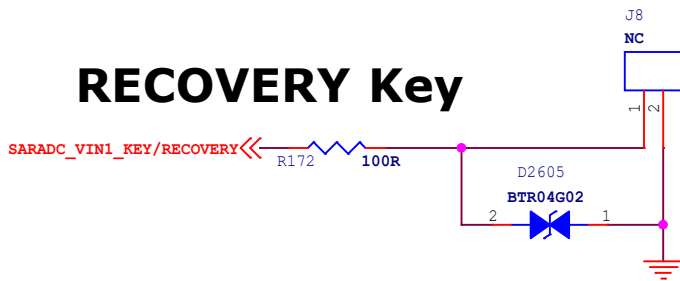
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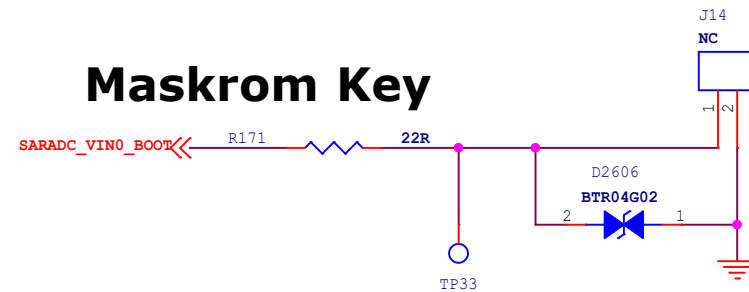
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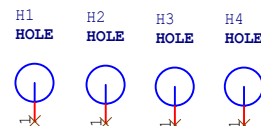
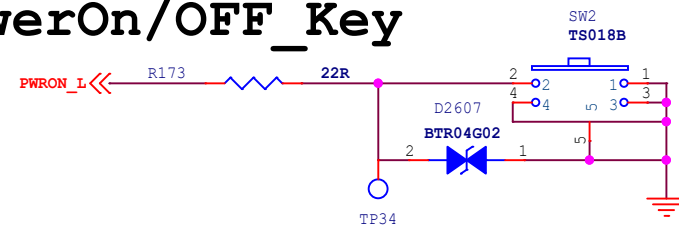
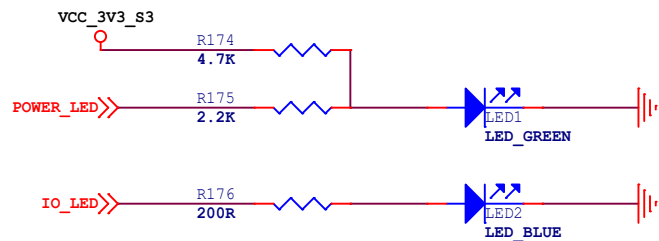
RECOVERY Key



Maskrom Key



PowerOn/OFF_Key



radxa

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