REVISIONS				
REV	ECN	DESCRIPTION	DATE	ENG APPROVAL
1	-	Initial Release	05/14/20	A. Tali
2	-	Change P1 and P2 pitch from .1 to .156	07/02/20	A. Tali
3	-	Remove R2 and R4 and reannotate	07/16/20	M. Huneycutt
A	-	Release to Manufacturing	08/19/20	M. Huneycutt
B	-	Changed to SMD, and added ICL (RT1)	08/26/20	M. Huneycutt
C	-	Added bypass for RT1 for single	09/10/20	M. Huneycutt
D	4465	Added D5	09/21/20	M. Huneycutt

1. Instructions:
   Assemble boards in accordance with IPC-A-610 Class 2.
   RoHS: Supplier shall certify that the parts, materials, and processes used to produce this design are in accordance with the RoHS directive 2011/65/EU.
2. Tooling Files and BOM:
   Tooling files listed in README.TXT of E4D Technologies controlled file 45013031_Power_Entry_D.zip. BOM supplied by E4D Technologies File =Variant_Name _D.=Unit_Type.xlsx, and supersedes any other document.
3. Solder:
   Solder paste and solder wire to be Lead free RoHS compliant.
4. Depanelization:
   Depanelize and bag/label boards individually with convenient size label (see LABELING); finish edges of CCA/FWA to remove loose/protruding fibers.
   After de-panelization, board dimensions to remain within tolerance and all polyimide, fiberglass, copper, epoxy or any other residue to be removed.
5. Cleaning:
   Clean circuits after assembly according to IPC J-STD-001.
6. Labeling:
   Supplier to affix serial number label of convenient size in the area indicated on Primary Side, with format:
   Line1: VYWWNNNN (0.04" minimum text height)
   V=assembly revision level,
   Y=last digit of assembly year
   WW=week number of year,
   NNNN=unit number of week.
   Example: A7251234
   Line2: E4D PCB assembly # and Revision (0.04" minimum text height)
   Example: 1234578 Rev. A
7. Testing:
   Conducted using E4D testing equipment and documentation, if available.
8. Packaging:
   Finished PCB assemblies should be wrapped in bubble wrap and then placed in an ESD bag labeling the outside of the bag with the PCB assembly # and Revision. Refer to D4D specification 10571700.
9. External References:
   ISO Standard 13485:2003, Section 7.5, 8.2.4 Quality System
   IPC-A-610 Acceptability of Electronic Assemblies

Controlled Document

UNLESS OTHERWISE SPECIFIED:
1. DIMENSIONS ARE IN MM.
2. REMOVE SHARP EDGES.
3. TOLERANCES: MACH.
   HOLE DIA ±0.0762
   HOLE LOCATION ±0.0762
   HOLE TO EDGE ±0.127
   ROUTED FEATURE:±0.127

INTERPRET GEOMETRIC TOLERANCING PER:ANSI Y14.5 M

MATERIAL
=Material

DO NOT SCALE DRAWING

	NAME	DATE
DRAWN	A. Tali	9/21/2020
CHECKED	M. Huneycutt	9/21/2020
ENG APPR.		9/21/2020
MFG APPR.		
Q.A.		

Notes

Document Status:

E4D Technologies, LLC

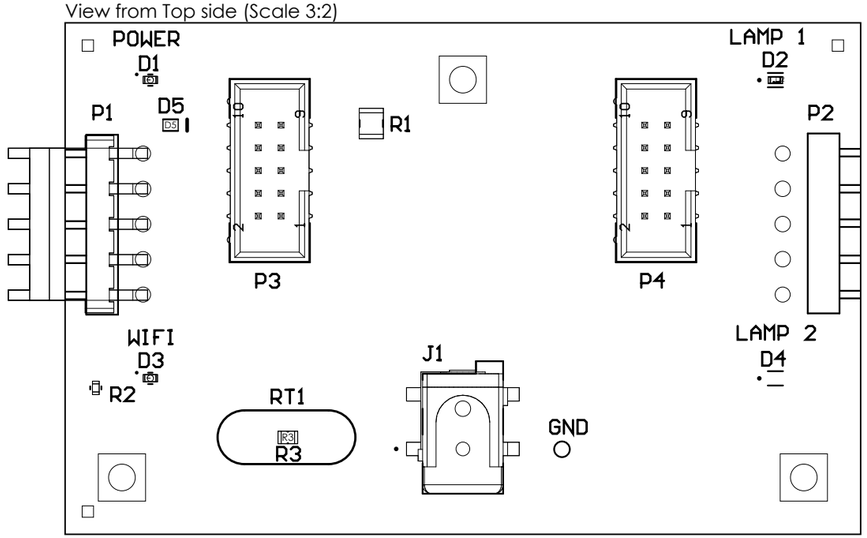
E4D TECHNOLOGIES

TITLE CIRCUIT CARD ASSEMBLY
CASPR
Power Entry

SIZE	DWG. NO.	REV
B	CA45013001	D

SCALE: 1:1 SHEET 1 OF 2

View from Top side (Scale 3:2)



Controlled Document

Document Status:			
E4D Technologies, LLC			E4D TECHNOLOGIES
TITLE CIRCUIT CARD ASSEMBLY CASPR Power Entry			
SIZE B	DWG. NO. CA45013001		REV D
SCALE: 1:1			SHEET 2 OF 2